MODELING OF DEVICES FOR MODERN VLSI CIRCUITS AND VLSI CIRCUIT DESIGN

Thesis Submitted by

Sudipta Ghosh

DOCTOR OF PHILOSOPHY (ENGINEERING)

Electronics and Telecommunication Engineering Department
Faculty Council of Engineering & Technology
Jadavpur University
Kolkata, India

2023

JADAVPUR UNIVERSITY
KOLKATA- 700032

INDEX NO. 178/17/E

1. Title of the thesis:

MODELING OF DEVICES FOR MODERN VLSI CIRCUITS AND VLSI CIRCUIT DESIGN

2. Name, Designation & Institution of the Supervisors:

Prof. P. Venkateswaran
Professor & Former Head
Department of Electronics and Telecommunication Engineering
Jadavpur University
Kolkata-700032, India

Prof. Subir Kumar Sarkar
Professor & Former Head
Department of Electronics and Telecommunication Engineering
Jadavpur University
Kolkata-700032, India

3. List of Publications:

Journal Publications (5)

1. **Ghosh. Sudipta**, Saha. Priyanka, Mukherjee. Adrija, Bose, Sayan. Venkateswaran, P., Sarkar. Subir Kumar, "Analytical Modeling of Core–Shell Junctionless RADFET dosimeter of Improved Sensitivity" Silicon (2022), 1876-9918, https://doi.org/10.1007/s12633-022-01690-y. [I.F:2.67, SCI Journal]

2. **Sudipta Ghosh**, P. Venkateswaran, and Subir Kumar Sarkar, "Analysis of circuit performance of Ge-Si hetero structure TFET based on analytical model", Circuit World, ISSN: 0305-6120. https://doi.org/10.1108/CW-08-2020-0175, 2021. [I.F:0.875, SCI Journal]

3. Sourav Guha, Prithviraj Pachal, **Sudipta Ghosh**, Subir Kumar Sarkar,"Analytical model of a novel double gate metal-infused stacked gate-oxide tunnel field-effect transistor (TFET) for low power and high-speed performance", Superlattices and Microstructures, Volume 146, 2020, ISSN 0749-6036, doi.org/10.1016/j.spmi.2020.106657. [Impact. Factor:2.658, SCI Journal]

4. S Nath, A K Chakravarty, **S Ghosh** and S K Sarkar, "FPGA Placement Optimization using Firefly Algorithm", Advances in Industrial Engineering and Management, American Scientific Journal, ISSN: 2222-7059Vol. 6, no. 2, pp. 97-102, 2017 Peer Reviewed Journal [Impact.Factor:1.60, DOAJ Indexed]

5. **S Ghosh**, S Nath and S K Sarkar "Performance Study of PSO Variants and its' Comparison with Firefly Algorithm in the context of VLSI Global Routing", SSRG International Journal of Electronics and Communication Engineering, Special Issue, ISSN: 2348 – 8549., pp. 63-77, 2015.Peer Reviewed Journal. [Impact.Factor:0.72, SCOPUS]

Conference Publications (6)

1. **Sudipta. Ghosh**, A. Jana, A. K. Agnihotri, S. Kundu, D. Das and S. K. Sarkar, "DC and Analog/RF Performance Comparison of Renovated GAA JLFET Structures," 2022 IEEE VLSI Device Circuit and System (VLSI DCS), 2022, pp. 80-84, doi: 10.1109/VLSIDCS53788.2022.9811488.

2. **Sudipta. Ghosh**, S. Bose, W. Anwar, M. Banerjee, P. Venkateswaran and S. K. Sarkar, "DC and Analog/RF Performance Analysis of Gate-Drain Underlapped and Channel Engineered TFET," 2022 IEEE VLSI Device Circuit and System (VLSI DCS), 2022, pp. 70-74, doi: 10.1109/VLSIDCS53788.2022.9811483.

3. **Sudipta Ghosh**, S. Kundu, S. Guha, J. Ghosh, P. Pachal and S. K. Sarkar, "Effect of Body Thickness on Device Performance of Graded Channel Tri-Metal Double Gate Stack Gate TFET," 2020 IEEE VLSI DEVICE CIRCUIT AND SYSTEM (VLSI DCS), Kolkata, India, 2020, pp. 427-431, doi: 10.1109/VLSIDCS47293.2020.9179899.

4. **Sudipta Ghosh**, P. Pachal, R. Kumar, S. Kundu, J. Ghosh and S. K. Sarkar, "Performance enhancement of p-n-p-n TFET with spacer induced hetero-dielctric gate oxide" 2020 IEEE VLSI DEVICE CIRCUIT AND SYSTEM (VLSI DCS), Kolkata, India, 2020, pp. 1-5, doi: 10.1109/VLSIDCS47293.2020.9179943.

5. **Sudipta. Ghosh**, S. Nath, R. Biswas, P. Venkateswaran, J. K. Sing and S. K. Sarkar, "PSO Variants and its Comparison with Firefly Algorithm in Solving VLSI Global Routing Problem," 2018 IEEE Electron Devices Kolkata Conference (EDKCON), Kolkata, India, 2018, pp. 513-518, doi: 10.1109/EDKCON.2018.8770397.

6. S Nath, **Sudipta Ghosh** and S K Sarkar, "A Novel Approach to Discrete Particle Swarm Optimization for Efficient Routing in VLSI Design", 4th IEEE International Conference on Reliability, Infocom Technologies and Optimization, Noida, India, 2014.

4. List of Patents: NIL

5. List of Presentations in National/International Conferences:

1. **Sudipta Ghosh**, P. Pachal, R. Kumar, S. Kundu, J. Ghosh and S. K. Sarkar, "Performance enhancement of p-n-p-n TFET with spacer induced hetero-dielctric gate oxide" 2020 IEEE VLSI DEVICE CIRCUIT AND SYSTEM (VLSI DCS), Kolkata, India, 2020, pp. 1-5, doi: 10.1109/VLSIDCS47293.2020.9179943.

Statement of Originality

I, Sudipta Ghosh, registered on 31st July, 2017, do hereby declared that the thesis entitled *"Modeling of Devices for Moder VLSI Circuits and VLSI Circuit Design"* contains literature survey and original research work done by undersigned candidates as part of Doctoral studies.

All information in this thesis have been obtained and presented in accordance with existing academic rules and ethical conduct. I declare that, as required by these rules and conduct, I have fully cited and referred all materials and results that are not original to this work.

I also declared that I have checked this thesis as per the "Policy on Anti Plagiarism, Jadavpur University, 2019", and the level of similarity as checked by iThenticate software is **1%.**

16/4/2024

Signature of Candidate:

Date: 16.04.2024

16/4/2024

Certified by Supervisor:

(Signature with date, seal)

Dr. P. Venkateswaran
PROFESSOR
Dept. of Electronics & Tele-Comm. Engg.
JADAVPUR UNIVERSITY
Kolkata-700 032.

Certified by Supervisor:

(Signature with date, seal)

Dr. Subir Kumar Sarkar
Professor and Former Head, Dept. of Electronics & Telecommunication Engg.
Jadavpur University, Kolkata-32

Dedicated To

My Grand Parents

Late Monimohan Ghosh & Late Bina Ghosh

My Parents

Late Ashim Kumar Ghosh & Late Ila Gosh

My Elder Sister

Late Soma Ghosh

For their heavenly blessings

And

My Wife

Smt. Shrabani Tarafder

For their constant support, cooperation

and selfless sacrifice

ACKNOWLEDGEMENTS

I would like to express my sincere love and gratitude to my supervisors, ***Prof. Subir Kumar Sarkar, and Prof. P. Venkateswaran*** *from Jadavpur University, Department of Electronics and Telecommunication Engineering, Kolkata-700032, for their tremendous guidance, sound counsel, ongoing support, kind actions, and inspirations over the course of my research work. They have not only helped me get the thesis to this point, but also extended their helping hands whenever I needed them.*

I would also like to take this opportunity to thank the Faculty Council of Engineering and Technology, Head of the Department, and all faculty members of Department of Electronics and Telecommunication Engineering at Jadavpur University for allowing me to continue my research and for providing me with various inputs and guidance when I needed it.

I would also like to thank Director Sir, Principal Sir and HOD Sir (Dept. of ECE) of Meghnad Saha Institute of Technology for extending their immense support on pursuing my research work. I will remain indebted to all my colleagues of Department of ECE, especially Dr. Manash Chanda and Dr. Sudip Dogra for their continuous support and motivation, that paved the way to complete my research endeavor successfully.

I would especially like to acknowledge Dr. Manash Chanda and Dr. Priyanka Saha and would always remain indebted to them for their constant technical supports, guidance, suggestions and help in my Ph.D. journey.

I would extend special thanks to my fellow research scholars Mr. Subhrapratim Nath, Dr. Anup Dey, Dr. Dinesh Kumar Dash, Mr. Bijoy Goswami, Dr. Subhasis Roy, Mr. Abir Jana, Ms. Komal Kumari for their continuous emotional supports and efforts to the laboratory making an interesting place to work.

I would like to thank Mr. Suman Mandal & family for their love, affection and emotional touch during my journey of Ph.D. work.

I would like to express my love and respect to my elder sister for her endless support and sacrifice without which the work could never been completed successfully.

Finally, heartful thanks to everyone for whom this thesis would have seen the light of the day.

(Sudipta Ghosh)

April, 2024
Jadavpur University
Kolkata-700 032

ABSTRACT

The ever-ending advancement in the fields of electronics, wireless communication and internet-of-things (IoT) fueled by a steady, uninterrupted growth of complementary metal oxide semiconductor technology has called for sustainable development of the downscaling of solid-state devices in sub-micrometer regime. As a result, the industry gets privileged with a profound escalation in packaging density and device performance. Moreover, the cost-per-function of modern state-of-art electronic modules has been drastically reduced, setting marks for economic precedence with every upgraded technological node. The scalability of devices acts as a boon for device performances with zero static power consumption, high integration density, lesser physical space, and simple process steps and layout design, driving the CMOS technology an integral part in our everyday life, starting from handheld electronics to transportation and communication.

However, the rapid cadence of device downscaling is no longer feasible in the sub-100 nm regime to fortify Moore's law, pursuing the conventional scaling strategies. Several device scaling issues stem from gate leakage, variabilities and reliabilities, and after all, short channel effects like drain induced barrier lowering (DIBL), gate induced drain leakage (GIDL), mobility degradation, and random dopant induced threshold voltage fluctuation. Nevertheless, the rise in leakage current restricts threshold voltage scaling further, posing barrier to supply voltage scaling, which is essentially required for high-speed ICs.

In the late 90s, the increasing demand for low-power technologies due to the extensive use of wireless and portable appliances forced Dennard's scaling theory to be practically implemented. Furthermore, the world-wise use of power-hungry smart gadgets calls for reduced power matrices (both active and standby power) by downscaling the supply voltage below 0.5V without compromising the circuit performance. This scenario motivated the researchers to explore new engineering concepts and novel device structures with better scalability and performance. Therefore, a series of researches have been carried out with the Bulk MOSFET technology improvising new structural engineering and amalgamation of novel materials, as well as, looking for alternative devices with the merit of below 60 mV/decade subthreshold swing. As a result, some impressive device structures come up as potential alternatives to overcome the encumbrances associated with nanostructures. For example, Silicon-on-Insulator (SOI) and Silicon-on-Nothing (SON) Metal Oxide Semiconductor attracted significant attention due to their higher scalability and lowered parasitic effects than

conventional MOSFETs. However, the SOI/SON-based circuit couldn't offer the best power-speed performance as expected, resulting in a further quest for new structures. Junctionless Transistors (JL FET) emerge as one of the best solutions due to their insusceptibility against short channel effects and simple fabrication process. However, despite its significant contribution to the VLSI domain, the device still suffers from degraded subthreshold swing, owing to its thermionic constraints, leading to an expensive power budget.

Hence, a MOSFET-like structure with alternative energy-efficient technology becomes inevitable to sustain CMOS logic design in future. The Tunnel Field Effect Transistor (TFET), one of the potential contenders, takes the privilege of quantum mechanical tunneling and ballistic transport phenomena driven by low power supply, offering a minimal power-speed product earnestly required for today's cut-in technological nodes. Moreover, the device is compatible with the latest fabrication technology, favoring ultra-high-density packaging to integrate billions of transistors in a single chip. However, two major constraints include low drive current and ambipolar conduction forbidding the device implementation in VLSI circuits.

VLSI Global routing is another back-end design aspect of optimizing the power-delay expenditure in today's level-headed industrial VLSI research. With ever-increasing layout complexity, the routing of interconnects gets more complicated and tedious task. Therefore, the routing problem during VLSI physical design is considered an NP-hard problem, where the solution lies in finding the minimal cost of Rectilinear Steiner Tree from the graph comprising all the terminal nodes to be electrically connected. In order to have an acceptable solution by Global routing, we need to shrink the core area and the critical path delay, where delay precisely depends on the total interconnected wire length and the number of vias used in a three-dimensional VLSI system. Swarm intelligence, inspired by the intellectual activity of the biotic creators of nature, is one of the emerging and promising optimization tools that may be implemented in this field to optimize interconnect lengths in achieving the desired performance (speed) of modern ICs.

Therefore, the present dissertation circumscribes comprehensive performance evaluations of TFET to register its footprint as a potential candidate in low-power, high-speed VLSI design. The multi-gate structure with work function engineering, implementation of stacked gate oxide to bar gate leakage, pocket implantation as channel engineering, and use of low bandgap material to construct heterostructures are strategically procured to escalate the drive current and submerge the ambipolar conduction of elementary TFETs, count on the derived analytical

model to justify the superiority of the proposed architectures over the conventional ones. Hence, the analytical results are validated through effective simulation to substantiate the accuracy of the proposed models. Moreover, the device-circuit interaction is investigated thoroughly by implementing the proposed TFET based inverter. The outcome revealed an excellent power-delay product (PDP) matric compared to the conventional CMOS logic to legitimize the worthiness of the proposed structure in energy harvesting applications. In addition, the responses of a core-shell junctionless transistor, deployed in circuit application as a robust radiation sensor in VLSI circuits, have been thoroughly examined and the outcomes are verified by both theoretically and simulation process.

Nevertheless, in the back-end design, swarm intelligence promises a near satisfactory solution to the global routing problem. Two new variants of discrete particle swarm optimization (DPSO) are formulated to optimize wire lengths, and finally, proposed variants of PSO have been compared with the Firefly algorithm in terms of optimization of timing budget by minimizing the interconnect delay as a primary concern. The merits of the proposed algorithms have been inspected through time complexity, computational load, and convergence rate as well.

Table of Contents

List of Figures

List of Tables

List of Abbreviations

VLSI	Very Large Scale Integration
ULSI	Ultra Large Scale Integration
SOC	Silicon-on-Chip
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
D-MOSFET	Depletion mode MOSFET
E-MOSFET	Enhancement mode MOSFET
CMOS	Complementary Metal Oxide Semiconductor
FET	Field Effect Transistor
SCE	Short Channel Effects
DIBL	Drain Induced Barrier Lowering
HCE	Hot Carrier Effect
SON	Silicon-on-Insulator
FD SOI	Fully-depleted Silicon-on-Insulator
PD SOI	Partially-depleted Silicon-on-Insulator
BOX	Buried Oxide
DG	Double gate
DM	Dual metal
TG	Triple gate
GAA	Gate-all-around
TFET	Tunnel Field Effect Transistor
BTBT	Band-to-band tunneling
EOT	Effective Oxide Thickness

CHAPTER 1

Introduction and Organization of the Thesis

1.1. Introduction

The ever-increasing technological demand of modern civilization calls for a tremendous advancement in every sphere of electronic applications, starting from industrial automation to home automation, automobile engineering to satellite communication, wireless communication to Internet-of-Things (IoT), and very precisely day-to-day consumer appliances and portable products. The first transistor was invented by Shockley, Barden, and Brattain in 1947 at Bell Lab [1.1], while the first integrated circuit was created by Jack Kilby at Texas Instruments in 1958 [1.2] posed remarkable impacts over the expansions of modern VLSI/ULSI industries. Integrated circuits, since then, have been the prime driving force behind the development of smart electronics, automated systems with high precision, faster communication systems with commendable security, and so on to quench the need of modern society. Therefore, the worldwide market started tiny, portable, flexible and smart electric goods that urge for low-standby power with high-speed operation. Thus, the ever-ending demand fuelled the realization of a single electronic module with complex functionalities, which entailed amalgamating a mighty number of devices into a single wafer to propel the IC industry from Very Large Scale to Ultra Large Scale Integration era.

Nevertheless, the assiduous demand for complex, multifunctional integrated circuits can only be possible by downscaling the device dimensions and integrating a hefty number of components on a solo piece of substrate. As a result, the dividends are earned in terms of minimum fabrication area and cost, enhanced circuit speed, multitasking ability, enriched packaging density, and minimal power consumption. Moreover, the feature of downscaling reinforced by CMOS technology performs a significant role in ameliorating the device's performances with improved processing speed while optimizing the area, power, and cost per function. Thus, the device scaling acts like a catalyst to uphold the growth of VLSI industries for future generation ultra-low-power, high-performance (speed) integrated circuits [1.3, 4, 5].

The paradigm shift from microelectronics to nanoelectronics has been possible due to the aggressive scaling of transistors, obeying the famous Moore's law, predicted by G. Moore. In the article "Creaming more components onto integrated circuits" [1.6], published in the electronics magazine of McGraw-Hill publication house, Gordon E. Moore, a co-founder of Intel Corporation, predicted that the number of transistors integrated into a chip will quadruple every two years in April 1965. Later the prediction was set as a target of miniaturization for the VLSI industry, continued shirking of device dimensions to increase the transistor count. Starting with thirty-two transistors integrated on a single chip, the market witnessed 65k components fabricated on the same platform, launched by Intel, after ten years of the forecast (Fig 1.1). The trend has continued, corroborating 14 nm technology in 2020 depicted in Fig 1.2.

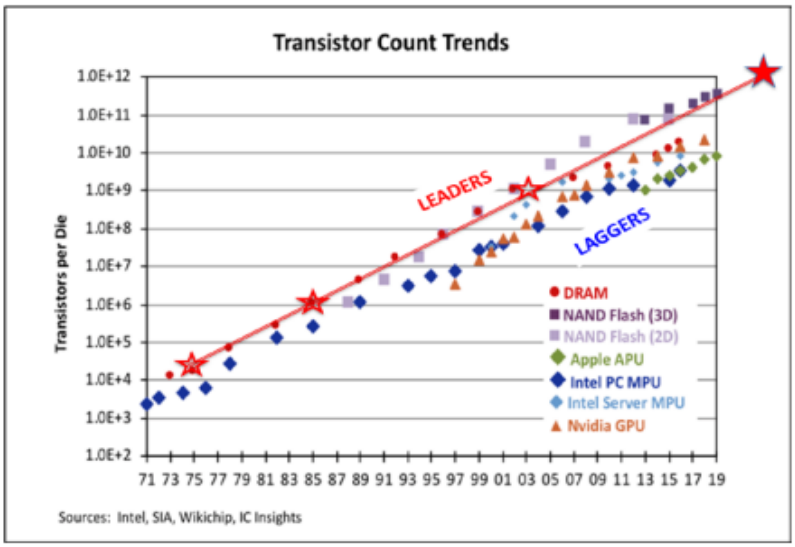


Fig1.1: The trend of semiconductor products as per the ITRS roadmap.

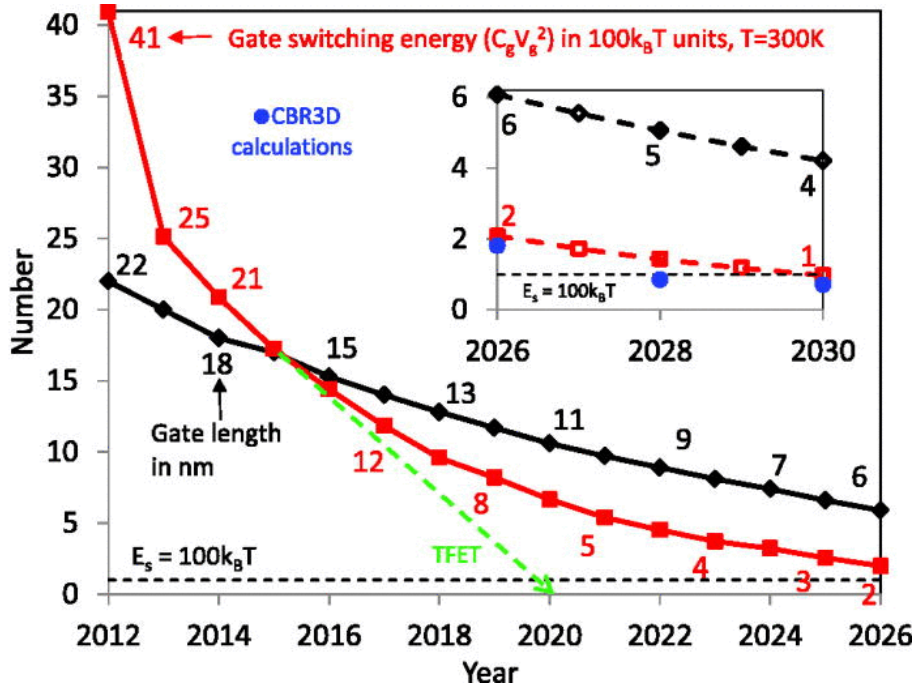


Fig 1.2: The trend of technology node speculated by the ITRS roadmap.

Till the late 90s, the threshold voltage (V_{th}) and the source voltage (V_{DD}) scaled down in proportion to the physical dimension of the semiconductor devices, following fruitfully Dennard's scaling theory proposed in 1974 [1.7]. As a result, the dynamic power consumption is reduced by an order of four times with decreasing supply voltage, only possible through device miniaturization, endorsed by excellent materialistic and electrostatic properties of the dielectric constant, silicon dioxide (SiO_2) used in MOSFETs.

The aggressive scaling gave rise to some adverse effects, known as short channel effects (SCEs), restricting further miniaturization of the MOS device. Therefore, several innovative devices have been invented in the last two decades to carry forward the CMOS technology by downscaling the device dimension to full throttle. For example, strained Silicon [1.8] technology in 90 nm node successfully contributed to VLSI foundry with upgraded features of high-performance circuits on subduing short channel effects. The process involves a SiGe layer over the silicon substrate exerting a tensile strain along the channel affording a high mobility carrier transportation through the channel of the device.

Down the lane later, due to charge carriers tunneling through small gate oxide, the 45 nm technological node has severe gate leakage, caused by aggressive scaling of gate dielectrics. Therefore, introducing high-k dielectrics [1.9] like Al_2O_3 (ε_r=9), HfO_2 (ε_r=25), TiO2(ε_r=85),

etc. bring down the gate leakage to a great extent, rolling the technology-wheel to the next phase,

The rise of thermal diffusion of charge particles, provoked by further device scaling, fuelled undesired escalation of leakage current, endorsing the implementation of unconventional MOSFET structures in CMOS technology. Therefore, the overshoot of static power consumption in integrated circuits promoted smart device architecture, viz. silicon-on-insulator, silicon-on-nothing [1.10], and FinFETs [1.11] to continue the pace of the miniaturization. To date, 7nm FinFETs are reported to be fabricating in bulk production.

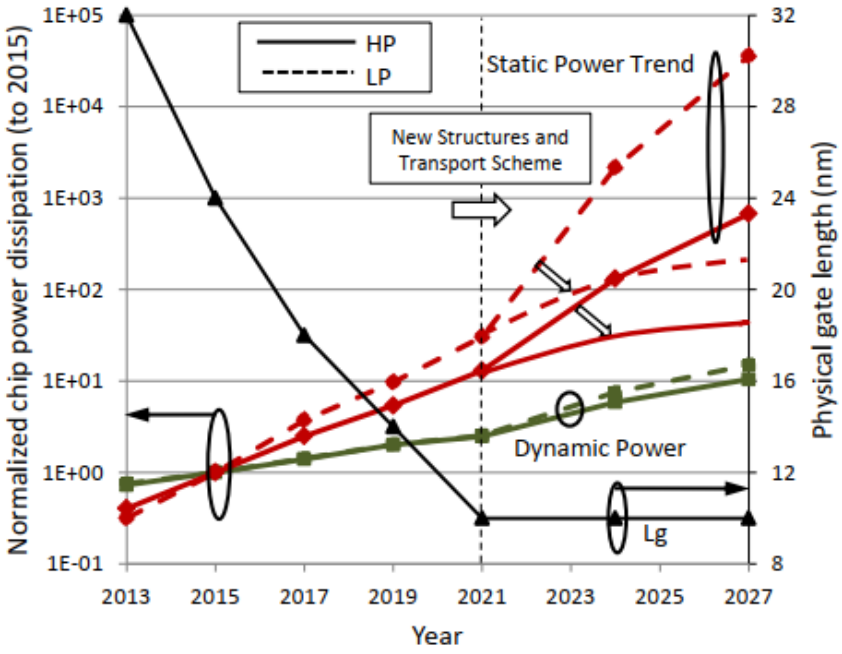


Fig1.3: Trends of Static and Dynamic power dissipation profiles with the decreasing technology nodes considering high-performance (HP) and low-performance (LP) devices.

On contributing superior performance against SCEs, silicon-on-insulators (SOI FET) have turned up as a prospective surrogate for future CMOS technology. The introduction of a buried oxide layer (BOX) below the fully depleted thin silicon channel made the device electrostatics free from high parasitic effects, subsequent propagation delay, enhanced subthreshold properties, and better immunity against absorbed radiation. The SOI device attracted immense attention to researchers due to its structural similarities with Bulk MOSFETs with better scalability, lesser fabrication complexity, and low coupling effect induced perfect device isolation [1.12]. However, the said structure failed to meet the increasing technological demand

to mitigate SCEs in due course of time, and soon some improvised structures based on conventional SOI came up to deaden short channel effects. The ultra-thin body raised drain/source FD SOI, metal gate source/drain FD SOI, multigate FD SOI, HALO doped FD SOI, and BOX engineered FD SOI are a few names that came into the research limelight to replace the conventional SOI structures, paying the dividend of better power-delay matric with higher immunity against SCEs [1.13, 1.14].

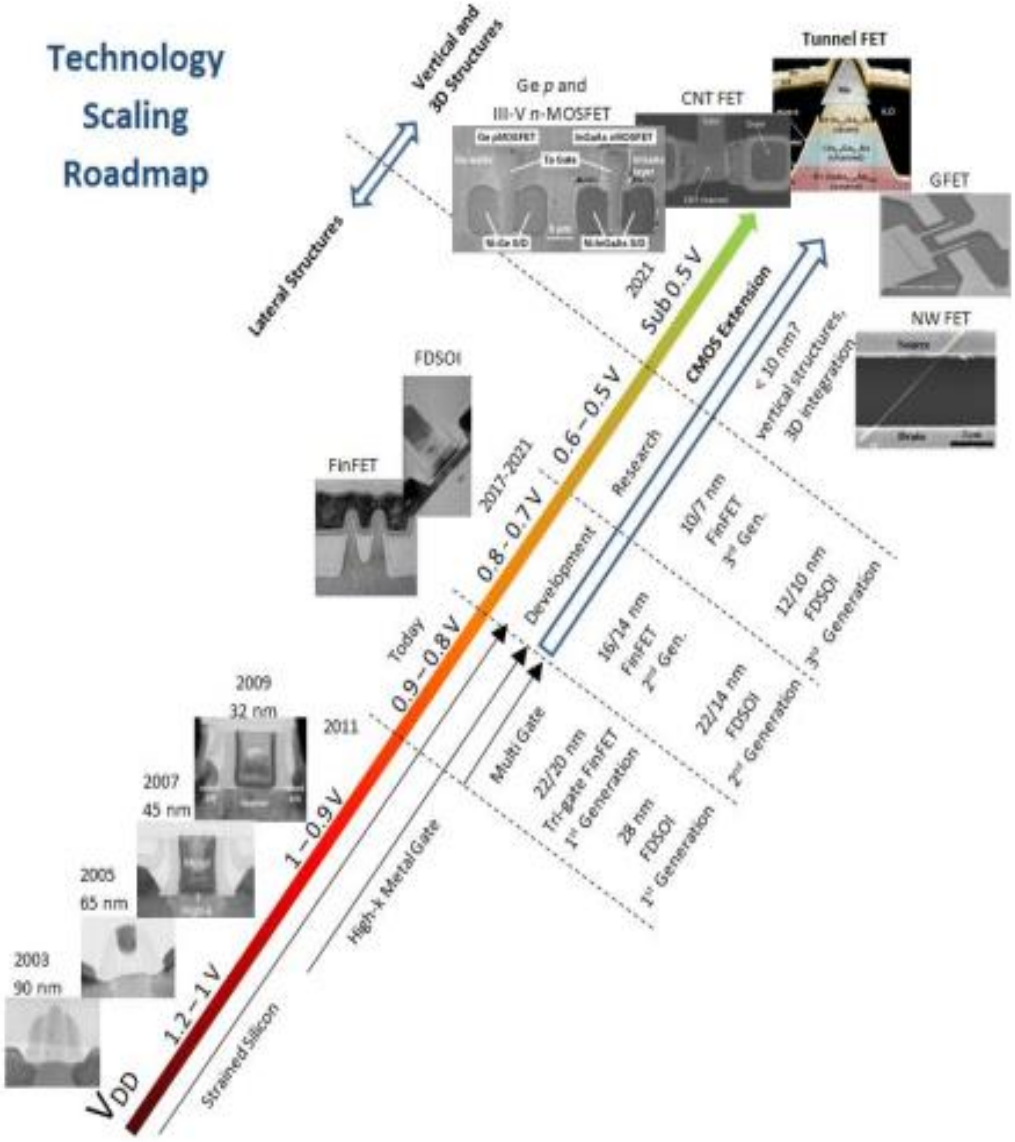


Fig 1.4: Technology scaling roadmap: evolution of short channel devices.

It was well-thought-out to replace the BOX layer of SOI FET with air (lowest permittivity = 1) to transform it silicon-on-nothing (SON) FET structure. The device was facilitated with even lower parasitic capacitance than its predecessor, with reduced DIBL effects and

diminished fringing field [1.15]. The silicon-on-nothing (SON) architecture is attributed to excellent subthreshold behavior favorable for low power-high speed applications. The candidate offered excellent credentials working in a hazardous environment with lesser self-heating problems.

Down the lane of scaling, As circuit elements for next-generation technological nodes, FinFETs first appeared. It is a multigate device with exceptional channel gate controllability, minimizing the impacts of small channels and resulting in a reduction in leakage power. made them extremely suitable for modern low-power/high-speed VLSI technology [1.16].

According to the ITRS roadmap (Fig 1.3), the downscaling of FET devices can only be sustained for another decade [1.17], as the physical dimension of MOSFETs is advancing towards only a few nanometers; equivalent to the net dimension of 100 atoms. Consequently, the quantum mechanical tunneling effects will be prevalent, leading to a large-scale leakage in transistors associated with other daunting short channel effects. Furthermore, the escalated static power dissipation beyond the tolerable limit will bottleneck the technology downscaling, barring the further growth of packaging density essential for economical industrial yield. Therefore, the industry started a deliverable effort looking for potential alternatives like non-planner device geometry, 3D integration, and device with different transport phenomena [1.18]. Fig.1.4 represents the growth of CMOS technology to date, incorporating the emerging device technology feasible to carry forward the scaling strategy for future technology nodes.

Therefore, some excellent research areas open up to encounter the futuristic challenges of VLSI technology. The use of Germanium and III-V materials to replace Silicon has been one of the major concerns in this regard. The concept involves deploying high mobility channel materials still to be implemented owing to the constraints of imperfect high-k oxide-substrate interface, high probability of quantum tunneling for small bandgap channel material, and complex manufacturing process flow [1.19, 1.20]. Silicon nanowire is another potential alternative to challenge planner MOSFET structure in deep-subnanometer regime. The gate-all-around architecture poses inherited quality in defeating short channel effects. Moreover, the vertical grown-up structure of the said device fulfils the forecast of next-generation IC technology. However, avoiding surface roughness and defects is still a challenging task in growing uniform nanowires. The next names came up with Carbone nanotube (CNT) and Graphene FET, which might be prospective successors in sub-10nm technology nodes. CNT offers high carrier mobility at room temperature. But, growing the uniform structure of the

device involves some complex fabrication issues. Whereas the Graphene FET is struggling to achieve efficient current gain (ON/OFF current ratio) due to zero bandgap material consisting of a single atomic layer despite having wide lucrative applications in the RF domain.

Junctionless transistors (JL FET) [1.21, 1.22] are a viable option for next generation technology due to their high scalability, better sustainability against SCEs, improved carrier mobility, simple fabrication feasibility, and last but not least low power consumption capability. However, the planner JL FETs require vertical junctions for better device isolation and more control over short channel effects.

TFETs appeared as the most prospective surrogate for low power-high performance applications due to their excellent electrostatic properties [1.23]. It can achieve sub-60mV/decade subthreshold swing due to its unique carrier transportation mechanism governed by quantum mechanical tunneling. TFETs can be operated under low operating voltage (below 0.5V) with high I_{ON}/I_{OFF} ratio. Moreover, the evolution of the III-V material process technology strongly contributed to TFET devices overcoming its shortcomings. Therefore, the device engineering growing faster attracts the limelight of the research field, aiding the front-end design technology to move forward to the next generation.

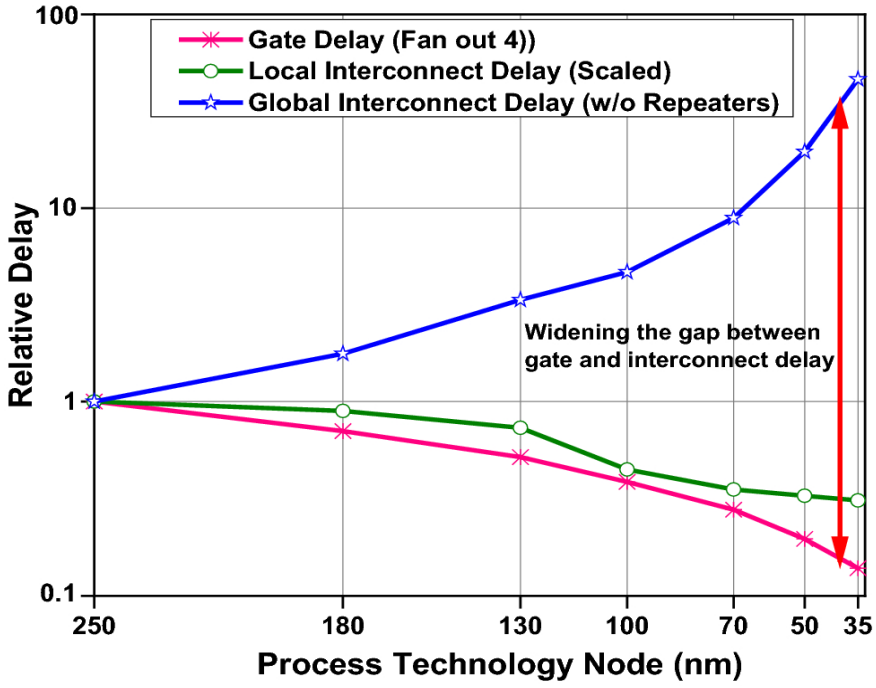


Fig 1.5: Trends of relative delays with process technology considering the possible parameters predicted in the ITRS roadmap.

The backend design of VLSI technology is not far away from the revolutionary impact of miniaturization. The level-headed VLSI research area, concentrating on the perpetual shirking of chip size, is looking forward to upgrading chip performances precisely regarding power-saving and delay reduction. With the aggressive scaling of VLSI technology, higher clock frequency and better operating speed is becoming essential. Since the number of components goes on increasing to fortify Moore's law, interconnect delay is becoming a major contributing factor in evaluating circuit performance on the platform of the increased layout complexity.

The impact of the process technology over the interconnect delay matric of an IC has been depicted in Fig. 1.5, based on the ITRS roadmap [1.18]. The gate delay has been compared with local and global interconnect delays without repeaters. It is evident that the interconnect delay is no longer a trivial parameter in today's complex, high-performance CMOS logic below the 130 nm technology node. Therefore, VLSI routing emerges as a challenging research field seeking all the attention of the research fraternity around the globe.

Finding a Minimal Rectilinear Steiner Tree (MRST) connected by all of the terminal nodes is the goal of the global routing phase, which is an NP-hard task. For a feasible solution, one needs to shrink the core area and the critical path delay. The delay extensively depends on the total interconnecting wire-length and the number of vias used in the 3-dimensional VLSI system.

Swarm intelligence, inspired by the intelligent activity of nature's biotic agents, is one of the emerging and promising optimization algorithms. Stimulated by the principle of self-organization and group activity of the creatures, this algorithm solves many critical problems such as finding food (herd of bees) or destination (flock of birds), building nests (ant colony), etc. The optimization techniques performed during global routing determine appropriate Steiner nodes to reduce the number of redundant interconnect wires. Swarm intelligence shows many promises in providing near-satisfactory solutions to the NP-hard problem.

1.2. Motivation

Supply voltage (V_{DD}) scaling is the prerequisite for low-power digital ICs compatible with modern state-of-art technologies. The dynamic power consumption is quadratically related to the V_{DD} scaling. However, due to specific constraints, the disproportional scaling of threshold voltage (Vth) with respect to source voltage gave rise to an exponential static power consumption stemming from undesired surge in leakage current. MOSFETs cannot avoid the

shortcoming as the subthreshold slope of the device is constricted by 60mV/decade in room temperature owing to the thermally dependent carrier transportation mechanism characterized by equation 1.1. [1.24]. According to the ITRS roadmap (Fig. 1.6) threshold voltage of transistors should be kept constant for both high and low-performance applications. Therefore, alternative devices with unconventional transport mechanisms have been looking for efficient threshold voltage scaling without sacrificing the static power budget.

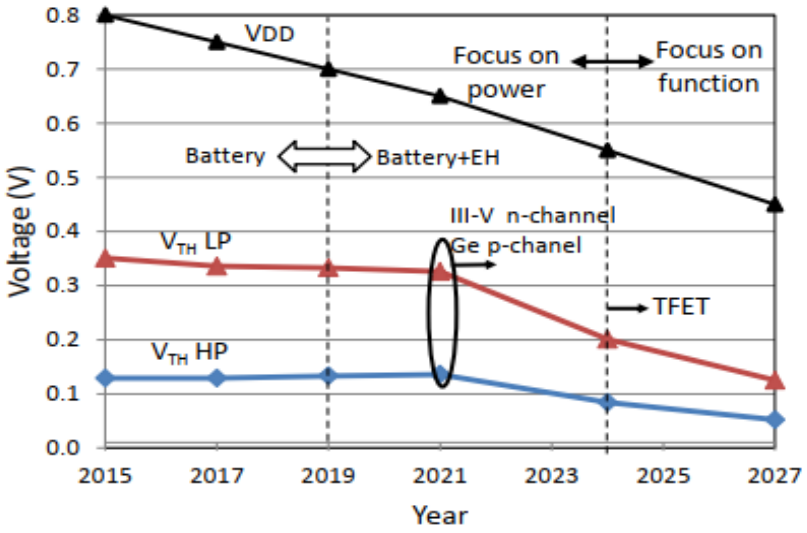


Fig 1.6: Threshold voltage trend of high and low-performance CMOS technology [18].

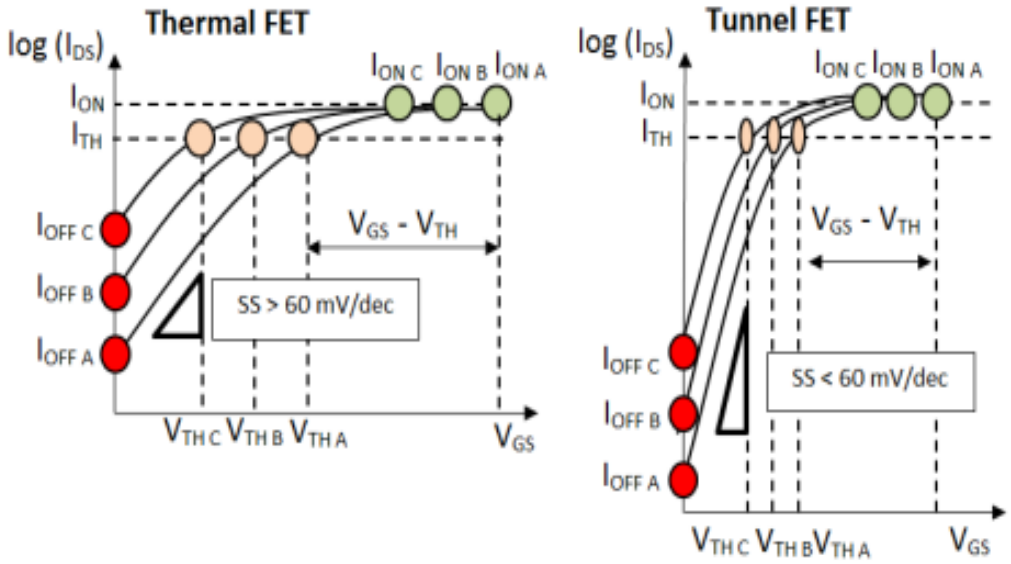


Fig 1.7: Subthreshold characteristics of MOSFET vs. TFET.

$$I_{sub-V_{th}} = KWe^{-\frac{V_{th}}{nV_T}}\left(1-e^{-\frac{V_{DD}}{V_T}}\right) \quad (1.1)$$

The hunt for steep subthreshold swing (below 60mV/dec) switching devices motivated today's research world to explore various possibilities with different current conduction mechanisms leading to TFETs, one of the most propitious device technologies for low power operations [1.25-1.26]. As shown in Fig. 1.6, tunnel field effect transistors (TFETs) have the superior ability to manage leakage current and the ensuing static/standby power consumption, allowing for a decrease in overdrive voltage (VGS-Vth). The increased electrostatic properties of the TFET device even in low-voltage operations make it a natural choice for low-power, high-performance applications.

On the other hand, there are two main stages for the wire-length estimation during the routing phase: global routing and detailed routing. The link length needs to be optimized during the global routing phase. The Rectilinear Minimal Steiner Tree Issue (RMST) [1.27], a well-known NP-Complete problem in Graph Theory, is the key to minimizing wire length. Swarm intelligence, a subfield of AI, could be very helpful in resolving such NP-complete issues. Swarms cooperate with one another to survive in any setting. These social agents are observed to have limited capacities on their own, but when working together, they are able to complete tasks rather intelligently, which is necessary for their survival. Modeling the behavior of these natural swarm systems was a top priority for scientists and engineers. G Beni and J. Wang first presented swarm intelligence in 1989 to address several real-world issues with global optimization [1.28]. Heuristic and meta-heuristic techniques are used in these algorithms. Heuristic means "to learn via trial and error." These techniques are very helpful for quickly locating ideal or almost ideal answers to challenging optimization problems (such as NP-complete issues). Because they involve local search & randomization tradeoffs, meta-heuristics (meta meaning "beyond" or "higher level") outperform heuristic algorithms in this regard. The PSO (Particle Swarm Optimization) and FA meta-heuristics algorithms are two of these well-liked methods (Firefly Algorithm).

1.3. Literature Review

With the ever-increasing efforts to cope with the next generation's technological demands, the device miniaturization directed by Moore's law, several challenging research technologies unfolded in recent times. The quantum computing, single-electron devices [1.29, 1.30], spintronics [1.31, 1.32], magnetic memory device are few names in this regard [1.33, 1.34]. In

the path of device scaling, the silicon-on-insulator structure captivated the research limelight due to its compatibility with conventional MOSFET structure, interesting electrostatic characteristics, and feasible fabrication process flow [1.35].

A short channel SOI MOSFET has been theoretically studied by Banna et al. to investigate the threshold voltage roll-off (TVRO) characteristics [1.36]. The TVRO of the FD SOI gets merely influenced than conventional MOSFETs, provided the channel length is constant. An improved model of FD SOI is reported in [1.37] claimed more accurate electrostatic behaviors considering the short channel effects like velocity saturation, drain induced barrier lowering, drain induced conductivity enhancement, channel length modulation, and floating body effects. An analytical model of short-channel FD SOI has been formulated by J. B. Roldán [1.38], contemplating the series resistance, velocity overshoot, and self-heating effects to investigate the said device's circuit performance. Later, a number of analytical models were developed to examine the electrical properties. of PD SOI [1.39], asymmetric double gate SOI [1.40] and meta-isolated FD SOI [1.41], that involve Poisson's equation in portraying the threshold voltage attributes.

The threshold voltage profiles and attributes of static power consumptions without compromising the enhanced saturation current are precisely investigated in [1.42, 1.43] by Sarkar et al. On the other hand. Double gate FD SOI, highly immune to random dopant fluctuations [1.44], was analytically modeled to investigate their subthreshold behavior [1.45-1.48], claiming their high scalability with reduced parasitic capacitance and lower propagation delay in 18nm technological node. In this regard, K. K. Young offered 2D Poisson's equation-based surface potential model [1.49] plays a significant role in device modeling to characterize the electrostatic and subthreshold behavior of semiconductor devices.

A research group led by Sarkar et al. published some revolutionary works on silicon-on-nothing (SON) [1.50-1.52] as a prosperous successor of silicon-on-insulator MOSFET. The buried oxide layer gets replaced by air, the dielectric material having the lowest permittivity in nature. The device produced some exciting outcomes, even better than its predecessor [1.53-1.55]. Introducing air as a buried dielectric medium yields lower intrinsic capacitance reducing the coupling effects between drain and source. As a result, the DIBL effect and two-dimensional charge-sharing effect have been significantly reduced. Thus, reduced body leakage with enhanced transient behavior is observed in the proposed device. Therefore, the SON structure offers implementation in low voltage, low power, and high-speed application fields subject to enhanced subthreshold behavior.

Moreover, the structure is more immune to the hazardous environment and self-heating problems. The authors delivered the feasibility of the fabrication process of the device with drain and source region connected to the body. The SON structure with manufacturing feasibility by selective etching of SiGe layer over the top of the BOX has exhibited outstanding prospects among future nanoscale devices.

The DG structure [1.56], which consists of two gates in the nanoscale domain, effectively shields the enhanced drain from the source electric field. In order to attain a near-60mV/dec subthreshold slope, stronger electrostatic control of gates over the channel locates may be achieved. This will improve subthreshold behaviour. Additionally, the strategic application of gate material engineering adds the benefit of more successfully suppressing short channel effects (SCEs) [1.57]. The work function engineering, executed by applying two gate materials effectively, discontinuing the channel electric field in such a proportion that intensifies the mobility of the charge carriers at the source side while screening the drain side electric field, consequently subduing the SCEs like hot carrier effect, gate leakage, etc. Many DMG-based structures are reported in the literature [1.58-1.60]. Therefore, the DMG associated with SOI/SON architectures provided more scalability and resilience against SCEs in the deep sub-nanometer region.

However, the MOS transistors have been incompetent in achieving the subthreshold slope below 60mV/dec due to its current conduction mechanism, governed by thermo-ionic emissions, a temperature-dependent mechanism. Tunnel Field Effect Transistors (TFETs) came to the surface as a future technology component due to their commendable performance in operating under low supply voltage, better subthreshold characteristics, and possible subthreshold slope far below 60mV/dec, since the carrier transportation is based on built-in tunneling phenomena.

Reddick and Amaratunga [1.61] first conceived silicon-based band-to-band tunneling (BTBT) transistors in 1994. Driven by the negative differential resistance phenomenon in Tunnel diode, the authors proposed the feasibility of such devices with increased drive current by tunnel width modulation by regulating the applied bias, depletion widths and forbidden energy gap of the constituent material.

A comparative analysis has been driven by Upasana et al. [1.62] on account of the performance of hetero-dielectric TFET (H/D TFET), dual material gate TFET (DMG TFET), and dual material gate hetero-dielectric TFET (DMG H/D TFET). A generalized model has

been developed to evaluate the energy-band, surface potential, and electric field profiles considering the interface trap charges. Moreover, the TCAD based simulation study evaluated circuit performance in terms of parasitic capacitance and transient responses. All the structures have been optimized based on metalwork functions and lengths. DMG H-D TFET emerged as the best alternative among all the proposed structures.

By linearly altering the mole percentage in the binary metal alloy gate, Sarkhel et al. developed a work function engineered double gate TFET [1.63], and a performance comparison with conventional double gate TFET was done after that (DG TFET). Based on the B-T-B-T tunneling generation rate across the tunneling volume, an analytical surface potential is produced, then an electric flux density and drain-to-source current model. The WFEDG TFET performed better than the DG TFET, as mentioned in the referenced research report.

By Priyanka Saha and Subir Kumar Sarkar, a novel gate-all-around elliptical heterojunction TFET [1.64] has been reported. The model and TCAD simulation considered the fabrication complexity of realizing ideal circular geometry, and therefore, a practical elliptical architecture has been taken care of in the paper [1.65-1.67]. The work also counted on staggered gap heterojunction with GaAsSb-InGaAs and Si-GeSi material system to achieve superior subthreshold swing and ON current characteristics.

A novel broken-gate TFET [1.68] architecture is proposed by Dutta and Sarkar. The renovated Silicon-based TFET has been modeled with 21nm channel length. The analytical drain-to-source current model was developed by Kane's equation. Therefore, the numerical simulation was carried out with Sentaurus TCAD using a non-local tunneling model. As a result, the device offered one of the best characteristics in terms of low ambipolar conduction, subthreshold swing, and high driving current compared to similar structures of comparable dimensions.

Later, Saha and Sarkar implemented the broken gate TFET (BG TFET) in pH sensing applications [1.69]. As a pH sensor, the semiconductor of the BG TFET was modified by electrolyte material. The chemical reaction between the gate dielectric and the electrolyte generates interface trap charges at the oxide-semiconductor interface, steering to a subsequent change in potential profile. The change in threshold voltage, thus realized, is the measure of pH sensing of the proposed sensor. The outcomes were corroborated by the ATLAS simulator justifying the satisfactory accuracy of the sensor.

Saha and Sarkar [1.70] attempted a different biosensing application using a dielectric modulated split gate TFET for the label-free detection of biomolecules. With the size of the biomolecules taken into account, the sensitivity of the devices was examined by varying the dielectric and charge densities. A comparable study by Mukhopadhyay [1.71] is based on an InGaAs-Si hetero TFET with an expanded gate and a single cavity that is dielectrically regulated. The maximum sensitivity of $1.3x10^8$, the highest I_{ON}/I_{OFF} of $2x10^{12}$, and the lowest subthreshold swing of 25.4mV/dec are observed for the proposed sensor with the dielectric constant of 12, which is one of the best-case scenarios amongst the benchmarked sensors found in contemporary pieces of literature.

Sharma et al. presented a technical letter on performance assessment of GaSn-InAs martial-based heterojunction TFET of 9nm channel length having an InAs underlapped layer between drain and source [1.72]. Non-Equilibrium Green Function (NEGF)-Poisson-Schrödinger simulation was used to obtain the device's transfer characteristics and band diagram. The performance of the device is evaluated in comparison to a 9nm traditional P-i-N hetero TFET. For 6nm underlapped length, the optimized device delivered best-case solutions.

An analytical model of dual material double gate TFET (DM DG SG TFET) with stacked gate oxide [1.73] has been formulated by Kumar et al. After deriving the Id-Vgs model, the threshold voltage model was developed following the maximum transconductance method. The model is also suitable for indirect bandgap material like SiGe and InAs channel-based TFETs. Besides, several structural engineering-based high-performance TFET models [1.74-1.77] have been reported recently.

Ahish et al. [1.78] reported for the first time a performance study of a common-source amplifier constructed with a heterojunction DG TFET. The circuit-level application is manifested with an InAs-Si heterostructure. The device's threshold voltage is extracted using transconductance and constant current methods to conduct the study further, revealing a 3-dB roll-off frequency of 230.11GHz and a unity-gain frequency of 5.4THz.

A simulation study of Ge(011) – Si(011) cylindrical heterojunction TFET has been proposed by Alam et al. [1.79]. The work introduced the orientation engineering of material systems to enhance the Ge-Si nanowire's electrical behaviors. As a result, the staggered band alignment eradicated the ambipolar behavior of the device. Furthermore, the shallow tunneling path at the heterojunction leads to a high ON current for V_{DD} = 0.4 and 0.6V. However, the

best output response achieved at V_{DD}=0.4V justifies the proposed heterostructure's potentiality for low-power applications.

The effects of the ferroelectric stacked gate oxide over the strained Si-On-Insulator (SOI) TFET structure were investigated by Kumar et al. [1.80]. The work revealed a device of sub-30 nm dimension having a subthreshold slope as low as 10mV/decade at V_{DD} = 0.5 V. A stacked gate architecture has been implemented with ferroelectric oxide and SiO_2 by exploiting PbO_3 (PZT) as the ferroelectric element. SiO_2 of 0.7nm has been merged with 1nm PZT to introduce a high dielectric constant to the device for improved coupling of gate electric field over the channel. The device's charge trapping and leakage phenomena are assumed to be the same as conventional TFET since the Si channel is not in direct contact with PZT due to the stack-gate geometry.

Kurniawan et al. [1.81] analyzed the impact of tunneling window over the performance of a Ge-Si heterojunction TFET nanowire. A high saturation current for the Tunneling transistor, required for circuit application, depends on the transmission probability. Hence, selecting the BTBT model for indirect bandgap semiconductors (i.e., Si, Ge, etc.) is pivotal for simulation purposes. Ge constructed a heterostructure with a larger tunneling window with a better ON/OFF current ratio and steeper subthreshold slope as a lower bandgap material.

A compact 2D modeling of a Si-Ge DMDG Vertical t-shaped TFET is presented by Singh and Raj [1.82]. The presented model well addressed the physics underlying the novel device structure along with bandgap and work function engineering. Moreover, the model was validated against different parameter variations, including mole fraction of Ge/Si, oxide thickness, the dielectric constant of high-k dielectric, gate work functions, and compound materials. The proposed model was proved to be a reliable one that accurately predicted the electrical characteristics of the proposed devices.

A semiempirical SPICE behavioral model of SON TFET proposed by Hong et al. [1.83] included the tunneling concept in a Zener diode to characterize the drain current of the said device. The terminal voltage-dependent factors liable for the modulation of current are incorporated. In addition, the voltage-dependent parasitic capacitances are also taken into consideration deriving the model. The reported model of n-TFET captured the I-V characteristics with an accuracy of 10% tolerance and parasitic with 1% to 2% tolerance.

With the aggressive scaling of semiconductor devices in VLSI technology, minimizing interconnect length under the global routing phase appears as a more difficult research field

recently. The Rectilinear Steiner Minimal Tree (RMST) problem is one of the fundamental problems in the Global routing arena. Introduction of meta-heuristic algorithms [1.84, 1.85], like particle swarm optimization (PSO), firefly algorithms (FA), etc., to solve the RMST problem in the global routing optimization field, secured tremendous achievement in wire length optimization in VLSI technology. Several research articles have been published showing commendable endeavors in this field.

Khan et al. developed a model particle swarm optimization technique [1.86, 1.87] to solve the NP-complete issue of finding the Rectilinear Steiner Minimal Tree. To determine the price of the RSMT, Prim's algorithm underwent a strategic tweak. Therefore, conventional PSO has been modified with mutation operator, successfully able to reduce wire lengths up to 20%. The Firefly method and the Artificial Bee colony algorithm were combined in the same application during the second phase of the project. The Firefly algorithm outperforms the Artificial Bee colony optimization in every respect, including precision, convergent rate, flexibility and robustness. However, the FA is more computationally expensive than the ABC algorithm.

Liu et al. [1.88-1.91] presented a multilayer obstacle-avoiding architecture for RSMT construction based on Particle Swarm Optimization (PSO). The SMY construction is a significant part of any optimization problems like wire length optimization, congestion minimization and time delay estimation. An obstacle avoiding X-architecture SMT has been proposed in work. As a prerequisite number of options of routing around obstacles and vias are counted. In the second phase, particles are employed with the ability through edge transformation strategy to bypass the obstacles while eliminating the invalid solutions. According to the X-architecture SMT, an edge-vertex encoding strategy is formulated in the final phase. Further, a penalty mechanism is derived for the particles to make them possible to easily bypass the obstacle and subsequently reduce the generation of vias. The experimental outcomes of the work exhibit utmost supremacy of the proposed architecture associated with the optimization mechanism, handling such global optimization problems with obstacles.

Nallathambi and Rajaram [Nallathambi, 1.92-1.94] introduced PSO in power optimization strategy in VLSI interconnect driven routing. Interconnect power consumption is a growing challenges area in the sub-nanometer regime. The buffer insertion, buffer sizing and interconnect sizing are some crucial aspects in this regard. Optimum power management is formulated considering the shortest wire lengths, buffers' position, and wire size constraints. Particle swarm optimization has been effectively used to optimize power dissipation in every

stage of VLSI routing. The optimal power consumption is secured by identifying the shortest route from source to sink.

The work proposed by Nath et al. [1.95] presents a modified constricted PSO algorithm with mutation factor of Genetic algorithm delivering for wire length minimization identifying the best position for buffer insertion. The strategy was to reduce the interconnect delay computed through the iterative RLC delay model. Therefore, a comparative study has been made between the proposed optimizer and BPSO (Binary Particle swarm optimization) to find a better alternative for minimizing interconnect delay.

Several research efforts have been delivered towards the increased potentiality of the Firefly algorithm in the global optimization problem [1.96-1.99]. Tilahun et al. [1.100] reported a modification applied over the Firefly algorithm (FA) aiming for discrete optimization problems. The literature covered a detailed survey on applications of FA interacted with problems dealing with binary, integers and mixed variables.

Chakrabarty et al. [1.101] dealt with two popular heuristics: Firefly algorithm (FA) and Cuckoo search optimization (CSO) in extracting the characteristics parameters of dual-diode lumped solar cell circuit. The observations portray the performance superiority of the FA and CSO over other evolutionary techniques like PSO and DE in terms of convergence rate, precision, and excellent final solutions.

Pei [1.102] et al. propose a novel hybrid Firefly algorithm (HFA) to combine the advantages of both the Firefly algorithm (FA) and Differential Evolution (DE). To encourage the population, exchange of information, and improve search efficiency, FA and DE are run concurrently. A wide range of carefully chosen benchmark functions is used to assess the effectiveness and performance of the proposed algorithm. These functions can be divided into two categories: unimodal and multimodal. The experimental results indicate that the proposed approach performs better in terms of avoiding local minima and speeding up convergence than the original Firefly algorithm (FA), differential evolution (DE), and particle swarm optimization (PSO).

From the outline of the above discussion, it can be summarized that plenty of research scopes exist regarding the formulation of new compact models based on improvised device structures that can mitigate the adverse short channel effects (SCEs) without compromising the device performance. Therefore, the future nanoscale VLSI device should have the merit of higher scalability, variable-aware design structure, and better robustness. Moreover, the

nanodevices should meet the demand of low power, high speed, and low-cost criteria of future generation nodes and bring down the computation complexity of backend VLSI design at the same time.

1.4. Organization of Thesis

The thesis is organized in different chapters comprising proposals of non-conventional device structures compatible with CMOS logic for advanced device performance. Analytical models of the devices are developed to characterize their electrostatics and validated with numerical simulation data. Device-circuit interaction has been demonstrated to evaluate the circuit performance of modern VLSI devices. Finally, the backend VLSI design has been taken into account for further improvement of the VLSI circuit as an end product.

Chapter 1 provides deep insight into the VLSI scaling trend from the time it started and possible solutions that the research world has adopted to spin the wheel of the technological growth of microelectronics industries. The contemporary research outcomes and course of exploitation have been the driving force behind the suitable persuasion of efforts towards finding modern, trendy semiconductor devices and appropriate optimization tools for the futuristic node of VLSI design.

Chapter 2 explained the journey of semiconductor device physics, starting from long channel MOSFET to short channel geometries with their shortcoming. Therefore the technology paradigm shifted in finding non-conventional devices like Junctionless FETs (JL FETs) and Tunnel Field Effect Transistors (TFETs) of advanced performance. The chapter also delivers the background of VLSI physical design as a platform for complex global routing problems in detail with the possible approach to solutions

An analytical 2-D model of a heterojunction tunnel field effect transistor (HTFET) with stack gate oxide is shown in **Chapter 3.** Bandgap engineering is used to improve performance by utilising Germanium as the source material and Silicon as the channel and drain materials. The generated model carefully looked at the energy band, surface potential, electric field, and drain current of the device. In comparison to heterostructures of a comparable design, the suggested optimised device shape offers remarkably low OFF current (order of 10-18 A/um), moderately strong ON current (5x10-5 A/um), a sharp sub-threshold slope (20 mV/decade), and an excellent ON-OFF current ratio (order of 1013). The suggested device has an extremely low threshold voltage, even less than 0.1 V, making it an appropriate replacement for MOSFET in

a CMOS-like digital circuit. As a result, the performance of the proposed device's resistive inverter circuit is compared to that of a CMOS inverter with a 45nm technology node. In terms of power dissipation, propagation delay, and power-delay product, the inverter circuit based on the proposed heterojunction tunnel FET performs better than the CMOS inverter (PDP).

Chapter 4 shows a 2-D analytical drain current model for a stacked gate-oxide tri-metal double gate (TMDG) TFET with a graded channel. The Poisson's equation for surface potential in the channel region has been solved using the parabolic approximation approach with appropriate boundary conditions. In order to get the drain current expression, the tunnelling generation rate is therefore integrated over the source-channel junction region. The suggested model shows how a graded channel may operate as a barrier at the channel region to lessen leakage current in both the ON and OFF states. Band-to-band tunnelling is accelerated by high doping concentration at the source-channel junction, which lowers the subthreshold slope. Better outcomes in terms of the ION/IOFF ratio and SS are obtained by carefully selecting the work function for the gate electrodes. Additionally, the stack gate topology offers less leakage current and improved gate control over the channel region. In the first section of the work, the analytical outcomes of the suggested model have been verified using TCAD simulation data.

The performance improvement of a double gate p-n-p-n (DG p-n-p-n) TFET structure that has been upgraded with hetero-gate dielectric materials is covered in the following section. HfO2 is used to create the source side of the oxide material's hetero gate dielectric, followed by SiO2 for the drain side. By adding high-k spacers to the source and drain sides of the gate oxide, the same structure is further modified. To track the differences in performance, hafnium dioxide (HfO2) and titanium dioxide (TiO2) have been used as spacers. At room temperature, the suggested structure displays a significant increase in Ion current, reduced Ambipolar conduction, and a substantially lower Subthreshold Swing (SS).

Chapter 5 For potential radiation-sensitive applications, it was suggested to use a Core-Shell Junctionless MOSFET as a RADFET dosimeter. To explore the electrostatic behaviours of the suggested device under post-irradiation conditions, analytical models of the surface potential, drain current, and threshold voltage are built. The threshold voltage shift is used to determine the sensitivity for a variety of applied doses. The results when compared to recent literature show that our suggested gadget performs better in terms of sensitivity. With a sensitivity of 2.03mV/Gy throughout a large radiation dosage range of 300Gy to 30,000Gy, it displays a linear sensitivity curve. In addition, when compared to the simulation outcomes produced by the SILVACO TCAD 3D device simulator, the analytical model accurately represents the

properties of the device. The Core-Shell Junctionless RADFET dosimeter is thus suggested as a promising candidate for upcoming VLSI CMOS technology.

Chapter 6 In the context of VLSI global routing, provides a self-adaptive mechanism for controlling the acceleration coefficient of PSO and evaluates its performance in comparison to the current acceleration coefficient controlled PSO variant in various distribution topologies of terminal nodes in a specified search space. We also look into the resilience and path minimizing capacity of the PSO variant with the constriction factor. Additionally, we provide a novel method for genetically changing the PSO and contrast the outcomes with inertia-weighted PSO and traditional FA.

Chapter 7 summarizes the outcomes of the research works portrayed in the dissertation and speculates the future prospects/opportunities that would be open up through the present work.

Reference

1.1. Shockley, W. "The path to the conception of the junction transistor," *IEEE Transactions on Electron Devices*, vol. 23, pp. 597–620, 1976.

1.2. Kilby, J. S. "Turning Potential Into Realities: The Invention of the Integrated Circuit," http://nobelprize.org/nobel_prizes/physics/laureates/2000/kilby-lecture.pdf, 2000.

1.3. Sergey Edward Lyshevski (Editor), "Nano and Molecular Electronics: Hand Book", CRC Press, Taylor & Francis, NW, 2007.

1.4. Shunri Oda, David Ferry," Silicon Nanoelectronics", CRC Press, Taylor & Francis, NW, 2006.

1.5. "Technology roadmap for nanoelectronics,", [Online]. Available: http://www. cordis.lu/ist/fetnid.htm, published by European Commission IST programme on Future and Emerging Technologies, Nov. 2000.

1.6. Moore, G. E. "Cramming more components onto integrated circuits", *Reprinted from Electronics*, vol. 38, no.8, pp. 114-117, 1965.

1.7. Dennard, R. H. et al. "Design of ion-implanted MOSFET's with very small physical dimensions," *IEEE J. Solid-State Circuits*, vol. 9, pp. 256–268, 1974.

1.8. Thompson, S. E. et al. "A 90-nm logic technology featuring strained-silicon," *IEEE Trans. Electron Devices*, vol. 51, no. 11, pp. 1790–1797, 2004.

1.9. Chau, R., et al. "High-k/metal-gate stack and its MOSFET characteristics," *IEEE Electron Device Letters*, vol. 25, no.6, pp. 408–410, 2004. 32 nm node.

1.10. Sugii, N. "Road to Vmin=0.4V LSIs with least-variability FDSOI and back-bias control," *SOI Conference, 2011 IEEE International*, pp. 1-19, 2011.

1.11. Wu, S. Y. et al., "A 7nm CMOS platform technology featuring 4th generation FinFET transistors with a 0.027μm2 high density 6-T SRAM cell for mobile SoC applications," *IEEE International Electron Devices Meeting (IEDM)*, pp. 2.6.1-2.6.4, 2016.

1.12. Kevin F. Brennan, April S. Brown, "Theory of Modern Electronic Semiconductor Devices, John Wiley & Sons, Inc., New York, 2002.

1.13. Colinge JP. Silicon on insulator technology: materials to VLSI. 2nd ed. Norwell, MA: Kluwer: Kluwer Academic Publishers; 1997.

1.14. M.Current, S.Bebell, I.Malik, L.Feng, F.Henley, "What is the future of sub-100nm CMOS: Ultrashallow junctions or ultrathin SOI?" Solid State Technology, 2000; 43.

1.15. S. Deb, N. B. Singh, D.Das, A.K.De, S.K.Sarkar, "Analytical model of Threshold Voltage and Sub-threshold Slope of SOI and SON MOSFETs: A comparative study", Journal of Electron Devices, Vol. 8, pp. 300-309, 2010.

1.16. Ferain, I., Colinge, C. A. and Colinge, J. P. "Multigate transistors as the future of classical metal-oxide-semiconductor field-effect transistors", *Nature*, vol. 479, pp. 310–316, 2011.

1.17. Courtland, R. "Transistors could stop shrinking in 2021," *in IEEE Spectrum*, vol. 53, no. 9, pp. 9-11, Sep. 2016.

1.18. "http://www.itrs2.net/," International Technology Roadmap for Semi- conductors, 2015.

1.19. Nainai, A. et al. "Engineering of Strained III-V Heterostructures for High Hole Mobility," *IEEE International Electron Device Meeting*, pp. 1-4, 2009.

1.20. Tsipas, P. and Dimoulas, A., "Modeling of negative charged states at the Ge surface and interfaces," *Appl. Phys. Lett*., vol. 94, 012114, 2009.

1.21. Y.-J. Lee *et al.*, "A novel junctionless FinFET structure with sub-5 nm shell doping profile by molecular monolayer doping and microwave annealing," in *IEDM Tech. Dig.*, Dec. 2014, pp. 32.7.1–32.7.4, doi: 10.1109/IEDM.2014.7047158.

1.22. Y.-J. Lee *et al.*, "High performance poly Si junctionless transistors with sub-5 nm conformally doped layers by molecular monolayer doping and microwave incorporating CO2 laser annealing for 3D stacked ICs applications," in *IEDM Tech. Dig.*, Dec. 2015, pp. 6.2.1–6.2.4, doi: 10.1109/IEDM.2015.7409638.

1.23. Ionescu, A. M. and Riel, H. "Tunnel field-effect transistors as energy- efficient electronic switches," *Nature*, vol. 479, pp. 329–337, November 2011.

1.24. Kim, N. S. et al., "Leakage current: Moore's law meets static power," in *Computer*, vol. 36, no. 12, pp. 68-75, Dec. 2003.

1.25. Ionescu, A. M. et al., "Ultra low power: Emerging devices and their benefits for integrated circuits," *Electron Devices Meeting (IEDM), IEEE International*, pp. 16.1.1-16.1.4, 2011.

1.26. Nikonov, D. E. and Young, I. A. "Uniform methodology for benchmarking beyond-CMOS logic devices," *in Technical Digest -International Electron Devices Meeting, IEDM*, pp. 25.4.1-25.4.4, 2012.

1.27. J.-M. Ho, G. Vijayan, and C.K. Wong, "New algorithms for the rectilinear Steiner tree problem", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 1990, pp. 185-193.

1.28. G. Beni and J. Wang, Swarm intelligence in cellular robotic systems. In NATO Advanced Workshop on Robots and Biological Systems, Il Ciocco, Tuscany, Italy, 1989.

1.29. Arpita Ghosh and Subir Kumar Sarkar, "Improved Small-Signal Model of Single-Electron Transistor," in IEEE Transactions on Nanotechnology, vol. 17, no. 6, pp. 1244-1251, Nov. 2018.doi: 10.1109/TNANO.2018.2871690.

1.30. Arpita Ghosh, Amit Jain, S.Gharami and Subir Kumar Sarkar , "Small Signal model for Single electron Transistor: Part 1", in Journal of Computational Electronics, Springer, DOI: 10.1007/s10825-017-0971-1, February 2017

1.31. Anup Sarkar, Sk. Halim, Ankush Ghosh, and Subir kumar Sarkar, "Implementation of PMN-PT/Ni based NOR Gate with Biaxial Anisotropy off ultra low energy dissipation", in Journal of Nanoelectronics and Optoelectronics,Vol.12,pp-1-6, January,2017.

1.32. Anup Sarkar, Pranab k Dutta, Ankush Ghosh, Sudhabindu Ray and Subir Kumar Sarkar, "Implementation of Universal Gates (NAND) based on nano-magnetic logic using multiferroics", in Quantum Matter , American Scientific Publishers,Vol-5,No.4,pp-1-5,2016

1.33. A. Ghosh, A. Jain, N. B. Singh, and S. K. Sarkar, "Stability aspects of single electron threshold logic based 4 bit carry look ahead adder," Proceedings of the 2015 Third International Conference on Computer, Communication, Control and Information Technology (C3IT), 2015, doi: http://10.1109/c3it.2015.7060138.

1.34. Saheli Sarkhel and Subir Kumar Sarkar, "A compact quasi 3D threshold voltage modeling and performance analysis of a novel linearly graded binary metal alloy quadruple gate MOSFET for subdued short channel effects", Superlattices and Microstructures, Elsevier, Vol. 82, pp-293-302, 2015.

1.35. S. G. Narendra, "Challenges and design choices in nanoscale CMOS," ACM Journal on Emerging Technologies in Computing Systems, vol. 1, no. 1, 2005.

1.36. Srinivasa R. Banna, Philip C. H. Chan, Ping K. KO, Cuong T. Nguyen and Mansun Chan, Threshold Voltage Model for Deep- Submicrometer Fully Depleted SOI MOSFET's, IEEE Transactions on Electron Devices, Vol. 42, No. 11, 1949 (1995).

1.37. Yuhua Cheng and Tor A. Fjeldly, Unified Physical I-V Model Including Self-Heating Effect for Fully Depleted SOIMOSFET's, IEEE Transactions On Electron Devices, Vol. 43, No. 8, 1291 (1996).

1.38. J. B. Roldán, F. Gámiz J. A. López-Villanueva and P. Cartujo-Cassinello, Deep Submicrometer SOI MOSFET Drain Current Model Including Series Resistance, SelfHeating and Velocity Overshoot Effects, IEEE Electron Device Letters, Vol. 21, No. 5, 239 (2000).

1.39. M. Y. Hammad and D. K. Schroder, "Analytical modeling of the partially-depleted SOI MOSFET," in IEEE Transactions on Electron Devices, vol. 48, no. 2, pp. 252-258, Feb. 2001, doi: 10.1109/16.902723.

1.40. Kim, Keunwoo & Fossum, Jerry. (2001). Double-gate CMOS: Symmetrical- versus asymmetrical-gate devices. Electron Devices, IEEE Transactions on. 48. 294 - 299. 10.1109/16.902730.

1.41. G. Katti, N. DasGupta and A. DasGupta, "Threshold Voltage model for mesa-isolated small geometry fully depleted SOI MOSFETs based on analytical solution of 3-D

Poisson's equation," in IEEE Transactions on Electron Devices, vol. 51, no. 7, pp. 1169-1177, July 2004, doi: 10.1109/TED.2004.830648.

1.42. Saheli Sarkhel, Bibhas Manna and Subir Kumar Sarkar, "Threshold voltage modeling and performance comparison of a novel linearly graded binary metal alloy gate junctionless double gate metal oxide semiconductor field effect transistor", Indian Journal of Physics, Springer, Vol. 89, Issue 6, pp.-593-598, DOI 10.1007/s12648-014-0584-5, June 2015.

1.43. Sourav Naskar and Subir Kumar Sarkar, "A quantum analytical model for inversion charge & threshold voltage of Short channel DMDG SON MOSFET", IEEE Transactions on Electron Devices, vol.60, no.9, pp.2734,2740, Sept. 2013.

1.44. Liu, Keng-Ming & Lee, Cheng-Kuei. (2013). Investigation of the random dopant fluctuations in 20-nm bulk MOSFETs and silicon-on-insulator FinFETs by ion implantation Monte Carlo simulation. International Journal of Nanotechnology. 11. 263-266. 10.1109/INEC.2013.6466018

1.45. Saheli Sarkhel, Bibhas Manna, P.K. Dutta and Subir Kumar Sarkar, "Analytical Model for performance comparison of a nano scale dual material double gate Silicon on insulator SOI and Silicon on nothing SON MOSFET," Journal of Nano engineering and Nano manufacturing, ASP, Vol.4, No.3, pp-182-188, September 2014.

1.46. Sanjoy Deb, Saptarsi Ghosh, N Basanta Singh and Subir Kumar Sarkar, "Twodimensional Analytical Model Based Comparative Threshold Performance Analysis of SOI-SON MOSFET" Journal of Semiconductor, IOP, Vol. 32 (10), 2011

1.47. Jeffrey W. Sleight and Rafael Rios, A Continuous Compact MOSFET Model for Fullyand Partially-Depleted SOI Devices, IEEE Transactions On Electron Devices, Vol. 45, No. 4, 821 (1998)

1.48. F.Balestra, S.Christoloveanu, M.Benachir, J. Brini, T.Elewa, "Double-gate silicon-oninsulator transistor with volume inversion: A new device with greatly enhanced performance," IEEE Electron Device Lett., vol. EDL-8, pp. 410-412, 1987

1.49. K. K. Young, "Short-channel effects in fully depleted SOI MOSFET's," IEEE Trans. Electron Devices, Vol. 36, pp. 399-402, 1989

1.50. S. Deb, N. B. Singh, D.Das, A.K.De, S.K.Sarkar, "Analytical model of Threshold Voltage and Sub-threshold Slope of SOI and SON MOSFETs: A comparative study", Journal of Electron Devices, Vol. 8, pp. 300-309, 2010

1.51. Sourav Naskar and Subir Kumar Sarkar, "A quantum analytical model for inversion charge & threshold voltage of Short channel DMDG SON MOSFET", IEEE Transactions on Electron Devices, vol.60, no.9, pp.2734,2740, Sept. 2013.

1.52. Pranab Kishore Dutta, Bibhas Manna and Subir Kumar Sarkar, "Analytical modeling of linearly graded alloy material gate recessed ultra thin body source/drain SON MOSFET", Superlattices and Microstructures, Vol. 77, pp-64-75, 2015.

1.53. Saheli Sarkhel, Bibhas Manna and Subir Kumar Sarkar, "A Compact Two Dimensional Analytical Modeling of Nanoscale Fully Depleted Dual Material Gate strained SOI/SON MOSFETs for subdued SCEs," Journal of Low Power Electronics, ASP Volume 10, Number 3, pp. 383-391, September 2014.

1.54. Saheli Sarkhel, Navjeet Bagga and Subir Kumar Sarkar ," A compact analytical model ofbinary metal alloy silicon-on-nothing (BMASON) tunnel FET with interface trapped charges", in Journal of Computational Electronics, Springer, DOI 10.1007/s10825-017-1030-7, July 2017.

1.55. Pritha Banerjee and Subir Kumar Sarkar, "3-D analytical modeling of high-k gate stack dual-material tri-gate strained silicon-on-nothing MOSFET with dual-material bottom gate for suppressing short channel effects", in Journal of Computational Electronics, Springer, Vol.16.No.3,pp-631-639,May 2017.

1.56. Pritha Banerjee, Priyanka Saha and Subir Kumar Sarkar," Two dimensional analytical modeling of a high-K gate stack triple-material double gate strained silicon-on-nothing MOSFET with a vertical Gaussian doping", in Journal of Computational Electronics, Springer, DOI 10.1007/s10825-017-1089-1, November 2017.

1.57. Tiya Dey Malakar ,Partha Bhattacharyya and Subir Kumar Sarkar , "Analytical surface potential modeling based small signal analysis and RF performance characterization of DMG SOI MOSFET for better RFIC application", IETE Technical Review,pp-1-10, February, 2017

1.58. M. Shur, "Split-gate field-effect transistor," Appl. Phys. Lett., Vol. 54, No. 2, pp. 162–164, Jan. 1989

1.59. X. Zhou and W. Long, "A novel hetero-material gate (HMG) MOSFET for deepsubmicronULSI technology," IEEE Transaction on Electron Devices, vol. 45, no. 12, pp.2546–2548, Dec. 1998.

1.60. Pritha Banerjee, Aman Mahajan and Subir Kumar Sarkar, "2-D Analytical Modeling of Dual-Material Double Gate Silicon-On-Nothing MOSFET", published in Advances in Industrial Engineering and Management, Vol. 6, No.1, 11-16,2017

1.61. W. M. Reddick and G. A. J. Amaratunga, "Silicon surface tunnel transistor," Appl. Phys. Lett.67, 494 (1995).

1.62. Upasana, R. Narang, M. Saxena and M. Gupta, "Modeling and TCAD Assessment for Gate Material and Gate Dielectric Engineered TFET Architectures: Circuit-Level Investigation for Digital Applications," in IEEE Transactions on Electron Devices, vol. 62, no. 10, pp. 3348-3356, Oct. 2015, doi: 10.1109/TED.2015.2462743.

1.63. Sarkhel, S., Bagga, N. & Sarkar, S.K. Compact 2D modeling and drain current performance analysis of a work function engineered double gate tunnel field effect transistor. *J Comput Electron* 15**,** 104–114 (2016). https://doi.org/10.1007/s10825-015-0772-3

164. Priyanka Saha, Subir Kumar Sarkar,"Drain current modeling of proposed dual material elliptical Gate-All-Around heterojunction TFET for enhanced device performance", Superlattices and Microstructures, Volume 130, 2019, Pages 194-207, ISSN 0749-6036, https://doi.org/10.1016/j.spmi.2019.04.022.

1.65. R. M. Y. Ng, T. Wang, F. Liu, X. Zuo, J. He, and M. Chan, "Vertically stacked silicon nanowire transistors fabricated by inductive plasma etching and stress-limited oxidation," IEEE Electron Device Lett., vol. 30, no. 5, pp. 520–522, May 2009

1.66. S. Bangsaruntip, G. M. Cohen, A. Majumdar, and J. W.Sleight, "Universality of short-channel effects in undopedbody silicon nanowire MOSFETs," IEEE Electron Device Lett., vol. 31, no. 9, pp. 903–905, Sep. 2010.

1.67. Lining Zhang, Lin Li,Jin He and Mansun Chan,"Modeling Short-Channel Effect of Elliptical Gate-All-Around MOSFET by Effective Radius", IEEE Electron Devices Letters, Vol. 32, No. 9, September 2011

1.68. Rounak Dutta and Subir Kumar Sarkar, "Analytical Modeling and Simulation based Optimization of Broken Gate TFET Structure for Low Power Applications",IEEE Transactions ON Electron Devices, Vol. 66, No. 8, August 2019

1.69. P. Saha and S. Kumar Sarkar, "Analytical Modeling of Ion Sensitive Broken Gate TFET for pH Sensing Applications," in IEEE Sensors Letters, vol. 4, no. 7, pp. 1-4, July 2020, Art no. 2000304, doi: 10.1109/LSENS.2020.2999207.

1.70. Priyanka Saha, Subir Kumar Sarkar, "Drain current characterization of dielectric modulated split gate TFET for bio-sensing application", Materials Science in Semiconductor Processing, Volume 124, 2021, 105598, ISSN 1369-8001, https://doi.org/ 10.1016/ j.mssp. 2020.105598.

1.71. S. Mukhopadhyay, D. Sen, B. Goswami and S. K. Sarkar, "Performance Evaluation of Dielectrically Modulated Extended Gate Single Cavity InGaAs/Si HTFET Based Label-Free Biosensor Considering Non-Ideal Issues," in IEEE Sensors Journal, vol. 21, no. 4, pp. 4739-4746, 15 Feb.15, 2021, doi: 10.1109/JSEN.2020.3033576.

1.72. A. Sharma, A. A. Goud and K. Roy, "GaSb-InAs n-TFET With Doped Source Underlap Exhibiting Low Subthreshold Swing at Sub-10-nm Gate-Lengths," in IEEE Electron Device Letters, vol. 35, no. 12, pp. 1221-1223, Dec. 2014, doi: 10.1109/LED.2014.2365413.

1.73. S. Kumar et al., "2-D Analytical Modeling of the Electrical Characteristics of Dual-Material Double-Gate TFETs With a SiO2/HfO2 Stacked Gate-Oxide Structure," in IEEE Transactions on Electron Devices, vol. 64, no. 3, pp. 960-968, March 2017, doi: 10.1109/TED.2017.2656630.

1.74. Dinesh Kumar Dash, Priyanka Saha and Subir Kumar Sarkar, "Analytical Modeling of Dielectric Engineered Strained DMDG-TFET", IET Circuits, Devices & Systems, DOI: 10.1049/iet-cds.2018.5293, June 2019

1.75. Dash, D.K., Saha, P. & Sarkar, S.K. 3-D Analytical Modeling of Triple Metal Tri-Gate Graded Channel High-k SON TFET for Improved Performance. *Silicon* 12, 2041–2052 (2020). https://doi.org/10.1007/s12633-019-00268-5

1.76. Disha Bhattacharjee, Bijoy Goswami, Dinesh Kumar Dash, Ayan Bhattacharya and Subir Kumar Sarkar," Analytical Modelling and Simulation of Drain Doping Engineered Splitted Drain Structured TFET and its Improved Performance in Subduing Ambipolar Effect", IET Circuits, Devices & Systems, DOI: 10.1049/iet-cds.2018.5261, May 2019

1.77. Dinesh Kumar Dash, Priyanka Saha, Aman Mahajan, Tripty Kumari and Subir Kumar Sarkar,"3D Analytical Modeling and Electrical Characteristics Analysis of Gate Engineered

SiO2/HfO2 stacked Trigate TFET", Indian Journal of Physics, Springer, DOI: 10.1007/s12648-019-01446-2, March 2019

1.78. S. Ahish, D. Sharma, Y. B. Nithin Kumar and M. H. Vasantha, "Performance Enhancement of Novel InAs/Si Hetero Double-Gate Tunnel FET Using Gaussian Doping," in IEEE Transactions on Electron Devices, vol. 63, no. 1, pp. 288-295, Jan. 2016, doi: 10.1109/TED.2015.2503141.

1.79. K. Alam, "Orientation Engineering for Improved Performance of a Ge-Si Heterojunction Nanowire TFET," in IEEE Transactions on Electron Devices, vol. 64, no. 12, pp. 4850-4855, Dec. 2017, doi: 10.1109/TED.2017.2766681.

1.80. M. Kumar and S. Jit, "Effects of Electrostatically Doped Source/Drain and Ferroelectric Gate Oxide on Subthreshold Swing and Impact Ionization Rate of Strained-Si-on-Insulator Tunnel Field-Effect Transistors," in IEEE Transactions on Nanotechnology, vol. 14, no. 4, pp. 597-599, July 2015, doi: 10.1109/TNANO.2015.2426316.

1.81. Kurniawan, Erry & Yang, Shang-Yi & Thirunavukkarasu, Vasanthan & Wu, Yung-Chun. (2017). Analysis of Ge-Si Heterojunction Nanowire Tunnel FET: Impact of Tunneling Window of Band-to-Band Tunneling Model. Journal of The Electrochemical Society. 164. E3354-E3358. 10.1149/2.0371711jes.

1.82. Singh, Shailendra & Raj, Balwinder. (2021). Analytical Modelling and Simulation of Si-Ge Hetero-Junction Dual Material Gate Vertical T-Shaped Tunnel FET. Silicon. 13. 10.1007/s12633-020-00505-2.

1.83. Y. Khatami and K. Banerjee, "Steep Subthreshold Slope n- and p-Type Tunnel-FET Devices for Low-Power and Energy-Efficient Digital Circuits," in IEEE Transactions on Electron Devices, vol. 56, no. 11, pp. 2752-2761, Nov. 2009, doi: 10.1109/TED.2009.2030831.

1.84. Pallabi Bhattacharya ,Abhinandan Khan, Souvik Sarkar and Subir Kumar Sarkar," An Artificial Bee Colony Optimization Based Global Routing Technique ",International Conference On Control ,Instrumentation, Energy, Communication(CIEC 14) Organized By Department Of Applied Physics, University Of Calcutta, IEEE Kolkata Section, 31st January to 2nd February, 2014.

1.85. Subhrapratim Nath and Subir Kumar Sarkar, "Metaheuristics-based routing optimisation, balanced workload distribution and security strategy in IoT environment" International Journal

of Advanced Intelligence Paradigms, Inderscience,Vol 9, Issue 1, https://doi.org/10.1504/IJAIP.2021.114586, April, 2021.

1.86. Abhinandan Khan, Sulagna Laha and Subir Kumar Sarkar, "A Novel Particle Swarm Optimization approach for VLSI Routing", IEEE International Advance Computing Conference, Dr. A.K Garg Institute, Ghaziabad, 22-23 February, 2013.

1.87. Abhinandan Khan, Pallabi Bhattacharya and Subir Kumar Sarkar," A Swarm Based Global Routing Optimization Scheme", International Conference On Advances In Electrical Engineering (ICAEE'2014), 9-11 January, 2014.

1.88. L. Zhang, Y. Huang, W. Chen, W. Guo and G. Liu, "X-architecture Steiner Tree Algorithm with Limited Routing Length inside Obstacle," 2021 11th International Conference on Information Technology in Medicine and Education (ITME), 2021, pp. 152-156, doi: 10.1109/ITME53901.2021.00040.

1.89. Z. Zhuang, X. Huang, G. Liu, W. Guo, W. Qian and W. -H. Liu, "ALIF Router: A Practical Architecture-Level Inter-FPGA Router for Logic Verification," 2021 Design, Automation & Test in Europe Conference & Exhibition (DATE), 2021, pp. 1570-1573, doi: 10.23919/DATE51398.2021.9474255.

1.90. W. Zhu, X. Zhang, G. Liu, W. Guo and T. -C. Wang, "MiniDeviation: An Efficient Multi-Stage Bus-Aware Global Router," 2020 International Symposium on VLSI Design, Automation and Test (VLSI-DAT), 2020, pp. 1-4, doi: 10.1109/VLSI-DAT49148.2020.9196219.

1.91. H. Tang, G. Liu, X. Chen and N. Xiong, "A Survey on Steiner Tree Construction and Global Routing for VLSI Design," in IEEE Access, vol. 8, pp. 68593-68622, 2020, doi: 10.1109/ACCESS.2020.2986138.

192. Nallathambi, G. & Rajaram, S.. (2014). Power aware VLSI routing using particle swarm optimization for green electronics. 1-6. 10.1109/ICGCCEE.2014.6922211.

1.93. Nallathambi, G. & Rajaram, S.. (2013). A particle swarm optimization approach for low power very large scale integration routing. Journal of Mathematics and Statistics. 10. 58-64. 10.3844/jmssp.2014.58.64.

1.94. Nallathambi, G. & Rajaram, S.. (2013). A particle swarm optimization approach for low power very large scale integration routing. Journal of Mathematics and Statistics. 10. 58-64. 10.3844/jmssp.2014.58.64.

1.95. Subhrapratim Nath, Pinaki Prasad Guha Neogi, Jamuna Kanta Sing and Subir Kumar Sarkar, "VLSI Routing Optimization based on modified Constricted PSO with Iterative RLC Delay model" IEEE International Conference on Current Trends towards Converging Technologies, Coimbatore, India. March 1-3, 2018

1.96. X. S. Yang, "Firefly algorithms for multimodal optimization," in *Proceedings of the 5th International Conference on Stochastic Algorithms: Foundation and Applications (SAGA '09)*, vol. 5792 of *Lecture notes in Computer Science*, pp. 169–178, 2009.

1.97. M. Negnevitsky, *Artificial Intelligence: A Guide To Intelligent System*, Henry Ling Limited, Harlow, England, 2005.

1.98. X. S. Yang, *Nature-Inspired Metaheuristic Algorithm*, Luniver Press, Beckington, UK:, 2nd edition, 2010.

1.99. T. Apostolopoulos and A. Vlachos, "Application of the firefly algorithm for solving the economic emissions load dispatch problem," *International Journal of Combinatorics*, vol. 2011, Article ID 523806, 23 pages, 2011.

1.100. Tilahun, S.L., Ngnotchouye, J.M.T. Firefly algorithm for discrete optimization problems: A survey. *KSCE J Civ Eng* 21**,** 535–545 (2017). https://doi.org/10.1007/s12205-017-1501-1

1.101. Tapas Chakrabarti, Tyajodeep Chakrabarti, Udit Sharma and Subir Kumar Sarkar, "Extraction of Efficient Electrical Parameters of SolarCell using Firefly and Cuckoo Search Algorithm", in IEEE-7th India' International Conference on Power Electronics' (IICPE) 2016, 17th-19th November, Thapar University, Punjab, India, Volume: IEEE Xplore.

1.102. W. Pei, G. Huayu, Z. Zheqi and L. Meibo, "A Novel Hybrid Firefly Algorithm for Global Optimization," 2019 IEEE 4th International Conference on Computer and Communication Systems (ICCCS), 2019, pp. 164-168, doi: 10.1109/CCOMS.2019.8821670.

CHAPTER 2

Semiconductor Devices and VLSI Physical Design: The Basics

2.1 Introduction

Over the last fifty years, the VLSI industry has been experiencing tremendous growth fixated by the consistent device miniaturization that increases the packaging density, ensuring the

reduction of fabrication costs. The eventual fate of VLSI, as anticipated by Gordan Moore around 1965, with proportional device scaling likewise depicts its encouragement through high operating speed with the least power utilization [2.1]. Notwithstanding the forceful downscaling of traditional MOS devices experiences the constraints of a complex fabrication process with related expenditure. In addition, the underlying device of the quantum mechanical concept is essential to handle nano-devices in circuit applications [2.2]. Nevertheless, the VLSI circuits, incorporating these devices, don't respond satisfactorily. Therefore, a significant research endeavor has been pursued while finding alternative MOS architecture, that can withstand the scaling limitations with consequent propulsion of device downsizing without affecting the circuit performances. Further, nano-scale devices can be divided broadly into two classes. One group includes of quantum wire, quantum well, and quantum dot-based devices like spintronics, HEMT, SET, etc. The second group deals with the structural innovations of the existing nano-scale devices like Ge-based devices, Carbon nano-tube FETs, Nanowire FETs, heterojunction-based FETs, strained engineered FETs, structurally refined FETs, etc. Ever-ending research endeavors in the quest for such unconventional devices can fortify the course of Moore's scaling and acknowledge outstanding functionality while avoiding inescapable second-order effects like hot carrier effect (HCE), punch through, gate-induced drain leakage (GIDL), drain-induced barrier lowering (DIBL), threshold voltage roll-off, etc. to mention a few [2.3]. The architecture, operating principle, and analytical models of the said devices are principally different from the conventional ones and have been dealt with in the present dissertation emphasizing the possible options to continue device scaling with suitable device optimization.

2.2 Semiconductor Device

Metal Oxide Semiconductor Field Effect Transistor has gained unparallel popularity amongst its group since the early 1970s, owing to its simple geometry, fabrication flexibility and cost, high input impedance, commendable operational speed, and significant noise immunity. It is the basic building block for CMOS technology applicable in both digital and analog domains. This is a unipolar device. The current conduction of FETs is governed by the transportation of the majority carriers which offers exceptional noise immunity along with minor leakage current to the device. The spontaneous advancement regarding MOSFET scaling benefits the VLSI industries on large scale over the last fifty years. Hundreds of millions of transistors can be fabricated nowadays to produce integrated circuits under 100 nm technology nodes. Thus, the consumers and the industry

has been facilitated by the boon of cost-effective integrated circuits with superior performance. The propulsion of device downsizing with a subsequent rise in packaging density, driving the technology towards complex circuit layout, offered a sensational impulse to the computing capacity of the end products. The scenario leads to manufacturing electronic goods with unparallel reduced cost that fortify Moore's law causing the evolution in the semiconductor industry down the sub-micron to the sub-nanometer regime of today's technology. However, the aggressive device scaling gives rise to detrimental short channel effects leading to significant performance deterioration in the sub-100 nm device dimension. The challenges to improve performance and overcoming the constraints of the second-order effects has become the motivation of researchers in looking forward to inventing non-conventional nano-devices. The successive literature conceives the underlying physics of semiconductor devices starting from bulk MOSFET to ultra-scale nano-devices to satisfy the quest for low-power high-performance nano-device for future-generation VLSI circuits.

2.2.1 Overview of MOSFET

The two-terminal representation of a MOS capacitor is shown in Fig. 2.1. A tiny film of oxide is deposited between a metal and a semiconductor in the MOS capacitor, which simply has a gate and body terminal. Based on the applied gate bias, the semiconductor's surface behaves as a metallic sheet; the polarity and strength of the gate voltage determine the operational mode of the MOS capacitor i.e., accumulation, depletion, and inversion modes.

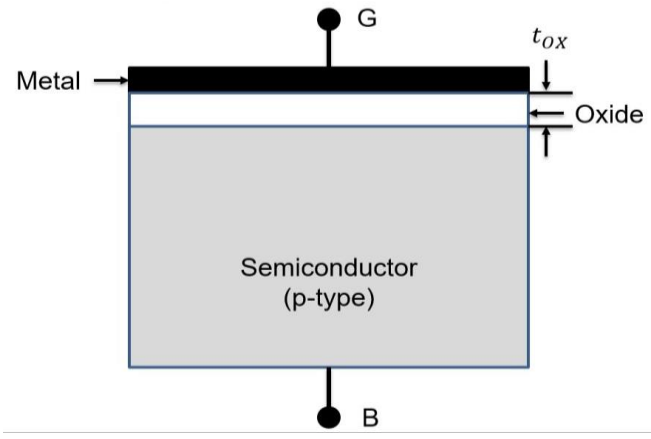


Fig. 2.1: Schematic view of MOS capacitor

An n-type MOSFET structure has been presented in Fig. 2.2. The symbols "L" and "W" stand for the device's channel length and width, respectively. The gate is electrically isolated from the

semiconductor channel by applying a dielectric layer between the channel and gate, constructing a voltage-controlled voltage device [2.4].

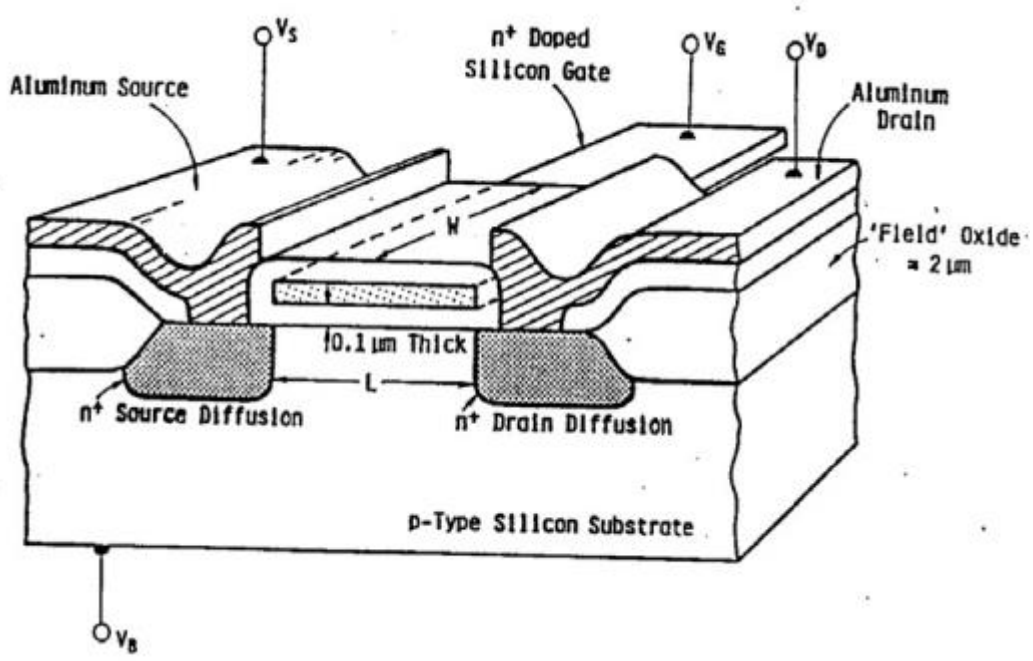


Fig. 2.2: Cross-sectional view of MOS Transistor [2.5]

The MOSFET can be divided into two groups based on the device structure: Depletion type (D-type) and Enhancement type MOSFET (E-type). A physical channel connects the source and drain of a D-MOSFET. For an n-type device, the supplied negative gate voltage draws in the positive holes. As a result of the recombination of e- - h+ pairs, the channel runs out of charge carriers. At a certain magnitude of positive gate voltage, the pinch-off condition occurs for the device, complying with the drain current to be '*zero*' and the device turned off. The device geometry with biasing, symbols, and output characteristics are manifested in Fig. 2.3, 2.4, and 2.5 [2.6] respectively.

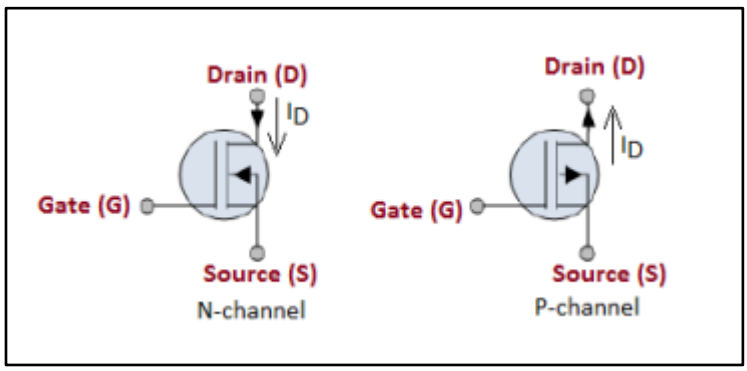


Fig. 2.3: Symbols of n and p-type Depletion type MOSFET

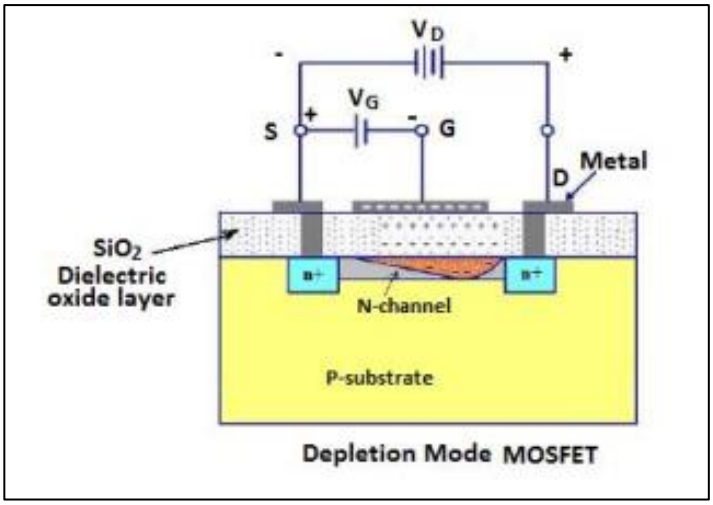


Fig. 2.4: Schematic view of a depletion-type n-channel MOSFET

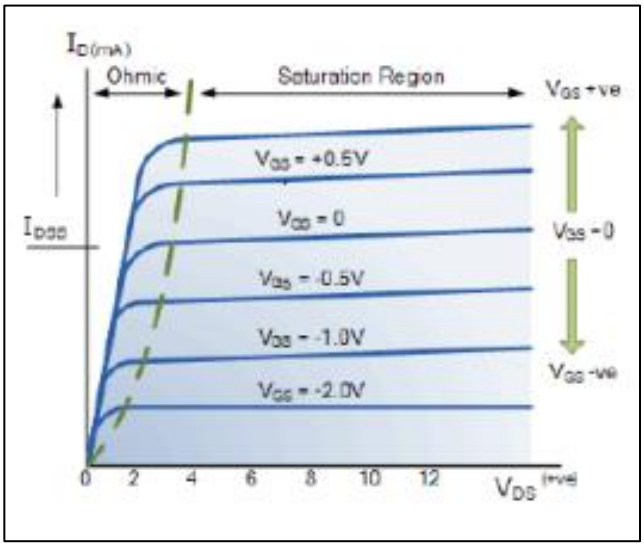


Fig. 2.5: Drain characteristics of a depletion-type n-channel MOSFET

On contrary, no channel region is physically present at the substrate for an E-MOSFET, between the source-drain region under no-bias condition i.e., gate voltage equal to zero. Since the holes are repelled and the electrons are unable to gather due to the screening effect of the stationary positive ions for an n-channel MOS, the substrate beneath the gate electrode initially becomes depleted of carriers when the gate electrode is biassed positively. Minority carriers and electrons build up at the substrate's surface as the gate voltage rises above the threshold voltage, forming an inversion layer known as a channel. Therefore, with an increase of gate bias, more and more carriers are attracted towards the channel, decreasing the channel resistance followed by increasing drain current through the device. The device, symbols, and output characteristics are depicted in Fig. 2.6, 2.7, and 2.8 respectively.

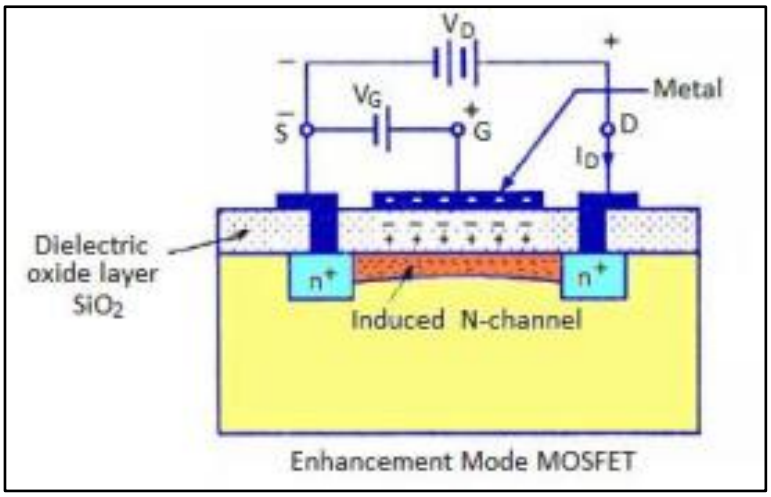


Fig. 2.6: Cross-sectional view of an Enhancement-type n-channel MOSFET

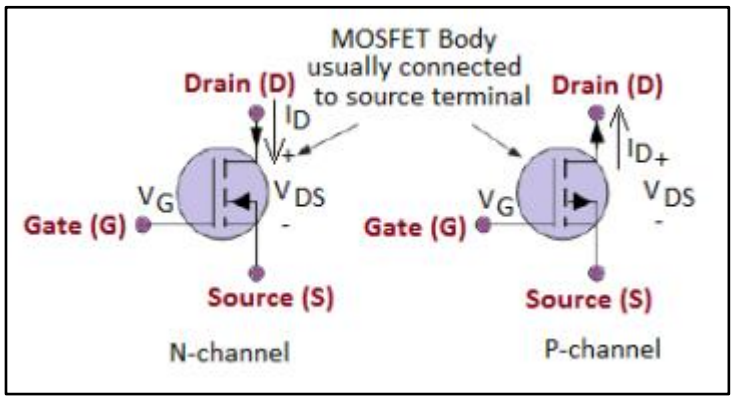


Fig. 2.7: Symbols of an n- and p-type Enhancement MOSFET

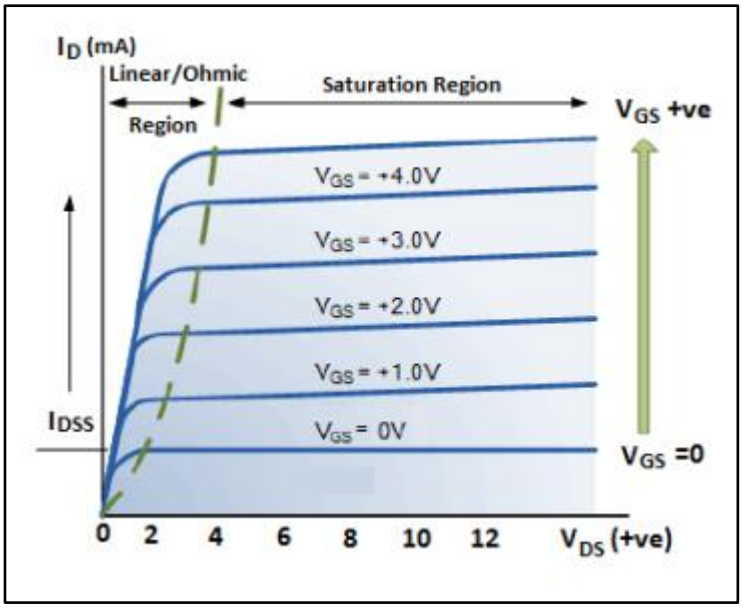


Fig. 2.8: Drain current characteristics of an Enhancement-type n-MOSFET

The linear or ohmic area, the saturation region, and the cut-off region are shown in Fig. 2.9 as the operating regions of an E-MOSFET. The gate voltage is more than the threshold voltage but less than the drain-to-source bias in the linear zone. When turned on, the gadget creates a channel between the source and drain. The component performs the function of a variable resistor under gate bias. The device's gate voltage for the saturation zone is higher than the threshold voltage but lower than the difference between the voltages at the drain and source. Once it reaches saturation (the maximum value), the drain to source current behaves like a continuous current source. Since the gate voltage is lower than the threshold voltage, the device was unable to construct a channel at the cut-off region. As a result, the device has no current flowing through it.

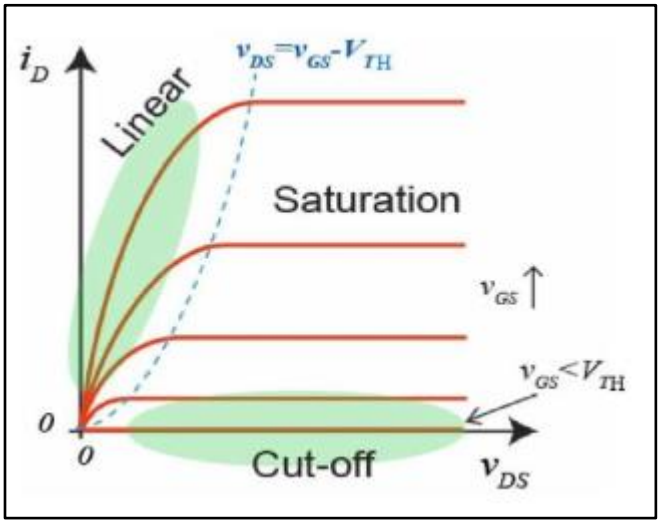


Fig. 2.9: Regions of operation an E-type n-MOSFET

2.2.2. MOSFET Models

The modeling of MOSFET devices deals with the underlying physics and the devices' characteristics under different working conditions. Moreover, the complex device structures stemming from the aggressive scaling led to several modeling approaches in characterizing the electrostatic behavior of MOSFETs [2.7 – 2.10].

i) Charged-Based Model:

A drain current-based model was formulated on the inversion charges across the channel region of the device. For example, EPFL, ACM, EKV, and Berkeley's BSIM 5 models followed this kind of approach, where a lesser number of fitting parameters are required for the empirical

expressions. The parameter extraction process for this model is comparatively easier and more popular in the low-power analog circuit design domain.

ii) Threshold Voltage-based model:

This is a piecewise modeling approach, precisely describing the weak and strong inversion characteristics of MOSFETs, demarcated by their threshold voltage. This is a simplified framework derived from Pao-Sah's benchmarked model. The well-established models, including BSIM1, BSIM2, BSIM3, BSIM42, Berkeley's LEVEL 1, LEVEL2, LEVEL 3, and Philips-MM9 MODEL are some examples of this category.

iii) Surface Potential based model:

The drain current equation is derived from the surface potential expression along with the channel length. With the aid of Poisson's equation, the surface potential is derived from the solution of the partial differential equation. its applications in RF circuits' simulation with excellent response to scaling-induced phenomenon modeling HiSIM 5, Philips MM11 and PSP belong to this surface potential-based model.

2.2.3 Analytical Modeling Approach of MOSFETs

The external gate bias is fixed to draw the inversion layer to the substrate's surface since the MOSFET's gate voltage efficiently regulates the charge flow of the device. The substrate of an n-type E-MOSFET is doped with p-type material. Therefore, to operate the MOSFET in inversion mode, a positive gate voltage is needed. At a gate voltage (V_{gs}) over the threshold voltage, a channel is formed (V_{th0}). After the channel has been established, a proper drain-to-source bias causes the charge carrier (electron) to drift from source to drain, which then causes current to flow from drain to source.

Therefore, the threshold voltage (V_{th0}) of the MOSFET comprises of following four components:

(i) the difference between gate and channel work function (Φ_{GC})

(ii) the Flat-Band voltage of the device (Φ_F)

(iii) Gate voltage compensation for the screening effects caused by the depletion charges ($-Q_{B0}/C_{ox}$).

(iv) Gate voltage component, compensating the oxide trap charges ($-Q_{ox}/C_{ox}$)

2.2.4. MOSFET Scaling

Because of their scalability, MOSFETs play a significant role in integrated circuits (ICs). Researchers are working to minimize practically every semiconductor device as a result of technological improvement. The MOSFET, which originally had channel lengths of several micrometers, has steadily been reduced down to tens of nanometers in contemporary integrated circuits during the past few years.

Thus according Moore's law [2.11], which is depicted in the accompanying graph, the MOS transistor's dimensions have been shrinking since 1960 at a rate of 30% every three years. Moore's law only shows the rate of increase in transistor density, but the shrinking of the MOS device's dimensions provides advantages as well, such as an increase in circuit density and speed in the following ways:

a) Shortening the gate's length (LG) causes the circuit's operational frequency to rise, making the circuit quicker.

b) As the chip's surface area lowers, the transistor density improves and the price of integrated circuits goes down.

c) The constant switching power density allows for fewer circuits to operate at the same power or with less power for each function.

CMOS technology offers some basic advantages endorsed by the defined scaling laws. The International Technology Roadmap for Semiconductors (ITRS) has established a roadmap for guiding the scaling of costs and power usage. The ITRS 2010 states that the physical channel extent for 2013 shall be 10 nm or less because its technology node is 22 nm.

Scaling, which is the controlled alteration of the device dimensions so that its chip area occupied lowers without impacting its performance characteristic of the long channel, has allowed device developers around the world to achieve this. In 1972, d. Dennard and his coworkers put forth the scaling approach [2.12].

Scaling not only results in a smaller device, which increases packing density, but it also lowers voltages, which reduces dynamic power consumption. As scaling progresses, it becomes clear that scaling should be done by the same factor for both the vertical and lateral portions of the transistor in order to prevent SCEs and offer effective electrostatic control during the production of smaller

devices. The same scaling factor can also be used to lower supply voltage as substrate doping concentration rises.

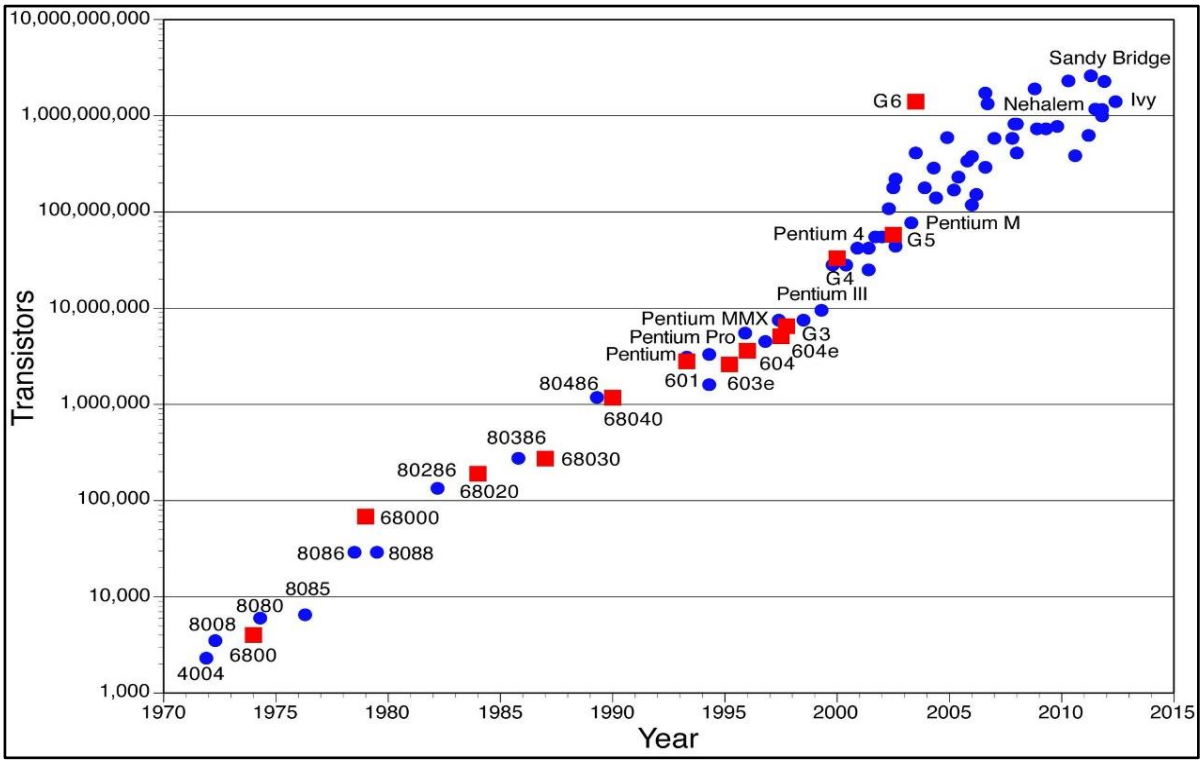


Fig. 2.9: Moore's law of scaling

Scaling causes the ION to increase as well as the circuit speed, power consumption, and space occupied by the circuit to decrease. Consequently, the power density of the circuit is unaffected.

Due to the difficulty of fabricating semiconductor devices at smaller sizes, the need to use extremely low voltages, and the inferior electrical performance, new circuit designs and innovations are required to address these issues. Scaling of MOSFETs also results in a number of short channel effects (SCEs), including punch-through, large leakage currents, quantum tunnelling via the gate, impact ionisation, and drain-induced barrier lowering (DIBL). All of these phenomena reduce a circuit's performance. Even with the optimization of the properties of the materials employed, the short channel effect of scaled MOSFETs cannot be prevented (e.g., peak doping concentration, strain engineering). The short channel effect's primary drawback is a loss of channel gate control. Additionally, an increase in leakage current may cause MOSFET properties to deteriorate.

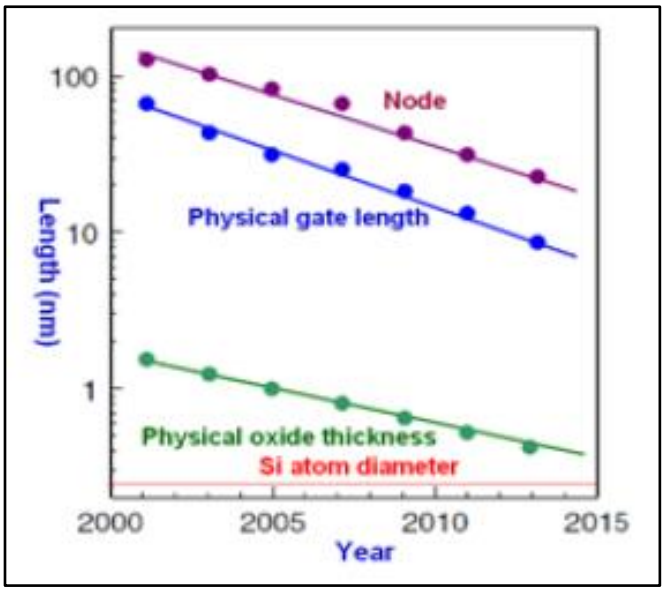


Fig. 2.10: Gate length shrinking with scaling years (Courtesy ITRS 2010)

It is quite difficult to predict when the size decrease will stop given the current state of technological development. We may be able to produce better materials to prevent leaking through this reduction. To continue the performance improvement we are used to now, however, we will eventually need to find a MOSFET replacement.

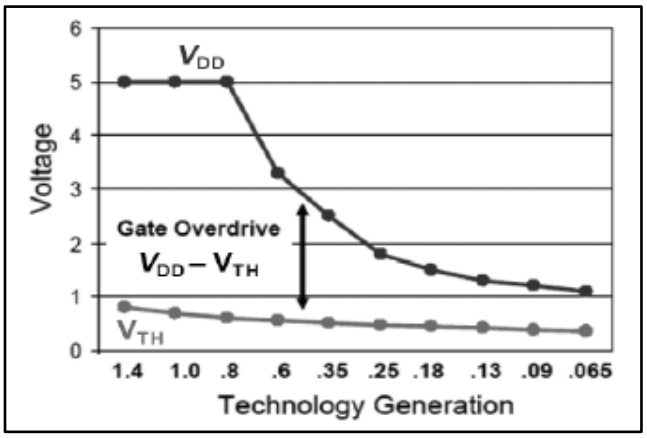


Fig. 2.11: The relationship between the trend of supply voltage scaling and threshold voltage

R. Dennard asserts that the only way to scale a MOSFET without altering the electric fields inside the device is to scale the device's dimensions by 1/ while raising the doping of the drain and source regions by a factor of. Additionally, a 1/ scale should be applied to the applied voltage. These guidelines had been followed by researchers since 1974, up until quite recently. The previous application of Dennard's scaling principles is no longer valid.

The scaling trend from the 1.4 m node to the 65 nm node is depicted in Figure 2.11. As can be observed, the threshold voltage Vt has decreased very little, despite the supply voltage VDD being decreased by around 20% of its starting value. Dennard scaling is the sole reason this has occurred. Other methods, such as adjusting the doping of the channel region under the gate, contributed to this. The electric fields inside a MOSFET remain unchanged when the scaling rules are correctly applied. Therefore, until we make further changes, the threshold voltage remains unchanged.

2.2.5. Short Channel Effects (SCEs)

When the channel length of a MOSFET device is on the same order of magnitude as the depletion-layer widths (xdD, xdS) of the source and drain junctions, the MOSFET is said to be short. When the channel length L is shortened to boost chip operating speed and component density, short-channel effects happen. The short channel effect is the decrease in a MOS transistor's threshold voltage as a result of a shorter channel length. When there is a large drain bias, the SCE is audible. The limitations on electron drift characteristics in the channel and the alteration of the threshold voltage brought on by the reduction of the channel length are two physical phenomena that are responsible for the short-channel effects.

Reduction of the channel length of MOSFETs leads to short-channel effects like:

2.2.5.1 DIBL (Drain-Induced Barrier Lowering)

The gate voltage, which generates the vertical electric field, regulates the population of channel carriers in long channel devices, whereas the horizontal field regulates the current flowing between the drain and the source. The development and preservation of an inversion layer on the surface are necessary for the channel's current to flow. The carriers (electrons) in the channel face a potential barrier that prevents flow if the gate voltage is insufficient to invert the surface (VG Vth). This potential barrier is decreased by raising the gate voltage, which eventually permits carriers to pass while being influenced by the channel's electric field. The vertical and horizontal electric fields can be thought of as having distinct effects on the properties of long-channel devices. When the gadget gets shrunk, the drain area comes nearer to the source, affecting the entire channel with its electric field. Without the help of the gate terminal, the drain-induced electric field also aids in drawing carriers to the channel. Because the drain lowers the potential barrier for the source

carriers to construct the channel, this phenomenon is known as drain induced barrier lowering (DIBL). To experience the effects of this phenomenon, the threshold voltage must be lower. A loss in gate control caused by DIBL's carrier attraction causes an increase in off-state leakage current.

2.2.5.2 Reduction of the Effective Threshold Voltage

The gate and the substrate regulate channel creation in a long-channel device. All of the space charge induced in the channel region is under the control of the gate voltage. The charge in the channel region diminishes as the channel length does. In a short-channel device, the n+ type source and the drain generate a significant portion of the depletion charge that cannot be ignored. As the drain bias is increased, the reverse biassed space charge area at the drain extends further into the channel and the gate control declines. Charge sharing, which is used with short-channel devices, refers to the division of the channel's charge control among the four terminals (gate, substrate, source, and drain). The source and drain both have depletion areas that are somewhat near to one another.

A significant fraction of the field lines coming from the bulk charge in a short-channel device terminates in the source and drain regions rather than the gate. The amount of channel charge is simpler for the gate to exhaust, resulting in a decrease in the device's threshold voltage. A greater surface potential and deeper depletion zone make the channel more alluring to electrons. The gadget may conduct greater current as a result. Given that the drain current is a function of Vth, this effect could be viewed as a lowering of Vth (VGS–Vth). The effective threshold voltage will fall as VDS rises and channel length contracts.

In other words, because the source and drain depletion junction really contributes a large amount of the overall charge in the depletion region under the gate, the bulk depletion charge contributed by the gate is less than the expected charge, controlled only by the gate. The equation must be changed to account for this decrease in the bulk depletion charge because the threshold voltage is a function of the bulk depletion charge caused by the gate. Vth (SC) = Vth- Vtho, where Vtho is the threshold voltage change from the long to the short-channel MOSFET, which can be used to express the threshold voltage of the short-channel MOSFET.

2.2.5.3 Off-State Leakage Current

An N-channel MOSFET is in the off-state at $V_{GS}<V_t$. Between the drain and the source, though, a bad leakage current might move. The subthreshold current is the MOSFET current

measured at $V_{GS}<V_t$. I_{OFF}, the MOSFET off-state current, is mostly caused by this. The ID measured at $V_{GS}=0$ and $V_{DS}=V_{DD}$ is known as $I_{OFF.}$ To reduce the static power that a circuit uses even while it is in standby mode, it is crucial to maintain I_{OFF} relatively minimal. A cell phone chip with 100 million transistors, for instance, would use so much standby current (10Amp) that the battery would be discharged in a matter of minutes without any calls being received or sent. This is assuming that I_{OFF} is a modest 100nA per transistor. A desktop PC chip could be able to withstand this static power, but not much more before running into costly cooling issues.

2.2.5.4. Impact Ionization

Due to the high electron velocities in high longitudinal fields that can produce electron-hole (e-h) pairs via impact ionisation, that is, by striking silicon atoms and ionising them, another unfavourable short-channel effect, particularly in NMOS, occurs. As a rule, the drain attracts the majority of the electrons, while the holes enter the substrate to contribute to the parasitic substrate current. Additionally, the area between the source and drain can function as the base of an n-p-n transistor, with the source acting as the emitter and the drain as the collector.

The usually reversed-biased substrate-source p-n junction will conduct noticeably if the aforementioned holes are collected by the source and the accompanying hole current causes a voltage drop in the substrate material of the order of 0.6V. Since this is the case, it is possible to inject electrons from the source into the substrate in a manner similar to how they are injected from the emitter into the base. As they go closer to the drain, they can gather enough energy to form new eh pairs. If some of the electrons produced by high fields escape the drain field and move into the substrate, the issue may get worse and harm other chip-based devices.

2.2.5.5. Drain punch through

The depletion region around the drain may extend to the source when the drain potential is sufficiently higher than the source potential, causing current to flow regardless of gate voltage (i.e. even if the gate voltage is zero). Drain Punch Through situation is what this is, and the punch-through voltage is provided by:

$$V_{PT} = \frac{qN_a L^2}{2\varepsilon_s} \qquad (2.1)$$

As a result, punch-through voltage rapidly drops as channel length L decreases (i.e., short channel length case).

In an extreme example of channel length modulation known as punch-through, the depletion layers surrounding the drain and source regions of a MOSFET combine into a single depletion zone. The drain current and field below the gate both then become highly reliant on the voltage across the drain-source junction. Punch-through results in a rapidly rising current when the drain-source voltage rises. This impact lowers the device's maximum working voltage and increases output conductance, both of which are undesired effects.

2.2.5.6. Hot Carrier Effect

As device voltages are difficult to scale to arbitrarily small values, electric fields tend to grow at smaller geometries. Short-channel devices consequently exhibit a variety of hot carrier effects. Impact ionisation and carrier multiplication are two effects that the field in the reversed biassed drain junction may produce. Some of the resultant holes may proceed to the source, where they reduce the source barrier and cause electrons to be injected into the p-region from the source, contributing to substrate current as they do. In reality, a source channel drain design can produce an n-p-n transistor, which prevents gate control of the current. The intense electrons' passage over (or tunneling through) the barrier and into the oxide is another hot electron phenomenon. Such electrons become trapped in the oxide, changing the device's I-V properties and threshold voltage. By decreasing the doping in the source and drain areas and making the junction fields lower, hot electron impacts can be mitigated.

However, due to contact resistances and other comparable issues, lightly doped source and drain regions are incompatible with small geometry devices. Lightly Doped Drain (LDD), a compromise MOSFET design, uses two levels of doping, with high doping over the majority of the source and drain areas and mild doping in a region next to the channel. The LDD structure lessens the field between the drain and channel areas, which lessens hot electron effects such as impact ionization, injection into the oxide, and others.

2.2.5.7. Velocity Overshoot Effect

It is a most important effect practically because it is directly related to the increase of current drive. It is possible when some fraction of carriers is acquiring sufficient thermal energy near the Drain region, which are hot electrons. Hot carriers are not in equilibrium with the Silicon Lattice. The velocity of a hot electron exceeds the velocity saturation; this condition is called Velocity overshoot.

2.2.5.8. Surface scattering

The longitudinal electric field component (Ey) increases and the surface mobility turns into a field-dependent property if the channel length decreases as a result of the lateral extension of the depletion layer into the channel region. The electrons move very slowly parallel to the interface because the carrier transport in MOSFETs is constrained to the narrow inversion layer and because surface scattering—the collisions that the electrons experience as they are accelerated toward the interface by Ex—reduces mobility. As a result, even for low values of (Ey), the average surface mobility is only about half as high as the bulk mobility.

2.2.5.9. Velocity saturation

Devices with short channels are particularly vulnerable to Velocity Saturation. The electric field expands and the channel's carriers move more quickly in short-channel devices. The electric field and velocity, however, are no longer linearly related at high fields because the velocity progressively reaches saturation velocity. The enhanced scattering rate of extremely energetic electrons is what is responsible for this velocity saturation.

So, when V_{ds} increase electric field reaches the value (E_c) critical electric field at that time carriers' velocity at the drain becomes saturated. When the electron field is below (10^4 V/cm), velocity increases linearly.

When the electric field exceeds 104 V/cm, the drift velocity tends to progressively increase until it approaches saturation at 300 K, where it achieves Vde (sat) = 107 cm/s and Ey = 105 V/cm. When bias voltage is not lowered when the channel length is shortened, velocity saturation rather than pinch-off limits drain current. The maximal gain for a MOSFET can be expressed as $g_m=W.C_{ox}.V_{DS\ (sat)}$.

2.2.5.10. Channel Length Modulation

The widening of the depletion layer at the drain as the drain voltage rises is what causes channel length modulation in a MOSFET. As a result, the channel length is reduced and the drain current is raised. Small devices with substrates that are low in doping often exhibit a more strong channel-length modulation effect. Punch-through, in which the channel length is reduced to zero, is a severe example of channel length modulation. By raising the doping density when the gate length is decreased, proper scaling can lower channel length modulation.

Due to base-narrowing in bipolar devices, a comparable rise in current is observed with higher collector voltage, which is known as the Early effect. The term "Early effect" for MOSFETs is another name for a similar phenomenon that is also referred to as "channel-length modulation."

2.2.5.11. GIDL (Gate Induced Drain Lowering)

A V_{GD} depletion zone is produced under a gate to drain overlap region for negative gate drain bias, and a strong electrical field in the region can cause valance band electrons to tunnel into the conduction band. Consequently, electron-hole pairs are produced. The drain collects electrons, and the substrate's holes carry the substrate current. In very thin oxide MOSFETs, a breakdown phenomenon is discernible at drain voltages considerably lower than the junction breakdown. The high electric field that the Gate induces in the Gate to drain overlap region is what leads to this breakdown. Gate Induced Drain Leakage Current is the name given to this leakage current. In a short-channel device, this current may be harmful at zero gate bias. Only the circumstances in the immediate gate-to-drain overlap zone affect the GIDL current. The oxide shape beneath the gate edge has a significant impact on this current. The decreased gate oxide thickness causes an exponential increase in gate-induced drain leakage.

2.2.5.12. Parasitic Bipolar Effect

Avalanche breakdown happens in the channel at the drain as the electric field in the channel is raised. The current is increased as in a p-n diode by this avalanche breakdown. Additionally, parasitic bipolar activity is present. Under the inversion layer, holes produced by the avalanche breakdown travel from the drain to the source. The source-bulk p-n diode is forward biassed by the hole current, which causes the injection of electrons as minor carriers into the p-type substrate beneath the inversion layer. When these electrons reach the drain, avalanche multiplication causes them to produce further electron-hole pairs. Breakdown occurs at lower drain voltage due to the positive feedback between the avalanche breakdown and the parasitic bipolar activity.

2.2.5.13. Subthreshold current

The sub-threshold current, which results from the fact that some electrons are induced in the channel even before substantial inversion is created, is one effect that is made worse by short channel designs. We anticipate that drift currents will be subordinate to diffusion currents at low

electron concentrations (usually in the sub-threshold zone) (proportional to carrier concentrations). The DIBL effect, which enhances the injection of electrons from the source, worsens the sub-threshold current.

2.2.6 Remedies of Short Channel Device

2.2.6.1 Silicon on Insulator MOSFET

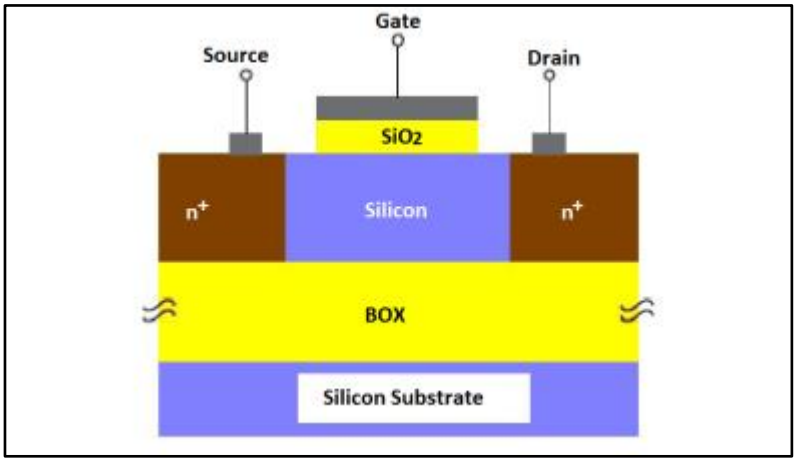


Fig. 2.12: Cross-sectional view of Silicon on Insulator MOS (SOI MOS)

Various short channel effects are caused when the channel length is decreased as a result of MOSFET scaling. The Classical conventional device structure is unable to give a solution by which we can further scale down the device. Innovative non-classical device structures can have a panacea to the various short channel effect. Silicon on Insulator MOSFET (SOI-MOS) is one such innovative substitute with lesser affected by SCEs indulges further scaling of semiconductor devices. The concept of housing a thick layer of silicon-di-oxide in between the silicon layer underneath the gate and the substrate is used for SOI structure. The thick oxide layer known as Buried Oxide (BOX) fabricated between the channel and the substrate makes it different from the conventional MOSFET. By oxidising silicon or implanting oxygen in silicon, the BOX is made. The presence of dielectric as a buried layer will restrict the extension of the depletion region to the substrate thereby decreasing parasitic capacitance and leakage current. Low leakage current and parasitic capacitance will make the device less electrical power consumption device, high speed, and support miniaturization. Constant innovation in SOI MOSFET structure expands the device from a single gate to multiple gates and surrounding gate structure [2.13 – 2.16]. The cross-sectional view of SOI MOSFET structure is shown in figure 2.12.

The thickness of the silicon layer of SOI MOSFET will classify it into two different modes of operation, Fully Depleted (FD) SOI and Partially-Depleted (PD) SOI. The cross-section view of SOI structures is shown in figure 2.13. The body region of the FDSOI is thinner in comparison to PDSOI making the gate depletion width higher than silicon thickness. Hence for both ON and OFF-state, the entire body region will be under depletion. Whereas in PDSOI the thickness of the silicon is larger than the gate depletion width so that the surface potential in the channel is not uniform. The floating body is more pronounced in the PDSOI due to the presence of an undepleted region in the back interface.

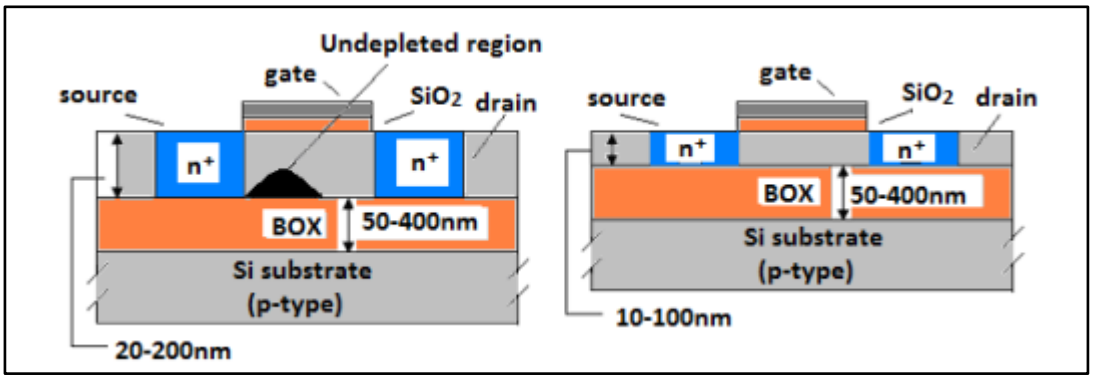


Fig 2.13: Cross-sectional views of Partially depleted and Fully depleted SOI MOSFETs

2.2.6.1.1. Characteristics of SOI

SOI structure has many advantages compared to bulk CMOS.

A glimpse of it can be seen through its characteristics.

(i) Kink Effect

The electron for a fixed gate voltage with a supplied drain to source voltage will move towards the drain region. The flow of electrons will get momentum due to the gaining of kinetic energy which will create additional hole electron pair because of impact ionization. The generated electron will enhance the drain current. The extra generated hole will move towards the source and starts accumulating there. The accumulated hole will reduce the threshold voltage which further increases the drain current. This is reflected in the sharp rise of drain current for a particular drain voltage. And the sharp rise in drain current phenomena is known as the kink effect [2.17 – 2.19].

(iii) Improved Subthreshold Slope

The steep Subthreshold slope is another characteristic of SOI MOSFET with a slope of 60mV/decade. Due to less SCE in FDSOI, it will have a better subthreshold slope than PDSOI [2.18 – 2.19].

(iv) Threshold Voltage Roll-off

The presence of SCE in a MOSFET will reduce the threshold voltage as the channel length decreases. This effect is also present in SOI MOSFET. But due to the reduced SCE in SOI MOSFET compared to bulk MOSFET the threshold voltage roll-off is less in SOI MOSFET.

(ii) Parasitic bipolar effect

The parasitic bipolar transistor created with an n+ source, drain and body region due to the accumulation of holes in the source region (because of impact ionization) will adversely affect the threshold voltage, subthreshold slope, and breakdown voltage between the drain and the source. The presence of an undepleted body region in PDSOI will make it more prominent in PDSOI.

(v) Self Heating Effect

The BOX layer which is used for better performance of SOI devices will also act as thermal insulation between the channel and the substrate. So, heat generated by the drain current will be thermally insulated to release through the substrate and the device become hotter. This is known as self-heating. The effect of self-heating will reduce the performance of the device. Reduced drive current, turning on the bipolar parasitic transistor, low breakdown voltage, and excess generation of hot carrier current are some of the negative effects of self-heating

(vi) Floating Body Effect

The body potential of an SOI MOSFET varies with different changes in the device's behavior. This is due to the complete isolation of the channel to the body. This phenomenon of having different body potentials for different induce effects is known as a dynamic floating body effect. The majority carrier redistribution and impact ionization are the main reason for changes in body potential. FDSOI is more immune to the floating body effect than PDSOI.

2.2.6.1.2 Advantages of SOI MOSFET

(i) Reduced Parasitic Capacitance

The presence of SiO2 (with a lower value of dielectric constant than silicon) buried oxide layer in the SOI device will reduce the capacitance between the substrate and drain/source. The reduction in parasitic capacitance will effectively reduce the switching speed of the device and in turn

increase the performance by 20 to 25 percent faster for the same power consumption. Moreover, for the same supply voltage, the power consumption of an SOI device is less than bulk MOSFET.

(ii) Ideal Device Isolation

The device placement for an SOI device can be made more compact by using a thin insulation film for lateral isolation between two devices and a thick BOX layer for vertical isolation for channel and substrate. This makes the perfect device isolation. The CMOS inverter output can be connected directly to p+ and n+ diffusion making the device more compact than bulk MOSFET.

(iii) No Latch-up

The buried layer prevents the formation of n-p-n-p (or p-n-p-n) thyristor in SOI MOSFET. So, no latch-up occurs like in bulk MOSFET

(iv) Small Leakage Current

The thinner top silicon layer reduces the p-n junction leakage current due to a small area. Therefore, low standby power is required [2.20 – 2.21].

(v) Improved Stack Gate Speed

The threshold voltage and fall time increase for a NAND gate designed by MOSFET. The presence of negative body bias connected to both pull-down transistors to the ground will generate this drawback. But in SOI MOSFET due to the presence of a buried layer, a positive body bias is obtained which will reduce the threshold voltage and fall time and increase the drain current.

(vi) Reduced Short Channel Effects

The gate has better control over the potential profile of the channel due to the miniaturization of the device compared to MOSFET. Better control of the gate over the channel will reduce the SCE drastically.

2.2.6.1.3 Disadvantages of SOI MOSFET

➢ At higher drain voltage, the body-source junction may get accidentally forward biased resulting in a sharp rise in off-state leakage current.

➢ Enough measures are taken to maintain the quality of the buried oxide-silicon layer interface to ensure reduced interface scattering effects.

➢ Another issue could arise in the BOX layer of the SOI structure as a result of silicon oxide's reduced thermal conductivity, which could cause a self-heating effect. Through a number of methods, this can substantially impair the performance and dependability of the device [2.22].

➢ Floating body aspect in partially depleted SOI MOSFETs returns undesired 'Kink effect' in DC circuits resulting in drain-current overshoot [2.23]. Thus, Dynamic floating body effects and parasitic bipolar effects can be described as inherent features of the SOI structure [2.24] that become significant in ultra-low dimensional SOI structure, thereby downgrading device performance.

2.2.6.2. SON MOSFET

The performance of the SOI structure has been reviewed rigorously for some structural changes by replacing the buried oxide with relatively low permittivity material of permittivity one to further examine its short-channel behavior. It can be noted that 'air', possessing the lowest relative permittivity of unity, offers better electrostatic isolation for the region of interest (active channel region) protecting from unwanted field line penetrations. This new innovative design (where the BOX layer is replaced with a layer of air) is popularly known as Silicon-On- Nothing (SON) technology. It has been proved both theoretically as well as experimentally that the SON structure is capable of suppressing major SCEs and exhibiting an excellent short channel performance [2.25 – 2.27] since the model embodies the benefit of both bulk and SOI structures promising higher performance in terms of reduced floating body effect, hot carrier effect, and offering improved radiation immunity in the extreme environment. Parasitic capacitances between the source/drain and substrate get significantly reduced, thereby considerably increasing the operating speed of SON devices [2.26 – 2.28]. It meets up with the aggressive scaling requirements of ITRS [2.29] promoting further scalability for achieving a higher speed of operation. The concept of the dual metal, triple metal, and gate-all-around SOI structure can thus be extended to SON architecture for improved performance.

The above discussion conveys the significance of device miniaturization to sustain the growth of the semiconductor and VLSI industry. However, shrinking of the device dimension gives rise to several bottlenecks degrading its performance operating in a sub-nano regime. Development of some innovative structures exploring novel ideas with improved material properties for ultra-scaled devices holds the key to continuous improvement in short-channel performance.

2.2.7 Overview of Tunnel FET (TFET)

VLSI industries have been driven by the strategy of downsizing device dimensions. The technology passes a long way from fabricating the first MOS transistor of gate length 300 μm to the present nano-device of 10 nm channel length. Therefore, today's cutting-edge technology accommodates billions of transistors in a chip.

MOSFET scaling supports many advantages besides increasing the packaging density of the chip. The switching speed of a circuit gets improved by lesser gate capacitance manifested by smaller gate lengths. Nevertheless, voltage scaling significantly reduces the power consumption of a scaled device.

OFF-state power consumption has been a critical issue of short channel MOSFET precisely below 50 nm gate length, operating at 0.5 V power supply. The current conduction mechanism of MOSFET is governed by thermos-ionic emissions. Therefore, the potential height between the source and channel regions gets reduced with an increase in gate voltage (V_{gs}). The issues that crop up for short channel devices are two-fold: (i) conduction of a significant amount of OFF-state leakage current and (ii) a degraded subthreshold slope affecting the switching characteristics of devices. A steeper subthreshold slope is highly desirable for high-performance devices to allow a better ON/OFF current ratio. The feature aids to reduce the power dissipation of MOS devices at OFF state conditions. Since the subthreshold swing (SS) of MOSFETs is expressed by,

$$SS = \frac{1}{\frac{d(\log_{10} I_{ds})}{dV_g}} = 2.3\frac{kT}{q}(1+\frac{C_d}{C_{ox}}) \qquad (2.2)$$

where C_d and C_{ox} are the depletion and gate oxide capacitance respectively. Therefore, the lowest possible value of subthreshold swing could be 2.3kT/q, which is equal to 60 mV/decade at 300 K. Thus, to attain an I_{on}/I_{off} ratio of 10^{10}, 0.6 V shift is required which is impossible for a circuit/system driven by 0.5V source voltage to provide for. Therefore, the conventional CMOS

logic with short channel MOSFET architecture failed to deliver a better ON/OFF current ratio, while retaining the scaling trend intact. Finding an alternative device, therefore, becomes an essential challenge to the researchers to continue with the scaling trend sustaining the growth of VLSI industries.

In the last several decades [2.30–2.35], TFETs have emerged as one of the promising alternatives to replace MOSFETs in CMOS logic. The charge carriers flow past the potential barrier between the source valence band and channel conduction band because the current conduction mechanism of TFETs is controlled by quantum mechanical tunnelling. At the OFF-state current, the gadget provides a little current. The subthreshold swing is also not constrained to 60 mV/dec because the device's current conduction is a quantum mechanical process. Additionally, TFETs are more resistant to short channel effects than traditional MOSFETs are below the sub-100 nm region, which is a major drawback for conventional MOSFETs.

2.2.8. TFET Structures

A conventional n-channel TFET is depicted in Fig 2.14(b). Similar to MOSFETs, the device has three sections with the names source, channel, and drain. The major differences between a MOSFET and a TFET are that an n-type TFET has a p-type doped source unlike MOSFET and a channel is of intrinsic or shallow p-type doping. Figure 2.14 (a) and (c) show the structures of an n-type MOSFET and a p-type TFET, respectively.

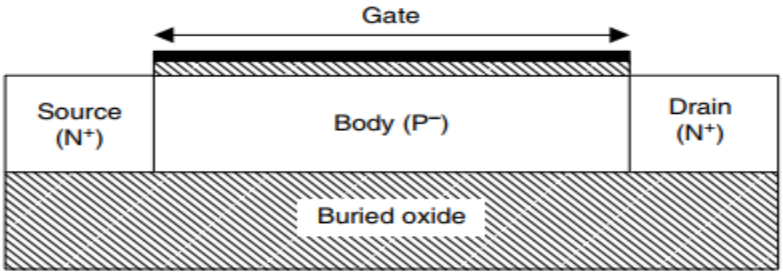


Fig 2.14 (a): View from the cross-section of an n-channel MOSFET.

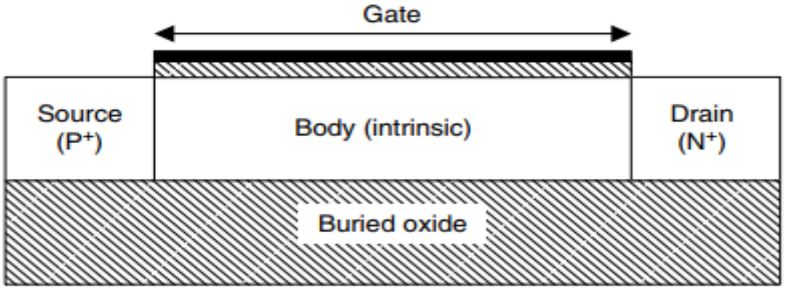


Fig 2.14 (b): View from the cross-section of an n-channel TFET.

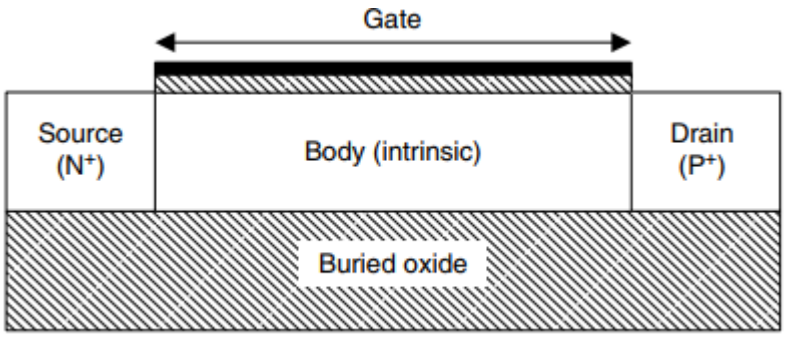


Fig. 3.14 (c): View from the cross-section of an p-channel TFET.

2.2.9 TFET V-I Characteristics

2.2.9.1 Qualitative Analysis

The band diagram of the device under various biassing conditions is the most effective technique to explain the current-voltage properties of TFETs. The transfer and output properties of the TFET under the appropriate biassing will be clearly illustrated in the literature that follows.

(A) OFF-State

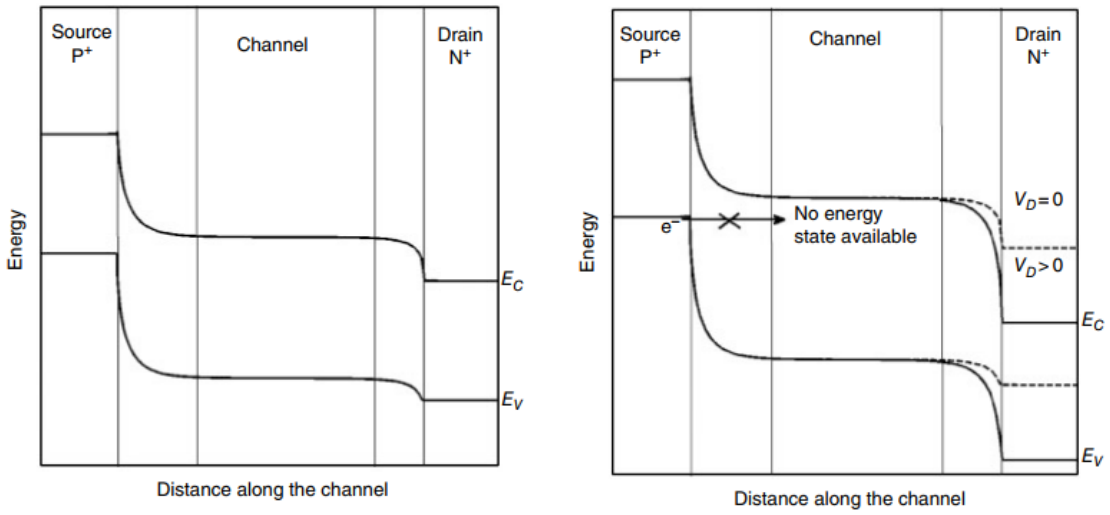


Fig 2.15 (a) Under unbiased conditions, the band diagram of a TFET is in an equilibrium state. (b) The band diagram of a TFET is in the off state for Vds>0 and Vgs=0.

Under no bias condition, i.e., $V_{gs}=V_{ds}=0$, the Tunnel FET lies in equilibrium condition. The corresponding band diagram has been depicted in Fig 2.15(a). At this condition, depletion regions are formed at the channel and source, and channel and drain interfaces. The device remains at an OFF-state with the biasing Vds>0 and Vgs=0. The respective band diagram is shown in Fig 2.15

(b). Under this condition, a few numbers of electrons (as the source is p-type doped) from the source injected into the channel, has been drifted to the drain through the channel conduction band being inebriated of the source to drain the electric flux density. Since the amount of charge is negligible, it only could produce an insignificant drain current. On a contrary, in MOSFETs, the source region is heavily n-type doped. Therefore, comparatively a greater number of electrons penetrating through thermionic emission produce subthreshold current (I_{OFF}) in MOSFETs compared to TFETs.

(B) ON State

With the increasing gate voltage (Vgs), the band structure of the TFET device gets modulated. Since Vgs > 0, the channel conduction band shifts downward, depicted in Fig 2.16 (a). A particular gate potential aligns the source valence band with the channel conduction band. Owing to degenerate p-type source material the electron of the source (being minority carriers) now finds affluents vacant energy positions in the channel conduction-band, which is separated from the source, by a Energy barrier equal to the forbidden band-gap 'Eg' of the source medium. Therefore, the drain current is created when charge carriers (electrons) tunnel through the barrier.

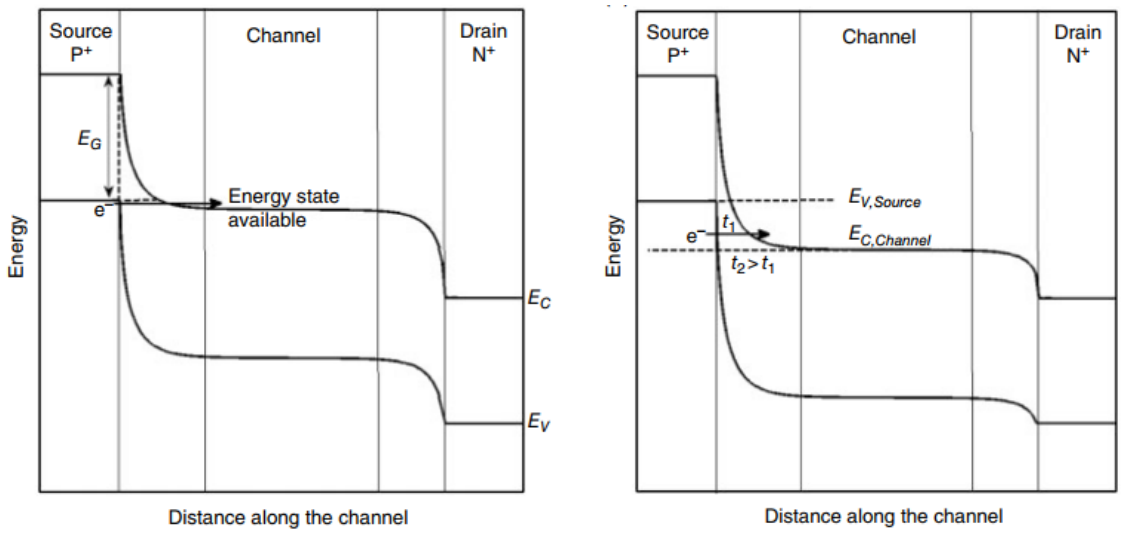


Fig 2.16 (a) Band alignment of an n-TFET at the onset of drain current (b) Further band bending ensures an exponential rise in drain current

Fig 2.16 (a) shows the valence band (VB) (source) – conduction band (CB) (channel) alignment at which the ON-state current starts conducting. The further increase of gate voltage (Fig 2.16 (b)) pushes the conduction band (channel) downwards ensuring more electrons transit from source to channel increasing the drain current exponentially.

The overlapped region between the VB of the source and CB of the channel rises with increasing gate voltages, decreasing the distance between the band edges, or the tunnelling length, as shown by a comparison of the band structures shown in Fig. 2.16(a) and (b). The tunnelling rate is larger for the lower tunnelling path because the barrier height (Eg) is the same in both scenarios. Furthermore, because the tunnelling probability is exponentially linked to the tunnelling width, the drain current increases significantly with increasing gate voltage.

Another crucial information about the likelihood that an electron will tunnel at the source's lowest energy level and at the VB's edge is explored in Fig. 2.16 (b). Both carriers share the same height of the barrier. As a result, the only factor affecting tunnelling probability is the tunnelling width, which is determined by the energy bands' slope. The slope is greatest at the junction areas of a p-n interface, and the slope is inversely proportional to the tunnelling width. Since the tunnelling width is bigger in the latter instance, the likelihood of a tunnelling for an electron located at the edge of the source region is significantly higher than for an electron lying at lower energy levels. The lower energy level carriers of the source valence band so contribute far less to the tola drain current.

(C) Pinning of the Channel

When the biassing conditions Vgs > Vds exist, the channel condition pins. The inversion charge density of the channel becomes comparable to the charge density of the drain region from this gate voltage onward. As a result, the channel and drain are effectively shorted, and the potential of the channel and drain are equal.

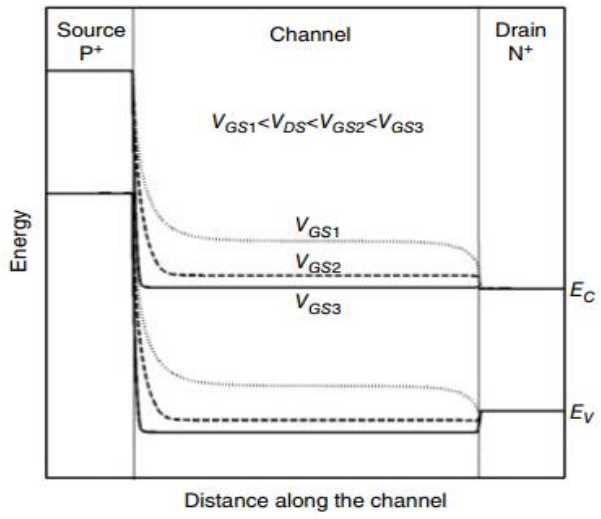


Fig 2.17. Band diagram pointing the pining of the channel condition with the biasing conditions Vgs > Vds

Following that, the device's band structure seldom changes due to gate biassing, and the channel is referred to as pinning. It happens gradually. The gate loses control over channel electrostatics at a point where Vgs Vds and loses total control when Vgs > Vds because the inversion charges rise with rising gate voltage.

Depending on two parameters, the drain current increases as the gate voltage increases. A greater number of electrons are forced to tunnel from more valence states of the source due to two factors: first, the higher gate voltage pushes the conduction band of the channel deeper than the source valence band. However, the channel-drain potential's pinning state no longer aids gate potential in further reducing the channel conduction band. The second factor is the electric field across the source-channel junction caused by the gate voltage, which shortens the effective tunnelling length. The energy band in Fig. 2.17 shows how the biassing circumstances Vg3> Vg2> Vd> Vg1 result in an increase in the electric field, which causes the channel locate to pin. As a result, the drain current for Vgs Vds increases with gate bias more quickly than for Vgs> Vds.

(D) Ambipolar Behavior

Unlike MOSFET, n-type TFET offers to drain current for gate voltages lesser than zero and that can be analyzed by the band diagram as follows:

As demonstrated in Fig. 2.18, when Vgs=0, electrons cannot tunnel from the valence band (source) to the conduction band (channel) or from the valence band (channel) to the conduction band (drain) (a). According to Fig. 2.18, the valence band (also known as the channel) travels upward relative to the conduction band (also known as the drain) as the negative gate voltage decreases (b). At a specific point of negative gate voltage, the valence band of the channel aligns with the conduction band of the drain, and electron tunnelling from the channel to the drain begins (Fig. 2.18(c)). The electrons are seen to tunnel in the same direction as they did for the positive gate bias. Due to two variables, an additional drop in negative gate voltage causes an exponential spike in drain current. First, the probability of the tunnelling rate is increased by the shorter tunnelling length. And secondly, the number of filled valence states of the channel locate grows as the overlapped area between the channel and drain (Fig. 2.18(d)) increases due to the negative gate voltage, providing a considerable number of electrons to tunnel from channel to drain. It is referred to as ambipolar conduction.

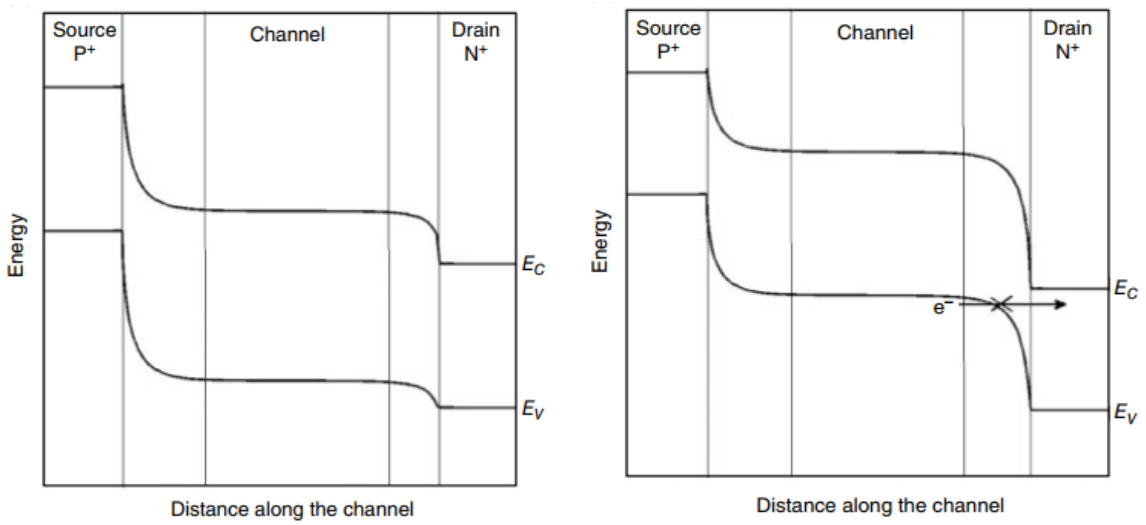


Fig 2.18 (a): Band diagram of an n-channel TFET for Vgs=0 (b) For Vgs < 0 the valence band of the channel moves upward compared to the conduction band of the drain

The channel potential becomes trapped with the source potential as the gate voltage continues to drop, as depicted in Fig. 2.18 (e). As a result, the external gate voltage barely affects the channel potential, and the negative gate bias is the only factor that affects the rise in drain current.

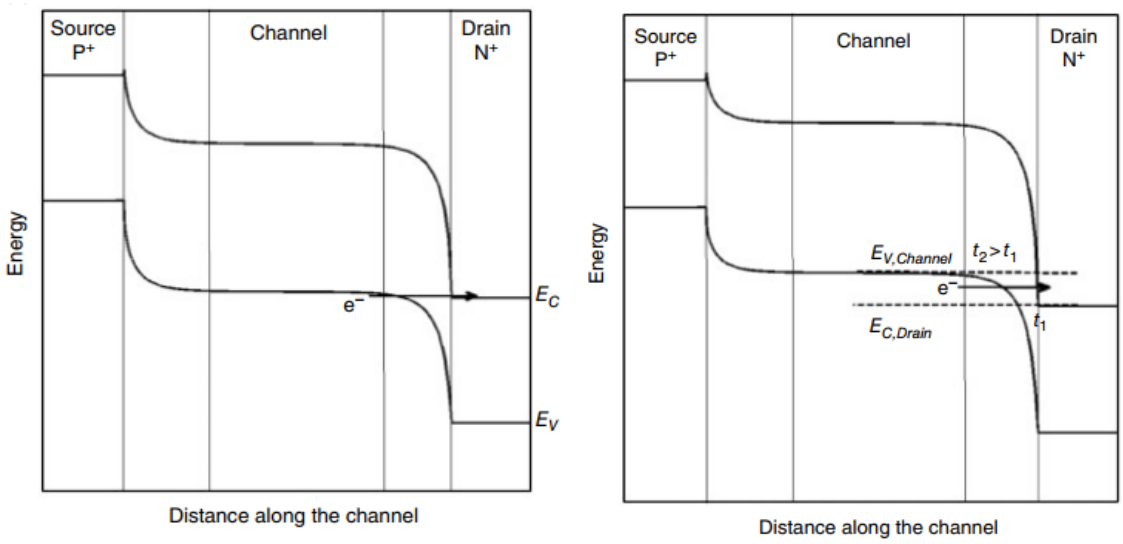


Fig 2.18 (c): At a specific negative gate voltage, the channel's valence band aligns with the drain's conduction band, and electron tunnelling from the channel to the drain begins (d) An exponential rise in drain current results from a further drop in negative gate voltage.

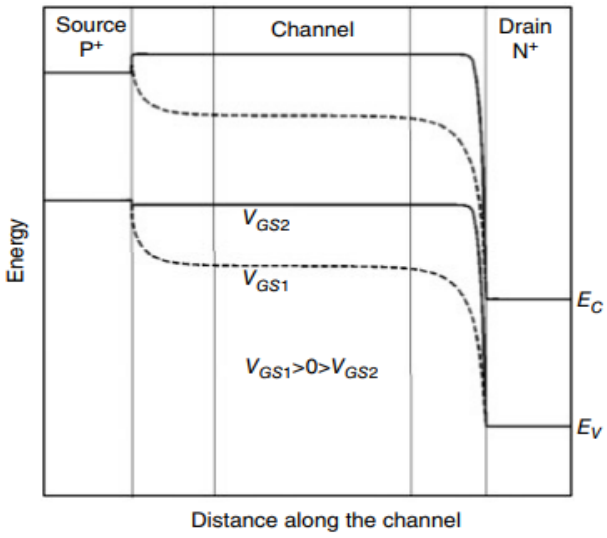


Fig 2.18 (e): The channel potential becomes pinned with the source potential as the gate voltage continues to drop.

2.2.9.2 Characteristic Curves

(A) Transfer Characteristics

Fig. 2.19 shows the n-type TFETs' transfer characteristics (a). Three operating regions of On-state characteristics are mentioned in the figure. For very low positive gate voltages, a shallow OFF-state current flows in the device. The band alignment of the source valence band with the channel conduction band causes the drain currents to rise dramatically as the gate voltage rises. More full valence states of the source find vacant conduction states in the channel and tunnel through it at higher positive gate voltages. The aforementioned figure displays the ON state's present region. The drain current begins to saturate because of the pinning phenomena at the point where the channel potential approaches the drain potential.

Fig 2.19 (b) presents the ambipolar behavior, that occurred due to applying a negative gate voltage to TFET devices. A symmetrical nature of the drain current is observed for the ambipolar behaviour. Since the gate potential is decreased below the '0' volt., the valence energy band of the channel gets overlapped with the conduction energy band of the drain at a certain point of negative Vgs, resulting start of 61unnelling of the carriers from channel to drain in the same direction, as it was for the ON state. This gives rise to the I_D, similar to the ON state current, for the negative gate bias too.

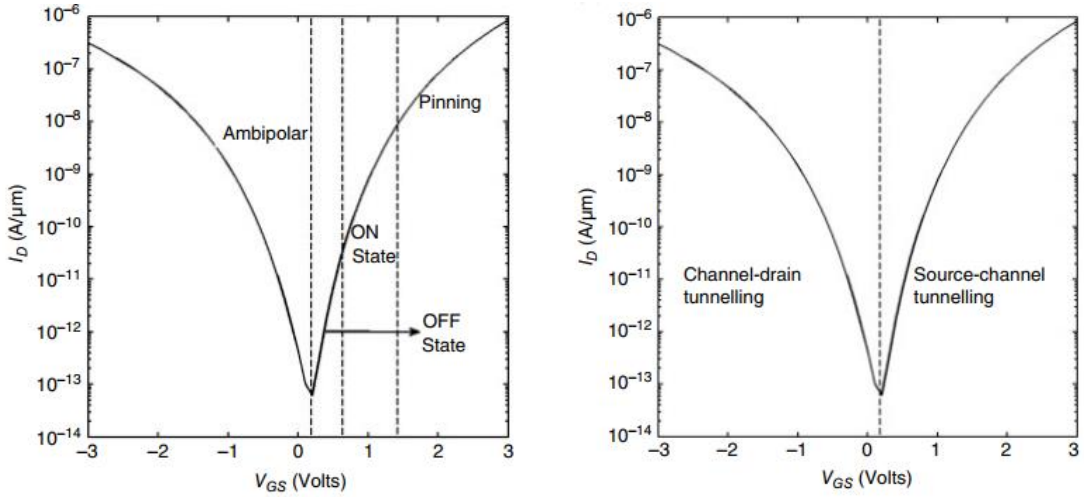


Fig 2.19 (a) A TFET device's transfer characteristics showing its ON, OFF, and ambipolar conduction states (b) This diagram illustrates the source-channel and drain-channel unnelling currents caused by positive and negative gate bias, respectively.

In Fig. 2.19 (c), the transfer characteristics of TFETs are contrasted at various drain voltages. It has been found that the drain voltage has a bigger impact on the conduction of the ambipolar current than the ON state current. If the drain voltage is raised for a fixed negative gate voltage, the energy bands get thinner. It results in an important change (increment) in drain current by widening the channel to drain tunnelling. Thus, drain bias can affect ambipolar conduction.

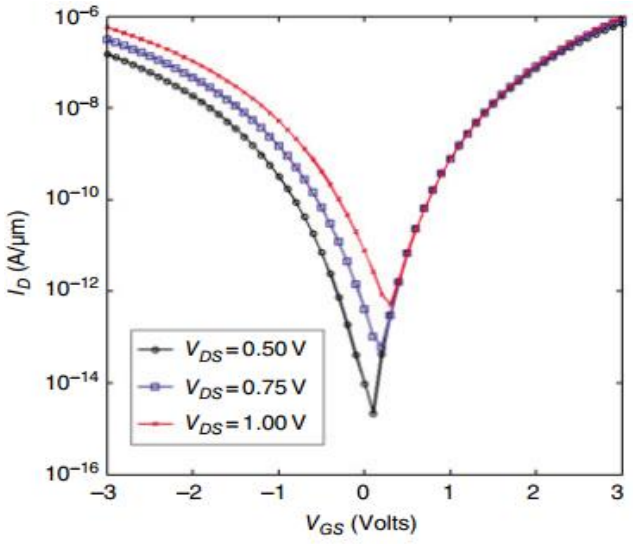


Fig 2.19 (c): The variation of ambipolar conduction due to different drain-to-source voltages (V_{ds})

Contrarily, given a constant positive gate voltage, the drain potential has no effect on the ON state current of TFETs, i.e., Vgs Vds. The source-channel tunnelling is just modulated by Vds

since the drain voltage has little effect on the channel potential. The increased drain voltage lowers the channel energy bands in relation to the source after pining for Vgs Vds has occurred.The greater number of source valence states get exposed for probable source-to-channel tunneling. However, the lower valence states are associated with wider tunneling lengths, which could contribute less in favor of the tunneling current. The tunneling process in such conditions is only dominated by carriers having shorter tunneling lengths. Therefore, a minimum impact of the ON state current is observed for the change in drain voltage for a given gate voltage.

(B) Subthreshold Characteristics

Subthreshold swing is the prime factor of TFETs, which made it considerable in replacing MOSFETs in CMOS logic technologies. The current conduction mechanism of TFET differs from the MOSFET. The subthreshold swing of a MOSFET is thermally restricted to the minimum value of 60 mV/dec. On the contrary, due to quantum mechanical tunneling, the subthreshold swing of the TFET could be far below 60 mV/dec.

The diffusion process in the MOSFET controls the subthreshold current, followed by the given expression [2.36]:

$$I_{DS} = \mu_{eff} \frac{W}{L} \sqrt{\frac{\varepsilon_{Si} q N_A}{4\psi_B}} \left(\frac{kT}{q}\right)^2 e^{q(V_{GS}-V_{th})/mkT} (1 - e^{-qV_{DS}/kT}) \qquad (2.3)$$

where Ψ_B stands for the silicon substrate's Fermi potential and all other variables have their usual meanings. Consequently, the MOSFET's subthreshold swing (SS) is given by,

$$SS = \frac{d \log(I_{DS})}{dV_{GS}} \qquad (2.4)$$

On the other hand, even the subthreshold conduction of TFETs is governed by quantum mechanical tunneling. Hence, the tunneling generation rate and the drain current are a function of the lateral electric field, given as,

$$I_{DS} \propto e^{-1/E} \qquad (2.5)$$

where E, a function of Vgs, represents the channel's lateral electric field. Therefore the subthreshold swing of TFET is not constant like MOSFET and two types of SS are defined for TFET devices. The first one is *point subthreshold swing* and is defined by the following expression, given below,

$$SS_{point}(V_{GS}) = \frac{d\log(I_{DS}(V_{GS}))}{dV_{GS}} \quad (2.6)$$

The second one is the *average subthreshold slope*, which is described as follows for a range of gate voltages:

$$SS_{avg} = \frac{V_{th} - V_{off}}{\log(I_{DS}(V_{th}) - I_{DS}(V_{off}))} \quad (2.7)$$

(C) Output Characteristics

The output characteristics of TFETs are depicted in Fig 2.20 (a). Initially for a given gate voltage channel is pinned due to the condition Vds < Vgs. Therefore, with the increasing drain voltage, channel potential increases, and the subsequent rise in drain current is observed in the figure. The channel electrostatics is no longer governed by the drain voltage when the drain potential approaches the gate potential. As a result, as the drain voltage rises, the drain current becomes saturated.

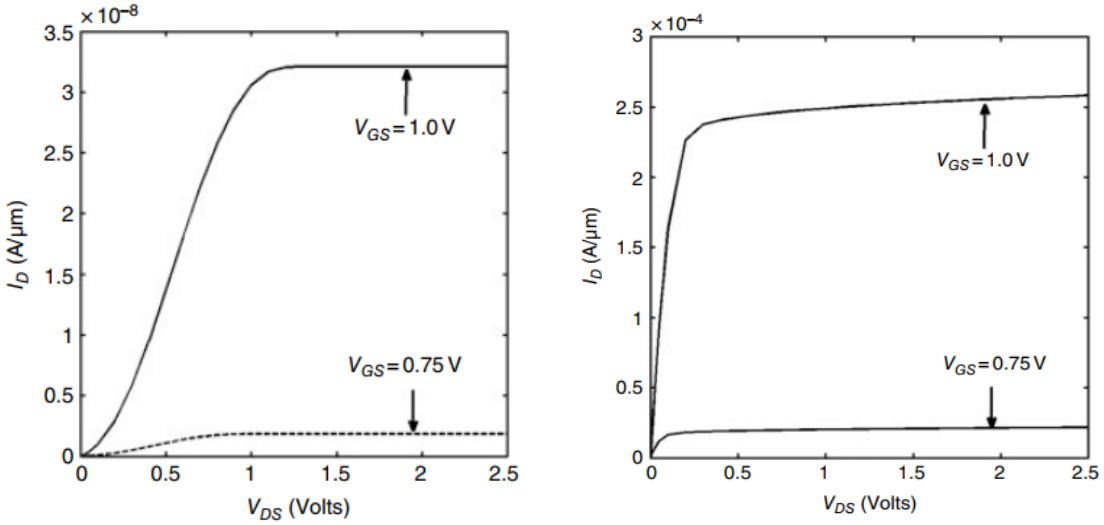


Fig 2.20 (a) Output characteristics of TFET for two different gate voltages, (b) Comparison of n-TFET and MOSFET output characteristics

Two significant discrepancies may be seen between the output characteristics of TFET devices and the MOSFETs (see Fig. 2.20 (b)). Since channel length modulation scarcely affects the drain current of TFETs in the saturation zone, its output resistance is significantly larger than

that of a MOSFET. Furthermore, the drain voltage has no effect on the drain current arising from source-channel unnelling since it has little of an impact on the channel energy bands.

The second distinction is that TFETs have a larger saturation voltage than MOSFETs. Delayed saturation is what causes this and reduces the suitability of TFETs for low-voltage analogue applications.

2.3. VLSI Physical Design

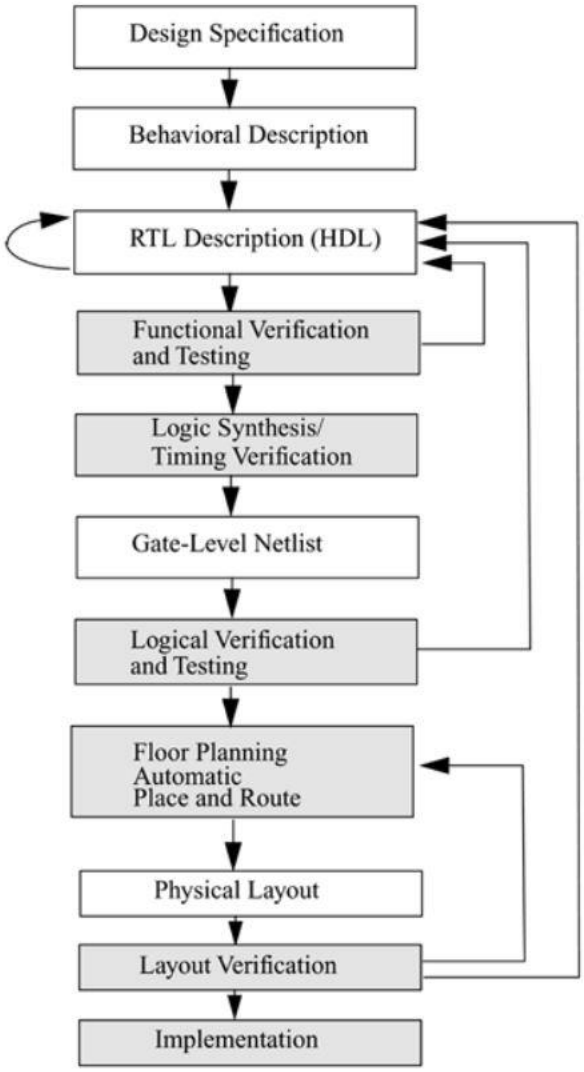
VLSI fabrication industries have been continuously upgrading their technology by introducing automation in every integration step of IC fabrication. A sizable number of electronic components adhere to a set of instructions on a silicon wafer to form integrated circuits. A design engineer's job is to translate the circuit description into a layout, which is a geometric description. Therefore, a layout offers a set of geometric representations of an electronic module in various layers possibly placed on a wafer. The patterns are then checked and verified in assuring to meet all their technology and function requirements. The results are recorded in a netlist in a form of a set of instructions. Therefore, following the netlist, an optical generator converts the designs into pattern files that are used to produce the masks for pattern generation.

The masks are used in photo-lithographic processes to contract the device-level components on the silicon wafer during the fabrication process. This tedious work required critical information about the geometric patterns and a high level of accuracy and expertise. The process of constructing electronic circuits based on the specified netlists is called physical design automation. Physical design is a very important and error-prone process because of the limited tolerance budget and nano-dimensional device structure. In Fig. 2.21, a typical VLSI design flow is shown.

To maintain a high level of accuracy and an error-free design process in IC fabrication with tiny dimensional devices, VLSI physical design phase demands extensive use of Computer Aided Design Tools (CAD) with every step controlled by partial or full automation.

VLSI Physical design has always been a broad area of study and research that works with creating new algorithms, putting them into practise, and creating the data structures necessary to enhance the physical design procedure. Achieving the needed functionality and performances while arranging devices in the best possible ways in two- or three-dimensional surfaces with effective interconnection schemes are the objectives of physical design. A semiconductor wafer is

precious real estate over which electronic modules are built. Hence, it is essential to define algorithms for space saving and optimal use of wafers to improve yield while lowering the cost at a time. Moreover, the placement arrangement of the electronic modules plays a crucial role in the performance of the integrated circuits. It is also a major concern to abide by the ***design rule check*** in the phase of physical design.



2.21: Vlsi Design Flow

2.3.1. VLSI Physical Design Cycle

VLSI physical design cycle consists of five stages. Through the five stages, it produces the layout of the circuit from the netlist, provided to it.

- Partitioning
- Floorplanning
- Placement
- Routing
- Compaction

The following Fig 2.22 depicts the above-mentioned stages of the physical design phase.

2.3.1.1 Partitioning

A present-day integrated circuit consists of billions of transistors. It is an impossible task to process the layout of an entire IC in a single stage owing to the constraints of memory size and computational power. Therefore, the whole circuit is divided into sub-circuits first. This is known as partitioning. Each sub-circuits are functional block. The size of the functional blocks and the interconnections between the blocks are primary concerns during the partitioning process. The outcomes of this stage are the sets of blocks with their interconnections defined by some set of rules. The modern-day partitioning process consists of 5 – 25 blocks at the top module followed by each block being partitioned recursively into smaller functional blocks ending with gate-level abstraction.

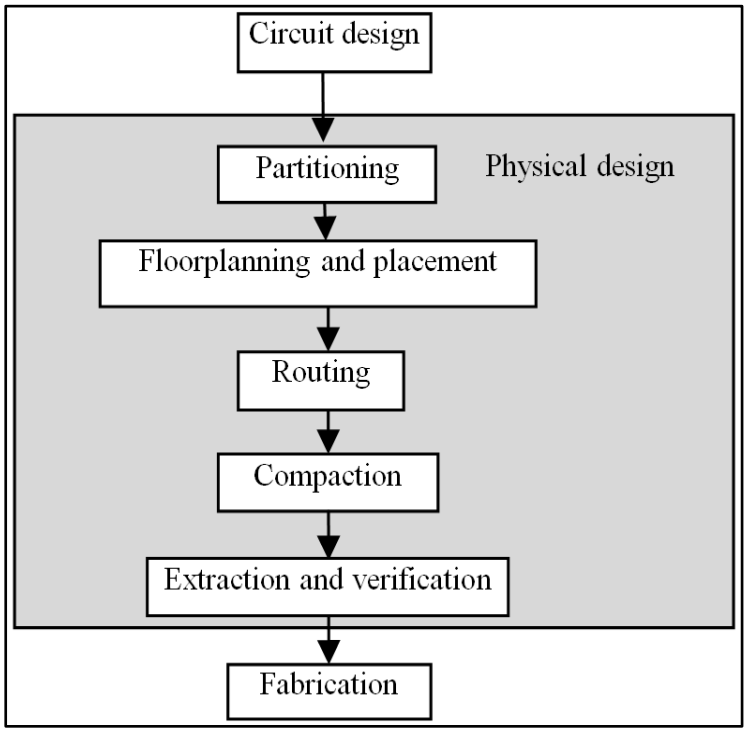


Fig 2.22: VLSI Physical Design Cycle

2.3.1.2 Floorplanning and Placement

During this stage, the blocks are arranged wisely on the entire chip area, considering the optimum utilization of the real estate. The whole chip area is effectively divided among the blocks while taking into account the number and the size of the blocks and the type of components in the blocks. The interconnecting area into the blocks is also to be well-thought-out. The size of the blocks is measured by aspect ratio. Though it can be varied by pre-defined instructions. The block shapes may be generalized by rectilinear shapes.

Floorplanning is an important stage during the physical design flow since it sets up the preliminaries for an effective layout. It is tedious computational work, and more often demands a design-engineer instead of a CAD tool, since a human eye better understands the entire floor to realize the block arrangements effectively for essential signal processing, taking into consideration. Therefore, based on the signal flow and the requirement of specific blocks' positioning at specific locations determines the efficacy of the floorplanning.

The exact positions of the functional blocks are determined during the placement stage. The prime concern is to allocate the optimum area for the blocks including their interconnections while satisfying the performance matrices. It essentially takes care of the routable area and the timing budget of some critical nets during placement. Therefore, two-fold approaches are required for the placement: first, a rough area distribution is carried out. Then, iterative methods are followed to achieve the minimum possible area for a compact layout for a given design specification. Some areas between the blocks are deliberated and left vacant to place the interconnects for the routing. The standard of placement couldn't be evaluated till the routing phase gets finished. The process of iteration may be continued if a unrouteable placement design may occur. The iterations of an efficient placement algorithm carry some effective estimation of areas required for possible routing in the next phase. Moreover, the circuit performance and routing efficiency both depend on the novelty of the placement algorithms since late changes in the placement phase degrade the design quality and increase the die size.

2.3.1.3 Routing

All the interconnections have been made according to the netlist in the routing phase. The routing space or areas have been allotted during partitioning, known as channels and switch boxes. The channels are assigned between the blocks (in 2D spaces) and over the blocks (in 3D spaces). The objective of an efficient router is to make interconnections between circuits with the possible

shortest path through channels and switch box areas, tactically avoiding all cross-connections. The routing is done in two phases: (i) Global routing and (ii) Detailed routing. In the global routing phase, all the functional blocks are connected as per the defined netlist, bypassing the exact details of wires and pins. The global router contains information on possible routing paths/areas for each interconnecting wire. The exact channels, pins, and routing paths are determined in the detailed routing. Precisely, detailed routing is composed of channels and switch box routing. Complete routing with point-to-point interconnections has been established in the phase of detailed routing.

2.3.1.4 Compaction

The total layout area must be minimized in all possible aspects and directions during compaction. Consequently, the interconnecting wire lengths have also been reduced, resulting in time delay minimization during signal processing. The more area will be reduced, the more ICs could be fabricated on a single wafer, effectively cutting the manufacturing cost. Compaction must confirm that there is no violation of the design rule of the layout.

2.3.1.5 Extraction and Verification

The components are all positioned to adhere to the fabrication criteria in this procedure, which accurately confirms the design rules. For instance, a standard design guideline assures a standard physical separation between two conducting wires that are positioned side by side. The Design Rule Check (DCR) extensively supervises dozens of design rules for error-free fabrication.

After the design rule check and subsequent elimination of possible errors in the layout, it is time to extract the circuit parameters. A reverse engineering process presents a circuit-level abstraction from the layout level. Therefore, the extracted circuit is validated with the original circuit descriptions. The process is known as layout versus schematics (LVS). The extracted circuit parameters in terms of resistance and capacitance through the timing budget of the circuit elements and interconnects are accurately calculated. The process is known as performance verification. The reliability of the circuits studied in this process is known as reliability verification, which ensures that the circuit can withstand the reliability issues like electro-migration, self-heating, etc. [2.37].

Physical design is a recursive process, i.e., each step repeats itself several times unless the desired results are obtained. The process is hierarchical, i.e., to maintain better quality results at any stage. The previous stage's outcome needs to be better. For example, a poor placement can't yield the best result through excellent routing. Therefore, partitioning, floorplanning, and

placement are more important in determining the chip area and performance than routing and compaction. The complexity of all the stages is liable to design constraints and design styles as well.

2.3.2 VLSI Routing

The exact position of the fundamental blocks and pins is assigned, and the netlist of interconnections is generated during the placement stage of the physical design cycle. The free space between the circuits and blocks is assigned for routing regions.

Routing is the term for all of the networks' geometric configurations. Under the condition that they are not short-circuited, nets should be routed through the channels and switch boxes. The following are the input parameters of a typical routing problem:

(i) A netlist
(ii) The timing budget of the nets, particularly the critical ones
(iii) Outcomes of the placements, including,
  (a) Locations of the blocks
  (b) Locations of the pins
  (c) Locations of the I/Os
  (d) RC delay/ length/ metal layer
  (e) RC delay per via

The complexity of routing depends on the types of IC to be manufactured. For example, optimizing net wire length while carrying out all interconnections in the routing phase is the assigned task for a general-purpose IC. On the other hand, for a high-performance IC, the timing budget of each net must be satisfied in the course of routing. And special routers are needed to be deployed to route the clock nets, power nets and ground nets.

The present-day VLSI technology allows fabrications of billions of transistors in a single IC, resulting in millions of nets being successfully routed maintaining the timing budget. There are thousands of routes available to channel a net from source to destination. Thus, the routing problem becomes computationally hard to deal with. Swarm intelligence (SI) based metaheuristics could be an appropriate tool to effectively solve the issues, that originated during the routing phase.

The routing of VLSI design is broadly divided into two phases: global routing and detailed routing. The list of routing areas is assigned for each net during the global routing phase, avoiding

the real geometric path for the wires. In the detailed routing phase, specific geometric paths are assigned for respective nets within the assigned channel. Each time, the detailed router count on one routing region in the channel and manifest the exact layout of the wires passing through the channel including the positions of vias for a complete layout. The channel and box routing problems are NP-complete problems. There are two approaches to solving the global routing problem because it cannot be addressed in a polynomial amount of time: (i) sequential approach and (ii) concurrent approach.

Sequential Approach

The nets are routed consecutively, as their name suggests, one after the other. Once one net is routed, it could present challenges for the routing of another net. Yet the process should be continued. Therefore, an algorithm is required to be framed to prioritize the routing of critical nets. The criticality depends on the importance of the net. For example, clocks are considered the highest critical nets as per their performances. So they retain the top priority under routing. The nets of the critical paths of the circuit are the next priority to be routed. Nonetheless, the sequencing technology is not foolproof. Therefore, a practical router always involves the routing phase followed by an improvement phase to remove the obstacles as and when required for future routing. However, this may not overcomes the shortcomings of this kind of approach.

The "rip and route" and "shove aside" are some samples of sequential approaches [2.38 – 2.29]. In the "rip and route" approach, the obstacle wires are ripped out and rerouted. In the "shove aside" technique, the wires are kept aside, through which a failed connection could be completed without affecting the existing connections. Another approach [2.40] involves the routing of the simple nets interconnected with 2-3 terminals only. Such a kind of connection usually covers 75% of the routing of a typical layout. Therefore, intermediate nets are routed through the Steiner tree algorithm. And finally, the remaining multiterminal nets comprised of clocks, power and ground nets are routed by Maze router. Therefore, the sequential routing comprises of:

(i) Two-terminal algorithm
   (a) Maze routing
   (b) Line-probe routing
   (c) Shortest path based approaches

(ii) Multiterminal algorithms
   (a) Steiner tree-based approach

(A) Concurrent Approaches

The routing of all nets collectively is avoided by the concurrent technique. Unfortunately, this is a computationally challenging approach, and not even for two-terminal nets is there an effective polynomial solution. One of the answers in this method is integer programming, albeit it is challenging to implement due to the size of the programme. In order to efficiently use integer programming to solve the complex programme, a hierarchical method is used to break it up into manageable pieces. Without exceeding the channel's capacity, global routing specifies a series of routing channels for each net. Additionally, it reduces the overall length of the wire. The optimization function is designed in high-performance circuits to reduce the net's RC latency.

2.3.3 Swarm Intelligence

A natural biological system consists of individual decentralized agents performing some intelligent tasks with self-organization, known as swarm intelligence. Under this discipline, the social behavior of natural agents is studied by exploring their group communications and interactions with their environment. Examples of swarm intelligence are an ant colony, a colony of termites, a school of fishes, a flock of birds, and a herd of animals. It can be classified into several categories based on specific criteria, mentioned as follows:

(a) Natural Vs. Artificial

Natural swarm intelligence consists of a biological system comprising natural agents. On the contrary, an artificial class is built with a man-made system or artifacts like a multi-robot system deployed for performing a specific task.

(b) Scientific Vs. Engineering

An alternative classification of swarm intelligence is made based on the kind of task to be achieved by it. The scientific model explores the agent-to-agent and agent-to-environment interaction of entire swarms in performing any intelligent task. The engineering model explores the scientific model further, framing the model suitable to perform any real-life practical problem.

The variant described above, natural, artificial, scientific, and engineering approaches, are orthogonal by nature. Therefore, while the scientific approach explores natural systems, the engineering approach exploits the artificial system primarily. However, the crossover models are frequently developed in critical problem-solving. For example, the analytical model of bio-creatures (scientific approach) has been justified using man-made robotic systems (artificial

systems). On the other hand, many real-life problems (engineering approach) have been addressed by exploring the social behavior of biological creatures (natural systems).

A typical swarm intelligent system consists of a group of homogeneous agents, either identical in nature or belonging to some topology. The individual and group behavior of the swarm is explored and mathematically modeled. Their interactions with the surrounding environment are also studied and modeled to solve practical problems. Moreover, the individual interactions of the swarm agents manifested the group behavior of a self-organized pattern.

A typical swarm intelligent system acts in a corroborative fashion without any group leader or external influence. This is an example of every individual's effort collectively toward the same direction in achieving some common interests. Despite the lack of any leading agent, the swarm acts intelligently with the combined efforts of spatially separated individual interactions following some simple rules.

Different kinds of swarms exist in nature with different levels of intelligence. However, self-organization is the key feature of any swarm behind their intelligent behavior. This self-organization of the swarm system has been characterized by [2.41] the following features:

(a) Positive Feedback

Through positive feedback, a swarm system maintains its recruitment and reinforcement like trail laying and following (observed in some ant species).

(b) Negative Feedback

Negative feedback is a counterbalance mechanism to avoid saturation or stagnation that may occur during positive feedback. It stabilizes the whole system.

(c) Fluctuations

It is randomness amongst the swarm particles exhibited through random walks or random task-switching among the swarm agents. This characteristic is essential for emerging structures to discover new or better solutions for the group.

(d) Multiple Iterations

This is the process of iterations between the two agents of a swarm while exchanging information. In addition, simultaneous performance sharing, division of labor, etc., are some intelligence of a swarm [2.42].

According to the studies [2.43], a swarm should satisfy the following principles/intelligencies:

(a) **Principle of Proximity**: All swarm agents should maintain space and time computations.

(b) **Principle of Quality**: All agents should reciprocate continuously with environmental changes.

(c) **Principle of Diverse Response**: All agents should interact with their neighbors placed as far as could possible.

(d) **Principle of Stability**: The swarm should not change its mode of action against every fluctuation in the environment.

(e) **Principle of Adaptability**: The swarm must change its course of action as and when required.

References

2.1. Simon Deleonibus (Editor), "Electronic Device Architectures for the NanoCMOS Era from ultimate CMOS scaling to beyond CMOS Devices", Pan Stanford Publishing Pte.Ltd. Singapore, 2009.

2.2. B. R. Nag, “Physics of quantum well devices”, 1st Edition, Vol. 7, Springer Netherlands, 2000.

2.3. Zikang Tang and Ping Sheng, "Nanoscale Phenomena Basic Science to Device Applications", 1st Edition, Vol. 2, Springer-Verlag New York, 2008.

2.4. Trond Ytterdal, Yuhua Cheng, Tor A. Fjeldly, Device Modeling for Analog and RF CMOS Circuit Design, UK, John Wiley & Sons Ltd, 2003.

2.5. Jon Ho Lee Class notes Kyungpook National University.

2.6. John D. Cressler (Editor), Silicon Heterostructure Handbook: Materials, Fabrication, Devices, Circuits and Applications of SiGe and Si Strained-Layer Epitaxy, CRC Press, Taylor and Francis 2005.

2.7. C.T. Sah, “A History of MOS Transistor Compact Modeling”, Proc. Tech. WCM 2005, pp.347–385, 2005.

2.8. B. Brooks, "Standardizing compact models for IC simulation", IEEE Circuits and Devices Magazine, vol. 15, no. 4, pp. 10-13, July 1999.

2.9. J. Mattausch, M. Miyake, T. Yoshida, S. Hazama, D. Navarro, N. Sadachika, T. Ezaki and M. Miura-Mattausch,"HiSIM2 Circuit simulation - Solving the speed versus accuracy crisis," in IEEE Circuits and Devices Magazine, vol. 22, no. 5, pp. 29-38, Sept.-Oct. 2006.

2.10. X. Zhou, S.B. Chiah, S. Chandrasekaran, G.H. See, W.Z. Shangguan, S.M. Pandey, M. Cheng, S. Chu and L.C. Hsia, "A Compact Model for Future Generation Predictive Technology Modeling and Circuit Simulation", 12th International Conference, MIXDES, Krakow, Poland, 22–25, June 2005.

2.11. Moore's Law "Predicts the Future of Integrated Circuits," Computer History Museum, 1965.

2.12. Giorgio Baccarani, Matthew R. Wordeman, and Robert H. Dennard, "Generalized Scaling Theory and Its Application to a MOSFET Design", *IEEE Transactions on Electron Devices*, ED-31 (4), 452 (1984).

2.13. Y. Taur, D. A. Buchanan, W. Chen, D. J. Frank, K. E. Ismail, S. Lo, G. A. Sai-Halasz, R. G. Viswanathan, H. C. Wann, S. J. Wind, and H.-S. Wong, "CMOS Scaling into the Nanometer Regime," Proceedings of IEEE, Vol. 85, pp. 486-504, April 1997.

2.14. B. Doyle, B. Boyanov, S. Datta, M. Doczy, S. Hareland, B. Jin, J. Kavalieros, T. Linton, R. Rios, and R. Chau, "Tri-Gate Fully-Depleted CMOS Transistors: Fabrication, Design and Layout," VLSI Technology Symposium Tech. Dig., pp. 133-134, June 2003.

2.15. J. P. Colinge, M. H. Gao, A. Romano-Rodriguez, H. Maes, and C. Claeys, "Silicon-on-Insulator 'Gate-All-Around Device," IEEE IEDM Tech. Dig., pp. 595-598, Dec. 1990.

2.16. T. Hiramoto, T. Saito, and T. Nagumo, "Future Electron Devices and SOI Technology – Semi-Planar SOI MOSFETs with Sufficient Body Effect–," Japanese Journal of Applied Physics, Vol. 42, pp. 1975-1978, April, 2003.

2.17. J. P. Colinge, Silicon-on-Insulator Technology: Materials to VLSI, Amsterdam, Kluwer Academic Publishers, 1991.

2.18. N. R. Santiago (PhD Thesis) Characterization, Modeling and Simulation of Decananometer SOI MOSFETs, University of Granda, 2007.

2.19. Alok Kumar Kushwaha "the modeling of dual-material doublegate fully-depleted silicon-on-insulator MOSFET" Dept. of ECE, NIT Kurukshetra, India, 2011.

2.20. L. Vancaille, et al., "Influence of HALO implantation on analog performance and comparison between bulk, partially-depleted and fully-depleted MOSFETs," IEEE SOI Conf., pp. 161-163, 2002.

2.21. Y. Taur, et al., "25 nm CMOS Design Considerations", IEDM Tech. Dig, Page(s) 789-792, 1998.

2.22. M. I. Current, S. W. Bedell, I. J. Malik, , L. M. Feng, F. J. Henley, 'What is the future of sub-100nm CMOS: Ultrashallow junctions or ultrathin SOI ?' Solid State Technology, Vol. 43(2000).

2.23. Kousik Naskar, C. J. Clement Singh, Subir Kumar Sarkar, "Analytical illimet of SON MOSFET and realization of future high speed and ultra-dense low power Circuits." Journal of Nano Electronic Physics (JNEP), Vol-4, No-2, 02023(5pp) (2012).

2.24. N. Collaert, P. Verheyen, K. De Meyer, R. Loo and M. Caymax, Silicon Nanoelectronics Workshop Digest 2002, 15–16, Honolulu (HI) and IEEE Trans. Of Nanotechnology, 1(4), pp 190–4, 2002.

2.25. Pritha Banerjee, Priyanka Saha and Subir Kumar Sarkar, "Analytical Modelling and Performance Analysis of Gate Engineered Tri-gate SON MOSFET", IET Circuits, Devices & Systems, DOI: 10.1049/iet-cds.2017.0473, March 2018.

2.26. Bibhas Manna, Saheli Sarkhel, Ankush Ghosh, S S Singh and Subir Kumar Sarkar,"Dual Material Gate Nanoscale SON MOSFET: For Better Performance", International Journal of Computer Application (IJCA), ISBN: 973-93-80875-27-15, 2013.

2.27. Deepon Saha and Subir Kumar Sarkar, "High-speed reduced-leakage SRAM memory cell design techniques for low-power 65 nm FD-SOI/SON CMOS technology", Microelectronics Journal, Elsevier, Vol. 45, pp- 848-856, July 2014.

2.28. Tiya Dey Malakar, Partha Bhattacharyya and Subir Kumar Sarkar, "Analytical Surface Potential Based Modeling of Drain Current & Trans- conductance of Work Function Engineered gate Recessed S/D SOI/SON MOSFET", published in Advances in Industrial Engineering and Management, Vol. 6, No.2, 107-110, 2017.

2.29. Koh R. Buried layer engineering to reduce the drain-induced barrier lowering of sub-0.05 lm SOI-MOSFET. Jpn J Appl Phys 1999; 38:2294–9.

2.30. A. C. Seabaugh and Q. Zhang, "Low-Voltage Tunnel Transistors for Beyond CMOS Logic", Proc. IEEE, vol. 98, no. 12, pp. 2095–2110, December 2010.

2.31. A. M. Ionescu and H. Riel, "Tunneling Field-Effect Transistors as Energy-Efficient Electronic Switches", Nature, vol. 479, pp. 329–337, November 2011.

2.32. S. Saurabh and M. J. Kumar, "Impact of Strain on Drain Current and Threshold Voltage of Nanoscale Double Gate Tunnel Field Effect Transistor (TFET): Theoretical Investigation and Analysis", Japanese Journal of Applied Physics, vol. 48, paper no. 064503, June 2009.

2.33. S. Saurabh and M. J. Kumar, "Estimation and Compensation of Process Induced Variations in Nanoscale Tunnel Field Effect Transistors (TFETs) for Improved Reliability", IEEE Trans. on Device and Materials Reliability, vol. 10, pp. 390–395, September 2010.

2.34. M. J. Kumar and S. Janardhanan, "Doping-less Tunnel Field Effect Transistor: Design and Investigation", IEEE Trans. Electron Devices, vol. 60, pp. 3285–3290, October 2013.

2.35. M. S. Ram and D. B. Abdi, "Single Grain Boundary Tunnel Field Effect Transistors on Recrystallized Polycrystalline Silicon: Proposal and Investigation", IEEE Electron Device Letters, vol. 35, no. 10, pp. 989–992, October 2014.

3.36. Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*, Cambridge University Press, Cambridge, UK, p. 128, 1998.

2.37. H. B. Bakoglu. Circuits, Interconnections, and Packaging for VLSI. Addison Wesley, 1990.

2.38. H. Bollinger. A mature da system for pc layout. Proceedings of first International Printed Circuit Conference, 1979.

2.39. W. A. Dees and P. G. Karger. Automated rip-up and reroute techniques. Proceedings of Design Automation Conference, 1982.

2.40. V. K. De. A Heuristic Global Router for Polycell Layout. PhD thesis, Duke University, 1986.

2.41. Bonabeau E, Dorigo M, Theraulaz G (1999) Swarm intelligence: from natural to artificial systems. Oxford University Press Inc., New York, NY, USA.

2.42. Bonabeau E, Sobkowski A, Theraulaz G, Deneubourg JL (1997) Adaptive task allocation inspired by a model of division of labour in social insects. In: Biocomputing and emergent computation: proceedings of BCEC97, World Scientific Press, pp. 36–45.

2.43. Millonas M M (1994) Swarms, phase transitions and collective intelligence. In: Langton C (Ed) Artificial life III. Addison-Wesley, Reading, MA, pp. 417–445.

CHAPTER 3

Exploring the Impact of Gate and Channel Engineering on the Output Performances of TFETs

3.1 Introduction

In the present era, the downscaling of semiconductor devices has accelerated the performance-boosting for low power VLSI systems and ultra large scale integration [3.1]. However, the adverse effects of scaling crop up short channel effects (SCEs), stirring up bottlenecks for further downscaling of the device, a deadlock situation for semiconductor manufacturing industries. Therefore, this crisis called for alternative devices to carry on the CMOS logic style to abide by Moore's law. As a result, tunnel field-effect transistors (TFET) have emerged as a feasible alternative to short channel MOSFET, fulfilling the futuristic low power technological needs.

Rigorous experimental studies justified the TFET devices as a better contender [3.2, 3.3], substituting short-channel MOSFETs due to their genetic insusceptibility against SCEs since the current conduction mechanism of such devices is governed by quantum mechanical tunneling instead of thermionic emission. Therefore, carrier transportation gets hardly affected by small-geometry effects. Furthermore, the subthreshold swing (SS), another performance matric, is not restricted to 60mV/dec since the device's switching character gets hardly affected by the thermal events, unlike MOS transistors.

However, despite having several advantages, TFETs suffer from shallow drive current, ambipolar conduction and high threshold voltage [3.4, 3.5]. Many engineering techniques have been implemented to improve the device performance by defeating the constraints. For example, heterojunctions with low bandgap materials [3.6, 3.7] for the source region open up remarkable output responses to amplify drive currents. On the other hand, wide bandgap materials are fruitfully applied to the drain region to suppress ambipolarity. In addition, previous works of literature reported a gate tunable barrier formation technique across the channel through the gate and workfunction engineering to control the drain current in reverse tunneling conditions [3.8]. The gate/drain overlapped architecture is another popular engineering technique [3.9, 3.10] to limit ambipolar conduction, though it suffers from low driving current. Gaussian doped drain TFETs attracted significant attention for suppressing ambipolarity [3.11, 3.12]. In addition, channel engineered TFETs [3.13], stacked gate architecture on double gate TFETs are some of the novel concepts for improving subthreshold swing and ON/OFF switching ratio.

Many analytical models are reported to date, deriving surface potential and electric field-based drain current models [3.14, 3.15]. Therefore, a dual material double gate TFET with graded channel and stacked oxide geometry is theoretically studied to explore its enhanced performance compared to conventional DMDG TFETs. Moreover, the analytical model successfully verified against the numerically simulated data and found excellent agreement.

Another promising candidate, p-n-p-n TFETs, conceived by Dawit Burusie [3.16], has been taken into account to exploit further with structural renovation aiming for better ON current and subthreshold swing [3.17-3.20]. The study focused on a step-by-step approach to structural improvisation by inducing high-k spacers. Thus, the end device hetero-oxide spacer-induced p-n-p-n TFETs deliver commendable performances compared to conventional p-n-p-n devices.

3.2. Reviewing the Relevant Works

A phenomenal work has been reported by Boucart and Ionescu [3.21] on the impact of the High-k gate dielectric and temperature on the Double Gate Tunnel FET's performances for the first time. Based on the numerical simulation, the work exposed the superiority of the double gate architecture with SiO_2 gate oxide over the single gate one. Moreover, the DG Tunnel FET device with high-k dielectric has been explored for improved performance. The effects of temperature on the device's performances were studied as well. As the prime parameters, a feasible geometry concerning device length and channel width, suitable with contemporary CMOS technology, was taken care of. According to the 2005 ITRS roadmap, a 50 nm device should offer 0.612 mA of ON current and 10 pA of OFF current, most appropriate for low standby power applications (LSTP). The static response of the proposed device with HfO2 gate dielectric exhibited 0.25 ON current at Vgs = 1.8 V with an average subthreshold swing of 57 mV/dec, where the minimum SS value was 11 mV/dec. The body thickness is optimized to be found as 7 – 8 nm for 50 nm gate length of the device in achieving the highest ON/OFF current ratio of $2x10^{11}$. Moreover, the subthreshold swing at a constant gate voltage (Vgs) was almost independent of the operational temperature.

Verhulst et al. proposed a TFET structure without gate-drain overlap [3.22], particularly compatible with vertical nanowire architecture to effectively reduce ambipolarity and switching speed through device simulation. In addition, the author extended their work [3.23] in developing some model frameworks for a direct comparison of performance analysis among single gate, double-gate, and gate-all-around tunnel FETs. Double-gate and GAA architecture

performed better than single-gate architecture due to more gate controllability over the channel. Therefore, superior performance was observed for the lesser channel width device of about 10 nm. Further, the effect of gate oxide thickness is more pronounced than Si-body thickness, and the scaling of oxide thickness yielded a more positive impact on the device performance.

Choi and Lee [3.24] presented a hetero-gate dielectric Tunnel field-effect transistor to eradicate the shortcomings of the TFET devices. The proposed structure attained high ON-current and suppressed ambipolar conduction. Nevertheless, different gate dielectrics at the source and the drain end succeeded in modulating the band structure. At the source, an abrupt ON-OFF current transition had been obtained by achieving a local minimum at the conduction band edge of the channel favored the tunneling mechanism. In contrast, the application of lower permittivity dielectric material like SiO_2 at the drain end subdued the ambipolar conduction to a great extent.

Further, the authors derived an analytical model [3.25] of single-gate Silicon-on-insulator (SOI) TFET. Finally, the work gleaned a mathematical framework with 2D Poisson's equation in abstracting the surface potential, electric field, and device drain current. They found an excellent agreement of the derived parameters with the FEM results. The proposed model captures the underlying physics of TFET, including SCEs.

Nonetheless, extensive studies have been conducted by the same author groups to investigate the effects of channel length, body thickness, and multi-gate architectures on the device characteristics [3.26]. Therefore, a single gate, double gate, and gate-all-around hetero-gate-dielectric (HG) TFETs were considered for the research. The HG architecture functioned like SiO_2 based TFET in low gate bias and high-k dielectric-based TFET in high gate bias. The study precisely focused on the transition region width (W_{TR}) and the tunneling barrier width (W_{TUN}) in attributing drive current and the switching behavior. The results perceived that long channel SOI TFET got smaller SS than multi-gate HG TFET. In contrast, reducing the channel thickness or increasing the number of gates procured better I_{ON} at high V_{DD}. However, a long channel single-gate structure was advantageous for the HG architecture. On the other hand, for a short channel, multi-gate structure, one needs to pursue higher dielectric material obtaining at par performances.

Mohota et al. set a benchmarked ON current performance [3.27] for 300 mV logic applications. First, a highly staggered heterojunction was formed by $GaAs_{0.35}Sb_{0.65}$-$In_{0.7}Ga_{0.7}As$ to construct hetero-tunnel FET ascertaining record ON current of 190 µA/µm and

100 µA/µm for 0.75 V and 0.3 V of the drain voltages. Parallelly, a homojunction was formed using $In_{0.7}Ga_{0.3}As$ to compare with the heterojunction counterpart. The laboratory experiment found a 400% boost of ON current provided by the hetero-TFET compared to homo-TFET. Later a calibrated simulation environment is created to imitate the fabricated device with an ultra-thin body and scaled EOT to match the device's performance most suitable for 300 mV logic applications.

Elahi et al. made a footprint [3.28] on deriving an analytical model of tunneling current through rigorous calculations of surface potential considering the carrier concentration in the channel for strong and weak inversion phenomena. In addition, Kane's tunneling model with line tunneling device architecture contributed to the drain current as a function of both gate (V_{GS}) and drain (V_{DS}) voltages. Finally, the sub-band quantization and solution of exponential integral functions in device modeling made the analytical expressions more accurate.

Silicon-on-Nothing (SON), an improvised version of Silicon-on-Insulator (SOI), could be made by fabricating a thin Silicon film of 5 – 20 nm thickness grown on the top of a buried oxide of 10 – 30 nm thickness, proven an excellent structure to deliver remarkable performances [3.29] with subdued short channel effects (SCEs). The SON structure is derived from SOI architecture, replacing the buried oxide with air, capable of reducing the SCEs further, applicable for MOSFETs and TFETs [3.30, 3.31]. Moreover, the structure is immensely beneficial for scalable devices of the future generation to meet the demands of the ITRS Roadmap [3.32].

The dual metal gate (DMG) is another extemporized version of the TFET structure. One gate consists of two materials of different work functions placed side-by-side along the direction of the channel, over the top of the gate oxide. The metal gate near the source-channel junction is the tunneling gate, while the metal gate near the drain-channel junction is the auxiliary gate. We can use the sidewall spacer techniques to fabricate the DMG structure [3.33, 3.34]. The tunneling gate should have a lesser work function than the auxiliary gate. The increasing gate voltage causes the channel conduction band to lower at the source side, boosting the ON current significantly due to a stepper band bending at the tunneling interface. On the contrary, the OFF current is reduced at the drain-channel junction due to inferior band bending caused by the higher work function metal of the auxiliary gate. It is observed for the single metal gate that the ON current is higher for the work function value of 4.8 eV than the value of 4.4 eV [3.35]. It also offers a lesser subthreshold swing. Nevertheless, we have to compromise with the OFF-

state current and subthreshold swing if we try to increase the ON current of the device and face crucial power dissipation due to undesirable leakage. However, DMG is attributed with both the merits by structural engineering – to achieve the ON current equivalent to SMG applying higher work function and an OFF current extracted from SMG with lower work function.

The role of gate oxide is bifold in TFET – to act as an insulator and commence gate control over the channel. As an insulating medium, gate oxide blocks the gate leakage. Nevertheless, depending on the nature of a dielectric medium, better capacitive action encourages more charge-accumulation in the channel, leading to a higher current drive at the same voltage. On the other hand, thinner gate oxide encountered the carrier tunneling resulting in the undesired gate leakage [3.36] manifesting more standby power dissipation. Deploying high-k oxide material is one solution to the said problem [3.37]. Moreover, the high-k oxides have added role to supply better electrostatic control by reducing the oxide capacitance.

Saurabh and Kumar exploited a dual material gate nanoscale tunnel FET [3.38] for improved output characteristics, viz, ON current, OFF current, threshold voltage, subthreshold slope, and immunity against drain induced barrier lowering. A strained DMDG structure with high-k dielectric had been deployed for simulation experiments with variation of design parameters, e.g., channel materials, channel lengths, gate oxide materials, and thickness source voltage. To summarize, the work function engineering delivered significant improvement in the overall characteristics of the proposed device. The work successfully achieved commendable performances in terms of I_{ON}, I_{OFF}, V_T, and average SS. Moreover, the SCEs were also suppressed. The work also predicts further performance improvements using smaller bandgap channel material, smaller channel length below 25 nm, smaller oxide thickness, use of high-k dielectric, and lower V_{DD} below 0.5 V.

Manna et al. [3.39] had drawn a comparative study between the performances of the SOI and the SON structure on the short channel MOSFET. They also introduced work function engineering through linear variation in mole fraction variation in the binary metal alloy gate. The theoretical study was based on mathematical modeling. In conclusion, the SON structure proved its superiority, being more immune to short channel effects (SCEs) and better driving current capability. Moreover, the SON structure offered a highly reduced threshold voltage roll-off stem of the work function engineering.

Bagga and Sarkar [3.40] reported another unique application of work function engineering for the enhanced performance of TFETs. An analytical model, derived for the first time of a

triple metal double gate TFET, was an example of tunneling barrier modulation. The work functions of the metals were so chosen that the device could deliver appreciable ON current due to sharp ban bending at the tunneling junction. At the same time, the shallow band bending at the drain-channel junction blocked the reverse tunneling significantly due to the bandpass filtering action served by work function engineering.

Sarkhel et al. [3.41] paid attention to modeling the parasitic fringe capacitance of a double gate TFET elaborating on the role of oxide over the device's performance. Mainly, the parasitic capacitance of the TFET is constituted of three components – gate to drain capacitance (C_{gd}), gate to source capacitance (C_{gs}), and total gate capacitance (C_{gg}). The carrier concentration varies due to the capacitive action of the gate and is directly related to the dielectric permittivity. Basically, one needs to modulate the capacitance of the channel in the preferred region by applying high-k/low-k dielectric materials for the desired switching performance of the device.

Low drive current, ambipolar conduction, and poor RF performance are three major constraints of TFET devices to be implemented in present VLSI circuits. At the gate voltage, below 0 V, the channel's energy bands get aligned so that the energy level of the drain conduction band matches with the channel valence band. As a result, it causes electrons to tunnel through the potential barrier between the channel and drain. Hence the current conduction started in the same direction as before in case of gate voltage greater than *zero*. Therefore, a more negative gate bias causes more drain current to flow for the following reasons: first, the reduced tunneling length in the drain-channel interface, i.e., reverse tunneling junction, and second, the greater number of filled states of the channel valence band gets ready to inject carrier to the vacant states of the drain conduction band. This is known as ambipolar current. Researchers are constantly experimenting with new, innovative structures to improve the device performance in terms of substantial ON current, subdued ambipolar conduction with improved RF characteristics.

Raad et al. [3.42] introduced dielectric and work function engineered TFET structure for better RF performance with lesser ambipolarity. A triple metal gate structure (TFET) with high-k dielectric had been proposed, where metal work functions 1 and 3 are equal, and that of 2 differs contributed to ambipolar suppression with higher ON current and improved RF figure of merits.

The research group led by Sarkar has delivered some important theoretical works [3.43-3.45] to improve the TFET's performance through gate and channel engineering. Moreover, they have justified their works with rigorous analytical modeling and structure renovations. Further, the paper works provide lucrative ideas and brilliant concepts over the underlying physics of TFET, aiming to deliver powerful performances through the renovated structures.

Outstanding research work is performed by Kwon and Park [3.46] to propose a design of asymmetric gate dielectric and body thickness TFET structure. The thinner source end gate dielectric with lesser body thickness ensures better drive current and subthreshold swing by reducing the tunneling resistance at the source-channel interface. On the other hand, thicker drain end gate dielectric and greater body thickness guarantee insignificant ambipolar conduction and reduced gate to drain capacitance (C_{gd}). Furthermore, the proposed device claimed an enhanced switching performance due to high ON current and reduced intrinsic capacitance achieved due to structural reform. The paperwork also suggested a fabrication process for the proposed structure with the contemporary integration technology and validated the steps with technology computer-aided design (TCAD) process.

Abdi and Kumar [3.47] proposed a gate/drain overlapped tunnel FET structure to mitigate the ambipolar condition. In conventional TFET, the tunneling barrier width at both source-channel and drain-channel junctions is controlled by the gate bias irrespective of the polarity. Therefore, it is observed through 2D device simulation that the overlapped gate on the drain region successfully controls the ambipolar current by modulating the barrier width at the reverse tunneling junction. However, the work also demands a significant performance improvement in suppressing I_{amb} even if the drain doping is as high as $10^{19}/cm^3$.

Upasana et al. [3.48] conducted a comparative analysis with gate material and gate dielectric engineered TFET structures. The proposed work considered dual material gate TFET, hetero-dielectric TFET, and dual material hetero-dielectric gate TFET for comparison. A comparative study was made based on the proposed analytical model, which essentially captured the impact of dielectric materials and metal gate length variations on the electrostatic behaviors of the aforementioned devices. A subsequent simulation-based investigation drive was conducted to evaluate the proposed devices' transient responses and intrinsic capacitances. Therefore, the structures got optimized based on gate dielectric and metal gate length.

3.3. Impact of the body thickness on the Device Performances of Graded Channel Tri-metal Double Gate TFET with Stack Gate Oxide

3.3.1. Device Structure

The two-dimensional cross-sectional view of graded channel tri-metal stacked gate oxide TFET is presented in Fig. 1. Channel engineering with work function engineering has been implemented through this device architecture. We used stack gate oxide instead of single Silicon dioxide to weaken the vertical field intensity and diminish short channel effects (SCEs) like hot carrier effects. The channel is divided into three regions of three different doping profiles. The three regions are named R1, R2, and R3, where region R1 is heavily doped, region R2 has the least doping, and region R3 is moderately doped. The lengths of the three regions are considered L1, L2, and L3, respectively, which altogether constitute the total length of the channel Lg. N_{ch1}, N_{ch2}, and N_{ch3} denote the doping concentrations of three regions. Following the lengths of three regions, the gates are constituted of three metals of different work functions of lengths L1, L2, and L3 as well. The work functions of the metal gates are denoted by Φ_{m1}, Φ_{m2}, and Φ_{m3}, respectively. The oxide layers' thickness is t_{Si} for SiO_2 layer, t_{HfO2} for HfO_2 layer. The effective oxide thickness (EOT) is $t_{oxeff} = t_{Si} + (\varepsilon_{Si}/\varepsilon_{HfO2})\, t_{HfO2}$, where ε_{Si} is the permittivity of SiO_2 layer, ε_{HfO2} is the permittivity of HfO_2 layer.

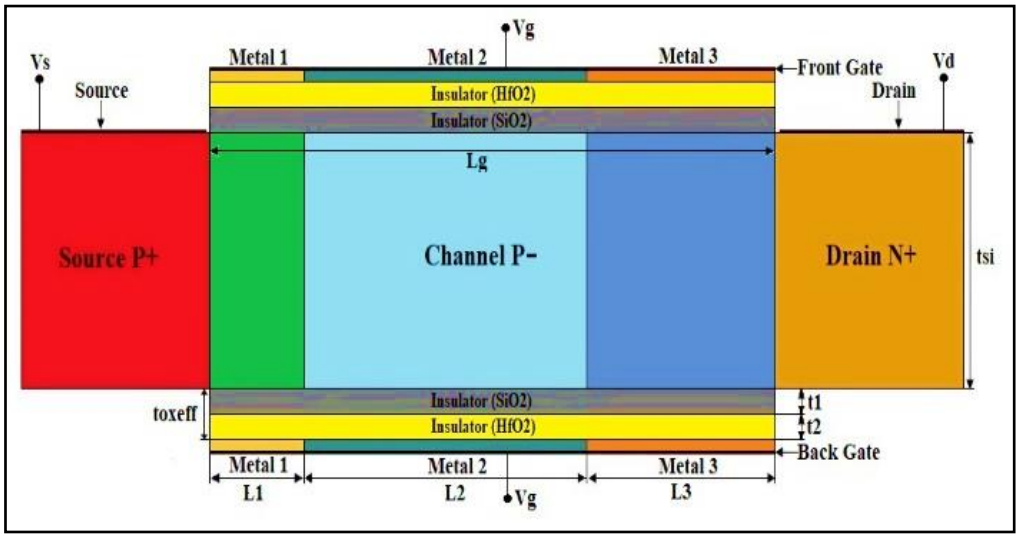


Fig.3.1: 2-D representation of the proposed TMDG-TFET

The device parameters used for analytical modeling and simulation are given in Table 3.1.

TABLE 3.1: PARAMETRS FOR PROPOSED MODEL

Parameters	t_{si}	t_1, t_2	L_1, L_2, L_3, L_g	ε_{ox1}, ε_{ox2}
Values	5nm 8nm	2nm, 2nm	10nm, 30nm, 20nm, 60nm	3.9 ε_0, 22 ε_0
Kane's Parameters	A = 4 x 10^{21} $m^{-1/2}V^{-3/2}s^{-1}$ B = 41 x 10^6 $V\,cm^{-1}$ $D1$ = 2.5 for Indirect Tunneling			
Parameters	N_s	N_d	N_{a1}, N_{a2}, N_{a3}	ϕ_{M1}, ϕ_{M2}, ϕ_{M3}
Values	10^{20} cm^{-3}	5x10^{18} cm^{-3}	10^{18} cm^{-3}, 10^{16} cm^{-3}, 10^{17} cm^{-3}	4.4eV, 5.08eV, 4.08eV

3.3.2. Analytical Modeling

3.3.2.1. Modeling of channel potential

Let N_{ch} be the doping concentration of the channel, and the channel is fully depleted under subthreshold condition. Therefore, the 2-dimensional Poisson's equation [3.49] of the surface potential for a p-type substrate is given by,

$$\frac{d^2\psi_i(x,y)}{dx^2}+\frac{d^2\psi_i(x,y)}{dy^2}=\frac{qN_{ch}}{\in_{si}} \qquad \text{for } (0\le x\le L_g, 0\le y\le t_{si}) \qquad (3.1)$$

For a graded channel, i=1, 2, and 3 stand for the different doping regions in the channel, as depicted in Fig 1. The channel length, denoted by Lg, consists of regions of three different concentrations, i.e., region1 of length L1, region 2 of length L2, and region 3 of length L3, respectively, with the doping concentration of N1, N2, and N3.

The second-order differential equation can't be directly solvable; therefore, we followed Young's parabolic approximation model [3.50], the equation (2), to transform the 2-D equation to 1-D ODE (ordinary differential equation).

$$\psi_i(x,y)=\psi_s(x)+c_{1i}(x)y+c_{2i}(x)y^2 \qquad (3.2)$$

The arbitrary constants c_{11}, c_{12}, c_{13}, c_{21}, c_{22}, and c_{22} could be derived by considering the equality of the potential and the continuity of the electric flux at the interface regions viz front gate oxide/substrate and back gate oxide/substrate interfaces.

$$c_{11}(x)=\frac{\varepsilon_{oxeff}}{\varepsilon_{si}}.\frac{\psi_{s1}(x)-V_{GS1}}{t_{oxeff}},\ c_{12}(x)=-\frac{\varepsilon_{oxeff}}{\varepsilon_{si}.t_{si}}.\frac{\psi_{s1}(x)-V_{GS1}}{t_{oxeff}} \tag{3.3}$$

$$c_{21}(x)=\frac{\varepsilon_{oxeff}}{\varepsilon_{si}}.\frac{\psi_{s2}(x)-V_{GS2}}{t_{oxeff}},\ c_{22}(x)=-\frac{\varepsilon_{oxeff}}{\varepsilon_{si}.t_{si}}.\frac{\psi_{s2}(x)-V_{GS2}}{t_{oxeff}} \tag{3.4}$$

$$c_{31}(x)=\frac{\varepsilon_{oxeff}}{\varepsilon_{si}}.\frac{\psi_{s3}(x)-V_{GS3}}{t_{oxeff}},\ c_{32}(x)=-\frac{\varepsilon_{oxeff}}{\varepsilon_{si}.t_{si}}.\frac{\psi_{s3}(x)-V_{GS3}}{t_{oxeff}} \tag{3.5}$$

The effective gate voltages and Flat band voltages for the three regions across the channel are given by,

$v_{GS_1}=v_{GS}-v_{FB_1}$, $v_{GS_2}=v_{GS}-v_{FB_2}$, $v_{GS_3}=v_{GS}-v_{FB_3}$

And, $v_{FB_1}=\phi_{m_1}-\phi_{si_1}$, $v_{FB_2}=\phi_{m_2}-\phi_{si_2}$, $v_{FB_3}=\phi_{m_3}-\phi_{si_3}$ where ϕ_{m_i} and ϕ_{si_i} are the work functions of the metal for respective materials and silicon substrate (due to different doping concentrations). The silicon work function is given by,

$\phi_{si_i}=\chi+E_g/2+\phi_{B_i}$. Where, $\phi_{B_i}=V_T\ln(N_{chi}/n_i)$, the built-in potential for three respective doping regions in the channel.

Substituting (3.3), (3.4), and (3.5) in (3.1), the generalized second-order 1-D Poisson's equation is derived as,

$$\psi''_{s_i}(x)+2C_{i2}(x)=\frac{qN_{ch_i}}{\varepsilon_{si}}, \text{ where } i=1, 2, \text{ and } 3. \tag{3.6}$$

The solutions of Eqn (3.6) for three different regions (i=1, 2, 3) are given as,

$$\psi_{s1}(x)=Ae^{kx}+Be^{-kx}+D_1, \text{ for reg 1;} \tag{3.7}$$

$$\psi_{s2}(x)=Ce^{kx}+De^{-kx}+D_2, \text{ for reg 2;} \tag{3.8}$$

$$\psi_{s3}(x)=Ee^{kx}+Fe^{-kx}+D_3, \text{ for reg 3;} \tag{3.9}$$

$$\text{where } k^2=2C_{oxeff}/(\varepsilon_{si}t_{si}) \text{ .} \tag{3.10}$$

$$D_1=V_{GS1}-qN_{ch1}/(\varepsilon_{si}k^2) \tag{3.11}$$

$$D_2=V_{GS2}-qN_{ch2}/(\varepsilon_{si}k^2) \tag{3.12}$$

$$D_3=V_{GS3}-qN_{ch3}/(\varepsilon_{si}k^2) \tag{3.13}$$

The arbitrary constants A, B, C, D, E, and F of (3.7), (3.8), and (3.9) could be computed from the following boundary conditions,

Continuity of potential at the interface of regions 1-2 and regions 2-3 is given by,

$$\psi_1(L_1,0)=\psi_2(0,0)\ \&\ \psi_2(L_2,0)=\psi_3(0,0) \tag{3.14}$$

Continuity of electric field at the interface of region 1-2 and region 2-3 is given by,

$$\frac{d\psi_1(x,y)}{dx}\Big|_{x=L_1}=\frac{d\psi_2(x,y)}{dx}\Big|_{x=0}\ \ \&\ \ \frac{d\psi_2(x,y)}{dx}\Big|_{x=L_2}=\frac{d\psi_3(x,y)}{dx}\Big|_{x=0} \tag{3.15}$$

The potential at the source-channel junction is given by,

$$\psi_1(0,0)=V_{bip}=V_T\ln(N_{srs}N_{ch_1}/n_i^2) \tag{3.16}$$

The potential at the drain-channel junction is given by,

$$\psi_3(L_3,0)=V_{bin}+V_{DS}=V_T\ln(N_{dr}N_{ch_3}/n_i^2)+V_{DS} \tag{3.17}$$

Following the method of substitution in solving the Eqn (3.7), (3.8), and (3.9) using the given conditions in (3.14), (3.15), (3.16), and (3.17), the constants' values are as follows,

$$B=m_1+m_2-m_3+m_4-m_5-m_6-m_7-m_8-m_9; \tag{3.18}$$

Where,

$$\left.\begin{aligned}
m_1&=V_{bid}/(e^{-kL_g}-e^{kL_g})\\
m_2&=V_{ds}/(e^{-kL_g}-e^{kL_g})\\
m_3&=V_{bis}e^{kL_g}/(e^{-kL_g}-e^{kL_g})\\
m_4&=D_1e^{kL_g}/(e^{-kL_g}-e^{kL_g})\\
m_5&=\frac{D_1-D_2}{2e^{kL_1}}e^{kL_g}/(e^{-kL_g}-e^{kL_g})\\
m_6&=D_3/(e^{-kL_g}-e^{kL_g})\\
m_7&=\frac{D_2-D_3}{2e^{k(L_1+L_2)}}e^{kL_g}/(e^{-kL_g}-e^{kL_g})\\
m_8&=\frac{D_1-D_2}{2e^{-kL_1}}e^{-kL_g}/(e^{-kL_g}-e^{kL_g})\\
m_9&=\frac{D_2-D_3}{2e^{-k(L_1+L_2)}}e^{-kL_g}/(e^{-kL_g}-e^{kL_g})
\end{aligned}\right\} \tag{3.19}$$

$$A=V_{bis}-B-D_1 \tag{3.20}$$

$$C = \frac{2Ae^{kL_1} + D_1 - D_2}{2e^{-kL_1}} \tag{3.21}$$

$$D = \frac{2Be^{-kL_1} + D_1 - D_2}{2e^{-kL_1}} \tag{3.22}$$

$$E = \frac{2Ce^{k(L_1+L_2)} + D_2 - D_3}{2e^{k(L_1+L_2)}} \tag{3.23}$$

$$F = \frac{2De^{-k(L_1+L_2)} + D_2 - D_3}{2e^{-k(L_1+L_2)}} \tag{3.24}$$

3.3.2.2. Modeling of Electric Field

Electric field is defined as the gradiant of potential. Therefore, the field intensity of the respective regions are derived on differentiating the calcilated surface potential w.r.t 'x' and 'y' to get the lateral and longitudinal field as follows,

$$E_1(x) = -\frac{d\psi_1(x,y)}{dx} = k(Be^{-kx} - Ae^{kx}) = E_{1x} \tag{3.25}$$

$$E_2(x) = -\frac{d\psi_2(x,y)}{dx} = k(De^{-kx} - Ce^{kx}) = E_{2x} \tag{3.26}$$

$$E_3(x) = -\frac{d\psi_3(x,y)}{dx} = k(Fe^{-kx} - Ee^{kx}) = E_{3x} \tag{3.27}$$

$$E_1(y) = -\frac{d\psi_1(x,y)}{dy} = -c_{11}(x) - 2yc_{12}(x) = E_{1y} \tag{3.28}$$

$$E_2(y) = -\frac{d\psi_2(x,y)}{dy} = -c_{12}(x) - 2yc_{22}(x) = E_{2y} \tag{3.29}$$

$$E_3(y) = -\frac{d\psi_3(x,y)}{dy} = -c_{13}(x) - 2yc_{23}(x) = E_{3y} \tag{3.30}$$

E1x, E2x, and E3x are electric field components along the channel length direction, considered lateral electric fields, and E_{1y}, $E_{2y,}$ and E_{3y} are electric field components along the channel height considered as longitudinal electric fields. The field E_1 in equation (3.31) refers the resultant electric field in region-1 of the channel of the proposed device.

$$E_1 = \sqrt{E_{1x}^2 + E_{1y}^2} \tag{3.31a}$$

Using eqn. 3.25

$$E_{1x} = k(Be^{-kx} - Ae^{kx});$$

Now using Taylor series expansion for exponential terms:

$$e^x = 1 + \frac{x}{1!} + \frac{x^2}{2!} + \frac{x^3}{3!} + \ldots$$

$$\therefore E_{1x} = k\{B(1-kx) - A(1+kx)\}$$

$$= k\{[(B-A) - kx(B+A)\}$$

$$= (B-A)k - xk^2(A+B)$$

$$= h_1 + xh_2$$

Where, $h_1 = (B-A)k$ and, $h_2 = k^2(A+B)$

Similarly using eqn. 3.28

$$E_{1y} = c_{11}(x) - 2yc_{12}(x)$$

$$= -\frac{\varepsilon_{oxeff}(\psi_{si}(x) - V_{gs1})}{\varepsilon_{si}t_{oxeff}} + \frac{2y\varepsilon_{oxeff}(\psi_{si}(x) - v_{gs1})}{\varepsilon_{si}t_{si}t_{oxeff}}$$

$$= -\frac{\varepsilon_{oxeff}\{(A+B+D1-V_{gs1}) + kx(A-B)\}}{\varepsilon_{si}t_{oxeff}} + \frac{2y\varepsilon_{oxeff}\{(A+B+D_1-V_{gs1}) + kx(A-B)\}}{\varepsilon_{si}t_{si}t_{oxeff}}$$

$$= h_3 + h_4x + 2yh_5 + 2yxh_6$$

Where, $h_3 = -\frac{\varepsilon_{oxeff}(A+B+D1-V_{gs1})}{t_{si}t_{oxeff}}$; $h_4 = -\frac{\varepsilon_{oxeff}k(A-B)}{\varepsilon_{si}t_{oxeff}}$ and;

$h_5 = \frac{\varepsilon_{oxeff}(A+B+D_1-V_{gs1})}{\varepsilon_{si}t_{si}t_{oxeff}}$; $h_6 = \frac{\varepsilon_{oxeff}(A-B)kx}{\varepsilon_{si}t_{si}t_{oxeff}}$

$$\therefore E = \sqrt{E_{1x}{}^2 + E_{1y}{}^2}$$

=

$$\left[(h_1{}^2 + h_3{}^2) + 2x(h_1h_2 + h_3h_4) + x^2(h_2{}^2 + h_4{}^2) + 4yh_3h_5 + 4y^2h_5{}^2 + 4xy(h_3h_6 + h_4h_5) + 4x^2y^2h_6{}^2 + 4yx^2h_4h_6 + 8y^2xh_5h_6\right]^{1/2} \quad (3.31b)$$

Therefore, *E1* can be evaluated by substituting h_1, h_2, h_3, h_4, h_5 and h_6 in the equation (3.31b).Similarly, electric fields of region-2 & 3 i.e., E_2 and E_3 can be derived. And the total electric field is defined as,

$$E_{Total} = \begin{Bmatrix} E_1, 0 \le L \le L_1 \\ E_2, L_1 \le L \le L_2 \\ E_3, L_2 \le L \le L_g \end{Bmatrix}$$

where, L_1, L_2, L_3 and L_g are defined in Table 3.1.

Since the electric fields E_2 and E_3 for region 2 & 3 respectively, are negligible compared to the field for region-1, E_1, therefore these two fields have insignificant role in computing the drain current.

3.3.2.3. Modeling of Drain Current

The drain current of the proposed TFET is defined as a number of tunneling charges per unit volume. Here Kane's local tunneling model [3.51] is used to derive the drain current by integrating the carrier generation rate across the tunneling volume.

$$I_{DS} = q\iint G dV = q\iint G dx dy \tag{3.32}$$

and, $$G(E) = A_1 E^{D1} \exp[\frac{-B_1}{E}] \tag{3.33}$$

The generation rate is a function of electric field, and A_1, B_1, and D1 are Kane's parameters mentioned in Table 3.1.

3.3.3. Results and Discussions

We have used the SILVACO ATLAS 2-D device simulator [3.52] to carry out the simulation process. The required physical models include the Shockley-Reed-Hall (SRH) and auger recombination models for minority carrier lifetime during the generation-recombination process, the Fermi-Dirac distribution principle to precisely attribute the band structure for heavily doped materials, bandgap narrowing model to capture the band bending at the junction regions, and Kane's model to derive the current due to quantum mechanical tunnelling for the TFET structures. All the simulations are conducted at room temperature, 300 K. Two different body thicknesses (t_{Si}=5nm and 8nm) are considered for the proffered structure to examine the impact of the body thickness variability on the device's response. The accuracy of the analytical model is verified against the results of the simulation data.

In Fig.3.2, the surface potential variation with different gate voltage at a fixed drain bias is presented for both structures with 5nm and 8nm body thickness. The same graph also presents potential variations with different drain voltages for a fixed gate bias. An accurate

reflection of potential barrier modulation along the channel region is depicted in the said Fig, implemented through appropriate work function engineering of the tri-metal double gate TFET structure. The barrier-hight created by the second metal gate, workfunction of which is intentionally kept higher to maintain a potential barrier between source and drain, could be modulated by the gate voltage. The advantage is twofold: first, it reduces the barrier at the onset of the ON state of the device; second, it provides a potential barrier at the ambipolar state to restrict the reverse tunneling conduction. As a result, the device offers a low ambipolar current with a high ON/OFF current ratio due to better barrier modulation by the 5 nm device than that of the 8nm device since the gate control is more pronounced for the 5nm body thickness device.

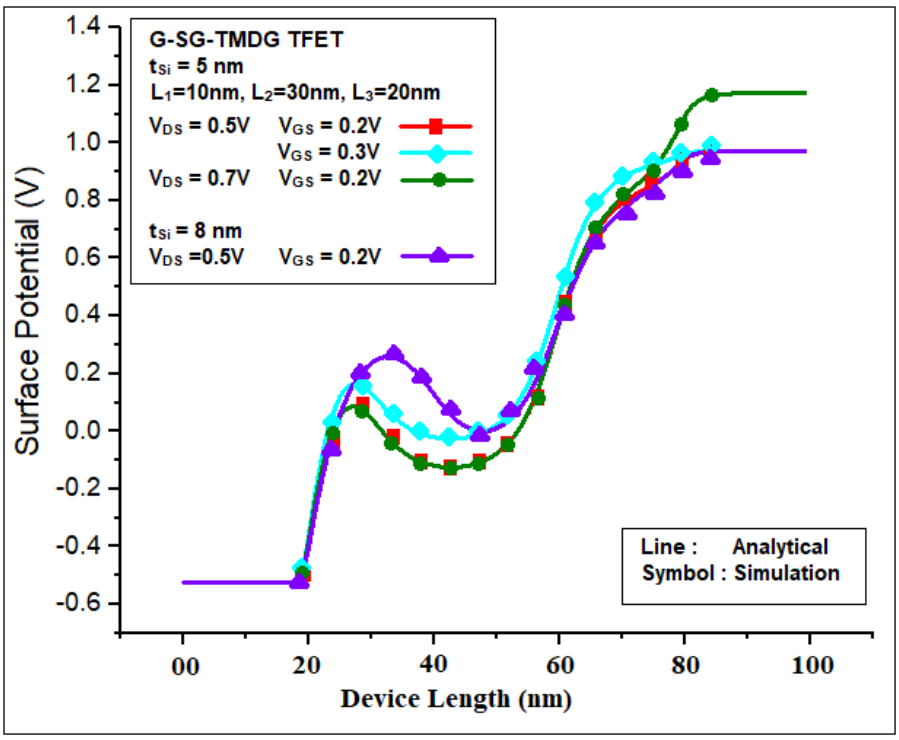


Fig. 3.2: Surface Potential profile along channel length of the proposed structures (tsi=5nm and 8nm) for different Gate voltages (at constant V_{DS}) and different Drain voltages (at constant V_{GS})

The total electric field distribution along the channel for both the device structures has been presented in Fig 3.3. The simulation process is conducted with a gate voltage of 0.3V (V_{GS}) and drain voltage (V_{DS}) of 0.5V. The peak electric field at the source end is higher for the 5nm device than the 8 nm device, justifying the device's better gate controllability. Moreover, it results in a higher carrier generation rate for the device than its contender, leading to a higher drive current. The field intensity gets shallower inside the drain region for the 5 nm device at the drain end, aiding more resistance against the reverse tunnelling of the charge carriers from

drain to channel. As a result, the 5 nm device should offer better ambipolar behavior than that of its counterpart.

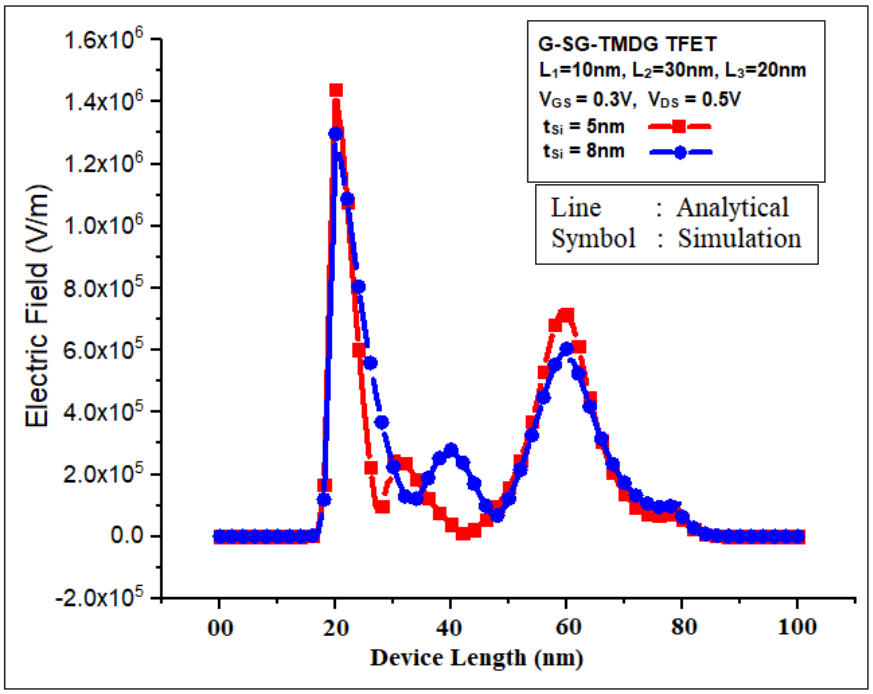


Fig. 3.3: Electric field profile along channel length of the proposed structures (tsi=5nm and 8nm) for V_{GS}=0.3V and V_{DS}=0.5V

The comparative study of the transfer characteristics on the linear scale is performed in Fig 3.4. It mainly explored the super-threshold characteristics of the devices. The drain current is plotted with 1.2V of the gate voltage (V_{GS}) and 0.5 and 1.0V of the drain voltages (V_{DS}). The device with lower body thickness (5 nm) generates more drive current. Moreover, the threshold voltage for the said structure is even lesser than that of the device with a larger substrate size.

For TFET devices, it has always been our primary aim to increase the I_{ON}/I_{OFF} ratio with a steep subthreshold slope while keeping the ambipolar conduction low. Therefore, the transfer characteristics of the devices under test are drawn on a log scale in Fig 3.5, precisely exploring the I – V behavior in the subthreshold region. Our work is thriving the strategy of channel engineering, performed by graded channel with three different regions in the channel with a suitable doping profile to boost the ON current while keeping the OFF current and ambipolar conduction as low as possible. The device performs well at the ON state with biasing conditions of V_{DS} = 0.5V and V_{GS} = 1.2V. The 5nm device offers a shallow OFF current and ambipolar conduction order of 10^{-16} following a trade-off against the ON current. However, we still have an ON current of order 0.1mA. The Silicon film thickness has negligible influences over the subthreshold swing (SS) of TFET devices. Still, the higher electric field for a smaller device

plays a role in improving the SS of that structure. The 8nm device structure possesses an SS of 41.5mV/decade in this work. In contrast, the 5nm structure holds an SS value of 40mV/decade, which is quite commendable for similar kinds of structures.

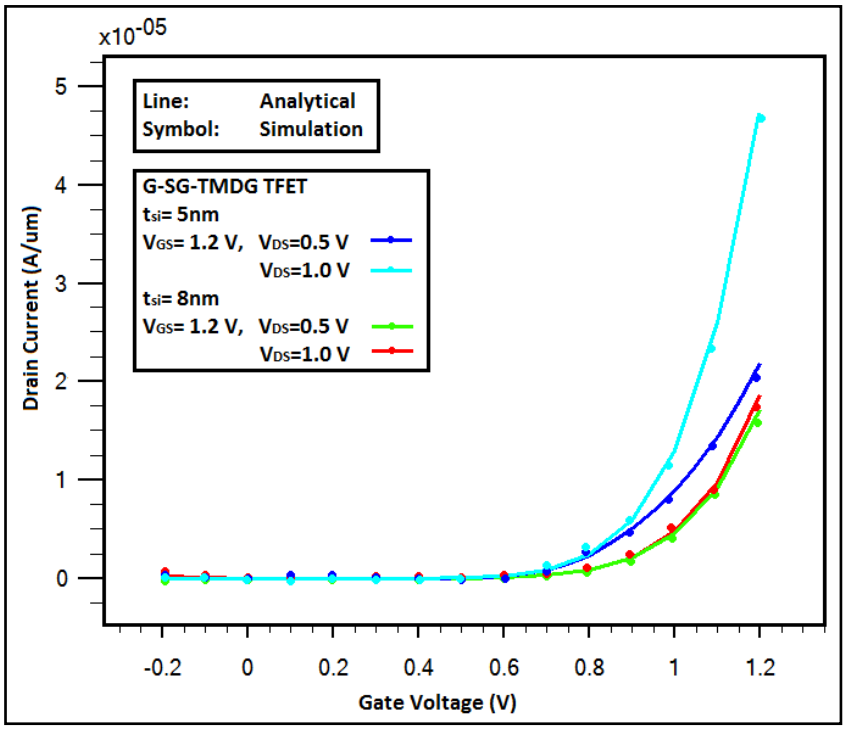


Fig. 3.4: Transfer characteristics of the proposed device structures (tsi=5nm and 8nm) for different V_{DS} at constant V_{GS} on a linear scale.

The work performed a comparative study of the proposed graded channel DMDG TFET with stack-gate architecture with two different substrate widths. An analytical model is derived and verified against the simulated results through the SILVACO ATLAS TCAD simulator. The performance of the proposed device is reasonably good at the low voltage range of 0.5V of V_{DS} and V_{GS} as well, justifying its potentiality in low-power VLSI applications. The ON current is about 0.1mA, and the OFF current is below the femto-ampere with I_{ON}/I_{OFF} ratio of 10^{11} and sub-threshold swing (SS) of 40mV/decade at room temperature 300K. The simulation data is in good agreement with the analytical model, validating its accuracy. The experiment was conducted with the 50nm gate length device and achieved satisfactory results. However, beyond that gate length, the short channel effects (SCEs) dominate the device performance, and hence alternative engineering is required for significant performances.

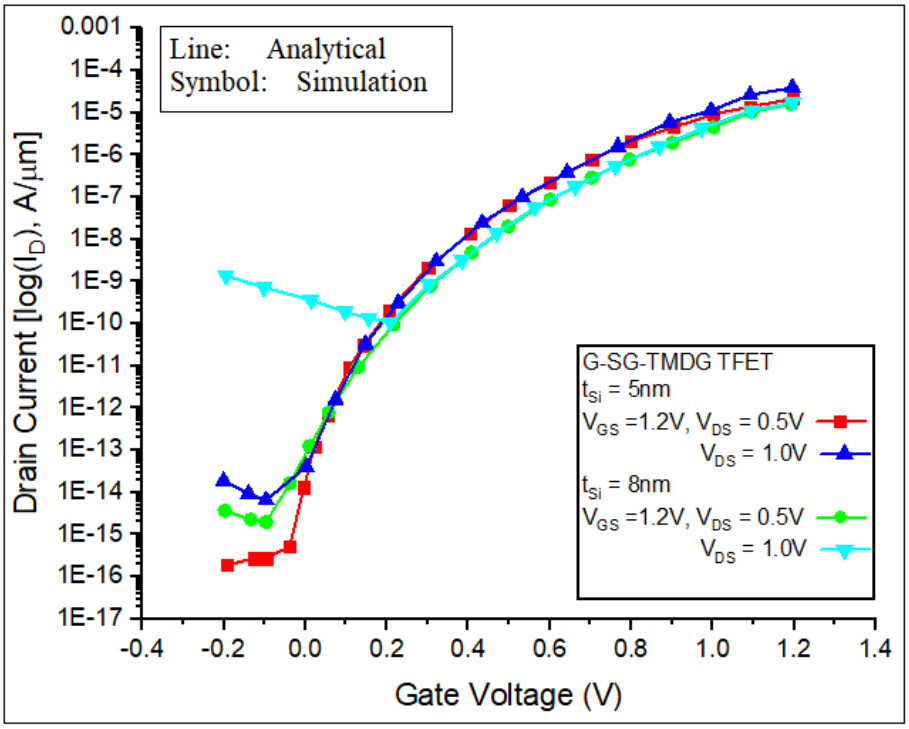


Fig. 3.5: Transfer characteristics of the proposed device structures (tsi=5nm and 8nm) for different V_{DS} at constant V_{GS} in Semi-Logarithmic Scale

3.4. Spacer Induced Hetero-gate Dielectric p-n-p-n TFET for Improved Performances

3.4.1. Proposed Device Structure

The 2D cross-sectional view of a conventional double gate p-n-p-n TFET is presented in Fig 3.6(a). The source is heavily doped with p-type, the drain is moderately doped with n-type, and the channel is lightly doped with p-type elements. In addition, a highly doped n-type pocket has been implanted near the source side in the channel to improve the ON current characteristics. Moreover, to subdue the OFF current and ambipolar conduction, drain doping is maintained lower than source doping. Typically, SiO_2 is used as the gate dielectric with Aluminium gates. Fig. 3.6(b), representing the hetero-gate oxide architecture of the p-n-p-n TFET, carries only the difference that oxide layers constituted with two oxides – HfO_2 and SiO_2 – from the source to drain side. The purpose is further to boost the ON current with high switching behaviour while retaining the OFF/ambipolar current as low as possible. In our design, the total gate oxide length is divided equally for HfO_2 and SiO_2.

Fig. 3.6(c) is the improvised architecture from the previous structure incorporating high-k spacers at the drain end of the gate oxides, called spacer induced hetero-gate dielectric p-n-p-n TFET. The simulations are carried out with two different spacer elements: Hafnium dioxide (HfO_2) and Titanium dioxide (TiO_2), and finally, a comparative study is made. Moreover, the effect of interface trap charges at the oxide–body interface is also considered in experiments. The length through which the trap charges are considered to present is known as damaged length and is denoted by L_d. The damaged length is considered on both sides of the channel. All the design parameters for modeling and simulations are provided in Table 3.2.

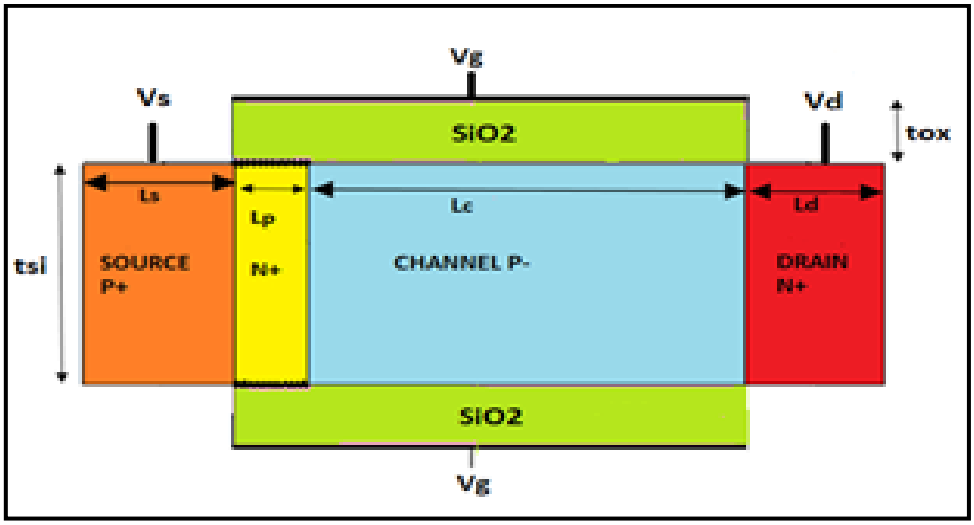


Fig. 3.6(a). Schematic view of Double gate p-n-p-n TFET (SiO_2 as gate oxide)

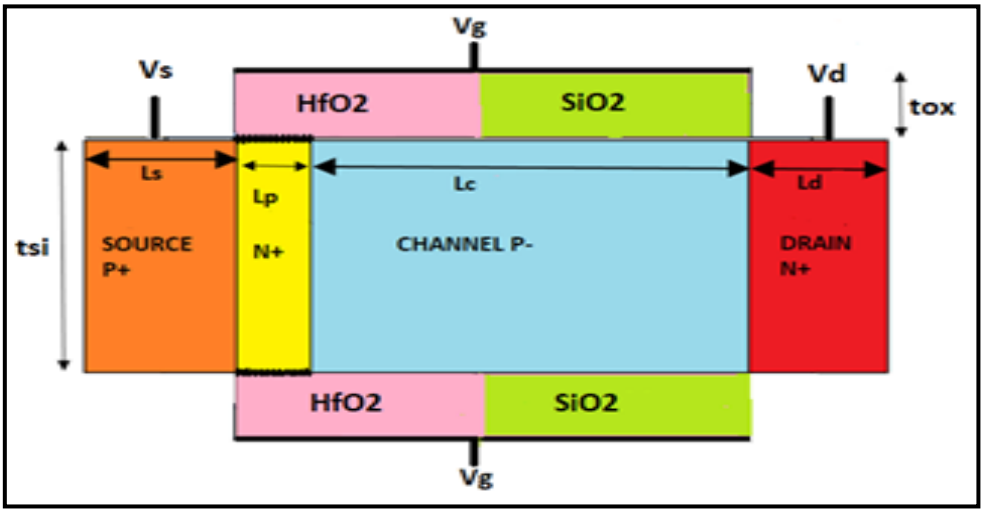


Fig. 3.6(b). Schematic view of Double gate p-n-p-n TFET (hetero oxide as gate oxide)

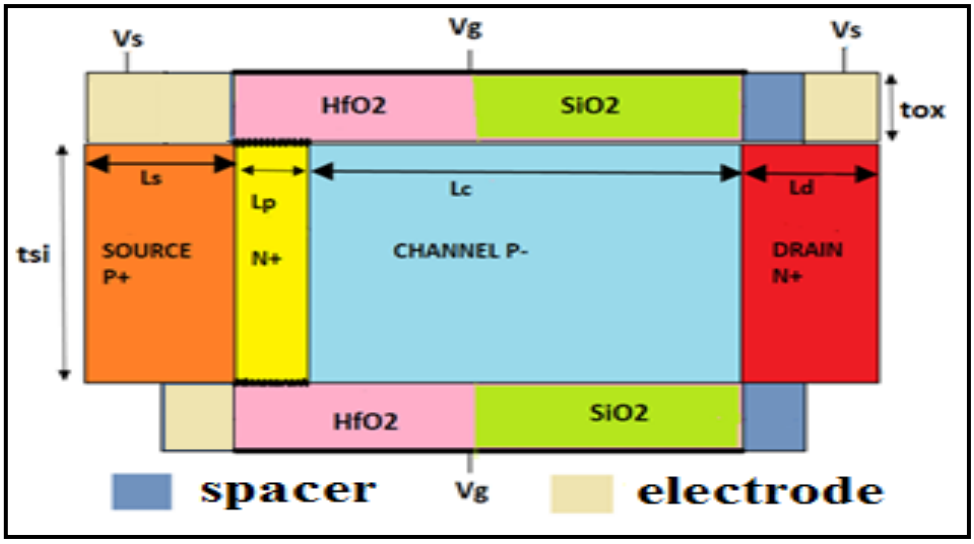


Fig. 3.6(c). Schematic view of Double gate p-n-p-n TFET (hetero gate oxide and spacer induced)

TABLE 3.2: PARAMETER VALUES FOR PROPOSED MODEL

Parameters	t_{si}	t_{ox}	L_p, L_d, L_g	ε_{SiO2}, ε_{HfO2}
Values	10nm	2nm	6nm, 6nm, 60nm	$3.9\varepsilon_0$, $22\varepsilon_0$
Kane's Parameters	$A = 4 \times 10^{21}\ m^{-1/2}V^{-3/2}s^{-1}$ $B = 41 \times 10^{6}\ V\,cm^{-1}$ $D_1 = 2.5$ for Indirect Tunneling			
Parameters	N_S	N_D	N_p, N_{Ch},	L_S, L_D
Values	10^{20} cm^{-3}	5×10^{18} cm^{-3}	5×10^{18} cm^{-3}, 10^{16} cm^{-3},	30nm, 30nm

3.4.2. Analytical Modeling

3.4.2.1. Surface Potential Modeling

A surface potential-based drain current model is derived as follows. Let, $\Psi_{s1}(x,y)$ and $\Psi_{s2}(x,y)$ is the 2-D surface potential of regions R1 and R2. Considering the channel is fully depleted, Poisson's equations [3.53] for the channel region-1 and 2 are given in (1) and (2).

$$\frac{\partial^2\psi_{s1}(x,y)}{\partial x^2}+\frac{\partial^2\psi_{s1}(x,y)}{\partial y^2}=-\frac{qN_{ch1}}{\varepsilon_{Si}}=-\frac{qN_1}{\varepsilon_{Si}} \tag{3.34}$$

$$\frac{\partial^2\psi_{s2}(x,y)}{\partial x^2}+\frac{\partial^2\psi_{s2}(x,y)}{\partial y^2}=\frac{qN_{ch2}}{\varepsilon_{Si}}=\frac{qN_2}{\varepsilon_{Si}} \tag{3.35}$$

Where, $N_{ch1}=N_1$ is the doping concentration of the n-type pocket region and $N_{ch2}=N_2$ is the doping concentration of the rest of the channel.

Young's parabolic approximation [3.54] method is applied to solve the surface potential from the PDE (Partial Differential Equation) given in (3.34) and (3.35). Let us consider, (3.36) and (3.37) are the approximate non-linear equations for the $\Psi_{s1}(x,y)$ and $\Psi_{s2}(x,y)$.

$$\psi_{s1}(x,y) = a_{01}(x) + a_{11}(x)y + a_{12}(x)y^2 \tag{3.36}$$

$$\psi_{s2}(x,y) = a_{02}(x) + a_{21}(x)y + a_{22}(x)y^2 \tag{3.37}$$

For Region-1:

$$\text{At } y=0;\ a_{01}(x) = \psi_{s1}(x); \tag{3.38}$$

Applying Gauss's law at the front gate-oxide interface, we have,

$$-\varepsilon_{Si}\left.\frac{\partial\psi_{s1}(x,y)}{\partial y}\right|_{y=0} = -\varepsilon_{Si}a_{11}(x) = \varepsilon_{ox}\frac{V_{GS}-V_{FB}-\psi_{s1}(x)}{t_{ox}}$$

$$a_{11}(x) = \frac{\varepsilon_{ox}}{\varepsilon_{Si}}\frac{\psi_{s1}(x)-V_{GS}-V_{FB}}{t_{ox}} = \frac{C_{ox}}{\varepsilon_{Si}t_{Si}}\left(\psi_{s1}(x)-V_{GS}-V_{FB}\right)$$

$$= \frac{C_{ox}}{\varepsilon_{Si}t_{Si}}\left(\psi_{s1}(x)-V_{GS}-V_{FB}\right);\ \left(\text{where, } C_{ox}=\frac{\varepsilon_{ox}}{t_{ox}}\right)$$

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}) \tag{3.39}$$

Similarly, applying Gauss's law at the back gate-oxide interface, we have,

$$-\varepsilon_{Si}\left.\frac{\partial\psi_{s1}(x,y)}{\partial y}\right|_{y=t_{Si}} = -\varepsilon_{Si}\left\{a_{11}(x)+2a_{12}(x)t_{Si}\right\} = -\varepsilon_{ox}\frac{V_{GS}+V_{FB}-\psi_{s1}(x)}{t_{ox}}$$

$$= -\varepsilon_{ox}\frac{V_{GS}+V_{FB}-\psi_{s1}(x)}{t_{ox}}$$

Substituting the value of $a_{11}(x)$ from (6), we got,

$$a_{22}(x) = -\frac{\varepsilon_{ox}}{\varepsilon_{ox}t_{Si}}\left(\frac{\psi_{s2}(x)-V_{GS}-V_{FB}}{t_{ox}}\right) = -\frac{C_{ox}}{\varepsilon_{Si}t_{Si}}\left(\psi_{s2}(x)-V_{GS}-V_{FB}\right)$$

$$= -\frac{C_{ox}}{\varepsilon_{Si}t_{Si}}\left(\psi_{s1}(x)-V_{GS}-V_{FB}\right);\ \left(\text{where, } C_{ox}=\frac{\varepsilon_{ox}}{t_{ox}}\right)$$

(3.40)

For Region-2:

$$\text{At y=0;}\ a_{02}(x) = \psi_{s2}(x); \tag{3.41}$$

Similarly, applying Gauss's law at $y=0$ and $y=t_{Si}$, we got the value of $a_{21}(x)$ and $a_{22}(x)$ as follows,

$$a_{21}(x)=\frac{\varepsilon_{ox}}{\varepsilon_{Si}}\frac{\psi_{s2}(x)-V_{GS}-V_{FB}}{t_{ox}} \tag{3.42}$$

$$a_{22}(x)=-\frac{\varepsilon_{ox}}{\varepsilon_{ox}t_{Si}}\left(\frac{\psi_{s2}(x)-V_{GS}-V_{FB}}{t_{ox}}\right)=-\frac{C_{ox}}{\varepsilon_{Si}t_{Si}}\left(\psi_{2}(x)-V_{GS}-V_{FB}\right) \tag{3.43}$$

As the device structure is symmetric along the y-direction, the surface potentials at the front gate and the back gate are equal. Therefore,

$$\psi_{s1}(x,0)=\psi_{s1}(x,t_{Si})=\psi_{s1}(x) \tag{3.44}$$

$$\psi_{s2}(x,0)=\psi_{s2}(x,t_{Si})=\psi_{s2}(x) \tag{3.45}$$

Therefore, the 2-D Poisson's equation is resolved to 1-D Poisson's equation, given by,

$$\frac{\partial^2\psi_{s1}(x)}{\partial x^2}+2a_{12}(x)=-\frac{qN_1}{\varepsilon_{Si}}\ \text{(for, R1)} \tag{3.46}$$

$$\Rightarrow \psi_{s1}^{''}(x)-k^2\psi_{s1}(x)=-\frac{qN_1}{\varepsilon_{Si}}-k^2V_{GS1};$$

Where, $V_{GS1}=V_{GS}-V_{FB}$; $k=\sqrt{\frac{2C_{ox}}{\varepsilon_{Si}t_{Si}}}$;

The general solution of the 1-D Poisson's equation in (3.46) is as follows,

$$\psi_{s1}(x)=Ae^{kx}+Be^{-kx}+k_1; \quad \text{where, } k_1=V_{GS1}+\frac{qN_1}{\varepsilon_{Si}} \tag{3.47}$$

Similarly, 1-D Poisson's equation for R2 is,

$$\frac{\partial^2\psi_{s2}(x)}{\partial x^2}+2a_{22}(x)=\frac{qN_2}{\varepsilon_{Si}} \tag{3.48}$$

$$\Rightarrow \psi_{s2}^{''}(x)-k^2\psi_{s2}(x)=\frac{qN_2}{\varepsilon_{Si}}-k^2V_{GS1}$$

Where, $V_{GS1}=V_{GS}-V_{FB}$; $k=\sqrt{\frac{2C_{ox}}{\varepsilon_{Si}t_{Si}}}$;

And, the general solution is,

$$\psi_{s2}(x)=Ce^{kx}+De^{-kx}+k_2; \quad \text{where, } k_2=V_{GS1}-\frac{qN_2}{\varepsilon_{Si}} \tag{3.49}$$

The arbitrary constants, A, B, C and D, will be found by the boundary conditions given below:

(i) At *x=0*, the surface potential is equal to the built-in potential,

$$\psi_{s1}(0) = A + B + k_1 = V_{bis} \tag{3.50}$$

(ii) At $x=l_1$, the potential is continuous at the interface of Reg-1 and Reg-2,

$$\psi_{s1}(l_1) = \psi_{s2}(0)$$

$$Ae^{kl_1} + Be^{-kl_1} + k_1 = C + D + k_2 \tag{3.51}$$

(iii) At x=lg, the surface potential is equal to the built-in potential at the drain/channel interface,

$$\psi_{s2}(l_2) = Ce^{kl_2} + De^{-kl_2} + k_2 = V_{bid} + V_{ds} \tag{3.52}$$

(iv) Condition for continuity of electric field at the interface of Reg-1 and Reg-2 yields that,

$$\left.\frac{d\psi_{s1}(x)}{dx}\right|_{x=l1} = \left.\frac{d\psi_{s2}(x)}{dx}\right|_{x=0}$$

$$Ae^{kl_1} - Be^{-kl_1} = C - D \tag{3.53}$$

Therefore, solving (3.50), (3.51), (3.52) and (3.53), A, B, C and D are found out, given as,

$$A = \frac{e^{-kl_2}\{(V_{bi} - k_1)e^{k(l_2 - l_1)} - (k_2 - k_1)e^{kl_g}\}}{2\mathrm{Sinh}(kl_1)} \tag{3.54}$$

$$B = \frac{e^{-kl_2}\{(k_2 - V_{bi})\mathrm{Cosh}(kl_2) - (V_{bi} + V_{DS} - k_2)(e^{k(l_1 - l_2)} - e^{-kl_g})\}}{4\mathrm{Sinh}(kl_1)} \tag{3.55}$$

$$C = \frac{e^{-kl_2}\{(k_2 - V_{bi}) - 2(V_{bi} + V_{DS} - k_2)\mathrm{Sinh}(kl_1)\}}{2\mathrm{Sinh}(kl_1)} \tag{3.56}$$

$$D = \frac{e^{-kl_2}\{2\mathrm{Sinh}(kl_2)(V_{bi} - 2k_1 + k_2) + (V_{bi} + V_{DS} - k_2)(e^{k(l_1 - l_2)} - e^{kl_g})\}}{4\mathrm{Sinh}(kl_1)} \tag{3.57}$$

3.4.2.2. Electric Field Modeling

The gradient of surface potential is defined as an Electric field. Therefore, the electric field equations are derived for Reg-1 and Reg-2 separately along x-direction and y-direction, given as:

$$E_1(x) = -\frac{d\psi_1(x,y)}{dx} = k(Be^{-kx} - Ae^{kx}) = E_{1x} \tag{3.58}$$

$$E_2(x) = -\frac{d\psi_2(x,y)}{dx} = k(De^{-kx} - Ce^{kx}) = E_{2x} \tag{3.59}$$

$$E_1(y) = -\frac{d\psi_1(x,y)}{dy} = -c_{11}(x) - 2yc_{12}(x) = E_{1y} \tag{3.60}$$

$$E_2(y) = -\frac{d\psi_2(x,y)}{dy} = -c_{12}(x) - 2yc_{22}(x) = E_{2y} \tag{3.61}$$

Hence the total electric field is calculated for Reg-1, given by,

$$E_1 = \sqrt{E_{1x}^2 + E_{1y}^2} \tag{3.62a}$$

Using eqn. 3.58:

$$E_{1x} = -\frac{d\psi_1(x,y)}{dx} = k(Be^{-kx} - Ae^{kx})$$

Now using Taylor series expansion for exponential terms:

$$e^x = 1 + \frac{x}{1!} + \frac{x^2}{2!} + \frac{x^3}{3!} + \ldots$$

Expression for E_{1x} becomes :

$$E_{1x} = k\{B(1-kx) - A(1+kx)\}$$

$$= (B-A)k - xk^2(A+B)$$

$$= h_1 + xh_2$$

Where, $h_1 = (B-A)k$; and; $h_2 = -k^2(A+B)$

Similarly using eqn. 3.60:

$$E_{1y} = -c_{11}(x) - 2y.c_{12}(x)$$

Substituting the values of $c_{11}(x)$ and $c_{12}(x)$, we get:

$$E_{1y} = -\frac{C_{ox}(\psi_{si}(x) - V_{gs1})}{\varepsilon_{si}} + \frac{2yC_{ox}(\psi_1(x) - V_{gs1})}{\varepsilon_{si}t_{si}}$$

$$= -\frac{C_{ox}\{(A+B+K_1) + kx(A-B) - V_{gs1}\}}{\varepsilon_{si}} + \frac{2yC_{ox}\{(A+B+K_1) + kx(A-B) - V_{gs1}\}}{\varepsilon_{si}.t_{si}}$$

$$= -\frac{C_{ox}\{(A+B+K_1 - V_{gs1}) + kx(A-B)\}}{\varepsilon_{si}} + \frac{2yC_{ox}\{(A+B+K_1 - V_{gs1}) + kx(A-B)\}}{\varepsilon_{si}t_{si}}$$

$$= h_3 + h_4 x + h_5 y + h_6 xy$$

Where, $h_3 = -\frac{C_{ox}(A+B+K_1-V_{gs1})}{\varepsilon_{si}}$; $h_4 = -\frac{C_{ox}k(A-B)}{\varepsilon_{si}}$

$h_5 = \frac{2C_{ox}(A+B+K_1-V_{gs1})}{\varepsilon_{si}t_{si}}$; $h_6 = \frac{2C_{ox}k(A-B)}{\varepsilon_{si}t_{si}}$

$$\therefore E_1 = \sqrt{E_{1x}{}^2 + E_{1y}{}^2}$$

$$= \sqrt{(h_1{}^2 + h_3{}^2) + 2x(h_1h_2 + h_3h_4) + x^2(h_2{}^2 + h_4{}^2) + 4yh_3h_5 + 4y^2h_5{}^2 + 4xy(h_3h_6 + h_4h_5) + 4x^2y^2h_6{}^2 + 4yx^2h_4h_6 + 8y^2xh_5h_6}$$

(3.62b)

Similarly, the electric field for region-2, E_2 is derived. And the total electric field is defined as,

$$E_{Total} = \begin{Bmatrix} E_1, 0 \le L \le L_p \\ E_2, L_p \le L \le L_g \end{Bmatrix}$$

where, L_p and L_g are defined in the Table 3.2

3.4.2.3. Drain Current Modeling

The drain current of the p-n-p-n Tunnel FET is the volume integral of the generated charge carriers, *G*, where the G is a function of electric fields [3.55]. The equations of drain current and corresponding filed dependant generation function are given in (3.63) and (3.63), respectively.

$$I_{DS} = q\iiint GdV = q\iint Gdxdy \quad (3.63)$$

$$G(E) = A_1E^{D1}\exp[\frac{-B_1}{E}] \quad (3.64)$$

3.4.3. Results and Discussions

The simulation process is carried out with SILVACO ATLAS TCAD, version 5.19.20.R, with the aid of the following physical models: mobility models CONMOB and FLDMOB; recombination models SRH and AUGER to describe minority carrier lifetime; CVT model to ascribe doping, electric field, and temperature effects; Trap assisted tunneling model; Kane's local tunneling model and BGN, the bandgap narrowing model. The design parameters are mentioned in Table 3.2. The work demonstrates the merits of the proposed structures educed through complete simulations of structure-1, structure-2, and structure-3 with HfO_2 and TiO_2 as spacers.

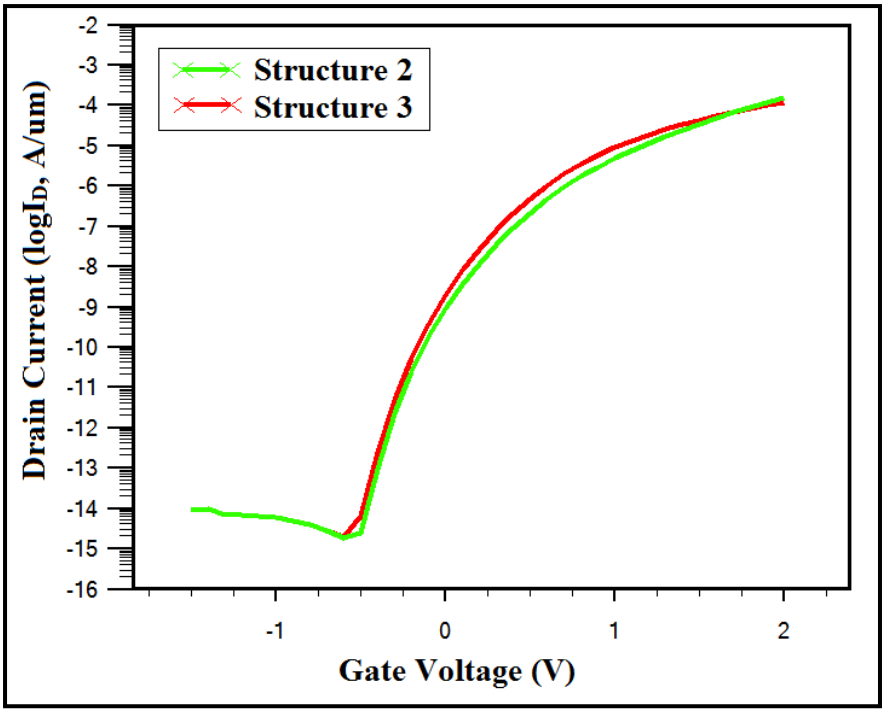


Fig. 3.7(a). I_D-V_{GS} Characteristics of two-sided spacer induced p-n-p-n TFET and one-sided spacer induced p-n-p-n TFET (spacer: HfO_2)

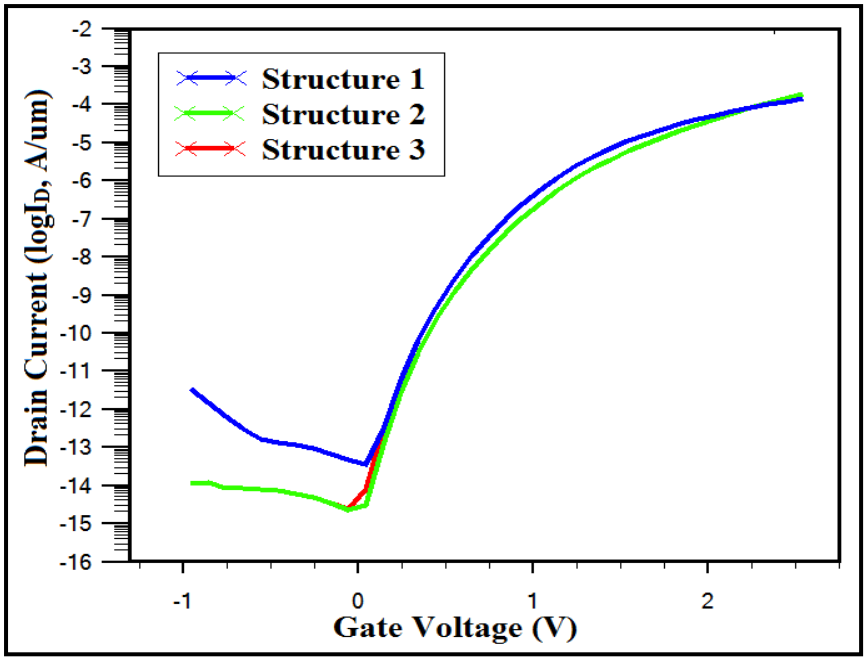


Fig. 3.7(b). I_D-V_{GS} Characteristics of p-n-p-n TFET and spacer induced (one-sided and two-sided) TFETs (spacer: HfO_2)

The present work aims to alleviate the ON current while bringing down the ambipolar conduction and the OFF current as much as possible. However, it has been a challenge to the researcher since the high drive current always induces a high OFF current, and reducing ambipolarity consequently affects the subthreshold swing (SS). Therefore, our work considered the p-n-p-n TFET an experimental structure due to its commendable current drivability. Therefore, minimizing the OFF-state current and ambipolarity is the principal concern of the proposed work. This is also noteworthy that the said structure experiences degraded subthreshold swing at room temperature.

The primary set of trials did to manage the ambipolar conduction of p-n-p-n TFET. However, the spacer oxide with high-k materials reduces the field intensity significantly. Therefore, the device presented in Fig. 3.6 is improvised by infusing high-k spacers in two ways. The first modification consists of two-sided HfO_2 deposition as spacers, and the second one is devised by one-sided HfO_2 (at the drain side) deposition as a spacer. For the sake of simple understanding, the proposed structures are mentioned as structure-1 (p-n-p-n TFET), structure-2 (p-n-p-n TFET with two-sided spacer), and structure-3 (p-n-p-n TFET with single-sided spacer), respectively in the following literature.

The spacer materials in the modified structures perform a crucial role in improving output characteristics, precisely demonstrated in Fig 3.7(a) and (b). In addition, it is evident that structure-3 provides better threshold voltage and subthreshold swing (SS). The source-side spacer diminishes the field intensity, resulting in a setback of rise-current for structure-2 compared to structure-3 (Fig. 3.7a). The drain-side spacer effectively controls the OFF current and ambipolar current on trimming the drain side electric field, as shown in Fig 3.7(b). The ambipolar current rating for structure-2 and 3 are in order of fA/μm for an operating range of negative Gate voltage (~ -1V). Therefore, structure-3 evolved performance-wise as the best device.

In the second set of trials, the conventional p-n-p-n TFET i.e., structure-1, is considered the foundation structure to be renovated for attaining a better subthreshold swing (SS) and ON/OFF current ratio. Therefore, hetero gate dielectric consisting of HfO2 and SiO2 is proposed in Fig. 3.6(b). In Fig. 3.6(c), another variant with one-sided (at the drain side) spacer is demonstrated. Moreover, experiments are performed with HfO_2 and TiO_2 as spacer oxides. In the following literature, the hetero-gate dielectric p-n-p-n TFET, HfO_2 spacer induced hetero-gate dielectric p-n-p-n TFET, and TiO_2 spacer induced hetero-gate dielectric p-n-p-n TFET structures are mentioned as structure-4, 5, and 6, respectively.

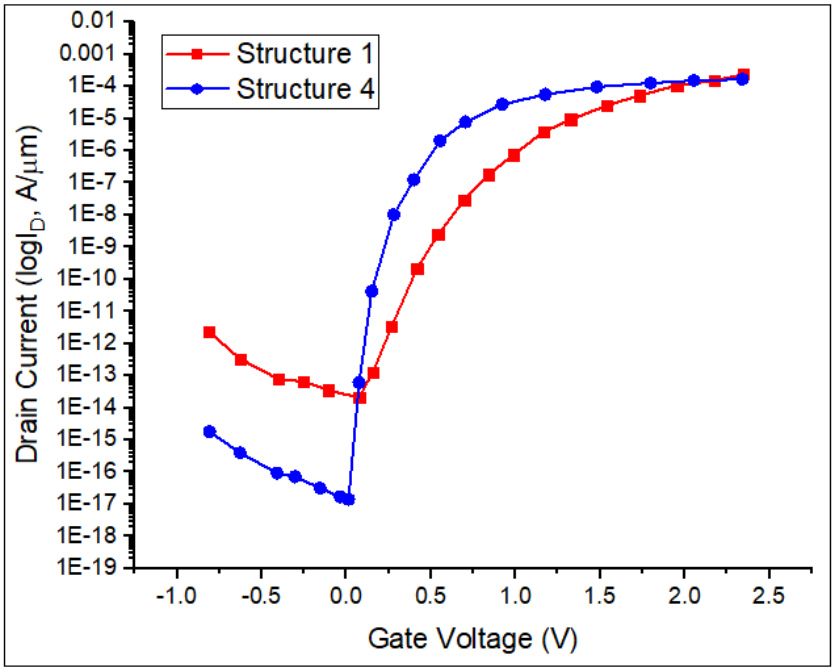


Fig. 3.8(a). I_D-V_{GS} Characteristics of p-n-p-n TFET and hetero-gate dielectric p-n-p-n TFET

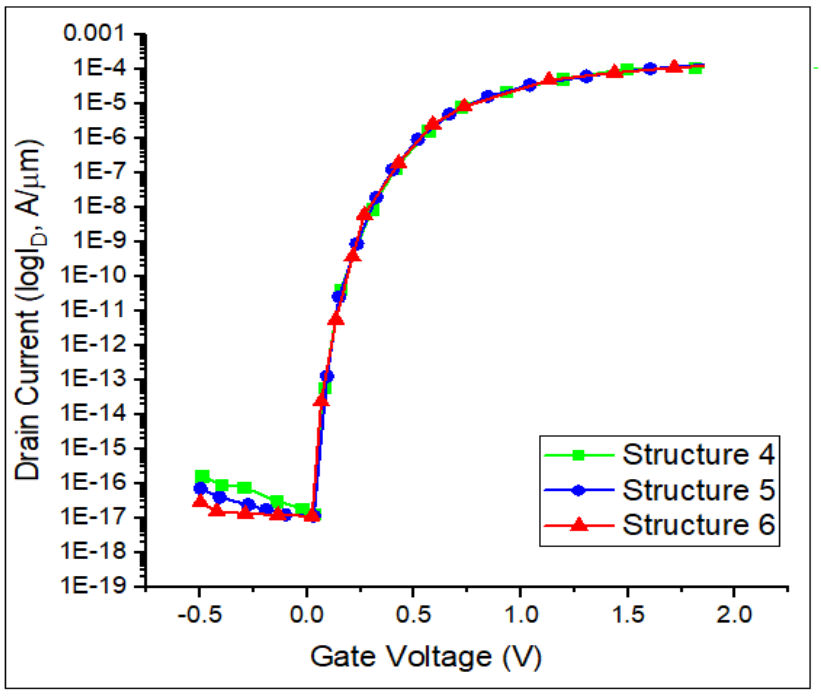


Fig. 3.8(b). I_D-V_{GS} Characteristics of hetero-gate dielctric p-n-p-n TFET and spacer induced hetero-gate dielctric p-n-p-n TFET

A fairly good performance improvement has been achieved by hetero-gate dielectric p-n-p-n TFET (structure-4) over conventional p-n-p-n TFET (structure-1) in terms of subthreshold

swing and ON/OFF current ratio (Fig. 3.8(a)). Nevertheless, the ambipolar behavior is more or less the same for both structures. A high ON/OFF current ratio (nearly 10^{11}), followed by a steep subthreshold behavior (nearly 19mV/dec) is realized for structure-4 as depicted in Fig. 3.8(a).

Structure-4, an upgraded variant of the conventional one, is fabricated with a one-sided (at the drain side) spacer to control and optimize the ambipolar conduction. Moreover, HfO_2 and TiO_2 are used as spacers to carry out simulations, and the results are displayed in Fig 3.8(b). The drain-side spacer appreciably suppresses the reverse tunneling, diminishing the electric field at the drain/channel interface. Therefore, the more the permittivity of the spacer, the more suppressed ambipolarity we gain. As a result, structure-6 with TiO_2 spacer (ε_r = 43 ε_0) outperforms structure-5 with HfO_2 spacer (ε_r = 22 ε_0) in this regard as evident in Fig 3(b). Structure-6 offers commendable I_{amb} current characteristics than structure-3, sustained for the gate voltage range 0 – 0.5V. Though the structures-4 & 5 have some ambipolar behavior compared to structure-6, however, we can use this kind of device for sensor applications for their superior Subthreshold behavior. Moreover, their ambipolarity can be suppressed by gate oxide engineering (as we have done in structure-6) or, modifying drain doping engineering [3.56], or gate-drain underlap/overlap engineering [3.57].

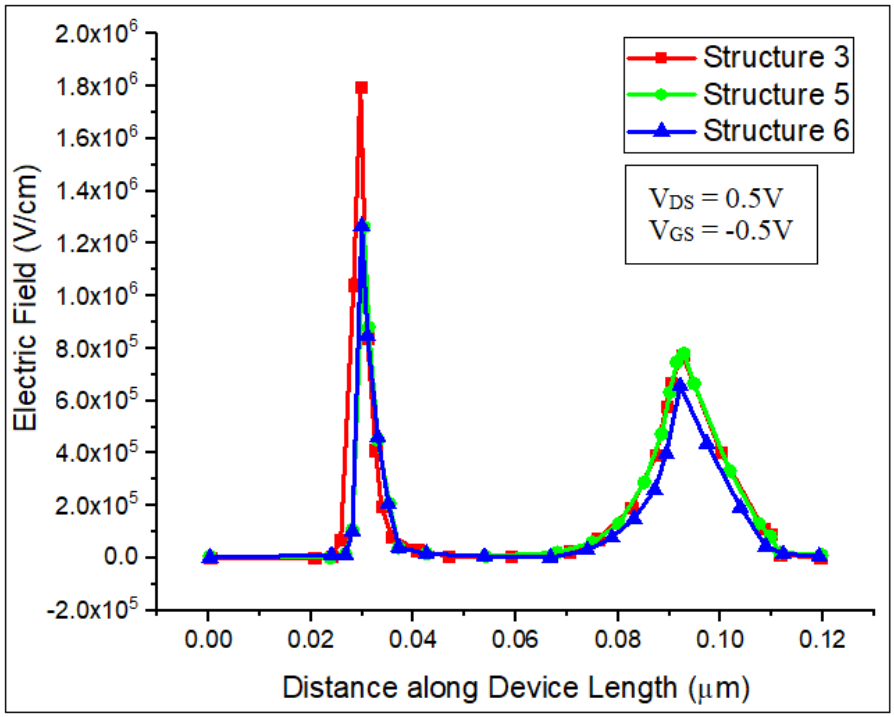


Fig. 3.9(a). Electric Field profile of the proposed structures 3, 5 and 6 in reverse tunneling mode

The electric field profiles of structure-3, 5 and 6 are depicted in Fig 3.9(a). The figure potrays the electric field profiles of the aforesaid structures with negative gate bias condition i.e. to comprehend the electric field at the reverse tunneling junction. It is observed that the field intensity for the structures 3 & 5 are more than that of structure 6. This underlying physics leads to subdued ambipolar behavior of structure 6 for a wide range of operational gate voltage (V_{GS}~ -1V), which is better than the ambipolar behavior of structure 3 & 5.

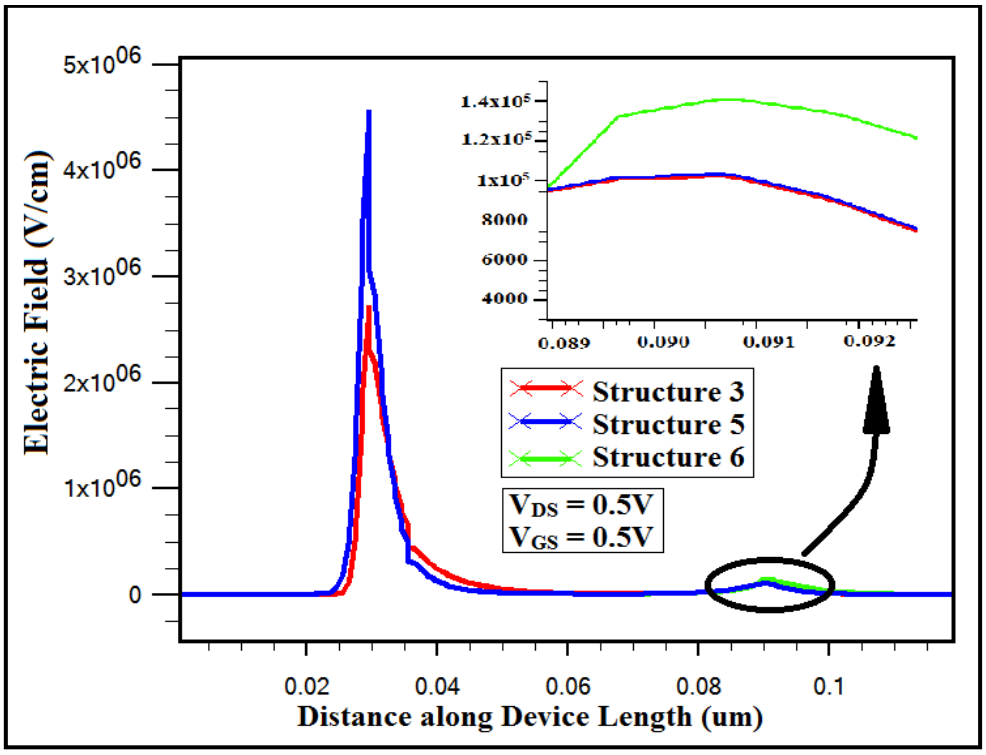


Fig. 3.9(b). Electric Field profiles of the proposed structures 3, 5 and 6 in forward-tunneling mode. The Field intensity at the channel-drain junction is shown in the inset of Figure

The electric fields of structures-3, 5 and 6 at forward-tunneling mode for positive gate voltages ($V_{GS} \geq 0V$) are furnished in Fig 3.9(b). The higher electric field in structure-5 and 6 (greater than structure-3) causes a steep ON current and higher ON/OFF current ratio.

Figure 3.10 displays the surface potentials along the channel length of structures 3, 5, and 6. At the gate voltage of V_{GS} = 0.5V and the drain voltage of V_{DS} = 1V, the potentials of the aforementioned devices are determined. As a result, it supports structure-5 and structure-6's superior gate electrostatic controllability over structure-3. The electric filed profile (Fig. 3.9b) is correlated with the potential profile (Fig. 3.10). The electric field gets its peaks at the source-channel and the drain-channel junctions and the it has nearly constant value (zero value) in

between the junctions. In Fig. 10, it is depicted that the surface potential, changing its magnitude at the source-channel and drain-channel junction, corresponds to the electric field profile.

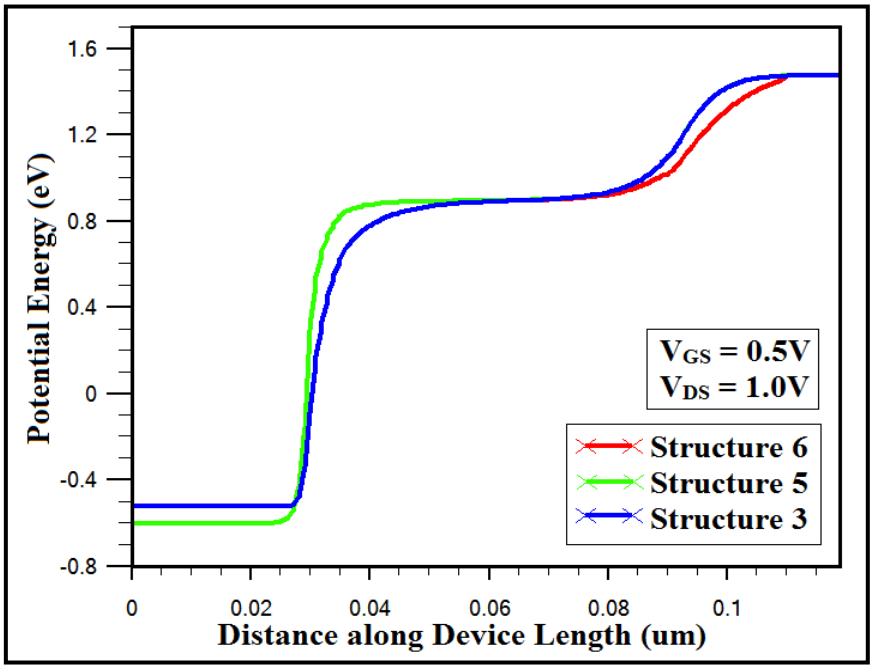


Fig. 3.10: Surface Potential profiles of the proposed structures 3, 5 and 6 at V_{GS}= 0.5V and V_{DS}= 1.0V

The extracted electrical parameters of the proposed structures are furnished in Table 3.2.

TABLE 3.2: EXTRACTED PARAMETERS OF PROPOSED STRUCTURES THROUGH SIMULATION

Structure	Sub-threshold swing (SS) (mV/decade)	I_{ON} (A/um)	I_{OFF} (A/um)	I_{ON}/I_{OFF}
Structure 1	88	$1.2\text{x}10^{-4}$	$3.02\text{x}10^{-14}$	10^{10}
Structure 2	58	$1.5\text{x}10^{-4}$	$1.9\text{x}10^{-15}$	10^{11}
Structure 3	58.5	$1.2\text{x}10^{-4}$	$1.9\text{x}10^{-15}$	10^{11}
Ambipolarity suppressed for -1V of V_{GS} with an order of fA/μm current for Structure 3 (best case)				
Structure 4	18.80	$1.5\text{x}10^{-4}$	$1.66\text{x}10^{-17}$	10^{13}
Structure 5	18.02	$2.5\text{x}10^{-4}$	$9.9\text{x}10^{-18}$	10^{14}
Structure 6	18.37	$2.0\text{x}10^{-4}$	$1.03\text{x}10^{-18}$	10^{14}
Ambipolarity suppressed for -0.5V of V_{GS} with an order of atto-A/μm current for Structure 6 (best case)				

References

3.1. Saheli Sarkhel, Bibhas Manna, P.K. Dutta and **Subir Kumar Sarkar**, "Analytical Model for performance comparison of a nano scale dual material double gate Silicon on insulator SOI and Silicon on nothing SON MOSFET," Journal of Nano engineering and Nano manufacturing, ASP, Vol.4, No.3, pp-182-188, September 2014.

3.2. A. M. Ionescu and H. Riel, "Tunnel field effect transistors as energy efficient electronic switches, Nature, vol. 479, pp. 329-337, 2011.

3.3. Tunnel Field-Effect Transistors: State-of-the-Art, Hao Lu And Alan Seabaugh, Volume 2, No. 4, July 2014.

3.4. Tunnel Field-Effect Transistors: Prospects and Challenges, Uygar E. Avci, Daniel H. Morris, And Ian A. Young, Volume 3, No. 3, May 2015.

3.5. Suman Datta, Rahul Pandey, Saurabh Mookerjea, "Opportunties and challenges of tunnel FETs" 2016 IEEE International Symposium on Circuits and Systems (ISCAS).

3.6. Wanjie Xu et. al, "Analytical modeling on the drain current characteristics of gate-all-around TFET with the incorporation of short-channel effects" Solid-State Electronics, Volume 138, December 2017, Pages 24-29.

3.7. S.Ahish et. Al, "Performance analysis of InGaAs/GaAsP heterojunction double gate tunnel field effect transistor" Superlattices and Microstructures,Volume 103, March 2017, Pages 93-101.

3.8. Gupta, S.K., Kumar, S., "Analytical Modeling of a Triple Material Double Gate TFET with Hetero-Dielectric Gate Stack" Silicon 11, 1355–1369 (2019). https://doi.org/10.1007/s12633-018-9932-y.

3.9. Abhijit Mallik et. al, "Impact of a Spacer–Drain Overlap on the Characteristics of a Silicon Tunnel Field-Effect Transistor Based on Vertical Tunneling" IEEE transactions on electron devices, Vol. 60, No. 3, March 2013.

3.10. Dawit B. Abdi et. Al, "Controlling Ambipolar Current in Tunneling FETs Using Overlapping Gate-on-Drain" IEEE transactions on electron devices, Vol. 2, No. 6, November, 2014.

3.11. Yasuhisa Omura; Abhijit Mallik; Naoto Matsuo, "Impact of a Spacer-Drain Overlap on the Characteristics of a Silicon Tunnel Field-Effect Transistor Based on Vertical

Tunneling," in MOS Devices for Low-Voltage and Low-Energy Applications , IEEE, 2016, pp.412-430, doi: 10.1002/9781119107361.ch35.

3.12. S. Ahish, D. Sharma, Y. B. Nithin Kumar and M. H. Vasantha, "Performance Enhancement of Novel InAs/Si Hetero Double-Gate Tunnel FET Using Gaussian Doping," in IEEE Transactions on Electron Devices, vol. 63, no. 1, pp. 288-295, Jan. 2016, doi: 10.1109/TED.2015.2503141.

3.13. Kiran Kumar, R., Shiyamala, S. A 2-D Analytical Modeling of Dual Work Function Metal Gate MOSFET Using High-K Gate Dielectric with Enhanced RF/Analog Performance for Low Power Applications. Silicon (2019). https://doi.org/10.1007/s12633-019-00290-7.

3.14. Saheli Sarkhel , NavjeetBagga , **Subir Kumar Sarkar** "Compact 2D modeling and drain current performance analysis of a work function engineered double gate tunnel field effect transistor" J Comput Electron (2016) 15:104–114.

3.15. Dinesh Kumar Das, Priyanka Saha and **Subir Kumar Sarkar**, " Analytical Modeling of Asymetric hetero-dielectric engineered dual-material DG-TFET", J Comput Electron, Springer, DOI 10.1007/s 10825-017-1102-8, 08 November 2017.

3.16. Dawit Burusie Abdi, Mamidala Jagadesh Kumar, "2-D Threshold Voltage Model for the Double-Gate p-n-p-n TFET with Localized Charges" IEEE Trans. Electon Devices, vol. 63, no. 9, Sept 2016.

3.17. V. Nagavarapu, R. Jhaveri, and J. C. S. Woo, "The tunnel source (PNPN) n-MOSFET: A novel high performance transistor," IEEE Trans. Electron Devices, vol. 55, no. 4, pp. 1013–1019, Apr. 2008.

3.18. R. Jhaveri, V. Nagavarapu, and J. C. S. Woo, "Effect of pocket doping and annealing schemes on the source-pocket tunnel field-effect transistor," IEEE Trans. Electron Devices, vol. 58, no. 1, pp. 80–86, Jan. 2011.

3.19. A. Tura, Z. Zhang, P. Liu, Y.-H. Xie, and J. C. S. Woo, "Vertical silicon p-n-p-n tunnel nMOSFET with MBE-grown tunneling junction," IEEE Trans. Electron Devices, vol. 58, no. 7, pp. 1907–1913, Jul. 2011.

3.20. Woo Young Choi, Woojun Lee, "Hetero-Gate-Dielectric Tunneling Field-Effect Transistors" IEEE Transactions on Electron Devices, Volume: 57 , Issue: 9 , Sept. 2010.

3.21. K. Boucart and A. M. Ionescu, "Double-Gate Tunnel FET With High-κ Gate Dielectric," in IEEE Transactions on Electron Devices, vol. 54, no. 7, pp. 1725-1733, July 2007, doi: 10.1109/TED.2007.899389.

3.22. Verhulst AS, Vandenberghe WG, Maex K, *et al*. Tunnel field-effect transistor without gate-drain overlap. Appl Phys Lett, 2007, 91: 053102.

3.23. Verhulst, A.S., Sorée, B., Leonelli, D., Vandenberghe, W.G., Groeseneken, G.: Modeling the single-gate, double-gate, and gate-all-around tunnel field-effect transistor. J. Appl. Phys. **107**, 024518 (2010)

3.24. W. Y. Choi and W. Lee, "Hetero-Gate-Dielectric Tunneling Field-Effect Transistors," in IEEE Transactions on Electron Devices, vol. 57, no. 9, pp. 2317-2319, Sept. 2010, doi: 10.1109/TED.2010.2052167.

3.25. Min Jin Lee, Woo Young Choi, "Analytical model of single-gate silicon-on-insulator (SOI) tunneling field-effect transistors (TFETs)", Solid-State Electronics,Volume 63, Issue 1, 2011, Pages 110-114, ISSN 0038-1101, https://doi.org/10.1016/j.sse.2011.05.008.

3.26. M. J. Lee and W. Y. Choi, "Effects of Device Geometry on Hetero-Gate-Dielectric Tunneling Field-Effect Transistors," in IEEE Electron Device Letters, vol. 33, no. 10, pp. 1459-1461, Oct. 2012, doi: 10.1109/LED.2012.2206790.

3.27. D. K. Mohata et al., "Demonstration of MOSFET-like on-current performance in arsenide/antimonide tunnel FETs with staggered heterojunctions for 300mV logic applications," 2011 International Electron Devices Meeting, 2011, pp. 33.5.1-33.5.4, doi: 10.1109/IEDM.2011.6131665.

3.28. Elahi, Mirza M. & Ahmed, Kawser & Islam, Md. Shofiqul. (2012). An improved analytical model of current in tunnel field effect transistor. 2012 7th International Conference on Electrical and Computer Engineering, ICECE 2012. 802-805. 10.1109/ICECE.2012.6471672

3.29. Saha, P. & Jain, A. & **Sarkar, S..** (2013). A Comparative Study of CMOS and Carbon Nanotube Field Effect Transistor Based Inverter at 32 nm Technology Node. Asian Journal of Chemistry. 25. S424-S426.

3.30. Dash, D.K., Saha, P. and **Sarkar, S.K.** 3-D Analytical Modeling of Triple Metal Tri-Gate Graded Channel High-k SON TFET for Improved Performance. *Silicon* **12,** 2041–2052 (2020). https://doi.org/10.1007/s12633-019-00268-5.

3.31. Tiya Dey Malakar , Partha Bhattacharyya, **Subir Kumar Sarkar** "Surface Potential based Threshold Voltage Modeling of Work Function Engineered Gate Recessed Source / Drain IR SOI/SON MOSFET for better nanoscale device performance" in the 'International Conference on Computational Science and Engineering'(ICCSE 2016), 4th-6th October,2016,RCC Institute of Information Technology, Kolkata,India.

3.32. Manna, Bibhas & Sarkhel, Saheli & Islam, Nurul & **Sarkar, Subir** & Sarkar, Samir. (2012). Spatial composition grading of binary metal alloy gate electrode for short-channel SOI/SON MOSFET application. Electron Devices, IEEE Transactions on. 59. 3280-3287. 10.1109/TED.2012.2220143.

3.33. Priyanka Saha, Pritha Banerjee, **Subir Kumar Sarkar,** "2D modeling based comprehensive analysis of short channel effects in DMG strained VSTB FET", Superlattices and Microstructures, Volume 118, 2018, Pages 16-28, ISSN 0749-6036, https://doi.org/10.1016/j.spmi.2018.03.070.

3.34. H. Wang et al., "A Novel Barrier Controlled Tunnel FET," in IEEE Electron Device Letters, vol. 35, no. 7, pp. 798-800, July 2014, doi: 10.1109/LED.2014.2325058.

3.35. Kardam, Upasana & Narang, Rakhi & Gupta, Mridula & Saxena, Manoj. (2013). Simulation study for Dual Material Gate Hetero-Dielectric TFET: Static performance analysis for analog applications. 2013 Annual IEEE India Conference, INDICON 2013. 1-6. 10.1109/INDCON.2013.6725867

3.36. Tiya Dey Malakar, Partha Bhattacharyya and **Subir Kumar Sarkar,** "Analytical Surface Potential Based Modeling of Drain Current & Trans- conductance of Work Function Engineered gate Recessed S/D SOI/SON MOSFET", published in Advances in Industrial Engineering and Management, Vol. 6, No.2, 107-110, 2017.

3.37. PK Dutta, N Bagga, K Naskar, **SK Sarkar**," Analysis and simulation of dual metal double gate son mosfet using hafnium dioxide for better performance", IET Digital Library.

3.38. S. Saurabh and M. J. Kumar, "Novel Attributes of a Dual Material Gate Nanoscale Tunnel Field-Effect Transistor," in IEEE Transactions on Electron Devices, vol. 58, no. 2, pp. 404-410, Feb. 2011, doi: 10.1109/TED.2010.2093142.

3.39. B. Manna, S. Sarkhel, N. Islam, S. Sarkar and **S. K. Sarkar**, "Spatial Composition Grading of Binary Metal Alloy Gate Electrode for Short-Channel SOI/SON MOSFET Application," in IEEE Transactions on Electron Devices, vol. 59, no. 12, pp. 3280-3287, Dec. 2012, doi: 10.1109/TED.2012.2220143.

3.40. Bagga, Navjeet & **Sarkar, Subir.** (2015). An Analytical Model for Tunnel Barrier Modulation in Triple Metal Double Gate TFET. Electron Devices, IEEE Transactions on. 62. 2136-2142. 10.1109/TED.2015.2434276.

3.41. S. Sarkhel, P. Saha and **S. K. Sarkar**, "Parasitic fringe capacitance modeling of work function engineered double gate TFET," 2017 Devices for Integrated Circuit (DevIC), 2017, pp. 495-499, doi: 10.1109/DEVIC.2017.8073999.

3.42. Raad, Bhagwan & Nigam, Kaushal & Sharma, Dheeraj & Kondekar, Pravin. (2016). Dielectric and Work function Engineered TFET for Ambipolar Suppression and RF Performance Enhancement. Electronics Letters. 52. 10.1049/el.2015.4348.

3.43. N. Bagga, S. Sarkhel and **S. K. Sarkar**, "Recent research trends in gate engineered tunnel FET for improved current behavior by subduing the ambipolar effects: A review," International Conference on Computing, Communication & Automation, 2015, pp. 1264-1267, doi: 10.1109/CCAA.2015.7148569.

3.44. P. Banerjee, P. Saha and **S. K. Sarkar**, "3-D analytical modeling and comprehensive analysis of SCEs of a high-K gate stack dual-material tri-gate silicon-on-insulator MOSFET with dual-material bottom gate," 2017 IEEE Calcutta Conference (CALCON), 2017, pp. 130-133, doi: 10.1109/CALCON.2017.8280710.

3.45. T. Kumari and **S. K. Sarkar**, "Performance analysis and comparative study of high-K triple metal double gate SON TFET with SOI equivalent," 2017 Devices for Integrated Circuit (DevIC), 2017, pp. 159-163, doi: 10.1109/DEVIC.2017.8073927.

3.46. Kwon, D. W. and Park, B.-G., "Tunnel field-effect transistor with asymmetric gate dielectric and body thickness", Japanese Journal of Applied Physics, vol. 56, no. 4, p. 044201, 2017. doi:10.7567/JJAP.56.044201

3.47. Shelly Garg, Sneh Saurabh, "Suppression of ambipolar current in tunnel FETs using drain-pocket: Proposal and analysis", Superlattices and Microstructures, Volume 113, 2018, Pages 261-270, ISSN 0749-6036, https://doi.org/10.1016/j.spmi.2017.11.002

3.48. Upasana, R. Narang, M. Saxena and M. Gupta, "Modeling and TCAD Assessment for Gate Material and Gate Dielectric Engineered TFET Architectures: Circuit-Level Investigation for Digital Applications," in IEEE Transactions on Electron Devices, vol. 62, no. 10, pp. 3348-3356, Oct. 2015, doi: 10.1109/TED.2015.2462743.

3.49. Malakar, Tiya & Bhattacharyya, Partha & **Sarkar, Subir**. (2016). Surface potential based threshold voltage modeling of work function engineered gate recessed

source/drain IR SOI/SON MOSFET for better nanoscale device performance: Proceedings of the International Conference on Computational Science and Engineering (ICCSE2016), Beliaghata, Kolkata, India, 4-6 October 2016. 10.1201/9781315375021-47

3.50. K. K. Young, "Short-channel effect in fully depleted SOI MOSFETs," in IEEE Transactions on Electron Devices, vol. 36, no. 2, pp. 399-402, Feb. 1989, doi: 10.1109/16.19942.

3.51. E.O. Kane,"Zener tunneling in semiconductors", Journal of Physics and Chemistry of Solids, Volume 12, Issue 2, 1960, Pages 181-188,ISSN 0022-3697,

doi:10.1016/0022-3697(60)90035-4

3.52. *ATLAS: 2-D Device Simulator*, SILVACO Int., Santa Clara, CA, USA, 2013.

3.53. Pritha Banerjee, Aman Mahajan and **Subir Kumar Sarkar**, "2-D Analytical Modeling of Dual-Material Double Gate Silicon-On-Nothing MOSFET",published in Advances in Industrial Engineering and Management, Vol. 6, No.1, 11-16,2017

3.54. Saheli Sarkhel, Bibhas Manna and **Subir Kumar Sarkar**, "Analytical Potential Distribution Model of Symmetric Double Gate Underlap MOSFET with Binary Metal Alloy as Gate Electrode for Subdued SCEs", AICERA, June 4-6, 2013, Kerala.

3.55. Saheli Sarkhel, Navjeet Bagga and **Subir Kumar Sarkar,** "Compact 2D Modeling and Drain Current Performance Analysis of a Work Function Engineered Double Gate Tunnel Field Effect Transistor." Journal of Computational Electronics, Springer, Vol. 15, Issue 1, pp. 104-114, March 2016.

3.56. D. Bhattacharjee, B. Goswami, **D. K. Dash**, A. Bhattacharya and S. K. Sarkar, "Analytical modelling and simulation of drain doping engineered splitted drain structured TFET and its improved performance in subduing ambipolar effect," in **IET Circuits, Devices & Systems**, vol. 13, no. 6, pp. 888-895, 9 2019.

3.57. R., P.K., S., M.T. & G., L. A Review of Engineering Techniques to Suppress Ambipolarity in Tunnel FET. *Silicon* **14**, 1887–1894 (2022). https://doi.org/10.1007/s12633-021-01018-2.

CHAPTER 4

Device – Circuit Interactions of Heterojunction TFET for Energy Harvesting Applications

4.1. Introduction

Over the past few decades, the average power consumption of the chip has drastically increased in order to maintain a pace with tremendous technological growth and scalability of feature size. A quadratic decrease in dynamic power (P_{dyn}) can be accomplished in the power-constrained application by lowering the source voltage (V_{DD}). At the same time, the corresponding decrease in threshold voltage is an absolute necessity to keep up with the On-state current (I_{ON}) for a similar performance. Nonetheless, in CMOS logic, the static power dissipation (P_{leak}), which is dictated by the off-state conduction (I_{OFF}), increases dramatically with the threshold voltage (V_{Th}) decrease, emerging from the thermally restricted parameter, sub-threshold swing (SS) of 60 mV/decade

during the on-off switching. Diminishing static power has turned into a critical challenge in a large number of the present-day's low power applications that reach from portable System-on-chip (SoC) to digital server farm applications. Therefore, the V_{DD} scaling has to be decelerated in the new technological ages to continue the system performance with the necessary drive current and power consumption. This tradeoff between the system performance and leakage power has evolved as a constraint factor for modern high-speed, low-power applications [4.1, 4.2].

Various device related technological developments have turned out to look beyond CMOS [4.3] to eradicate the acute energy crisis with the traditional silicon MOSFETs. Therefore, new device ideas have been cropped up in the last couple of decades viz. spintronic devices [4.4, 4.5], negative differential capacitance FETs [4.6], Silicon on Insulator/Nothig (SOI/SON) [4.7-4.11], Junctionless Transistors [4.12], Strain engineering [4.13-4.14] focusing on an optimum device scaling, reduced power dissipation with maximum possible functionalities. Moreover, several CMOS-like structures such as Nanowire Gate All Around (GAA) MOSFETs [4.15-4.16], FinFETs [4.17], Impact ionization FETs (I-FET) [4.18-4.20], and TFETs [4.21-4.23] were demonstrated by various research groups, in order to minimize the short channel effects (SCE) and to lower the source-drain leakage current. Among these devices, only TFETs and I-MOSFETs promise a subthreshold swing less than 60mV/dec and improved short channel performance, which is attributed to fundamentally a different mechanism used for carrier injection from source to channel. However, proven that I-MOSFET requires very high voltage operation, TFET is the only promising solution for the future technological era available beyond FinFET and Nanowire FETs. By exploiting the quantum mechanics-driven energy shifting through charge particles in the band-to-band tunneling (BTBT) process, TFETs, on a fundamental level, can accomplish a sub-60 mV/decade subthreshold slope at the room temperature (T = 300 K). As a result, sharp switching of this device can provide a higher ON current at low V_{DD}, which empowers V_{DD} scaling without forfeiting the I_{ON}/I_{OFF} and accordingly bypasses the non-scalability of the V_{Th} in traditional silicon MOSFETs [4.24].

The inherited hindrance of Si TFET is low drive current proportional to the tunneling probability of the charge carriers (electrons and holes) through the barrier potential at the source-channel junction [4.25]. Therefore, in TFET design, selecting material systems, device geometry, defects in dielectric interfaces, etc., must be carefully considered to achieve projected energy

performance. Moreover, TFETs have shortcomings like unidirectional conduction, low voltage operation, and asymmetrical source/drain structure directly affecting digital and analog/RF performances of circuits and systems. Further, some issues related to parasitic effects, process variation, electrical noise, single-event-upset, etc., arise due to diversified material systems and various circuit operations. Thus, a thorough analysis of the device to circuit transition and corresponding modeling framework is an essential call for a critical exploration of the energy-efficient property of this steep switching device.

The chapter deals with the Tunnel Field Effect (TFET) Transistor's state-of-art technology and its performance merit from the device to circuit point of view. The theoretical and analytical endeavor eliminates the bottleneck of the power crisis of modern technology with traditional CMOS logic through this steep slope switching device. The device characteristics are studied, and the design framework of a device to circuit implementation is thoroughly discussed. Finally, the application of the proposed device in a CMOS-like circuit and its performance evaluation renders the prominent role of this fast-switching device as a potential alternative in energy-efficient applications.

4.2. Reviewing the Relevant Works

Due to the steep subthreshold swing, tunnel field effect transistors (TFET) have evolved as a strong contender to MOSFET in VLSI circuit design. Theoretically, the subthreshold swing could be far below 60mV/dec (the thermal limit), which has been a great interest and concern for the last couple of decades in retaining the pace of technological nodes with low power dissipation energy-efficient digital ICs. However, the scaling of the MOSFET below 45nm node triggers an acute subthreshold leakage caused by detrimental short channel effects (SCEs), increasing second-order parameter variations and strong coupling between leakage current and temperature. On the contrary, the major hindrance of the TFET devices is their low ON current, which made it challenging to be implemented in CMOS logic circuits. Several approaches have been pursued in this area to boost the drive current of the TFET, amongst which the bandgap engineering with heterostructures emerged as a successful one.

From the early 90s onward, heterostructures were explored in the research field associated with tunneling mechanisms [4.26-4.28]. Osama et al. reported [4.29] a TFET structure with strained Si-Ge heterojunction with type-II band alignment for low power applications. A shallow energy barrier at the tunneling interface made the transistor suitable for working below the source voltage of 0.5V. The TFET structure reported having a steady ON current and steep subthreshold slope over many decades.

A study has been carried out by Verhulst et al. [4.30] on complementary circuit implementation with heterojunction TFET. A semi-analytical model was derived where low bandgap materials Ge and $In_xGa_{1-x}As$ were suggested as source materials of all-silicon TFET structure. As a result, the inverter circuit comprising Ge-Si and $In_xGa_{1-x}As$-Si heterostructures as n-TFET and p-TFET delivered an ON current at par with the MOSFET based inverter circuit. The studies used material parameters like reduced tunneling mass, relative dielectric constants, DOS in the valence and conduction bands, and band offsets (conduction band offset between Ge-Si = 0.05eV and valence bands offset between $In_{0.6}Ga_{0.4}As$-Si = 0.08eV). In addition, the high-K material hafnium dioxide (thickness = 4nm) is used as a gate dielectric in the said structure. Furthermore, it was observed that the onset voltage of heterostructures is relatable with all-Si TFETs. The threshold voltage of 0.2V is achieved with work functions of 4.0 eV and 5.2eV for Ge-source Si TFET and InGaAs-source Si TFET, respectively.

A thorough experimental study was administered by Royer and Mayer [4.31] regarding SOI (Silicon on Insulator), SiGeOI, and GeOI TFET structures with high-*k* and metal gate-stack by using fully depleted CMOS process technology. The work introduced smaller bandgap materials like SiGe or Ge as source constituents, grown through a double epitaxial process in device integration, where HfO_2 (3 nm) and TiN (10 nm) have been utilized as gate-stack. As a result, 30 times lower I_{OFF} value was recorded over a temperature range of 25^0 to 125^0C together with an amplified-ON current with increasing temperature due to the thermally enhanced BTBT event. Therefore, the gain of I_{ON} was reported as 250% higher over a slight change of supply voltage V_{DD} = -0.6V.

A modeling and simulation approach of a DG TFET with multi-layer gate dielectric was pursued by Narang et al. [4.32] to highlight precisely the role of gate-stack over the device performances. Low drive current has always been the major hindrance of the TFET device. Using high-*k* gate dielectric could be a feasible solution since it could provide better electrostatic control of the gate over the channel due to its reduced thickness. At the same time, some unacceptable events crop up for high-k materials, viz. interface trap states, the density of bulk fixed charges, and reduced carrier mobility in the channel. A gate-stack geometry comprised of a thin layer of SiO_2 sandwiched between the channel and high-k oxide has come up as a solution with the same effect of minimized oxide thickness still having an improved subthreshold behavior of the device. The work rendered an analytical model for contemporary device architecture with a stacked gate geometry of 1nm SiO_2 and 2nm high-*k* oxide material successfully captured the device's electrostatics with improved performance in high drive current with a steeper subthreshold swing.

An experimental work led by Mohata et al. [4.33] demonstrated a staggered heterojunction TFET with EOT (Effective Oxide Thickness) scaling in order to achieve a high drive current and ON-OFF current ratio. To study the role of EOT scaling over the switching characteristics of the device was one of the principal objectives of the work. Therefore, the minimum value of Subthreshold Swing at higher ON currents values is required for TFET to perform like MOSFET in CMOS logic. Moreover, the EOT scaling from 2nm to 1.75nm improved the device ON current and DIBT characteristics.

A novel fabrication scheme for Ge-source tunnel FET has been implemented by a research group led by Rooyackers et al. [4.34]. Epitaxially grown source region with a relatively low thermal budget made the process feasible for constructing a high-doped source with abrupt tunneling junction for complementary device integration. The device outperformed the SiGe-source Si homojunction vertical TFET counterparts in every respect. Furthermore, negligible variability is observed for the device over the ON current, while reliability decreases across the TAT (Trap Assisted Tunneling) region. A point-slope approximately 50mV/dec was achieved for the device at 78k temperature.

Moreover, the device exhibits a steeper SS and higher drive current for thinner gate-oxide with a high-k material. The better electrostatic control of the gate over the channel region was attained through the tunneling junction caused by smaller EOT (Equivalent Oxide Thickness) through stack-gate architecture. Therefore, the structure manifested an earlier onset current with a steeper subthreshold swing due to its smaller tunneling length.

An experimental study had been carried out by Walke et al. [4.35] to fabricate a Si-SiGe TFET structure, equipped for line tunneling phenomena. The tunneling current increased with increasing gate length viz. a 1µm device produced 20µA/um current at $V_{GS}=V_{DS}=1.2V$. A point subthreshold swing of 22mV/dec is obtained from the device at 78K temperature. Quantum confinement effects were profound to increase onset voltage by 0.35 V. Variability analysis was also performed in the said work.

Kim et al. [4.36] paid attention to a high-performance Ge-Si heterostructure with Al_2O_3 as gate oxide delivering 58mV/decade subthreshold swing and over 10^7 I_{ON}/I_{OFF} ratio. In addition, the authors emphasized the improvement of the device characteristics considering the interface state density of the source and channel at the metal-oxide-semiconductor (MOS) interfaces. The work demonstrated a molecular beam epitaxial (MBE) process at shallow temperature (200^0C) to grow a Boron-doped Ge layer onto the SOI substrate to fabricate a uniform and abrupt Ge-Si heterostructure. After that, Ta/Al_2O_3/GeO_x/Ge gate-stacks are constructed using ECR post plasma oxidation. Finally, the device performances are optimized by tuning the interface state density (Dit) at the MOS interfaces using post-metallization annealing in an N_2 environment under 200^0C–400^0C temperature.

Dash et al. proposed a triple-metal-graded-channel high-k SON TFET [4.37] to achieve an appreciable drive current with suppressed SCEs. In addition, the authors developed a 3D analytical model to justify the device-level abstraction of the proposed structure, offering sharp band bending at the tunneling junction and wide tunneling width at the reverse tunneling junction. Thus the structure is avle to revamp the tunneling current while subduing the ambipolar conduction. Experiments were carried out with 40nm channel length and 10nm channel width exhibiting excellent scalability with commandable immunity to SCEs like DIBL and HCE.

A study contributed by Kim et al. [4.38] dealt with the hump effects of Ge-Si heterojunction TFET. The effect is attributed to the switching of BTBT phenomena from indirect bandgap to direct bandgap with a gradual increase in Gate voltage (V_{GS}). Therefore, the intrinsic Ge channel length could be optimized to suppress the hump effect, or the increasing source doping to enhance the gate-channel controllability may be an alternative.

Bhattacharjee et al. proposed an innovative splitted drain non-planer TFET structure [4.39] in their work. The lower doped drain segment is placed below, the higher doped drain part. An analytical model has been proposed based on Density-of-States (DOS) and switched-band structure. All the device characteristics analyzed by the proposed model are validated by SILVACO ATLAS simulation results, finding a better response of the proposed device in all aspects, specifically more subduing ambipolar conduction than conventional planner TFETs. Furthermore, the proposed devices are optimized in terms of doping and drain segmentation to extract maximum output performances from them.

Saha et al. paid attention to high-k stacked oxide TMDG strained SON MOSFET with Gaussian-like doping [4.40]. As a result, the device offered the best immunity against SCEs in its classes. In addition, threshold voltage roll-off and DIBL were significantly eliminated. Moreover, using stacked oxide structures comprising high-k TiO_2 and low-k SiO_2 reduces the HCE remarkably. Hence, further power consumption could be regulated, endorsing the application of the proposed device in the low power paradigm.

A novel 3D modeling of Dual material Trigate SON TFET with SiO_2-HfO_2 stacked gate was proposed by a research group led by Sarkar et al. [4.41] to study the impact of gate engineering and dielectric engineering on the device's characteristics. As a result, the device outperformed the conventional DMTG SON and equivalent SMTG TFET structure in terms of higher ON current, better ON/OFF ratio, and a steeper Subthreshold swing.

Saha et al.proposed a three-dimensional analytical model of triple-metal-trigate SON MOSFET [4.42] in their paperwork. 3D Poisson's equation with suitable boundary conditions was solved to characterize the device's response. The proposed model was validated by 3D numerical

simulations. As a result, the device is highly immune to Short Channel Effects (SCEs), precisely DIBL, threshold voltage roll-off, Hot Carrier Effects (HCE), affirming its reduced static power loss and reliability. Furthermore, the desired subthreshold swing (SS) corroborated low power dissipation offering the proposed device suitable for low power applications.

A research group led by Rao et al. [4.43] comprehended the shortcomings of the device modeling to be taken care of to predict the circuit performances accurately. The work proposed to optimize the drive current based on the controlling parameters like the bandgap of the source material, oxide thickness, and tunneling distance. The drain bias affects the source-side tunneling distance resulting in degraded output conductance and saturation voltage of the said device. Moreover, the DOS of the source material and the oxide thickness immensely impact the Millar Capacitance. Therefore, choosing the semiconductor material wisely and optimizing the device geometry are necessary conditions to obtain an efficient device model for circuit-level implementation. Hence, the work presented a design perspective considering the drive current, drain saturation voltage, and threshold voltage as controlling parameters obtaining minimum propagation delay. In addition, the higher gate capacitance has also been optimized for lesser power dissipation while maintaining the same speed of operation against its COMS counterpart.

Núñez and Avedillo have carried out a comparative study with TFET and CMOS technology [4.44, 4.45] to determine the benchmarking circuit for low-power, high-performance applications. In addition, the authors considered the minimum supply voltage, switching activity, and logic depth as other criteria for performance matrices. Five TFET models, comprising two transistors from Pennsylvania State University (PSU) and three from Notre Dame University (NDU), were compared with four contemporary CMOS models, out of which two high-performance, low power MOS transistors followed by two high-performance and low stand-by power FinFETs. All the circuit performances (8-bit adder) are evaluated in terms of energy-delay product (EDP), average energy per operation, and power-delay product (PEP), considering the V_{DD} as design parameters and conclusion derived. The NDU-heterostructure turned out with significant advantages for both energy and PEP, while the PSU-heterostructure exhibited excellent performance of EDP, where frequency was the primary concern. The authors extended their studies in the subsequent work, looking for application-specific TFET models in the light of switching activity, logic depth (LD),

and operating frequency as performance matrices for typical fan-out 4 (FO4) inverter or even more complex circuits.

Moreover, design architecture is another critical criterion in circuit analysis. In conclusion, NDU-hetero-1 was proved as a potential candidate for low-switching activity products where static power dominates; PSU-hetero was the most competent one considering the low power and energy systems for a given frequency range defined by LD and switching frequency. PSU-hetero and NDU-hetero-2 were evolved as promising candidates for high-speed applications with excellent drive current.

Strangio et al. [4.46] benchmarked a complementary InAs-AlGaSb heterojunction TFET against the performance projection 0f 10nm CMOS FinFET technology. The work investigated the impacts of device-asymmetry over inverters and ring oscillator circuits' performances designed with TFET heterostructures to determine the best W_p/W_n ratio for optimum functionality. The study carried out below 500 mV supply voltage finds an excellent outcome regarding circuit performance in terms of power and speed matrices.

A novel architecture of heterojunction TFET has been proposed by Yang et al. [4.47], contributing to the excellent performances of a digital inverter. Moreover, the gate control has been enhanced due to the line tunneling geometry. Therefore, the effective tunneling area and current could be modulated for the said device aiming to the exact requirement of the digital applications.

The performance of a Ge-Si vertical TFET as a building block of an inverter circuit has been analyzed by Tripathy et al. [4.48]. The gate-drain underlapped structure achieved a higher cut-off frequency at a source voltage of 0.5V. Hence, the device is best suited for RF applications. Therefore, the designed inverter's DC and transient responses justified the device's application in the low-power VLSI domain.

Kumar et al. [4.49] reported a compact 2D analytical model of channel potential, electric field, threshold voltage, and drain current of a DG TFET with stacked oxide architecture. The finite concentration of the source/ drain doping has been considered in the modeling for the first time.

Furthermore, the tunneling current is derived by exploiting the concept of the shortest tunneling path having a strong influence on the BTBT generation rate. Nevertheless, the model considered the source/ drain depletion region in derivation. Finally, threshold voltage has been modeled by using the maximum transconductance method. In conclusion, the work finds no threshold voltage roll-off for the said structure, increase in threshold voltage with Si body thickness and decrease in V_{th} with an increase in high-k oxide thickness. The model accurately captured the device characteristics.

A simulation-based study has been conducted by Chander et al. [4.50] to investigate the temperature effects on the digital and analog performances of the Si-Ge heterojunction SOI TFET. The digital parameters viz. tunneling length, threshold voltage, subthreshold swing, and ON/OFF current ratio and the analog parameters like gate capacitance, transconductance, output conductance, and conductance-to-drain current ratio have been taken into consideration for the said work. The simulation is carried out over a broad range of temperatures, from 200 K to 400 K. The study unveiled an insignificant dependence of SS on the temperature, the faster rise of OFF current than ON current for temperature rises, and a negligible impact of temperature over analog performances in conclusion.

Saha et al. reported a Dual-material Elliptical GAA heterojunction TFET of commendable performances [4.51]. The analytical model includes both source-channel and drain-channel depletion regions and is validated by Sentaurus numerical simulator. The device structure eas optimized through strategic utilization of work function engineering, selection of the justified ratio of metal lengths, channel widths, staggered gap hetero material systems, and gate dielectric oxides. The characterization of the proposed device aims to amplify the ON current and suppress ambipolar conduction, outperforming its equivalent structures, justifying its superiority.

Dash et al. proposed a novel Trigate TFET structure with stacked oxide involving materials and dielectric engineering [4.52]. A 3-dimensional analytical model was derived by solving 3D Poisson's equations with suitable boundary conditions. Therefore, The proposed structure having with and without high-k stacked gates are compared in the literature. Finally, 3D numerical

simulations were done to validate the model. Acceptable agreement of the derived model against the simulation date bore the testimony of the model.

A group led by Sarkar et al. conducted research works related to Trimetal double-gate hetero-dielectric SON-TFETs [5.53, 5.54], delivering the best performance in their classes. First, a 2-D analytical model was developed to characterize the proposed device, successfully endorsed by numerical simulation. Front gate oxide comprises high-k HfO2 at the source side and low-k SiO2 at the drain side. Further, the bottom gate dielectric was replaced by air able to attain a high ON current with suppressed ambipolarity.

4.3. Proposed Device Structure

The cross-sectional view of the proposed Dual material Double gate heterojunction TFET with stack gate oxide is demonstrated in Fig. 4.1. An n-type TFET is realized with a heavily Germanium doped p-type source, Silicon doped channel with least doping, followed by a moderately Silicon doped drain region. Dual material Double gate asymmetric gate design has been incorporated with work function engineering to improve the ON current while maintaining the ambipolar conduction sufficiently low, essentially required for circuit applications. Further, stack gate architecture has been introduced with SiO_2/HfO_2 to extract optimum device performances since the structure offers better electrostatic control over the channel to boost the drain current, minimizing the gate leakage. The channel length of the device is taken as 45nm, 10nm body thickness with 80nm extended source/drain regions. The thickness of the SiO_2, as the bottom layer of the stacked oxide, is 1nm, followed by a 2nm HfO_2 layer at its top, constructing an effective oxide thickness (EOT) of 1.32nm for the proposed device. Work functions of the metals are considered as 4.2eV and 4.6eV for tunneling gate and auxiliary gate, respectively.

The dimensions of the proposed device are denoted as follows for reference purposes in the successive literature: l_g is the gate length, l_1 and l_2 are channel lengths of region 1 (Reg-1) and region 2 (Reg-2) respectively, shown in Fig.1, where $l_1 + l_2 = l_g$; l_{sr} and l_d are the length of the source and drain region. Both front and back gates consist of two metal contacts Metal-1and Metal-2 with work functions ϕm1and ϕm2 respectively. The doping concentrations of the source, channel, and

drain are N_{sr}, N_{ch}, and N_d, respectively. The thickness of the oxide layers is t_{ox} for the SiO_2 layer and t_{hk} for the HfO_2 layer. The effective oxide thickness is given by, $t_{eff} = t_{ox} + (\varepsilon_{ox}/\varepsilon_{hk})\, t_{hk}$, where ε_{ox} is the permittivity of the SiO_2 layer, and ε_{hk} is the permittivity of the HfO_2 layer. The device parameters used for the analytical modeling and simulation process are provided in Table 4.1.

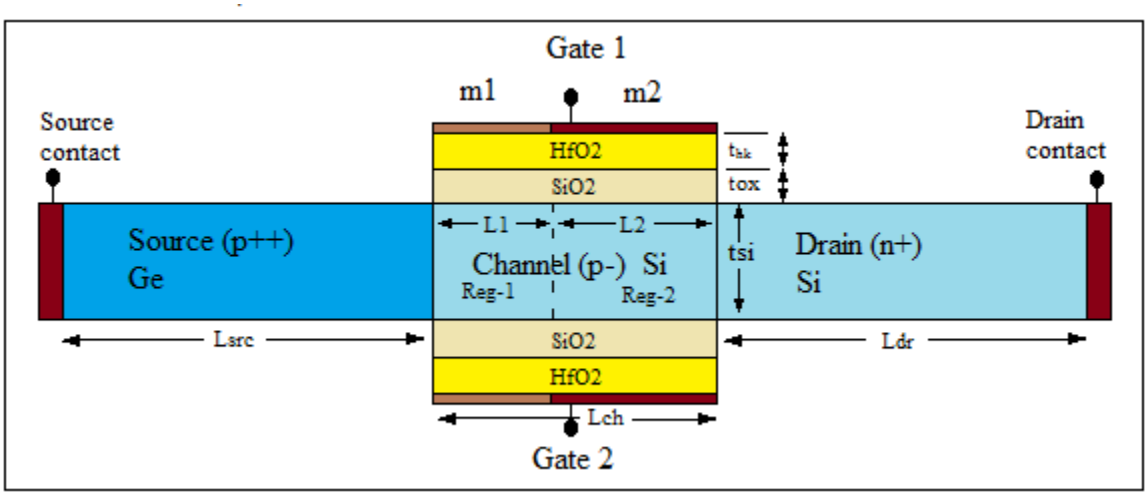


Fig. 4.1: 2-D cross-sectional view of the proposed TMDG-TFET

4.4. Analytical Modeling of the Proposed Device

4.4.1. Surface Potential

The general form of 2D Poisson's equation [4.55] to characterize the potential profile of the proposed device structure is given by (4.1), which is realized considering the immobile charges in the channel locale, attributing the channel potential in the subthreshold condition. The solution of the second-order partial differential equation (PDE) in (4.1) yields the surface potential of the proposed device.

$$\frac{\partial^2 \psi_{s,i}(x,y)}{\partial x^2} + \frac{\partial^2 \psi_{s,i}(x,y)}{\partial y^2} = \frac{qN_{ch}}{\varepsilon_{Si}} \tag{4.1}$$

, for $0 \le x \le l_{ch}$, and $0 \le y \le t_{Si}$; where i=1,2 refers the reg-1 and reg-2 respectively. We have adopted Young's parabolic approximation model [4.56] to solve the equation (4.1). Let's consider the parabolic equation given in (4.2) as a general 2D solution of the Poisson's equation.

$$\psi_{s,i}(x,y) = C_{i0}(x) + C_{i1}(x)y + C_{i2}(x)y^2 \tag{4.2}$$

C_{i1} and C_{i2} are the functions of 'x' to be found using suitable boundary conditions along the y-axis.

For Reg 1:

$0 \le x \le l_1$:

(i) The potential at the gate oxide-Si body interface is the surface potential:

$$\psi_{s,1}(x,0) = \psi_{s,1}(x,t_{Si}) = \psi_{s,1}(x) \tag{4.3}$$

(ii) The electric field is continuous across the front-oxide/ body interface:

$$\left.\frac{d\psi_{s,1}(x,y)}{dx}\right|_{y=0} = -\frac{\varepsilon_{ox}(V_{GS1} - \psi_{s,1}(x))}{\varepsilon_{Si}t_{eff}} \tag{4.4}$$

(iii) The electric field is continuous across the back-oxide/ body interface:

$$\left.\frac{d\psi_{s,1}(x,y)}{dx}\right|_{y=t_{Si}} = \frac{\varepsilon_{ox}(V_{GS1} - \psi_{s,1}(x))}{\varepsilon_{Si}t_{eff}} \tag{4.5}$$

For Reg 2:

$l_1 \le x \le l_1 + l_2 (= l_g)$:

(iv) The potential at the gate oxide-Si body interface is the surface potential:

$$\psi_{s,2}(x,0) = \psi_{s,2}(x,t_{Si}) = \psi_{s,2}(x) \tag{4.6}$$

(v) The electric field is continuous across the front-oxide/ body interface:

$$\left.\frac{d\psi_{s,2}(x,y)}{dx}\right|_{y=0} = -\frac{\varepsilon_{ox}(V_{GS2} - \psi_{s,2}(x))}{\varepsilon_{Si}t_{eff}} \tag{4.7}$$

(vi) The electric field is continuous across the back-oxide/ body interface:

$$\left.\frac{d\psi_{s,2}(x,y)}{dx}\right|_{y=t_{Si}} = \frac{\varepsilon_{ox}(V_{GS2} - \psi_{s,2}(x))}{\varepsilon_{Si}t_{eff}} \tag{4.8}$$

where, V_{GSi} is the effective gate voltage and V_{FBi} is the Flat band voltage of the respective regions; V_{GS} is the applied gate voltage.

$$\left.\begin{aligned} V_{GS1} &= V_{GS} - V_{FB1} \\ V_{GS2} &= V_{GS} - V_{FB2} \end{aligned}\right\} \tag{4.9}$$

Flat band voltage is defined as the work-function difference of the metal and semiconductor.

$$\left.\begin{aligned} V_{FB1} &= \phi_{m1} - \phi_{Si} \\ V_{FB2} &= \phi_{m2} - \phi_{Si} \end{aligned}\right\} \tag{4.10}$$

Where,

$$\phi_{Si} = \chi + \frac{E_g}{2} + \phi_{bi}\text{, and } \phi_{bi} = V_T \ln(N_{ch}/n_i) \tag{4.11}$$

χ = electron affinity of Silicon, E_g = Band gap of Silicon, and ϕ_{bi} = built-in potential. V_T= temperature equivalent voltage (26mV approx.)

For Reg 1:

Substituting (4.3) into (4.2) we get,

$$C_{i0}(x) = \psi_{s,1}(x) \tag{4.12}$$

Substituting (4.4) into (4.2) we get

$$C_{11}(x) = \frac{\varepsilon_{ox}}{\varepsilon_{Si}} \frac{\psi_{s,1}(x) - V_{GS1}}{t_{eff}} \tag{4.13}$$

and, substituting (4.5) into (4.2) we get

$$C_{12}(x) = -\frac{\varepsilon_{ox}}{\varepsilon_{Si} t_{Si}} \frac{\psi_{s,1}(x) - V_{GS1}}{t_{eff}} \tag{4.14}$$

For Reg 2:

Similarly, substituting (4.6), (4.7) and (4.8) into (4.2) we get

$$C_{i0}(x) = \psi_{s,2}(x) \tag{4.15}$$

$$C_{21}(x) = \frac{\varepsilon_{ox}}{\varepsilon_{Si}} \frac{\psi_{s,2}(x) - V_{GS2}}{t_{eff}} \tag{4.16}$$

$$C_{22}(x) = -\frac{\varepsilon_{ox}}{\varepsilon_{Si} t_{Si}} \frac{\psi_{s,2}(x) - V_{GS2}}{t_{eff}} \tag{4.17}$$

By using (4.12), (4.13) and (4.14) we get

$$\psi_{s,1}(x,y) = \psi_{s,1}(x) + C_{11}(x)y + C_{12}(x)y^2\text{, for Reg-1;} \tag{4.18}$$

By using (4.15), (4.16) and (4.17) we get

$$\psi_{s,2}(x,y) = \psi_{s,2}(x) + C_{21}(x)y + C_{22}(x)y^2\text{, for Reg-2;} \tag{4.19}$$

Therefore, the general form of second order 1D linear differential equation is obtained by using (4.18) and (4.19) into (4.1), for both the regions as follows,

$$\frac{\partial^2 \psi_{s,i}(x)}{\partial x^2} + 2C_{i2} = \frac{qN_{ch}}{\varepsilon_{Si}} \tag{4.20}$$

The final solutions of the surface potential for Reg-1 & 2 are,

$$\psi_{s,1}(x) = A\exp(kx) + B\exp(-kx) + k_1 \tag{4.21}$$

$$\psi_{s,2}(x) = C\exp(kx) + D\exp(-kx) + k_2 \tag{4.22}$$

where $k^2 = \frac{2C_{ox}}{\varepsilon_{Si} t_{Si}}$; and $k_i = V_{GSi} - \frac{qN_{ch}}{\varepsilon_{Si} k^2}$ (4.23)

and, A, B, C and D are the arbitrary constants to be found by using suitable boundary conditions along x-directions are as follows,

(vii) The potential at the source-channel heterojunction is [4.57]

$$\psi_{s,1}(0,0) = V_{bis} = -\frac{1}{q}(\chi_1 - \chi_2) + \frac{1}{2}(E_{g1} - E_{g2}) + qV_T \ln(N_{sr}/N_{ch}) \tag{4.24}$$

where, χ_1, χ_2 = electron affinities of source, channel materials;

E_{g1}, E_{g2} = Forbidden gap of source, channel materials;

N_{sr}, N_{ch} = doping concentration of source, channel materials;

(viii) The surface potential in reg-1 at x=0 is

$$\psi_{s,1}(x)\big|_{x=0} = A + B + k_1 \tag{4.25}$$

Using (4.24) and (4.25) we get

$$A + B + k_1 = V_{bis} \tag{4.26}$$

(ix) The built-in potential at the drain-channel junction is

$$\psi_{s,2}(l_2, 0) = V_{bid} + V_{DS} \tag{4.27}$$

where, $V_{bid} = qV_T \ln(N_d N_{ch}/n_i^2)$ (4.28)

(x) The surface potential in the Reg-2 at the drain end is

$$\psi_{s,2}(l_2, 0) = C\exp(kl_2) + D\exp(-kl_2) + k_2 \tag{4.29}$$

By using (4.27) and (4.29), we get

$$C\exp(kl_2) + D\exp(-kl_2) + k_2 = V_{bid} + V_{DS} \tag{4.30}$$

(xi) The potential is continuous at the junction of Reg-1 & 2,

Therefore, $\psi_{s,1}(l_1, 0) = \psi_{s,2}(0,0)$

$$=> A\exp(kl_1) + B\exp(-kl_1) + k_1 = C + D + k_2 \tag{4.31}$$

(xii) The electric field is continuous at the junction of Reg-1 & 2,

Therefore, $\left.\frac{d\psi_{s,1}(x,y)}{dx}\right|_{x=l_1} = \left.\frac{d\psi_{s,2}(x,y)}{dx}\right|_{x=0}$

$$=> A\exp(kl_1) - B\exp(-kl_1) = C - D \tag{4.32}$$

Solving the equations (4.26), (4.30), (4.31), and (4.32), we get the value of the constants A, B, C, and D,

$$A = \frac{1}{4\sinh(k\,l_g)}\left[2(V_{bid} + V_{DS} - k_2) + (k_2 - k_1)(e^{kl_2} + e^{-kl_2}) - 2(V_{bis} - k_1)e^{-k\,lg}\right] \tag{4.33}$$

$$B = \frac{1}{4\sinh(k\,l_g)}\left[2(V_{bis} - k_1)e^{k\,lg} - (k_2 - k_1)(e^{kl_2} + e^{-kl_2}) - 2(V_{bid} + V_{DS} - k_2)\right] \tag{4.34}$$

$$C = \frac{1}{4\sinh(k\,l_g)}\left[2(V_{bid} + V_{DS} - k_2)e^{kl_1} + (k_2 - k_1)e^{-kl_2}(e^{kl_2} + e^{-kl_2}) - 2(V_{bis} - k_1)e^{-k\,l_2}\right] \tag{4.35}$$

$$D = \frac{1}{4\sinh(k\,l_g)}[2(V_{bis} - k_1)e^{k\,l_2} - (k_2 - k_1)e^{kl_2}(e^{kl_2} + e^{-kl_2}) - 2(V_{bid} + V_{DS} - k_2)e^{-kl_1}] \tag{4.36}$$

4.4.2. Electric Field

The lateral and longitudinal electric field can be calculated by differentiating the surface potential equations w.r.t 'x' and 'y':

The lateral field of Reg-1 is

$$E_1(x) = -\frac{d\psi_{s,1}(x,y)}{dx} = k(Be^{-kx} - Ae^{kx}) = E_{1x} \tag{4.37}$$

The longitudinal field of Reg-1 is

$$E_1(y) = -\frac{d\psi_{s,1}(x,y)}{dy} = -C_{11}(x) - 2yC_{12}(x) = E_{1y} \tag{4.38}$$

The lateral field of Reg-2 is

$$E_2(x) = -\frac{d\psi_{s,2}(x,y)}{dx} = k(De^{-kx} - Ce^{kx}) = E_{2x} \tag{4.39}$$

The longitudinal field of Reg-2 is

$$E_2(y) = -\frac{d\psi_{s,2}(x,y)}{dy} = -C_{21}(x) - 2yC_{22}(x) = E_{2y} \tag{4.40}$$

The resultant field of Reg-1 is

$$E_1 = \sqrt{E_{1x}^2 + E_{1y}^2} \tag{4.41}$$

The resultant field of Reg-2 is

$$E_2 = \sqrt{E_{2x}^2 + E_{2y}^2} \tag{4.42}$$

Since, the gates of the proposed device consist of two different metals of two different work functions, therefore the channel region is divided into two regions Reg1 & 2 for the purpose of analytical modeling. The respective electric fields for the regions are E_1 and E_2. Therefore, the overall electric field along the channel can be determined by,

$$E_{Tot} = \begin{Bmatrix} E_1, 0 \le L \le L_1 \\ E_2, L_1 \le L \le L_g \end{Bmatrix} \tag{4.43}$$

4.4.3. Drain Current

In TFET device the drain to source current depends on the generation of charge carriers due to band-to-band tunneling phenomenon. Therefore, we get I_{DS} by integrating the generation rate over the tunneling cross section for 2D modeling.

$$I_{DS} = q\int G dv = q\gamma \int G dx dy, \tag{4.44}$$

where γ is fitting parameter [4.58, 4.59]: $\gamma = 1 - \frac{2}{1 - e^{(V_{ds}/kV_T)}}$

(4.45)

The generation rate, G, a electric field dependent parameter is defined as follows by Kane's model [4.60]

$$G(E) = A_K E^{D1} \exp(\frac{-B_K}{E}) \tag{4.46}$$

$= A_K E_1 E_{avg}^{D1-1} \exp(\frac{-B_K}{E_{avg}})$ [The electric field possesses 2 components: local and average field]

$= A_K E_1 \left(\frac{E_{g_{eff}}}{qx}\right)^{D1-1} \exp\left(\frac{-B_K q}{E_{g_{eff}}} x\right)$ [Substituting (4.55) into (4.46)]

(The local electric field considers only E_1 since the tunneling phenomenon occurs at the junction of source and channel)

$$= A_K \sqrt{E_{x1}^2 + E_{y1}^2} \left(\frac{E_{g_{eff}}}{qx} \right)^{D1-1} \exp\left(\frac{-B_K q}{E_{g_{eff}}} x \right) \text{ [Substituting (4.41) into (4.46)]}$$

(The observation of the simulation studies concludes that the longitudinal field component hardly affects the total field component regarding the generation of charge carriers during the tunneling process)

$$= \frac{A_K E_{g_{eff}}^{D1-1} E_{x1}}{q^{D1-1} x^{D1-1}} \exp\left(-B_{1K} x\right) \tag{4.47}$$

$$\left(B_{1K} = \frac{B_K q}{E_{g_{eff}}} \right)$$

Where A_K and B_K are Kane's parameters dependent on the tunneling process [4.61],

$$\left.\begin{aligned} A_K &= \frac{q^2 m_r^{1/2}}{18\pi\hbar^2 E_{g_{eff}}^{1/2}} \\ B_K &= \frac{\pi m_r^{1/2} E_{g_{eff}}^{1/2}}{2q\hbar} \end{aligned}\right\} \text{ [Tunneling for Direct band-gap materials]} \tag{4.48}$$

and,

$$\left.\begin{aligned} A_K &= \frac{D^2 q^{5/2} (1+\exp(E_\perp / kT))(m_c m_v)}{\rho E_\perp (1+\exp(E_\perp / kT)) 2^{27/5} \pi^{5/2} m_r^{5/4} E_{g_{eff}}^{7/4}} \\ B_K &= \frac{4(2m_r)^{1/2} E_{g_{eff}}^{3/2}}{3q\hbar} \end{aligned}\right\} \text{ [Tunneling for Indirect band-gap materials]} \tag{4.49}$$

Where,

m_r = Reduced tunneling mass

D = Deformation potential

kT = Thermal energy

m_c = DOS effect mass for Conduction Band

m_v = DOS effect mass for Valence Band

ρ = Mass density

$E_\perp$ = Transverse acoustic photon energy

And, D1=2.5

Therefore,

$$I_{DS} = q\int_0^{t_{Si}}\int_{l_{\min}}^{l_{\max}} \frac{A_K E_{g_{eff}}^{D1-1} E_1(x)}{q^{D1-1}x^{D1-1}} \exp\left(-B_{1K}x\right) dxdy \tag{4.50}$$

$$= \frac{A_K E_{g_{eff}}^{D1-1}}{q^{D1-2}} \int_0^{t_{Si}}\int_{l_{\min}}^{l_{\max}} \frac{E_1(x)}{x^{D1-1}} \exp\left(-B_{1K}x\right) dxdy$$

$$= \frac{A_K E_{g_{eff}}^{D1-1}}{q^{D1-2}} \int_0^{t_{Si}}\int_{l_{\min}}^{l_{\max}} \frac{E_1(x)}{x^{D1-1}} \exp\left(-B_{1K}x\right) dxdy$$

$$= \frac{A_K E_{g_{eff}}^{D1-1}}{q^{D1-2}} \int_0^{t_{Si}}\int_{l_{\min}}^{l_{\max}} \frac{k(Be^{-kx} - Ae^{kx})}{x^{D1-1}} \exp\left(-B_{1K}x\right) dxdy$$

$$= \frac{A_K E_{g_{eff}}^{D1-1}}{q^{D1-2}} \int_0^{t_{Si}}\int_{l_{\min}}^{l_{\max}} \frac{k(Be^{-kx} - Ae^{kx})}{x^{D1-1}} \exp\left(-B_{1K}x\right) dxdy$$

$$= \frac{A_K E_{g_{eff}}^{D1-1} k}{q^{D1-2}} \int_0^{t_{Si}}\int_{l_{\min}}^{l_{\max}} \frac{\left\{(B-A) - k(A+B)x + k^2(B-A)x^2/2\right\}}{x^{D1-1}} \exp\left(-B_{1K}x\right) dxdy$$

$$= A_{1K}\int_0^{t_{Si}}\int_{l_{\min}}^{l_{\max}} \left\{\frac{B-A}{x^{3/2}} - \frac{k(A+B)x}{x^{3/2}} + \frac{k2(B-A)x^2}{2x^{3/2}}\right\} \exp\left(-B_{1K}x\right) dxdy$$

$$= A_{1K}\int_0^{t_{Si}}\int_{l_{\min}}^{l_{\max}} \left\{\frac{p_1}{x^{3/2}} - \frac{p_2}{x^{1/2}} + p_3 x^{1/2}\right\} \exp\left(-B_{1K}x\right) dxdy$$

$$= A_{1K}\left\{p_1[I_1]_{l_{\min}}^{l_{\max}} - p_2[I_2]_{l_{\min}}^{l_{\max}} + p_3[I_3]_{l_{\min}}^{l_{\max}}\right\}\int_0^{t_{Si}} dy$$

$$= A_{1K}\left\{p_1[I_1(l_{\max}) - I_1(l_{\min})] - p_2[I_2(l_{\max}) - I_2(l_{\min})] + p_3[I_3(l_{\max}) - I_3(l_{\min})]\right\} t_{Si}$$

$$= A_{2K}\left\{p_1 I_1(l) - p_2 I_2(l) + p_3 I_3(l)\right\} t_{Si} \tag{4.51}$$

Where,

$$I_1 = \int \frac{1}{x^{3/2}} \exp\left(-B_{1K}x\right) dx$$

$$= -\frac{x^{-3/2}e^{-B_{1K}x}}{B_{1K}} + \frac{3x^{-5/2}e^{-B_{1K}x}}{2B_{1K}^2}, \text{ [neglecting higher order terms]} \tag{4.52}$$

$$I_2 = \int \frac{1}{x^{1/2}} \exp\left(-B_{1K}x\right) dx$$

$$= -\frac{x^{-1/2}e^{-B_{1K}x}}{B_{1K}} + \frac{I_1}{2B_{1K}}$$

$$= -\frac{x^{-1/2}e^{-B_{1K}x}}{B_{1K}} + \frac{1}{2B_{1K}}\left(-\frac{x^{-3/2}e^{-B_{1K}x}}{B_{1K}} + \frac{3x^{-5/2}e^{-B_{1K}x}}{2B_{1K}^2}\right) \quad (4.53)$$

and,

$$I_3 = \int x^{1/2}\exp\left(-B_{1K}x\right)dx$$

$$= -\frac{x^{1/2}e^{-B_{1K}x}}{B_{1K}} + \frac{I_2}{2B_{1K}}$$

$$= -\frac{x^{1/2}e^{-B_{1K}x}}{B_{1K}} + \frac{1}{2B_{1K}}\left[-\frac{x^{-1/2}e^{-B_{1K}x}}{B_{1K}} + \frac{1}{2B_{1K}}\left(-\frac{x^{-3/2}e^{-B_{1K}x}}{B_{1K}} + \frac{3x^{-5/2}e^{-B_{1K}x}}{2B_{1K}^2}\right)\right] \quad (4.54)$$

4.4.4. Tunneling Length Calculation

$$E_{avg} = \frac{E_{g_{eff}}}{qx} = \frac{E_{g_{eff}}}{ql_m} \quad (4.55)$$

$$E_{g_{eff}} = E_{g2} - \Delta E_v$$

$$\Delta E_v = \left|\frac{\chi_2 - \chi_1}{q}\right| + \left|\frac{E_{g2} - E_{g1}}{q}\right|$$

$$l_m = l_{\max} - l_{\min} \quad (4.56)$$

Where l_m = difference between maximum and minimum tunneling length [4.62],

l_{max} = maximum tunneling length,

l_{min} = minimum tunneling length;

$$\psi_s(x)\big|_{\min} - \psi_0 = \frac{E_{g_{eff}}}{q}$$

$$\psi_s(x)\big|_{\max} - \psi_0 = \frac{E_{g_{eff}} + \Delta\psi}{q}$$

$$\Delta\psi = E_{CB_{src}} - E_{VB_{src}}$$

$$l_{\min} = \frac{-k(A-B) + \sqrt{k^2(A-B)^2 - 4k^2(A+B)(A+B+k_1 - E_{g_{eff}}/q)}}{k^2(A+B)} \tag{4.57}$$

$$l_{\max} = \frac{-k(A-B) + \sqrt{k^2(A-B)^2 - 4k^2(A+B)\left\{A+B+k_1 - (E_{g_{eff}} + \Delta\psi)/q\right\}}}{k^2(A+B)} \tag{4.58}$$

4.5. Results and Discussions

The previous subsection dealt with the analytical model of the proposed Dual material Double gate heterojunction TFET with stack gate architecture. First, the surface potential, electric field, and drain current expressions are derived through an exhaustive mathematical approach to underlying physics. After that, this section analyses the results, obtained from the simulation data, to validate the accuracy and reliability of the proffered analytical model. The simulation is done by SILVACO Atlas device simulator, version 5.20.2.R [4.63]. The physical parameters of the proposed structure provided in Table 1 are the same for both modeling and numerical simulations. Finally, at the end of this article, a thorough discussion finds a higher degree of accuracy of the proposed model according to the simulation data comparison.

Table 4.1: Design Parameters for Proposed Model and Simulation

Parameters	**Values**
Source doping (N_{src})	$1x10^{-20}$ cm^{-3}
Channel doping (N_{ch})	$1x10^{-16}$ cm^{-3}
Drain doping (N_{dr})	$8x10^{-18}$ cm^{-3}
Channel length	45 nm
Channel thickness	10 nm
SiO2 thickness	1 nm
HfO2 thickness	2 nm
Metal-1 work function (Φ_{m1})	4.2 eV
Metal-2 work function(Φ_{m2})	4.6 eV
Length of Metal-1(L_{m1})	20 nm
Length of Metal-2(L_{m2})	25 nm

The numerical simulations are performed involving the physics-based general models like Lombardi (CVT) model, Shockley-Reed-Hall (SRH), Auger recombination models, Field and

Concentration-dependent mobility models, along with Fermi-Dirac statistics and Bandgap narrowing (BGN) models. In addition, the non-local tunneling model has been invoked to calculate the Drain current accurately. The Quantum correction model has been deliberately bypassed in the simulation since the device thickness is kept below 7nm technology. Our proposed TFET structure is abbreviated as HTFET in the successive literature for simple understanding and references.

The target device possesses a staggered heterojunction fabricated with Ge and Si as the source and channel/ drain regions. Due to the forbidden gap energy of 0.67eV for Ge and 1.12eV for Si at room temperature, 300K builds a band offset at the source-channel junction, which aggressively boosts the onset drive current. Fig. 4.2 depicted the band offset, illustrating the impact of the work function engineering over the device performance in the context of high drive current. Furthermore, the energy of the conduction band of the channel gets lower with an increase of the applied gate potential, resulting in a more overlapping area at the tunneling junction in the source/channel interface.

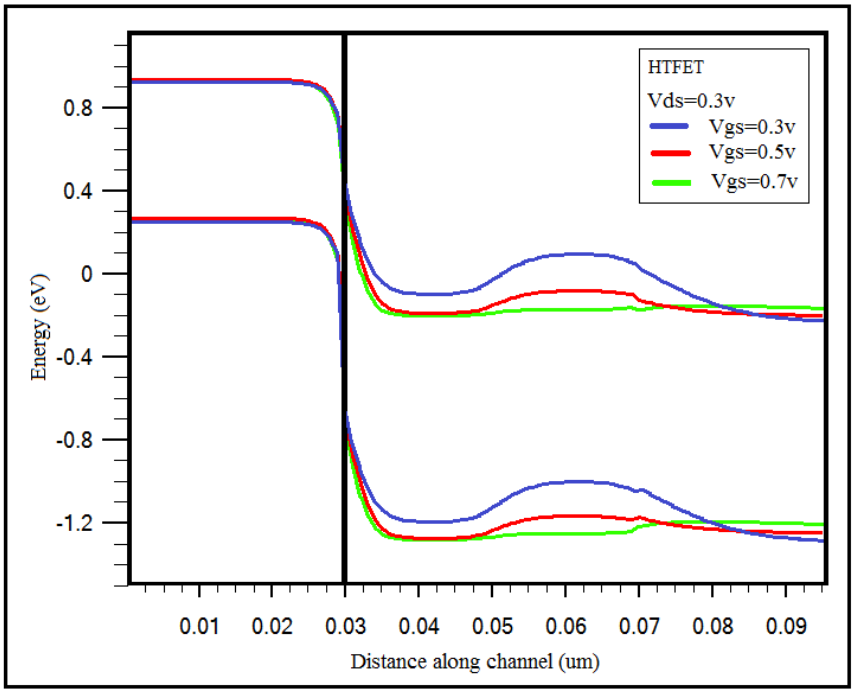


Fig. 4.2: Energy band diagram of HTFET under different gate biasing for constant drain voltage

As a result, it leads to a higher tunneling probability across the potential barrier at the junction region. Thus, a staggered heterojunction immensely influences the minimum tunneling length to

drive the ON current remarkably to its peak. In addition, through the work function engineering, one can achieve a satisfactory higher ON current, lower OFF current, and steeper subthreshold slope (SS) out of the target device. Moreover, the SiO_2/ HfO_2 stack gate helps to enhance the electric field at the tunneling junction while limiting the gate leakage to a great extent. The band diagram is shown in Fig. 4.2 for V_{gs} = 0.3, 0.5, and 0.7 V at a constant V_{ds} of 0.3 volts.

In Fig. 4.3, the surface potential profile along the channel length is plotted against the gate to source voltage (V_{gs}). The curves for a different drain to source voltages (V_{ds}) are depicted in the figure with respective color legends. The red and blue curves in the figure represent the potential profiles for V_{gs} = 0.3V and 0.4V, respectively, at constant V_{ds}=0.5V. According to the underlying physics, the applied gate voltage reduces the energy of the conduction band of the channel, and once it gets aligned with the level of the valence band of the source, the tunneling takes place. Therefore, the figure shows that the gate voltage (V_{gs}) lowering the barrier height increases the surface potential. The green curve, depicting the potential characteristics for the V_{gs}=0.3V at V_{ds}

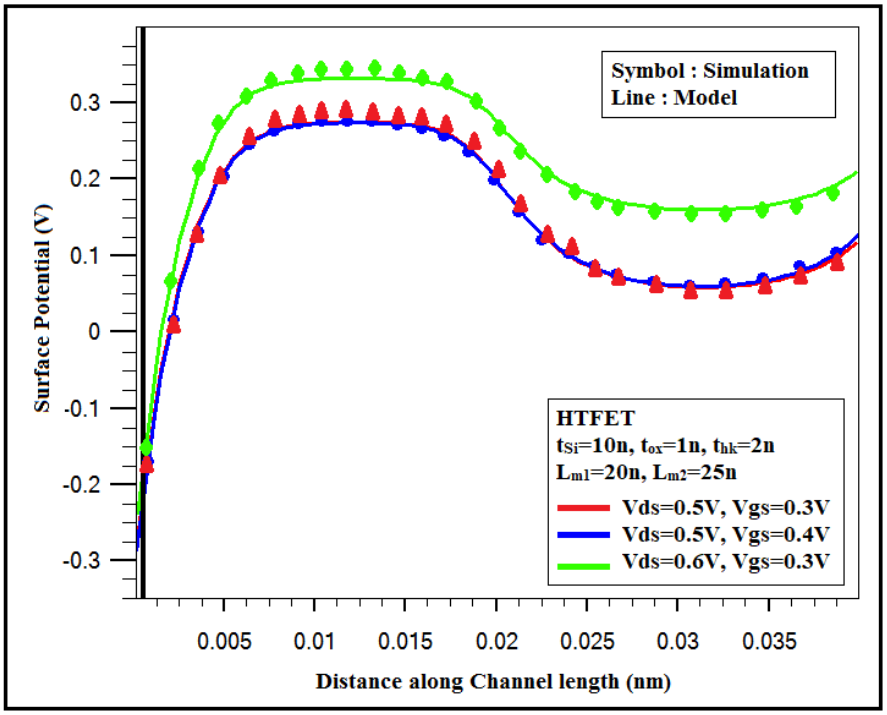


Fig. 4.3: Surface Potential profile along channel length of the proposed heterostructure (t_{si}=10nm, tox=1nm and t_{hk}=2nm) for different Gate voltages (at constant V_{DS}) and different Drain voltages (at constant V_{GS}).

=0.6V moves upward compared to the previous set of curves, implicating the higher surface potential, i.e., lower barrier height. It is noteworthy, that the proposed analytical model is derived based on the subthreshold condition to explore the device characteristics in the said biasing condition. Therefore, the inversion charges and the condition of the depletion region have not been considered while modeling, leading to an underestimated potential at the middle of the channel, followed by an overestimation at the drain end of the same. However, we have overcome these slight imperfections by introducing suitable fitting parameters in the modeling. As a result, the simulation-model overlay shows an excellent agreement in the said figure.

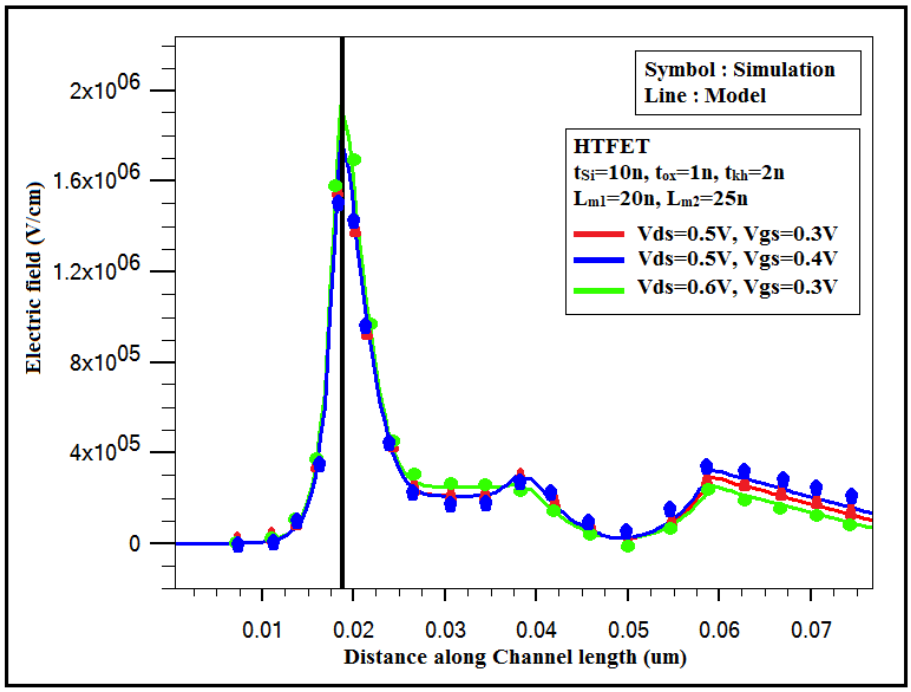


Fig. 4.4(a): Electric field profile along channel length of the proposed heterostructure (tsi=10nm, tox=1nm and thk=2nm) for various V_{GS} and V_{DS}

The total electric field profiles along the channel length are depicted in Fig. 4.4(a) for various bias conditions. A set of curves are extracted for V_{gs}=0.3V and 0.4V at a V_{ds}=0.5V, along with a curve drawn for V_{gs}=0.3V at a V_{ds}=0.6V. The numerical simulations are carried out with the metal work functions of 4.2eV and 4.6eV for the tunneling gate and the auxiliary gate, respectively, following the oxide thickness of 1nm and 2nm for the SiO_2 and HfO_2, respectively. The field intensity attains its highest peak (Fig. 4.4a) at the source/channel (tunneling) junction and gets shallow from the drain/ channel (reverse tunneling) junction towards the drain region. The phenomena manifest the utmost carrier tunneling across the tunneling junction, supporting a

poor reverse tunneling across the reverse tunneling junction, rendering the proposed device's high ON state and low OFF-state current. As a result, the field intensity reflected by the green curve acquires the maximum value at the source end and plunges effectively at the drain end of the channel for the optimized structure design. The right side peak (nearly at the middle of the channel) exhibits the change in electric field due to change in the work functions of metal-1 & 2. The extreme right peak, at the drain-channel junction, occurs due to the difference in doping concentration in the channel and drain regions.

A thorough assessment of longitudinal and resultant electric field profiles is drawn and compared in Fig 4.4(b). A set of characteristic curves has been extracted at constant V_{ds}=0.5 V for V_{gs}=0.3 and 0.4 Volts, followed by V_{ds}=0.6 V for the same set of V_{gs} values mentioned above. It is evident from the figure that more rise in V_{gs} puts the barrier potential down, which ultimately endorses more carrier injection phenomena across the tunneling region. However, the said phenomena reinforce the reverse tunneling consequently. Similarly, the drain to source voltage (V_{ds}) equally amplifies the electric field intensity at the source/ channel junction, stimulating the ON-state current further in conjunction with OFF-state/ ambipolar current on account of the drain side electric field. However, both the figures (Fig. 4.4 (a) & (b)) well justified the accuracy of the derived analytical model.

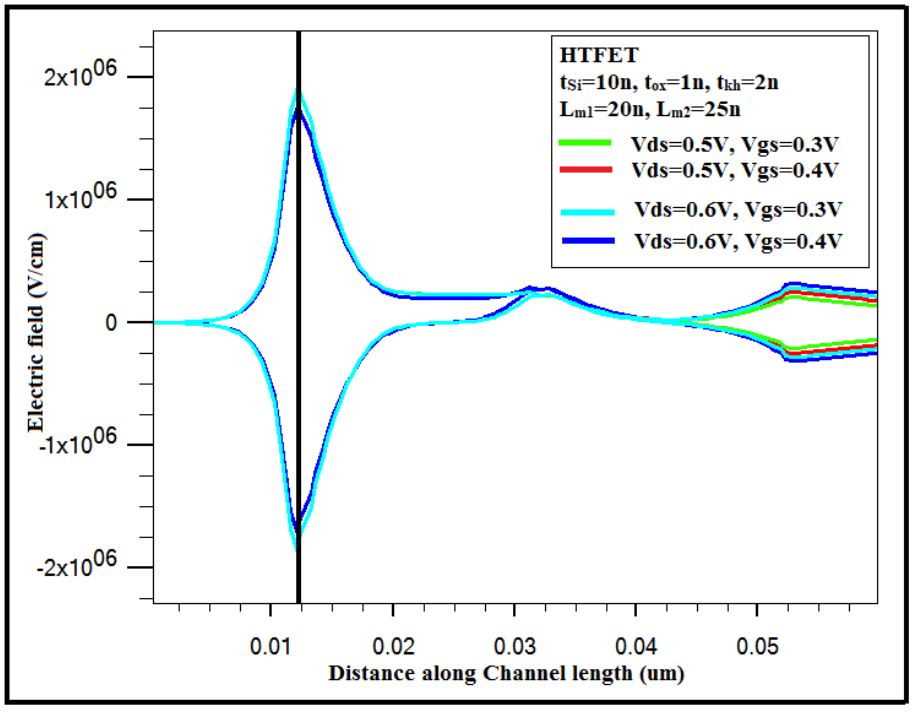


Fig. 4.4(b): Comparison of Electric field profile along channel length of the proposed heterostructure (t_{si}=10nm, tox=1nm and t_{hk}=2nm) for various V_{GS} and V_{DS} values.

The tunneling path, another significant parameter, plays its role in determining the drain current based on the tunneling probability across the source/ channel interface. The minimum tunnel length, a function of the gate to source voltage (V_{gs}), shrinks with the increase of the V_{gs} since the applied gate voltage modulates the band bending at the junction region. In Fig. 4.5, the minimum tunneling length is attributed with respect to the gate to source voltage. The figure renders the exponential reduction of the minimum tunnel length with rising in V_{gs}, leading to a subsequent escalation in ON state drain current. The minimum tunneling length derived from the analytical model is compared with the simulation data, finding an excellent fitment as shown in the said figure.

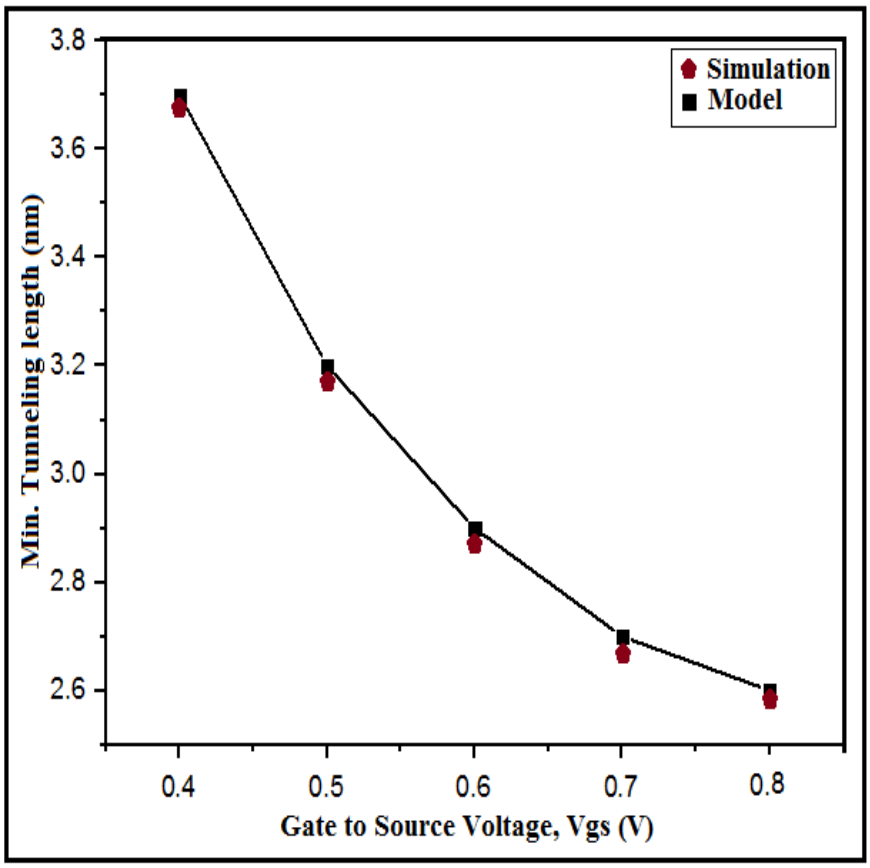


Fig. 4.5: Calculated and simulated data of Minimum tunneling length with respect to Gate voltages.

Next, to proceed with the analysis of the transfer characteristics of the proffered HTFET has been demonstrated in Fig. 4.6. Figure 4.6 (a) refers to the I_D - V_{gs} characteristics manifested for different work functions of the Metal-1 (M1) while keeping the Metal-2 (M2) work function at a constant value of 4.6 eV. The impact of work function engineering is studied exclusively over the device performances in terms of ON current, OFF current, ambipolar conduction, and subthreshold swing. Metal-1 work function, ϕ_{m1} for the tunneling gate, has been varied from 4.05 eV to 4.3 eV. Betterment in the subthreshold swing is manifested in the said figure for the higher values of ϕ_{m1}. A close observation finds inaccuracy in the transfer characteristics for ϕ_{m1} lesser than 4.05 eV. On the other hand, the drive current drops significantly for ϕ_{m1} more than 4.3 eV, resulting from freezing the said parameter value as 4.2 eV for tunneling gate to achieve the highest tunneling probability leading to satisfactory drive current along with better ON/OFF current ratio and subdued leakage current.

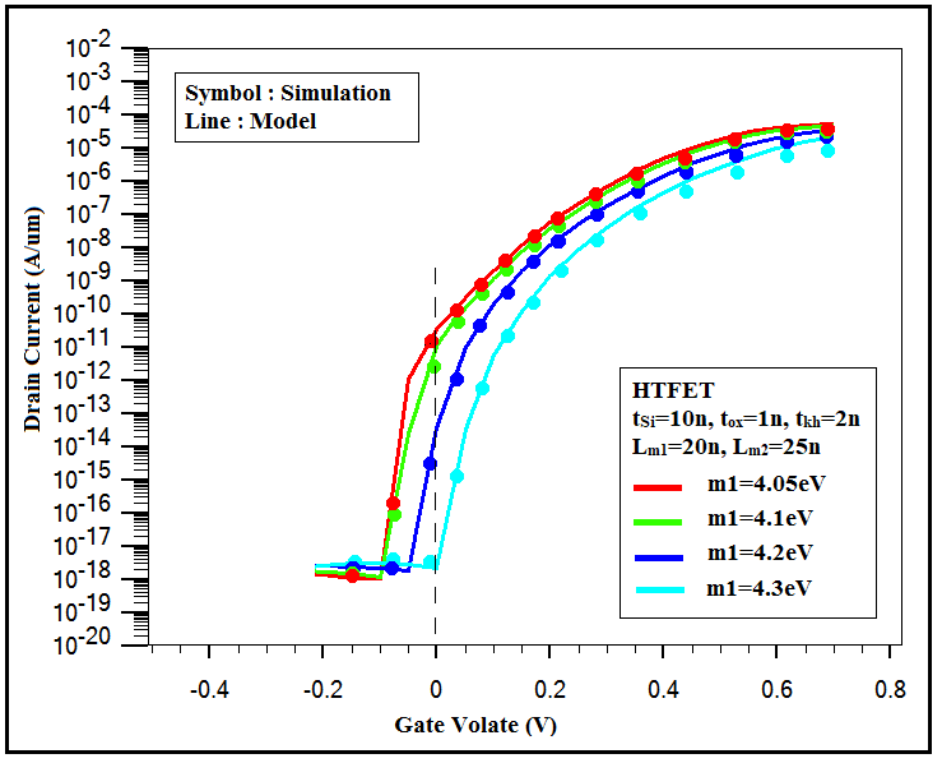


Fig. 4.6(a): Transfer characteristics of proposed HTEF with varying metal-1 work function for a constant metal-2 work function (4.6eV).

Alternatively, the Metal-2 work function, ϕ_{m2} for the auxiliary gate, is varied from 4.4 eV to 4.7 eV with constant ϕ_{m1}=4.2 eV in obtaining the optimum performance of the target device. Fig. 4.6(b) illustrated the impact of ϕ_{m2} over the drain current characteristics (I_D - V_{gs}). It is observed from the figure that this parameter has hardly any influence in controlling drive current since it is the feature of auxiliary gate material situated at the drain side of the channel. Instead, this part of the metal gate tries to get control over the ambipolarity of the device. As a result, the said device performance has been optimized in suppressed ambipolarity, lower leakage, and steeper subthreshold swing for ϕ_{m2}=4.6 eV. The performance degradation is observed with higher leakage and subthreshold swing for ϕ_{m2} lesser than 4.2 eV, which affect the circuit behaviors consequently on static power dissipation and stand-by power consumptions. On the contrary, the drain current gets saturated for ϕ_{m2} more than 4.7 eV. Hence the auxiliary gate work function is set to 4.6 eV in delivering the optimum device performances and circuit.

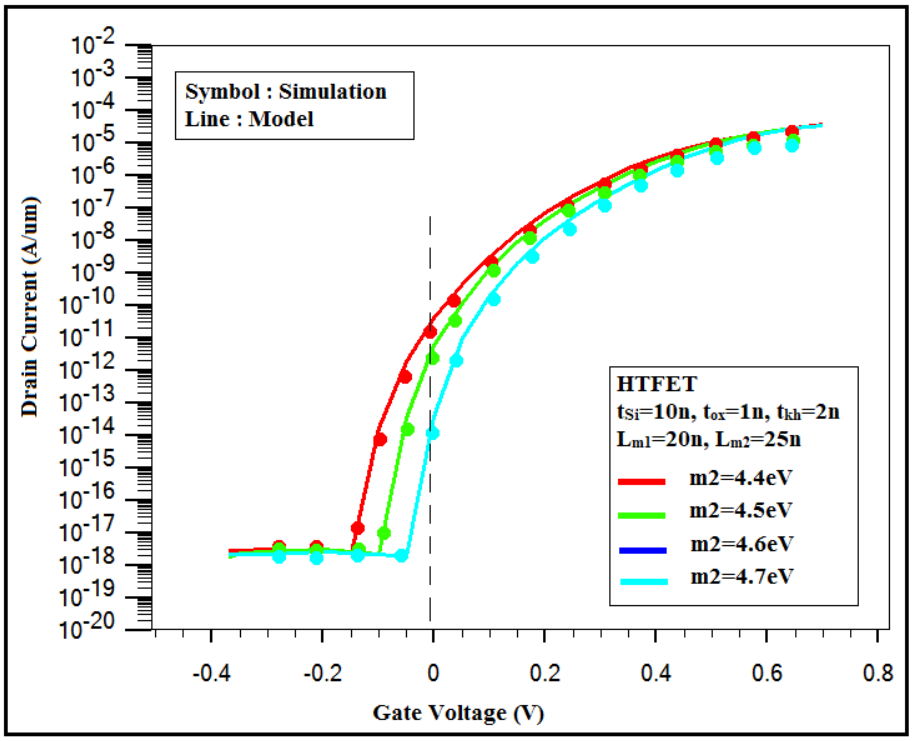


Fig. 4.6(b): Transfer characteristics of proposed HTEF with varying metal-2 work function for a constant metal-1 work function (4.2eV).

The TFET device suffers from low drive current and ambipolar conduction over the MOSFET. The prime objective of this work is to design the TFET structure, which can address these odd issues effectively, extracting the best performances out of the proposed device while delivering the optimum circuit performances in terms of power, delay, and power delay product (PDP). Our proposed structure is facilitated with oxide engineering, work function engineering, along low bandgap engineering implemented with heterojunction. The stack oxide architecture boosts the ON current while restraining the leakage, followed by a dual metal-double gate structure to extend the ON current to its peak, subsequently clamping the OFF current and ambipolar conduction.

Low bandgap materials, preferred for heterojunctions for high drive current, are endorsed in this work with Germanium as source material and Silicon as channel/ drain materials, respectively. The proffered heterostructure plays its role in accelerating the ON current through better tunneling probability. Even better results would have been achieved by modulating the device dimensions viz the thicknesses of oxide and substrate. Our simulation work is extended finally to incorporate the body thickness as 5 nm, which is lesser than the threshold limit of 7 nm. Notably, the quantum correction models are essential to simulate the device having thickness below the threshold limit. Similarly, the oxide thickness is set to 1 nm as a case study where the gate leakage would be unavoidable. Finally, the numerical simulation is carried out without the quantum physical models to predict the device characteristics and circuit performances for future references. The extracted data are registered in Tables 4.2 and 4.3, respectively.

Table 4.2: Study of Characteristics Parameters for Various Body Thickness

t_{si} (nm)	I_{ON} (uA/um)	I_{OFF} (aA/um)	SS (mV/dec)
10	1.01	3.67	30.2
7	1.86	2.81	24.8
5	3.36	1.72	20.6

Table 4.3: Study of Characteristics Parameters for Various High-K Oxide Thickness

t_{hk} (nm)	I_{ON} (uA/um)	I_{OFF} (aA/um)	SS (mV/dec)
1	3.07	2.71	23.8
2	1.86	2.61	24.8
3	0.92	2.46	25.2

4.6. Circuit Level Analysis

The second phase of the proposed work focused on implementing a CMOS-like resistive inverter circuit with the HTFET, investigating the circuit performances viz. power, delay, and power delay product to conclude the work. A resistive inverter circuit is designed with the n-type HTFET as a driver and compatible load resistance and capacitance in order to achieve optimum circuit performance. In addition, the biasing condition needs to be taken care of for the circuit to restrain the device from conducting in forward bias mode. Thereafter, a similar resistive inverter circuit is realized with the same technology node to carry out the comparative studies in the successive literature.

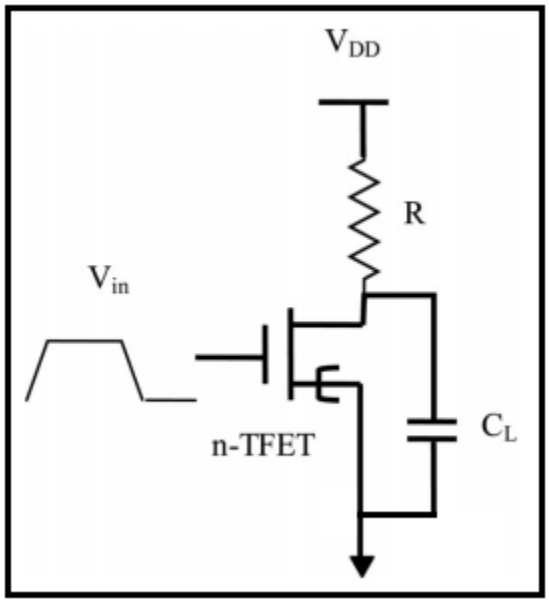


Fig. 4.7: Resistive load inverter circuit with proposed HTFET

The output characteristics of the proposed HTFET have been depicted in Fig. 4.8, demonstrating the overlay of the model and simulation results. At first, the device characteristics

are calibrated with the numerically simulated data to ensure accurate compatibility between device and circuit characteristics. An excellent validation of analytical modeling against TCAD results encouraged in further extraction of device parameters like I_d - V_{ds}, the gate to source capacitance (C_{GS}), and the gate to drain capacitance (C_{GD}) to execute Verilog-A model, which intern contributed to framing the model file of our proffered structure that to be included in the Spice netlist for circuit simulation, performed by Tanner EDA [4.64]. The D.C characteristics of the device are manifested through the Tanner Spice circuit simulator that has validated the modeled results accurately (inferring Fig. 4.8), justifying the use of look-up table-based Verilog-A model in circuit-level implementation.

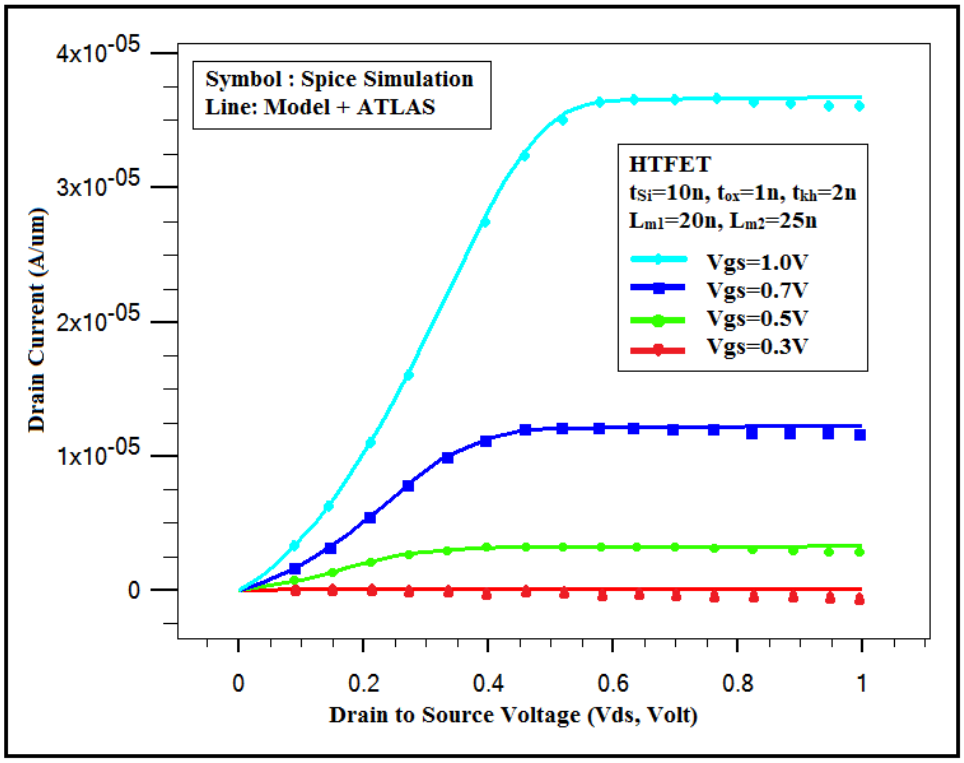


Fig. 4.8: Drain characteristics of the proposed HTFET device

The circuit diagram of a CMOS-like resistive HTFET based inverter is presented in Fig. 4.7. The load resistance value is set to 750 Kohm, determined through the iteration process to achieve optimal circuit performances. The extracted gate capacitance value is found in order of 10^{-17} F. For a range of output capacitance, from 1fF to 10 fF, the circuit performances are evaluated and noted down. After that, the responses of the proposed inverter are compared with that of the CMOS

resistive inverter, both having the same design parameters implemented in the 45 nm technological node. A strained Ge-Si-based PTM model file, owing threshold voltage and OFF current at par with the proposed HTFET based inverter, has been utilized in the simulation to draw the comparative analysis of both circuit performances.

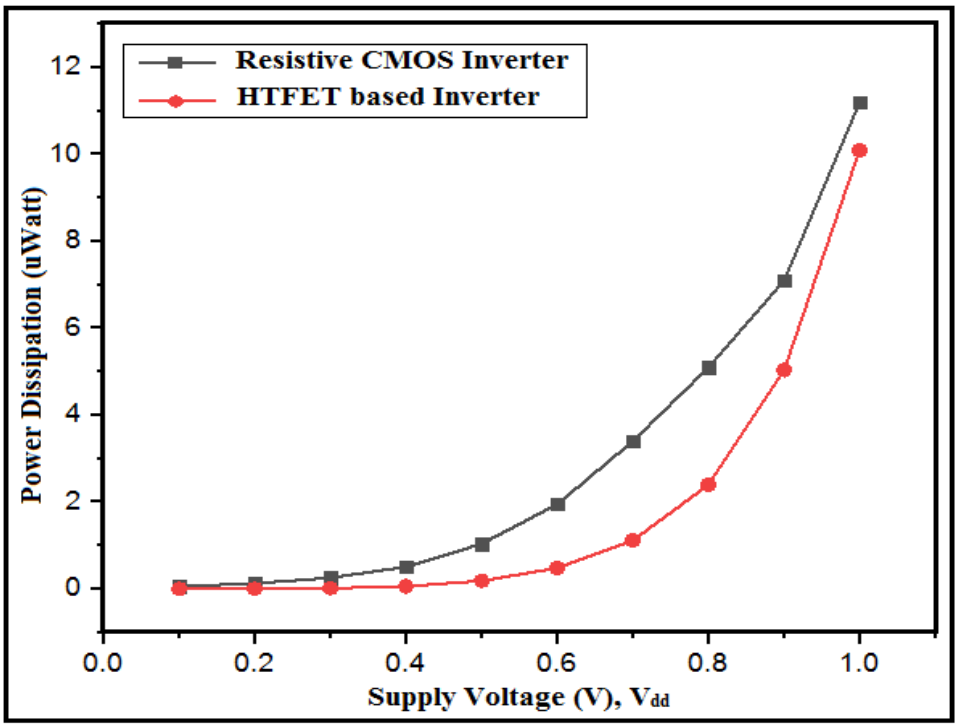


Fig. 4.9: Power dissipation characteristics of CMOS inverter and TFET-based inverter for various supply voltages.

The comparison in power dissipation has been demonstrated in Fig. 4.9. The simulation test has been executed for the supply voltage range from 0.1V to 10V in 0.1V step size. Both the circuits responded in a similar fashion, owing to exponential growth with an increase in supply voltage. For the desired operational voltage ramps from 0.4V to 0.8V, our proposed inverter beats its counterpart in power consumption to a great extent. The result predicts a 76.24% hike in power dissipation of conventional CMOS logic than that of the HTFET-based one. Further, the supply voltage scaling has less impact on the power matrix of the proffer circuit. It is needless to say that the proposed HTFET-based inverter circuit can be widely used in low power applications.

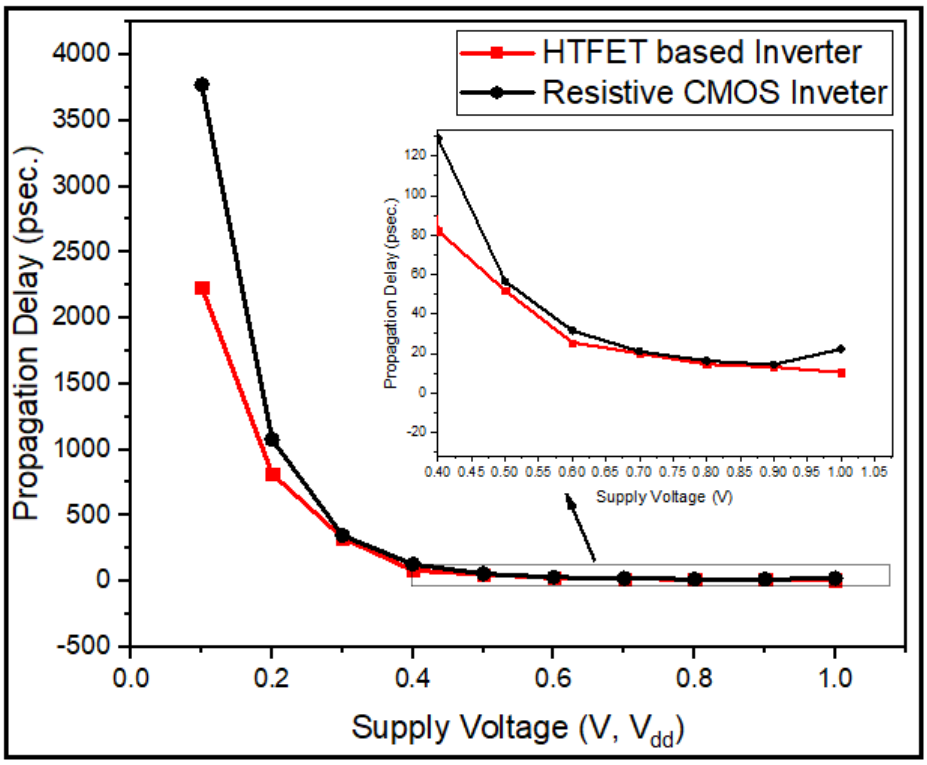
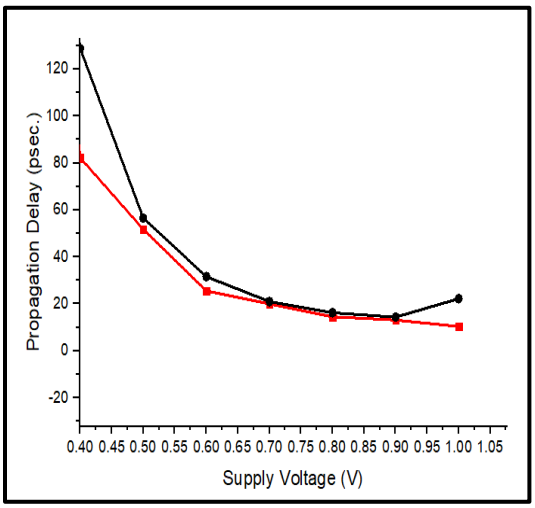
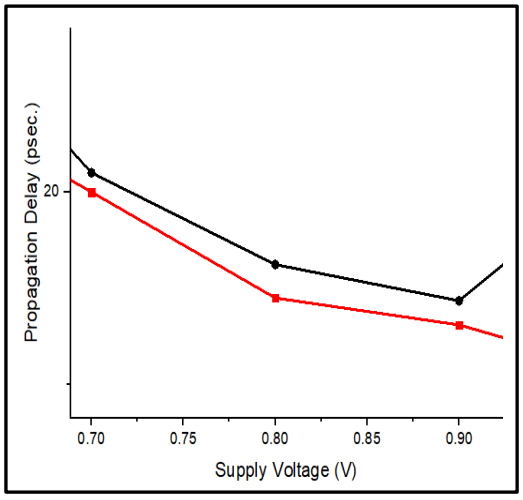


Fig. 4.10: Delay characteristics of CMOS inverter and TFET-based inverter



Inset Fig from voltage range 0.4V to 1V



Inset Fig from voltage range 0.67V to o.93V

The propagation delay characteristics of the respective inverters, portrayed in Fig.4.10, depict the evaluated RC delay for the supply voltage range 0.1V to 1V, featuring an exponential decay for the entire V_{dd} sweeps. A comparative study reveals a better delay response of our proposed circuit than that of the CMOS one. It is found that the CMOS resistive inverter responded 52.4% slower than that of HTFET-based inverter, establishing the superiority of the HTFET-based circuit over the CMOS counterpart in this regard. It is also evident that the propagation delay is a function of supply voltage.

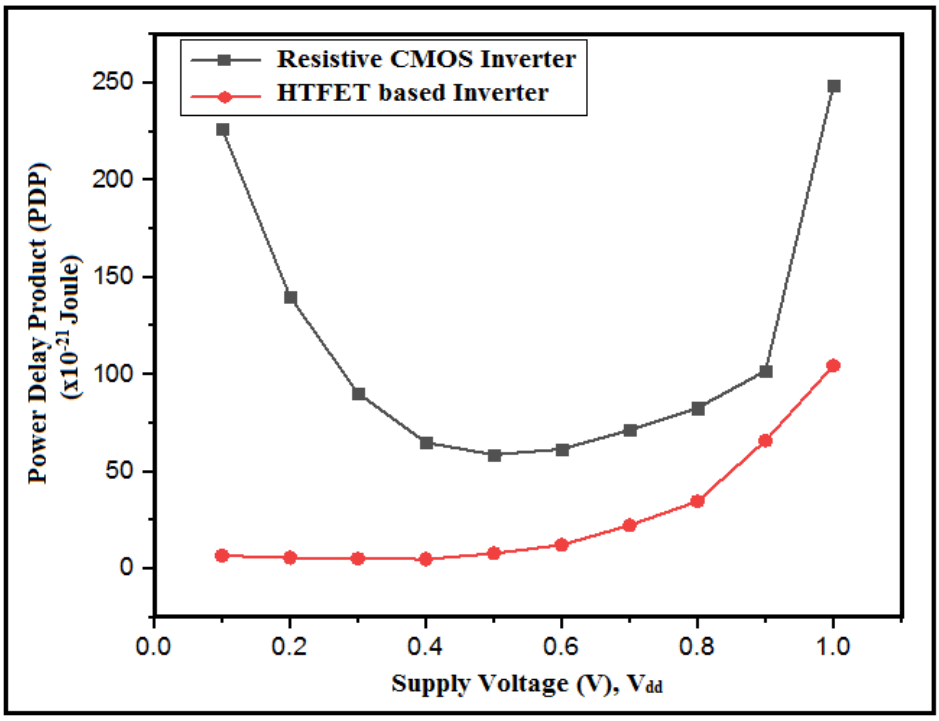


Fig. 4.11: Power Delay Product of CMOS inverter and TFET-based inverter

Last but not least, the power delay products of both circuits have been derived, depicted in Fig. 4.11. A prominent difference is noted in the PDP curves of the respected circuits that the CMOS inverter possesses 58.7×10^{-21}Joule to 248.75×10^{-21}Joule PDP variation. In contrast, it has been 4.93×10^{-21}Joule to 104.53×10^{-21}Joule for the HTFET bases inverter for the same bound of supply voltages. Therefore, the proposed circuit attained a 32.41% lesser PDP value than the CMOS one. Minute observations find some optimum values in the PDP curves of the CMOS circuit, which are absent for the HTFET based inverter. Notably, both the circuits' power dissipation characteristics curves hold a similar set of data points for the lower range of supply voltage (V_{dd}), from 0.1V to 0.35V. Beyond that limit, $V_{dd} \geq 0.35$V, power dissipation has been increased radically for CMOS inverters.

Table 4.4: Comparative Study of Characteristics Parameters for CMOS and HTFET based Inverter

POWER			
Inverter	**Min. Value**	**Max. Value**	**Avg. Value**
CMOS	0.06 uW	9.2 uW	2.87 uW
HTFET	0.002 uW	10.1 uW	1.94 uW
DELAY			
CMOS	14.35 ps	3773 ps	548.93 ps
HTFET	10.35 ps	2235.6 ps	360.17 ps
PDP			
CMOS	61.58×10^{-21} J	226.3×10^{-21} J	110.2×10^{-21} J
HTFET	4.93×10^{-21} J	106.3×10^{-21} J	27.23×10^{-21} J

In context of propagation delay, the CMOS logic consumes more time to respond than HTFET based logic for the same lower range of supply voltage (V_{dd}), from 0.1V to 0.35V approximately. However, both the logic styles attribute almost similar performance for the higher span of the source voltage, i.e., $V_{dd} \geq 0.35V$. Thus, the CMOS inverter circuit profile manifests a sharp fall off at the starting range of V_{dd} (typically between 0.1V - 0.5V), followed by a steep upswing for the span of higher V_{dd} (typically above 0.5V). On the contrary, HTFET based inverter circuit exhibits a steady growth for the entire Vdd sweep in its PDP curve. However, the overall PDP value of the proposed circuit remains always lesser than that of its competitor, advocating the proffered logic over the conventional CMOS one for possible ultra-low power applications.

In addition, the proposed work has been extended to a comparative study with some state-of-art technologies on the context of power dissipation & propagation delay. The comparison is drawn between an adiabatic inverter with a contemporary CMOS inverter, reported in the work [4.65] based on the performance matrix named “energy gain”, implying the percentage of the ratio of the dissipated power of the proposed circuit to that of the conventional CMOS logic. Adiabatic logic [4.66 – 4.68] circuits are well known to achieve ultralow power by restricting the current flow

across the device and recycling the energy of output node capacitances to the AC power supply. Therefore, the merit of our proffered circuit is estimated through the parameter mentioned above by experimenting with two sample voltages (V_{DD}) for the same design parameters and physical conditions. Finally, the outputs are registered and tabulated in Table 4.5. The recorded data unfold that our designed inverter outruns the adiabatic one in power consumption. The adiabatic inverter dissipates about 30-35% of the power consumed by CMOS one, whereas our HTFET inverter drains less than 20% of the power for the same experimental framework.

Table 4.5: Comparative Study of Energy Gain

Supply voltage (mV)	Energy gain for Adiabatic Inverter (%) [32]	Energy gain for HTFET based Inverter (%) [proposed work]
400 mV	32.33	11.76
500 mV	30.39	18.26

An analytical delay modeling of a CMOS inverter in a subthreshold regime is reported [4.33] for ultra-low-power applications. Again, a comparison drawn with our work unveils that the propagation delay recorded for the proposed circuit is only a fraction of nano-seconds, typically about 0.81ns, which is much less than its COMS counterpart, typically about 10-20ns, under the same design perspectives.

References

4.1. Bijoy Goswami, Debadipta Basak, Ayan Bhattacharya, Sutanni Bhowmick, Koelgeet Kaur and **Subir Kumar Sarkar**,"Analytical Modeling and Simulation of Low Power Salient Source Double Gate TFET ", in 3rd International Conference, 2019 Devices for Integrated Circuits (DevIC)", Kalyani Government Engineering College, West Bengal, India, March 23rd-24th, 2019.

4.2. Bijoy Goswami, Ayan Bhattacharya, Komal Kumari, Priyadarshini Das, Wasim Reja and **Subir Kumar Sarka**r, " A Novel Double Source TFET for Low Power Application" in 14th IEEE ICIIS University of Peradeniya, Srilanka,18-20th December 2019

4.3. Nikonov, D. E., et al, "Uniform methodology for benchmarking beyond-CMOS logic devices," in IEEE IEDM Tech. Dig., p.25.4.1- 25.4.4, 2012.

4.4. Subir Kumar Sarkar: "Spintronics Device Based VLSI Chip for Error Correction in Wireless Cellular Communication"AIUB Journal of Science and Engineering.Volume 8 Number 1 August 2009.

4.5. G. P. S Mishra, A. Ghosh, K. M Rajanna, and **Subir Kumar Sarkar**, "Spintronics Devices for Real Life Applications: A Case Study"2nd National Conference on Computing Communication Electronica and Management, conducted by collage of Engineering and information technology jalgaon, Maharashtra.

4.6. Chun Wing Yeung; Khan, A.I.; Sarker, A.; Salahuddin, S.; Chenming Hu, "Low power negative capacitance FETs for future quantum-well body technology," VLSI Technology, Systems, and Applications (VLSI-TSA), 2013 International Symposium on , pp.1,2, 22-24 April 2013.

4.7. Priyanka Saha, Pritha Banerjee, Dinesh Kumar Dash and **Subir Kumar Sarkar**, "Exploring the short channel characteristics of Asymmetric Junctionless Double Gate Silicon On Nothing MOSFET", Journal of Materials Engineering and Performance**,** Springer, DOI: 10.1007/s11665-018-3281-2, March 2018.

4.8. Pritha Banerjee, Anup Sarkar and **Subir Kumar Sarkar**," Exploring the short channel characteristics and performance analysis of DMDG SON MOSFET", Microelectronics Journal, Elsevier, Volume 67, , Pages 50-56, September 2017.

4.9. Tiya Dey Malakar, Partha Bhattacharyya and **Subir Kumar Sarkar**, "Analytical Surface Potential Based Modeling of Drain Current & Trans- conductance of Work Function Engineered gate Recessed S/D SOI/SON MOSFET",published in Advances in Industrial Engineering and Management**,** Vol. 6, No.2, 107-110,2017

4.10. Pritha Banerjee, Aman Mahajan and **Subir Kumar Sarkar**, "2-D Analytical Modeling of Dual-Material Double Gate Silicon-On-Nothing MOSFET", published in Advances in Industrial Engineering and Management**,** Vol. 6, No.1, 11-16,2017

4.11. Tiya Dey Malakar, Moutushi Singh, **Subir Kumar Sarkar**, "Surface Potential Profile of Nano Scaled Work Function Engineered Gate Recessed IR Silicon on Insulator MOSFET", in 2nd International Ethical Hacking Conference 2019 (eHaCON 2019), Institute of

Engineering and Management, Kolkata, August 22nd 2019 and in the series of Advances in Intelligent Systems and Computing volume 1065, by Springer.

4.12. Priyanka Saha, Dinesh Kumar Dash and **Subir Kumar Sarkar**, "Asymmetric Junctionless Double Gate (JLDG) Silicon on Nothing (SON) MOSFET Modified with the Concept of Work Function Engineering: A Comparative Performance Study", published in Advances in Industrial Engineering and Management, Vol. 6, No.1, 17-21,2017

4.13. Dinesh Kumar Dash, Priyanka Saha and **Subir Kumar Sarkar**, "Analytical Modeling of Dielectric Engineered Strained DMDG-TFET", IET Circuits, Devices & Systems, DOI: 10.1049/iet-cds.2018.5293, June 2019.

4.14. Priyanka Saha, Pritha Banerjee and **Subir Kumar Sarkar**, "2D modeling based comprehensive analysis of short channel effects in DMG strained VSTB FET", Superlattices and Microstructures**,** Elsevier**,**doi.10.1016/j.spmi.2018.03.070, vol. 118, pp-16-28, March 2018

4.15. Priyanka Saha and **Subir Kumar Sarkar**, "Explicit threshold voltage modeling insight for short channel characterization of WFE Elliptical GAA strained-Si MOSFET", Journal of Electronic Materials, Springer, vol. 49, pp.7486-7494, (DOI: 10.1007/s11664-020-08503-1, September 2020

4.16. Pritha Banerjee and **Subir Kumar Sarkar**, "Analysis of short channel characteristics in Graded Channel Dual-Material Elliptical Gate-All-Around (GC DM EGAA) MOSFET", DOI: 10.1088/1361-6641/aafc86, Semiconductor Science and Technology, IOP, January 2019.

4.17. Pritha Banerjee and **Subir Kumar Sarkar**, "Comprehensive analysis of subthreshold short channel behavior of a Dual-material gate strained Trapezoidal FinFET",Superlattices and Microstructures**,** Elsevier**,** doi.org/10.1016/j.spmi.2018.02.034, February 2018.

4.18. S. Lal, J. Lu, B. J. Thibeault, M. H. Wong, S. P. DenBaars and U. K. Mishra, "Suppression of Anomalously Large Threshold Voltage in Wafer-Bonded Vertical Transistors by Enhancing Critical Field to Impact Ionization," in IEEE Transactions on Electron Devices, vol. 65, no. 3, pp. 1079-1086, March 2018, doi: 10.1109/ TED.2018 .2797046.

4.19. A. Lahgere and M. J. Kumar, "The Charge Plasma n-p-n Impact Ionization MOS on FDSOI Technology: Proposal and Analysis," in IEEE Transactions on Electron Devices, vol. 64, no. 1, pp. 3-7, Jan. 2017, doi: 10.1109/TED.2016.2622741.

4.20. T. J. Thornton, W. Lepkowski and S. J. Wilk, "Impact Ionization in SOI MESFETs at the 32-nm Node," in IEEE Transactions on Electron Devices, vol. 63, no. 10, pp. 4143-4146, Oct. 2016, doi: 10.1109/TED.2016.

4.21. Dinesh Kumar Dash, Priyanka Saha and **Subir Kumar Sarkar**, "Analytical modeling of asymmetric hetero-dielectric engineered dual-material DG-TFET", in Journal of Computational Electronics, Springer**,** DOI 10.1007/s10825-017-1102-8 , November 2017.

4.22. Sharmistha Shee Karnar, Dinesh Kumar Dash and **Subir Kumar Sarkar** "Comparative study of threshold characteristics in low dimensional TFET with quantum confinement" in 7th International Conference on Computers and Devices for Communications (CODEC-19) December 19-20, 2019.

4.23. Bijoy Goswami, Sutanni Bhowmick, Arindam Haldar, Debadipta Basak, Goutika Paul and **Subir Kumar Sarkar**," Implementation of L-shaped Double Metal Dual Gate TFET towards Improved Performance Characteristics and Reduced Ambipolarity" in Information, Photonics and Communication 2019 (IPC'19) 1st-3rd February, 2019, organized by Department of Electronics and Communication Engineering in assocaiation with SPIE Student Chapter, B. P. Poddar Institute of Management and Technology (BPPIMT), Kolkata.

4.24. H. Liu, S. Datta and V. Narayanan, "Steep Switching Tunnel FET: A Promise to Extend the Energy Efficient Roadmap for Post-CMOS Digital and Analog/RF Application", in 2013 IEEE International Symposium on Low Power Electronics and Design (ISLPED'13), pp.145-150, Sep.2013.

4.25. S. Datta, et al., "Tunnel Transistors for Energy Efficent Computing" IEEE Int. Reliability Physics Symp.(IRPS),Monterey, California, April, 2013.

4.26. K. F. Longenbach, R. Beresford and W. I. Wang, "A complementary heterostructure field effect transistor technology based on InAs/AlSb/GaSb," in IEEE Transactions on Electron Devices, vol. 37, no. 10, pp. 2265-2267, Oct. 1990, doi: 10.1109/16.59918.

4.27. T. J. Cunningham, E. R. Fossum and S. M. Baier, "An analysis of the temperature dependence of the gate current in complementary heterojunction field-effect transistors," in IEEE Electron Device Letters, vol. 13, no. 12, pp. 645-647, Dec. 1992, doi: 10.1109/55.192872.

4.28. H. Fawaz, J. Gest and J. Zimmermann, "A novel model of the gate current in heterojunction FETs," in IEEE Transactions on Electron Devices, vol. 40, no. 5, pp. 846-851, May 1993, doi: 10.1109/16.210189.

4.29. O. M. Nayfeh, C. N. Chleirigh, J. Hennessy, L. Gomez, J. L. Hoyt and D. A. Antoniadis, "Design of Tunneling Field-Effect Transistors Using Strained-Silicon/Strained-Germanium Type-II Staggered Heterojunctions," in IEEE Electron Device Letters, vol. 29, no. 9, pp. 1074-1077, Sept. 2008, doi: 10.1109/LED.2008.2000970.

4.30. A. S. Verhulst, W. G. Vandenberghe, K. Maex, S. De Gendt, M. M. Heyns and G. Groeseneken, "Complementary Silicon-Based Heterostructure Tunnel-FETs With High Tunnel Rates," in IEEE Electron Device Letters, vol. 29, no. 12, pp. 1398-1401, Dec. 2008, doi: 10.1109/LED.2008.2007599.

4.31. C. Le Royer and F. Mayer, "Exhaustive experimental study of tunnel field effect transistors (TFETs): From materials to architecture," 2009 10th International Conference on Ultimate Integration of Silicon, 2009, pp. 53-56, doi: 10.1109/ULIS.2009.4897537.

4.32. R. Narang, M. Saxena, M. Gupta and R. S. Gupta, "Modeling and simulation of multi layer gate dielectric double gate tunnel field-effect transistor (DG-TFET)," IEEE Technology Students' Symposium, 2011, pp. 281-285, doi: 10.1109/TECHSYM.2011.5783830.

4.33. D. K. Mohata et al., "Demonstration of improved heteroepitaxy, scaled gate stack and reduced interface states enabling heterojunction tunnel FETs with high drive current and high on-off ratio," 2012 Symposium on VLSI Technology (VLSIT), 2012, pp. 53-54, doi: 10.1109/VLSIT.2012.6242457.

4.34. R. Rooyackers et al., "Ge-Source Vertical Tunnel FETs Using a Novel Replacement-Source Integration Scheme," in IEEE Transactions on Electron Devices, vol. 61, no. 12, pp. 4032-4039, Dec. 2014, doi: 10.1109/TED.2014.2365142.

4.35. A. M. Walke et al., "Fabrication and Analysis of a ${\rm Si}/{\rm Si}_{0.55}{\rm Ge}_{0.45}$ Heterojunction Line Tunnel FET," in IEEE Transactions on Electron Devices, vol. 61, no. 3, pp. 707-715, March 2014, doi: 10.1109/TED.2014.2299337.

4.36. M. Kim, Y. K. Wakabayashi, M. Yokoyama, R. Nakane, M. Takenaka and S. Takagi, "Ge/Si Heterojunction Tunnel Field-Effect Transistors and Their Post Metallization Annealing Effect," in IEEE Transactions on Electron Devices, vol. 62, no. 1, pp. 9-15, Jan. 2015, doi: 10.1109/TED.2014.2371038.

4.37. Dinesh Kumar Dash, Priyanka Saha and **Subir Kumar Sarkar**, "3-D Analytical Modeling of Triple Metal Tri-Gate Graded Channel High-k SON TFET for Improved Performance" Silicon, Springer, vol.12, pp-2041-2052, DOI: 10.1007/s12633-019-00268-5, Dec 2019.

4.38. S. W. Kim and W. Y. Choi, "Hump Effects of Germanium/Silicon Heterojunction Tunnel Field-Effect Transistors," in IEEE Transactions on Electron Devices, vol. 63, no. 6, pp. 2583-2588, June 2016, doi: 10.1109/TED.2016.2555928.

4.39. Disha Bhattacharjee, Bijoy Goswami, Dinesh Kumar Dash, Ayan Bhattacharya and **Subir Kumar Sarkar**," Analytical Modelling and Simulation of Drain Doping Engineered Splitted Drain Structured TFET and its Improved Performance in Subduing Ambipolar Effect", IET Circuits, Devices & Systems, DOI: 10.1049/iet-cds.2018.5261, May 2019.

4.40. Pritha Banerjee, Priyanka Saha and **Subir Kumar Sarkar**,"Two dimensional analytical modeling of a high-K gate stack triple-material double gate strained silicon-on-nothing MOSFET with a vertical Gaussian doping", in Journal of Computational Electronics**, Springer,** DOI 10.1007/s10825-017-1089-1, November 2017.

4.41. P. Saha, S. Sarkhel, P. Banerjee and **S. K. Sarkar,** "3D Modeling based Performance Analysis of Gate Engineered Trigate SON TFET with SiO2/HfO2 stacked gate oxide," 2018 IEEE International Conference on Electronics, Computing and Communication Technologies (CONECCT), 2018, pp. 1-4, doi: 10.1109/CONECCT.2018.8482379.

4.42. Pritha Banerjee, Priyanka Saha and **Subir Kumar Sarkar**, "Analytical Modelling and Performance Analysis of Gate Engineered Tri-gate SON MOSFET", IET Circuits, Devices & Systems**,** DOI: 10.1049/iet-cds.2017.0473, March 2018.

4.43. A. Pal, A. B. Sachid, H. Gossner and V. R. Rao, "Insights Into the Design and Optimization of Tunnel-FET Devices and Circuits," in IEEE Transactions on Electron Devices, vol. 58, no. 4, pp. 1045-1053, April 2011, doi: 10.1109/TED.2011.2109002.

4.44. J. Núñez and M. J. Avedillo, "Comparative Analysis of Projected Tunnel and CMOS Transistors for Different Logic Application Areas," in IEEE Transactions on Electron Devices, vol. 63, no. 12, pp. 5012-5020, Dec. 2016, doi: 10.1109/TED.2016.2616891.

4.45. Nuñez, Juan & Avedillo, Maria. (2016). Comparison of TFETs and CMOS Using Optimal Design Points for Power-Speed Tradeoffs. IEEE Transactions on Nanotechnology. PP. 1-1. 10.1109/TNANO.2016.2629264.

4.46. S. Strangio, P. Palestri, M. Lanuzza, F. Crupi, D. Esseni and L. Selmi, "Assessment of InAs/AlGaSb Tunnel-FET Virtual Technology Platform for Low-Power Digital Circuits," in IEEE Transactions on Electron Devices, vol. 63, no. 7, pp. 2749-2756, July 2016, doi: 10.1109/TED.2016.2566614.

4.47. S. Yang, H. Lv, B. Lu, S. Yan and Y. Zhang, "A Novel Planar Architecture for Heterojunction TFETs With Improved Performance and Its Digital Application as an Inverter," in IEEE Access, vol. 8, pp. 23559-23567, 2020, doi: 10.1109/ACCESS.2020.2970502.

4.48. M. R. Tripathy, A. K. Singh, A. Samad, K. Baral, P. K. Singh and S. Jit, "Performance Comparison of Ge/Si Hetero-Junction Vertical Tunnel FET with and Without Gate-Drain Underlapped Structure with Application to Digital Inverter," 2020 4th IEEE Electron Devices Technology & Manufacturing Conference (EDTM), 2020, pp. 1-4, doi: 10.1109/EDTM47692.2020.9117840.

4.49. S. Kumar, E. Goel, K. Singh, B. Singh, M. Kumar and S. Jit, "A Compact 2-D Analytical Model for Electrical Characteristics of Double-Gate Tunnel Field-Effect Transistors With a SiO2/High- k Stacked Gate-Oxide Structure," in IEEE Transactions on Electron Devices, vol. 63, no. 8, pp. 3291-3299, Aug. 2016, doi: 10.1109/TED.2016.2572610.

4.50. Sweta Chander, Sanjeet Kumar Sinha, Sanjay Kumar, Prince Kumar Singh, Kamalaksha Baral, Kunal Singh, Satyabrat Jit, Temperature analysis of Ge/Si heterojunction SOI-Tunnel FET, Superlattices and Microstructures, Volume 110, 2017, Pages 162-170, ISSN 0749-6036, https://doi.org/10.1016/j.spmi.2017.08.048.

4.51. Priyanka Saha and **Subir Kumar Sarkar**," Drain current modeling of proposed Dual Material Elliptical Gate-All-Around Heterojunction TFET for enhanced device performance", in Superlattices and Microstructures, Elsevier, DOI: 10.1016/j.spmi.2019.04.022, April 2019.

4.52. Dinesh Kumar Dash, Priyanka Saha, Aman Mahajan, Tripty Kumari and **Subir Kumar Sarkar**,"3D Analytical Modeling and Electrical Characteristics Analysis of Gate Engineered SiO2/HfO2 stacked Trigate TFET", Indian Journal of Physics, Springer, DOI: 10.1007/s12648-019-01446-2, March 2019

4.53. Aman Mahajan , Dinesh Kumar Dash, Pritha Banerjee and **Subir Kumar Sarkar** ,"Analytical Modeling of Triple Metal Hetero Dielectric DG SON TFET", Journal of Materials Engineering and Performance**,** Springer, vol:27, Issue 3, February 2018.

4.54. Priyanka Saha, Saheli Sarkhel and **Subir Kumar Sarkar**," Compact 3D Modeling and Performance Analysis of Dual Material Tri-Gate Tunnel Field Effect Transistor", DOI :10.1080/02564602.2018.1428503,IETE Technical Review **,**Taylor & Francis, January 2018.

4.55. N. Bagga and **S. K. Sarkar,** "An Analytical Model for Tunnel Barrier Modulation in Triple Metal Double Gate TFET," in IEEE Transactions on Electron Devices, vol. 62, no. 7, pp. 2136-2142, July 2015, doi: 10.1109/TED.2015.2434276.

4.56. K.K. Young," Short Channel Effects in fully depleted SOI MOSFETs", IEEE Trans. Electron Devices, Vol.36, No.2, pp-399- 402, Feb. 1989.

4.57. Y. Taur, J. Wu and J. Min, "An Analytic Model for Heterojunction Tunnel FETs With Exponential Barrier," in IEEE Transactions on Electron Devices, vol. 62, no. 5, pp. 1399-1404, May 2015, doi: 10.1109/TED.2015.2407695.

4.58. Priyanka Saha, **Subir Kumar Sarkar,** "Drain current modeling of proposed dual material elliptical Gate-All-Around heterojunction TFET for enhanced device performance", Superlattices and Microstructures, Volume 130, 2019, Pages 194-207, ISSN 0749- 6036.

4.59. Mahdi Gholizadeh and Seyed Ebrahim Hosseini "A 2-D Analytical Model for Double-Gate Tunnel FETs" IEEE Transactions on Electron Devices, Vol. 61, No. 5, May 2014.

4.60. E. O. Kane, "Zener tunneling in semiconductors," J. Phys. Chem. Solids, vol. 12, no. 2, pp. 181–188, 1960, doi: 10.1016/0022- 3697(60)90035-4.

4.61. S. Kumar et al., "2-D Analytical Modeling of the Electrical Characteristics of Dual-Material Double-Gate TFETs With a SiO2/HfO2 Stacked Gate-Oxide Structure," in IEEE Transactions on Electron Devices, vol. 64, no. 3, pp. 960-968, March 2017, doi: 10.1109/TED.2017.2656630.

4.62. S. Kumar et al., "2-D Analytical Drain Current Model of Double Gate Heterojunction TFETs With a SiO2/HfO2 Stacked Gate-Oxide Structure," in IEEE Transactions on Electron Devices, vol. 65, no. 1, pp. 331-338, Jan. 2018, doi: 10.1109/TED.2017.2773560.

4.63. ATLAS: 2-D Device Simulator, SILVACO Int., Santa Clara, CA, USA, 2013.

4.64. Tanner EDA: https://www.mentor.com/tannereda/t-spice.

4.65. M. Chanda, S. Mal, A. Mondal and C. K. Sarkar, "Design and analysis of a logic model for ultra-low power near threshold adiabatic computing," in IET Circuits, Devices & Systems, vol. 12, no. 4, pp. 439-446, 7 2018, doi: 10.1049/iet-cds.2017.0386.

4.66. Chanda, M., Dandapat, A., Rahaman, H.: 'Ultra low-power sequential circuit implementation by a quasi-static single phase adiabatic dynamic logic (SPADL)'. TENCON 2009 – 2009 IEEE Region 10 Conf., 2009, pp. 1–5

4.67. Moon, Y., Jeong, D.K.: 'An efficient charge recovery logic circuit', IEEE J. Solid-State Circuits, 1996, 31, (4), pp. 514–522

4.68. Oklobdzija, V.G., Maksimovic, D., Lin, F.C.: 'Pass-transistor adiabatic logic using single power-clock supply', IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process., 1997, 44, (10), pp. 842–846

CHAPTER 5

Sensitivity Analysis of Core-Shell Junctionless MOSFET as Radiation Sensor

5.1. Introduction

The recent advancement of the atomic industry, clinical radiology, research in high energy physical science aggressively focuses on improving high-sensitive compact sensors to measure ionization radiation. The impact of radiation triggers the variations in electro-physical matrices of all semiconductor devices. Yet, Field Effect Transistors (FETs) [5.1-5.4] are assumed, by all accounts, to be the most promising candidate in this field. Thus, they are utilized as sensors as soon as the rise of modern large-scale manufacturing of FETs [5.5-5.10] due to reduced power cost, higher sensitivity, readily available readings and ease calibration. Modern cut-in-age technology instigates the innovations of characterizing the parameters of the conventional MOSFETs to be best fitted for radiation sensors [5.11-5.14]. Subsequent developments

involving some novel architectures like gate-all-around geometry, bilayer gate oxide, multigate architecture have been experimented with [5.15-5.18] to intensify the sensitivity of the MOSFET dosimeter retaining the reliability intact. Nonetheless, the new structural inventions appeared with more cost, complex fabrication steps, and additional equipment for measuring radiation since threshold voltage is the output parameter for radiation sensing required to be measured by specific setups.

Currently, junctionless transistor (JL FET) has been reported as a potential contender of sensor elements due to their high immunity against SCEs, low thermal budget, and susceptibility to oxide defects [5.19-5.22]. Further, they are compatible with current CMOS-based fabrication technology. Lee et al. introduced a brand-new monolayer doping (MLD) followed by microwave annealing (MWA) at low temperature shell doped junctionless FET (SD JL FET) structure [5.23] for low power application. Jaiswal et al. [5.24-5.25] extend the semi-analytical model to describe the electrical properties of the system.

Therefore, we carried on studies to design a JL DG MOSFET-based radiation sensor by characterizing the radiation-induced electrical parameters. Analytical models of drain current, electric field, surface potential and sensitivity are derived considering the local defects originated by the irradiation. The SILVACO ATLAS 3D device simulator has therefore been used to mimic the structure. Both the results are compared to justify the proposed structure to be performed as a radiation sensor.

To summarize, we conducted this study to design a low-cost, low-power, and commercially feasible semiconductor radiation sensor with state-of-art technology based on a CMOS compatible platform. The shift of threshold voltage is the concerned parameter to be investigated since the irradiation manifested defects in the dielectric oxide compelled to shift the threshold voltage through band bending caused by the change in flat band voltage. Therefore, this study aims to design a high-sensitive, low-power cost-effective radiation sensor with an advanced FET structure with a minimum number of components.

5.2. Reviewing the Relevant Works

Holmes-Siedle is one of the pioneers who contributed groundbreaking research [5.26-5.29] on radiation effects and dose measurements starting in the late 80s. On working Nuclear Instrumentation, he published a report on "*The Use of RADFETS in Radiation Dose Measurement: Report on Three Lots Prepared for the U.S. Army*." The object was to evaluate

the sensitivity of radiation-sensitive FETs with the predicted dose range from 0.05 to 50 Gy, delivered to the U.S. Army by a U.K. manufacturer in the field of strategic dosimetry systems.

The same research group extended their experiments for Single Event Upset (SEU) detection and dose measurement [5.30]. This experiment was conceived to extract the orbital performance of semiconductor memory and RADFET array sensors during solar flares under aerospace engineering. The Geostationary orbital satellite was launched in 1988, and the intercepted data for two years were compared with ground tests. Experimental studies were carried out successfully with varying oxide thickness and biasing conditions of the RADFETs to deliver a wide sensitivity range.

The work had extended further to a remarkable achievement [5.31] by constructing a dosimeter to monitor the radiations inside a Space Technology research Vehicle launched in 1998. The project was a three-year mission with 450 by 1600 Km orbital dimensions owing to an estimated dose of 10 Krads. The On-Chip development of this project successfully measured doses from rads to Mrads.

In the 90s, a research group led by Kelleher published some excellent articles on pMOS dosimeter [5.32-5.36]. With the ever-increasing demands of pMOS dosimeters in spacecraft, warfare, and medicines, it was crucial to look at how the gate-oxide manufacturing technology affected the RADFET's sensitivity. In the early 90s, application-specific RADFETs were used in dosimetry. For example, in the personnel dosimetry, some milli-rad to 1Krad, in medicine 1rad to 50Krad, and in spacecraft, 10rad to 0.5Mrad dosimeters were required. The gate-oxide processing method, gate-oxide thickness, irradiation electric field, and absorbed dose all affect a RADFET dosimeter's sensitivity. According to [5.32], some sensitivity values were 15mV/rad for an oxide thickness of 700nm and an electric field of 1MV/cm, and 10mV/rad for an oxide thickness of 850nm and an electric field of 0.23MV/cm. The experiment was carried out to address the following issues regarding the RADFET sensitivity of a pFET dosimeter with a dielectric thickness of 400nm, consisting of dry/wet/dry oxide combinations: I the variation in oxide thickness, (ii) the variation in temperature needed for oxide growth, (iii) the variation in gate-oxide anneal time and temperature, and (iv) the variation in metal sinter temperature. An ideal set of processing settings to maximise a RADFET's radiation sensitivity was presented in the article's conclusion.

The re-use of RADFET dosimeters was another critical concern for the researchers. The possibility of re-useable dosimeters had been reported [5.33], where studies were conducted to

measure the response of an irradiated RADFET, tried to annealed back to its original threshold voltage to make it possible in further use. Space research is a critical application field for dosimeters, where satellites use RADFETs for reliable information exchange. However, the trapped states inside the oxide got saturated as time passed. Therefore, the dose monitoring of the onboard spacecraft system failed, and difficulties occurred to estimate the lifetime of the onboard electronics critically affected by absorbed radiation. It was essential then to re-use the same dosimeters to restore the operations of space systems.

We need to consider another issue to re-use a dosimeter, i.e., fading. It is an event where a relaxation of the threshold voltage occurred in the dosimeter, removed to prepare it for further use. There are two kinds of fading, negative and positive, depending on the type of interface traps and the annealing of the trapped holes. In conclusion, the work found the possibility of re-using a RADFET dosimeter by thermal annealing at 150^0C and irradiating them further. However, the device's sensitivity gets reduced for the second time than that of the first time used.

A new design approach was proposed [5.34] to overcome the disadvantages of application-specific dosimeters and limited sensitivity problems. The method introduced a stack architecture of RADFETs in dosimeter reader circuitry where the system's sensitivity is the sum of the sensitivity of the individual device. Therefore, the sensitivity of the designed tool could be modulated from a tiny range to desired higher ranges by introducing the auto-scaling concept. The experiment had been successfully carried out on staking pFETs with 50nm gate oxide, which can measure many decades of radiation dose. The work also eliminates the constraint of making radiation-specific dosimeters.

A reported work experimented with the viability of using an on-chip poly-resistor heater in annealing dosimeters to revert to its pre-radiated condition [5.35]. The experimental study investigated the feasibility of 100% annealing of irradiated dosimeters through heating at 300^0C by poly-silicon resistors to remove oxide trapped charges. Furthermore, the poly-silicon heater has another advantage in setting the temperature of the RADFET. Thus it eliminated the temperature dependence, and the RADFET gets ready for accurate measurement of doses since its threshold voltage is no longer dependent on the ambient temperature. The experiment was conducted over two kinds of RADFET sensors, viz. device with a poly-silicon gate and 800 nm thermal oxide and a device with a metal gate, 50 nm gate oxide followed by 800 nm thermal oxide. The first one evolved as a suitable candidate for dosimeter. The poly-resistor heater also

proved its efficiency for annealing, provided you choose a stable gate oxide. Moreover, the poly-heater eliminated the temperature fluctuation of the RADFET onboard sensors.

The efficacy of the stacked RADFET architecture over the sensitivity for low-dose medical applications has been studied by O'Connell et al. [5.36]. 40 RADFETs were stacked in a dosimeter to obtain about 220 times greater sensitivity than a single RADFET. Mathematical analysis carried out on this work supported the experimental results. The merit of the work lies in the fabrication of stacked RADFETs on-chip using a single substrate technology. The composite structure with ***n*** devices exhibits a much higher output voltage than ***n*** times of a single RADFET output voltage. Moreover, the scaling of the RADFET dosimeter was analyzed in the context of stacked architecture. The study reveals a linear relationship of RADFET sensitivity against the no. of RADFET, an ever expecting characteristics of dosimeters.

The study has been extended further to control the output voltage of the stacked RADFETs by applying suitable bulk bias [5.37]. Aiming for higher sensitivity, introducing Zero temperature coefficient (ZTC) bulk bias, and W/L adjustment yielded promising output. As a result, improved sensitivity of 84mV/rad has been obtained for the 940nm device. Bulk bias with ZTC provided a feasible alternative for 400nm devices though some constraints regarding oxide thickness may be considered in structural design. Nevertheless, the highest sensitivity value, 120mV/rad, could be possible with appropriate design considerations, as concluded in work.

Schwank et al. [5.38] reported a dual dielectric RADFET dosimeter comprising thermally grown oxide and CVD deposited nitride for low dose space applications. Irradiation-induced trap charges are deposited at the SiO_2/Si_3N_4 interface. The experiments were pursued with dose rates from 0.002 to 50 rad/sec, bias conditions from -5 to -20 Volts, and annealing temperature of 100^0C for 10^7 secs. Satisfactory results with no fading were observed in the study.

Fabrication of a new type of floating gate MOSFET dosimeter was explored by Tarr et al. [5.39] by using commercial CMOS technology. The floating gate initially charged got discharged partially by irradiation, resulting in a change in threshold voltage to measure absorbed doses. As a result, the measurement doesn't need any external biasing. The device can measure up to 70mV/Gy sensitivity with lesser than 2% tolerance, and the sensor is re-useable.

Experimental studies have been carried out [5.40] with RADFET sensors of two different makers to study the irradiation and post-radiation responses. In addition, two types of

commercial RADFETs of 100 nm gate oxide, fitted for space and nuclear research and industry applications, have been considered for testing sustainability under a radiation environment of several 100 Gy absorbed doses. The study explored a deeper insight into the microscopic process during irradiation and annealing. It is concluded to optimize the defect centers' numbers, locations, and energy to extract the best performing of the RADFETs by controlling high-temperature processes like oxidation and annealing. Moreover, oxide/nitride-based structures could be an alternative instead of thermally grown oxide-based architecture.

Haran et al. [5.41] paid attention to the response of a RADFET experiencing temperature fluctuations and long-time fading. The study was conducted with both implanted and unimplanted oxide-based RADFET structures. Three different temperature compensation techniques have been discussed in this context. One is to set the drain current at the ZTC (Zero Temperature Coefficient) point. The second is to adopt the parallel differential measurement method for the dosimeter made of two identical MOSFETs on the same chip. The third is obtaining the results free from the temperature dependence with the help of laboratory experiments' data. The study thoroughly explored the fluctuation of temperature coefficient followed by irradiation and annealing process.

The role of fixed and switching traps in fading for the implanted and unimplanted oxide-based RADFETs has been analyzed [5.42] by Haran et al.. Notably, 400nm and 1000nm gate oxide thick dosimeters are considered in the study. 400 nm implanted RADFET exhibited significant fading under high border traps followed by subsequent annealing. However, the same device that underwent irradiation with *zero* bias was affected by lower fading.

An energy-dependent sensitivity of a clinical RADFET sensor for radiotherapy application has been analyzed in the literature [5.43]. The device's response attained approximately 3.2 times energy dependence over the energy range of 50kVp to 10MVp. Therefore, a second-order polynomial can theoretically address the sensitivity of the device. However, a further appropriate model can be formulated to acquire a higher degree of accuracy of the sensitivity of the dosimeter.

In their literature, Shaneyfelt et al. demonstrated a CMOS compatible SOI MOSFET dosimeter [5.44]. A discrete SOI RADFET associated with the read-out circuitry was fabricated in commercially available radiation-hardened CMOS SOI technology. Experiments were conducted under various radiation environments, followed by annealing. The results revealed a lesser fading effect in the proposed sensor than dual-dielectric RADFETs. A suitable read-

out circuit was also incorporated to monitor the post-radiation leakage current due to radiation-induced charges into the buried oxide. The radiation characteristics of the device justified the feasibility of fabrication of the dosimeter for low dose rate, low power applications.

A Monte Carlo simulation [5.45] was conducted to look into the response of a RADFET sensor penetrated through photons, protons, electrons, and neutrons. The experiments were carried on with commercially available RADFET chip with DIL 14 ceramic packages that contain four sensor devices. Out of the four, two devices are designed with 50 um gate length, 300 um width, and the other two devices are featured with 15 um gate length, 690 um gate width. The maximum peak for photon radiation is found at 50 keV, followed by a second highest peak at 1 MeV. For electronic radiations, the peak is found at an energy level of about 1.5 MeV with the regular lid, which is 3.6 MeV for the Titanium lids. In the case of proton radiation, the peak is found at 10 MeV energy. The response for neutron radiation finds a constant increase in absorbed dose during the range from 1 MeV to 1 GeV.

The potential of two popular charge neutralization techniques has been investigated in the literature [5.46]. Fowler-Nordheim method and inversion of oxide field are processes in demand to erase the trapped charge during irradiation for the commercial RADFETs of 300 nm gate oxide thickness. However, these processes could neutralize a small percentage of trapped charges, leaving a sufficient amount of border traps inside the oxide seems to be untractable. The work looked into this problem to find a solution to it. The study found the space charge erasure technique efficient for thick gate oxide RDAFETs. The Fowler-Nordheim injection and the Radiation-Induced Charge Neutralization methods were also very fruitful solutions in the post-radiation process for erasing RADFETs.

The experimental works [5.47] were carried on over the test methods developed for TID (Total Ionising Dose) measurements considering the temperature effects. Two experimental setups were demonstrated, carrying the concept of different I-V curve measurements of commercially available PMOS transistors as dosimeters. In addition, the setups were incorporated with a commercially available thermionic cooler to control the temperature during irradiation more accurately. As a result, the temperature coefficient (TC) has been measured explicitly in the in-situ TID measurement. Furthermore, the tailor-made software and temperature control equipment successfully measured the radiation dose as high as 200 krad for Silicon dosimeters.

Zero temperature coefficient (ZTC) has been an essential parameter in dosimetry since the readings of the read-out circuit are taken from the I-V characteristics at this particular point of ZTC. The work [5.48] proposed a novel method to eliminate the adverse effect of temperature over the I_{ZTC} shift. The experiments included five kinds of RADFETs with three different oxide thicknesses in testing the proposed method under radiation environment and thermal cycles. The method involved one MOSFET for measurement and two other MOSFETs to reduce thermal drift. The thermal drift of the output voltage measured by the proposed method was compared with that of the conventional technique. The results reveal a linear temperature coefficient reduction of 33% from 80%, with the IZTC shift from -15% to 65% favoring the proposed work.

Pejocic et al. [5.49] compared the sensitivity of RADFET with that of commercial power VDMOSFET (p-channel IRF9520) under gamma-ray radiation. Both the FET structure with the same oxide thickness (100 nm) were undergone through the experiments to examine the potentiality of the power MOSFET as a radiation sensor. Moreover, the fading characteristics of the devices had been investigated at room temperature for 24 hours. The devices were exposed to radiation doses from 100 to 500Gy with and without gate bias. Under 10 V gate bias during radiation, the linear relationship between threshold voltage shift and radiation dosage has been demonstrated. The sensitivity of the RADFET and the power FET were measured as 6.52 mV/Gy and 7.62 mV/Gy, respectively. The fixed and switching traps density was higher in power MOS than the RADFET. Further, the fading is more pronounced in power MOS than in RADFET.

Ashrafi et al. [5.50] have studied the radiation dose-dependent threshold voltage shift in commercial MOSFETs (3N163 and ZVP3306A) in the biased and unbiased condition. The responses of the RADFETs were examined, and sensitivity was measured under 1 – 5 Gy Gamma radiation dose with 662 keV energy. The biasing voltage of 5V for 2N163 and of 8V for ZVP3306A had been taken for the experiments.

A research group led by Hofman et al. [5.51] paid attention to the limitations inherited in the conventional techniques measuring the shift of threshold voltage due to absorbed radiation. The techniques determine the MTC (Minimum Temperature Coefficient) or ZTC (Zero Temperature Coefficient) point on the V-I curve, which points are temperature dependent. It was observed that the MTC point and the TC value are critically dependent on TID (Total Ionising Dose). Therefore, the post-radiation measurement of TC is highly susceptible to error

subject to a parallel thermal annealing process. In the proposed work, in-situ measurement of RADFET's TC for five biasing conditions has been demonstrated for sustained radiation environment and annealing cycles. The temperature sensitivity and threshold voltage shift were measured with 60 krad radiation followed by a 55 days annealing period. The novelty of the work lies in an accurate measurement of the temperature coefficient leading to mature in-situ temperature compensation techniques.

In their work, Tang et al. [5.52] addressed an issue regarding the declining longevity of the on-chip electronics since they are kept exposed to the challenging radiation environment for a long span. Moreover, the many RADFETs with floating gate architecture could not support the single-poly processes for mixed-signal applications compatible with the sub-nanometer CMOS technology node. Therefore, the present work comprises two types of devices: core logic devices and I/O devices. The sensor is built on a 65 nm technological node, where the I/O devices are constructed with thicker oxide (5 – 10 times thicker) than that of logic devices. The supply voltage was 1V for the logic device, whereas the I/O devices were operated with 1.8V. A new sensor architecture was designed to extract the shift of threshold voltage from the direct comparison of readings between logic and I/O devices. TSMC 65 nm general-purpose CMOS technology had been used where all the electronics components were exposed to a dose rate of 265rad(Si)/sec with TID up to 100 Mrad by a source of Cobalt 60. The sensor prototype required 500 x 500 μm silicon area with an approximate power consumption of 7.1 mW exposed to 75 Mrad irradiation. The dosimeter can be fabricated into a SOC with deep sub-micron CMOS technology to avoid the erosion of co-integrated circuits due to intense radiation.

The major limitation of a RADFET sensor lies in measuring the instantaneous dose rate. Therefore, it worked as a TID sensor in a radiation environment. The drawback leads to the work [5.53] of a innovative method to estimate the dose rate and the TID (Total Ionising Dose) proposed by Kulhar et al.. Conventionally, RADFET sensors are operated in the Current Measurement (CM) method. In contrast, the authors suggested operating the structure in the Pulsed Counting (PC) mode. Each radiation event detected by the sensor system would increase the dose count based on specific criteria. In addition, the read-out circuit was equipped with a temperature compensation system lied on the concept of ZTC (Zero Temperature Coefficient) point. The proposed PC method attributed certain advantages like higher sensitivity, flexible response time as a function of dose rate, minimum measurable dose rate, and little thermal effect on the sensor performance.

Moreover, the PC model had included a temperature compensation measure in a given temperature range. However, the model had to compromise with accuracy and maximum measurable dose rate. Finally, the authors discussed the source and drain (drain is tied to bulk) p-n junction, usually connected to the ground during irradiation, had a minor role in TID sensitivity. Furthermore, the efficacy of the proposed method, the impact of reverse bias on amplifier gain and noise characteristics, and finally, the sensitivity as a function of dose rate and reverse bias have been discussed thoroughly in the literature. The work dealt with the analysis of the sensing device's V – I and C – V curves unveiling linear characteristics in gamma counting ranging from 10μGy to 10Gy/h radiation. Nevertheless, the sensitivity showed a non-linearity from 10 – 30 Gy/h. The sensitivity to the dose rate was reported 1838±9 CPS (cycles per second) at 1±0.05 Gy/h with a minimum detectable 0.5 mGy/h dose rate. The method remarkably performed in sensing the dose rate from 0.5 mGy/h to 10 Gy/h justified its novelty.

A simulation-based study has been conducted by [5.54] to explore the radiation sensitivity of a gate-all-around carbon nanotube (CNT) FET of sub-nanometer dimension for the first time. A CNT structure with 20nm intrinsic gate length, 10 nm drain/source length of $2x10^9$/m, a highly n-type doped material, and 5 nm silicon dioxide thickness was considered the DUT (Device Under Test) in work. The quantum-based simulation incorporated the Poison-Schrodinger equation solver with NEGF formalism. Over a broad range of radiation doses, the study found a linear relationship between sensitivity and the threshold voltage shift. It is also found that the sensitivity of the dosimeter could be appreciably increased by stretching the CNT diameter and gate oxide thickness.

It is experienced that the sensitivity of MOSFET dosimeters improves at the cost of lifespan. Therefore, Biasi et al. [5.55] tried to boost the sensitivity without compromising the lifespan of the dosimeter. They suggested boron implantation through SiO_2 under the gate could be an option to maintain a balance between sensitivity and lifespan of the device since the implantation manifested additional traps at the boron-oxide interface, thereby enhancing sensitivity. The authors chose the setup of an Al-gate p-type MOSFET of 0.80 x 0.60 x 0.35 mm^3 dimensions with 0.68/1 μm thick SiO_2 and 0.2 $\mu C/cm^2$ or 0.6 $\mu C/cm^2$ with implantation energy of 60keV. The work concluded that the device would have higher sensitivity with thicker gate oxide. Further, boron implantation helps to curtail the initial threshold voltage, therefore compensating the linearity and reliability-related issues to a great extent.

Meddour et al. [5.56] reported a junctionless double gate RADFET for enhanced sensitivity. The work analytically explained the sensitivity and other performance matrices in the context of the radiation environment of the proposed device. The proffered device structure was further optimized through a multi-objective genetic algorithm to refine the device as a high-performance radiation sensor. The effect of graphene work function over the sensor's performance has been thoroughly examined to construct a CMOS-compatible device with modern state-of-art technology.

5.3. Device Structure and Radiation Does Profiles

The cross-section view of a core-shell double gate MOSFET is presented in Fig. 5.1. A shalow doped core region is surrounded by a highly doped shell region. The core and shell doping concentrations are 10^{15} cm^{-2} and 10^{18} cm^{-2}. Total body thickness is 10 nm, core thickness is varied from 2nm to 8nm, oxide thickness is taken 2nm, 3nm, and the channel length is considered from 20 nm to 100 nm in this study. The device parameters are enlisted in Table 5.1.

The effect of Gamma-Ray on RADFET is widely presented in many references as mentioned earlier. In the SiO2 layer, ionization radiation generates lots of electron-hole pairs. While a portion of the holes created recombine in their original positions, the electron proceeds fast towards the direction of the gate [5.67-5.68]. The remaining holes then pass through several localised defect states in the SiO2 layer as they make their way towards the oxide-body interface. The total defects in the oxide layer are the sum of the intrinsic defects and the radiation-induced defects. Some portions of the holes are trapped into these defects and form positive trap charges. And the rest are trapped by the interface traps originated through the fabrication process in the oxide layer at the proximity of the Si-body. The electrical properties of the device are greatly influenced by the number of trap charges present in the oxide layer and the interface layer proportionate to the absorbed doses. Additionally, a shift in the threshold voltage is produced by the variation in the trap charge density. The ratio of the Vth-shift to the absorbed dosage is the last method for determining the dosimeter's sensitivity.

In Fig. 5.1, the irradiation-induced trap charges are depicted along the Si-body and oxide interface. The channel has been segregated into three regions to conduct a comparative study of various electrical parameters based on different trap charge profiles. The channel extensions into the source and drain have been considered by regions 4 and 5 (R4 and R5).

The trap charge profiles considering three hypothetical cases are depicted in Fig. 2, where one uniform and two non-uniform profiles are considered for the proposed work. Fig. 2(a) presents the uniform trap charge profile with a constant charge density of $10^{12}cm^{-2}$. Fig. 2(b) refers to a non-uniform profile where regions 1 and 3 (R1 and R3) are only exposed to the radiation environment along with a third profile that represents a step-wise increase in trap charge density along the channel as depicted in Fig. 2(c).

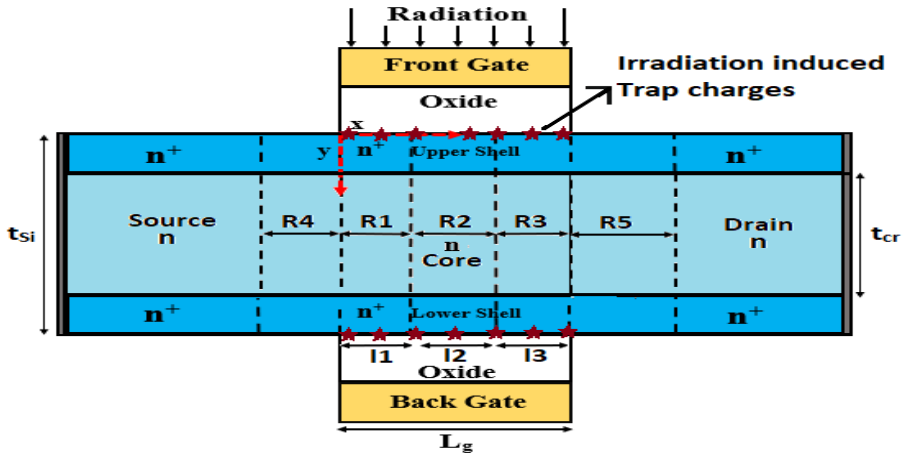


Fig 5.1: View of the Core-Shell double gate junctionless MOSFET (C-S DGJL MOSFET) structure from a cross-section that has been subjected to a lot of radiation.

Table 5.1: Design criteria for the suggested model and simulation

Parameters	**Symbol**	**Values**
Channel length	l_{ch}	30, 60, 80, 100 nm
Channel width	***W***	**0.1 um**
Si-body thickness	t_{Si}	10 nm
Gate oxide thickness	t_{ox}	2, 3 nm
Core thickness	t_{cr}	2, 5, 8 nm
Work function of metal	φ_m	5 eV
Shell doping	N_d	$5x10^{18}cm^{-3}$, $2x10^{19}cm^{-3}$
Core doping	N_{cr}	$1x10^{15}cm^{-3}$

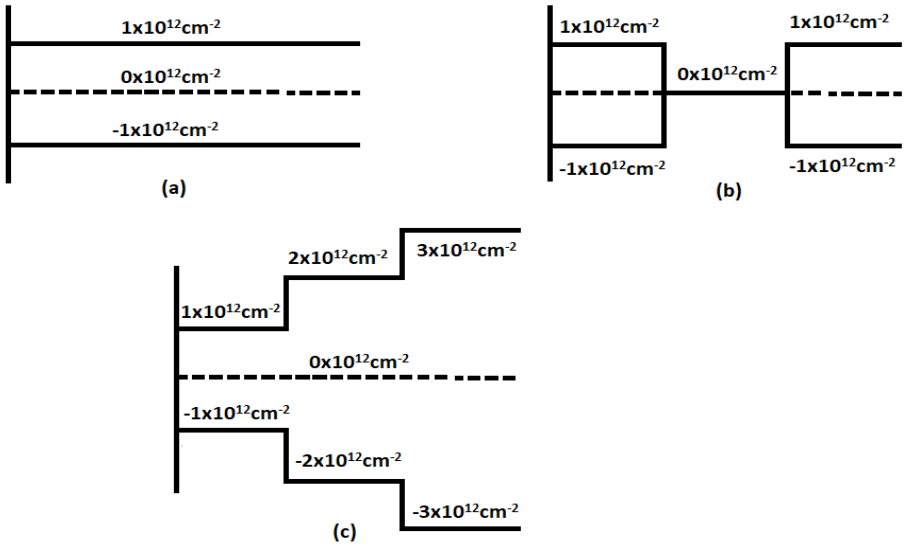


Fig 5.2: (a) Total trap charge density and uniform charge distribution profile (both positive and negative) (b) non-uniform charge distribution profile taking into account various total trap charge densities (c) a step profile with a non-uniform charge distribution that takes total trap charge density into account.

5.4. Analytical Model Formulations

5.4.1. Surface Potential Modeling

A. Poisson's Equation and Parabolic Approximation Model

2D Poisson's equations [5.57, 5.58] are given below to derive the surface potential of the Core-Shell junctionless MOSFET, considering the proposed device working in the subthreshold region [5.59, 5.60].

$$\frac{\partial^2\psi_{u,i}(x,y)}{\partial x^2}+\frac{\partial^2\psi_{u,i}(x,y)}{\partial y^2}=-\frac{qN_d}{\varepsilon_{Si}};\ 0\le y\le\frac{t_{Si}-t_{cr}}{2}\text{; for the upper shell region} \quad (5.1)$$

$$\frac{\partial^2\psi_{l,i}(x,y)}{\partial x^2}+\frac{\partial^2\psi_{l,i}(x,y)}{\partial y^2}=-\frac{qN_d}{\varepsilon_{Si}};\ \frac{t_{Si}+t_{cr}}{2}\le y\le t_{Si}\text{; for the lower shell region} \quad (5.2)$$

$$\frac{\partial^2\psi_{cr,i}(x,y)}{\partial x^2}+\frac{\partial^2\psi_{l,i}(x,y)}{\partial y^2}=-\frac{qN_c}{\varepsilon_{Si}}+\frac{qn_{ic}}{\varepsilon_{Si}}e^{\left\{\frac{\psi_{cr,i}(x,y)-V_f(x)}{V_T}\right\}};\ \frac{t_{Si}-t_{cr}}{2}\le y\le\frac{t_{Si}+t_{cr}}{2}$$

; for core region. (5.3)

We assumed the following three equations of 2-D potential distributions for the upper, lower shell, and core region of the channel in accordance with Young's parabolic approximation model.

$$\psi_{ui}(x,y) = a_{0,i}(x) + a_{1,i}(x)\,y + a_{2,i}(x)\,y^2 \tag{5.4}$$

$$\psi_{l,i}(x,y) = c_{0,i}(x) + c_{1,i}(x)\left(y - t_{Si}\right) + c_{2,i}(x)\left(y - t_{si}\right)^2 \tag{5.5}$$

$$\psi_{cr,i}(x,y) = b_{0,i}(x) + b_{1,i}(x)\left(y - \frac{t_{Si}}{2}\right) + b_{2,i}(x)\left(y - \frac{t_{Si}}{2}\right)^2 \tag{5.6}$$

By employing appropriate boundary conditions, the coefficients of equations (5.4, 5.5, and 5.6) can be found. The following are the boundary constraints for the device geometry along the Y-direction:

(i) Both the y- and x-directions of the proposed device construction are symmetric. The surface potential is the potential at y=0 and tSi. The centre potential is defined as $y=t_{Si/2}$, which is the potential at the device's centre.

$$\left.\begin{aligned}\psi_{u,i}(x,0) = \psi_{l,i}(x,t_{Si}) = \psi_{s,i}(x)\\ \psi_{cr,i}(x,t_{Si}/2) = \psi_{c,i}(x)\end{aligned}\right\} \tag{5.7}$$

(ii) The electric field at y=0 and t_{Si} is given as,

$$\frac{\partial\psi_{u,i}(x,0)}{\partial y} = -\frac{\partial\psi_{l,i}(x,t_{Si})}{\partial y} = \frac{C_{ox}\left[\psi_{Si}(x) - \psi_{g,i}\right]}{\varepsilon_{Si}} \tag{5.8}$$

(iii) The potential is identical at the upper region of shell and core region interface. And the same is true for the lower shell and core region.

$$\left.\begin{aligned}\psi_{u,i}\left(x,\frac{t_{Si}-t_{cr}}{2}\right) = \psi_{cr,i}\left(x,\frac{t_{Si}-t_{cr}}{2}\right)\\ \psi_{cr,i}\left(x,\frac{t_{Si}+t_{cr}}{2}\right) = \psi_{l,i}\left(x,\frac{t_{Si}+t_{cr}}{2}\right)\end{aligned}\right\} \tag{5.9}$$

(iv) The electric flux density is continuous at both the interfaces of the upper-shell /lower-shell and the core.

$$\left.\begin{aligned}\frac{\partial\psi_{u,i}(x,y)}{\partial y} = \left.\frac{\partial\psi_{cr,i}(x,y)}{\partial y}\right|_{y=\frac{t_{Si}-t_{cr}}{2}}\\ \frac{\partial\psi_{cr,i}(x,y)}{\partial y} = \left.\frac{\partial\psi_{l,i}(x,y)}{\partial y}\right|_{y=\frac{t_{Si}+t_{cr}}{2}}\end{aligned}\right\} \tag{5.10}$$

(v) The electric field is considered to be 0 at the oxide-body interfaces (front and back) at the source/ drain extension regions, assuming no fringing field effect over that,

$$\frac{\partial \psi_{u,j}(x,0)}{\partial y} = -\frac{\partial \psi_{l,j}(x,t_{Si})}{\partial y} = 0 \tag{5.11}$$

B. Center Potential at the Source/Drain Extention Region and Channel

The core potential at the channel areas is given with the boundary conditions as stated above as,

$$\psi_{cr,i}(x,y) = \psi_{c,i}(x) - \frac{4\varepsilon_{Si}\{\psi_{c,i}(x)-\psi_{s,i}(x)\} - C_{ox}\{\psi_{s,i}(x)-\psi_{gi}\}(t_{Si}-t_{cr})}{\varepsilon_{Si}t_{Si}t_{cr}} \times \left(y-\frac{t_{Si}}{2}\right)^2 \tag{5.12}$$

Similarly, with the proper boundary conditions, at the source/drain extension region the core potential is given as,

$$\psi_{cr,j}(x,y) = \psi_{c,j}(x) - \frac{4\left[\psi_{c,j}(x)-\psi_{s,j}(x)\right]}{t_{Si}t_{cr,i}}\left(y-\frac{t_{Si}}{2}\right)^2 \tag{5.13}$$

, where, $\psi_{g,i} = V_{GS} - V_{FB} + \frac{qN_{f,i}}{C_{ox}}$ (5.14)

, where the defect density due to absorbed dose is attributed by $N_{f,i}$.

With the suitable boundary conditions, (5.1), (5.3), and (5.12), the relation between the the core potential and surface potential at the channel region is as follows,

$$\psi_{s,i}(x) = \frac{8\varepsilon_{Si}\psi_{c,i}(x) + 2C_{ox}t_{Si}\psi_{g,i} + q(N_d - N_c)t_c(t_{Si}-t_{cr})}{2(4\varepsilon_{Si} + C_{ox}t_{Si})} \tag{5.15}$$

With the suitable boundary conditions, (5.1), (5.3), and (5.13), at the source/drain extension region the relation between the core potential and the surface potential is as follows,

$$\psi_{s,j}(x) = \psi_{c,j}(x) + \frac{qt_{cr}(t_{Si}-t_{cr})}{8\varepsilon_{Si}}[N_d - N_c + n_{ic}e^{\left\{\frac{\phi_{d,j}(x,y)-V_f(x)}{V_T}\right\}}] \tag{5.16}$$

By resolving the 1-D Poisson's equation derived from (5.3), (5.12), and (5.15), as shown below, the centre potential can be found.

$$\frac{d^2\psi_{c,i}(x)}{dx^2} - \left\{\frac{\psi_{c,i}(x)-k_i}{\lambda^2}\right\} = 0 \text{ , where,} \tag{5.17}$$

$$k_i = \psi_{g,i} + \frac{q\left[N_d t_{Si} + \left(N_c - N_d\right)t_{cr}\right]}{2C_{ox}} + \frac{q\left[N_d\left(t_{Si} - t_{cr}\right)^2 + N_c\left(t_{Si} - t_{cr}\right)^2 t_{cr}\right]}{8\varepsilon_{Si}} \quad \text{and} \quad (5.18)$$

$$\lambda = \sqrt{\frac{4\varepsilon_{Si} t_{Si} + C_{ox} t_{Si}^{\,2}}{8C_{ox}}} \quad (5.19)$$

Similarly, by (5.3), (5.13), and (5.4), the 1-D Poisson's equation of the core potential for the source/drain extension regions is obtained (5.16). The answer to which is provided as,

$$\psi_{s,j(x)} = \psi_{c,j}\left(x\right) + \frac{qt_{cr}\left(t_{Si} - t_{cr}\right)}{8\varepsilon_{Si}}\left(N_d - N_c\right) \quad (5.20)$$

As a result, the following equations are used to represent the generic solutions of the core potential at the channel, source-/drain-extension:

$$\psi_{c,i}\left(x\right) = A_i e^{x/\lambda} + B_i e^{-x/\lambda} + k_i \quad \text{; for channel} \quad (5.21)$$

$$\psi_{c4}\left(x\right) = V_S - E_S\left(x + l_{sx}\right) - \frac{qN_{eq}}{2\varepsilon_{Si}}\left(x + l_{sx}\right)^2 \quad \text{; for source extension} \quad (5.22)$$

$$\psi_{c5}\left(x\right) = V_D - E_D\left(x - l_g - l_{dx}\right) - \frac{qN_{eq}}{2\varepsilon_{Si}}\left(x - l_g - l_{dx}\right)^2 \quad \text{; for drain extension} \quad (5.23)$$

The boundary conditions to obtain the unknown parameters of (5.21)-(5.23) are as follows,

(vi) The potential at the interface of reg-4 and source is Vbif. The potential at the interface of the reg-5 and drain is Vbif+Vds.

$$\left.\begin{aligned}\psi_{c4}\left(-l_{sx}\right) &= V_{bif}\\ \psi_{c5}\left(l_g + l_{dx}\right) &= V_{bif} + V_{ds}\end{aligned}\right\} \quad (5.24)$$

(vii)No electric field is present at the reg-4/source interface and the reg-5/drain interface,

$$\left.\begin{aligned}\frac{d\psi_{c4}\left(-l_{sx}\right)}{dx} &= 0\\ \frac{d\psi_{c5}\left(l_g + l_{dx}\right)}{dx} &= 0\end{aligned}\right\} \quad (5.25)$$

(viii) The equal potential at the interface of the reg 3 - 5 and the reg 1-4,

$$\left.\begin{aligned}\psi_{c1}(0)&=\psi_{c4}(0)\\ \psi_{c3}(l_g)&=\psi_{c5}(l_g)\end{aligned}\right\} \tag{5.26}$$

(ix) The continuity of the electric flux density at the interface of the reg 3-5 the reg 1-4 yields as,

$$\left.\begin{aligned}\frac{d\psi_{c1}(0)}{dx}&=\frac{d\psi_{c4}(0)}{dx}\\ \frac{d\psi_{c3}(l_g)}{dx}&=\frac{d\psi_{c5}(l_g)}{dx}\end{aligned}\right\} \tag{5.27}$$

(x) The potential equality at the interface of the reg-1, 2 and the reg-2, 3 at the channel yields as,

$$\left.\begin{aligned}\psi_{c1}(l_1)&=\psi_{c2}(0)\\ \psi_{c2}(l_2)&=\psi_{c3}(0)\end{aligned}\right\} \tag{5.28}$$

(xi) The flux density is continuous at the interfaces of the reg-1, 2 and the reg-2, 3 at the channel,

$$\left.\begin{aligned}\frac{d\psi_{c1}(l_1)}{dx}&=\frac{d\psi_{c2}(0)}{dx}\\ \frac{d\psi_{c2}(l_2)}{dx}&=\frac{d\psi_{c3}(0)}{dx}\end{aligned}\right\} \tag{5.29}$$

The solutions of A_i and B_i of (5.21) obtained by solving the simultaneous equations formed by suitable boundary conditions, mentioned above, are given as,

$$\left.\begin{aligned}A_1&=\frac{1}{2\cosh(l_1/\lambda)}\left[(V_{bix}-k_1)e^{-l_1/\lambda}+A_2e^{-l_1/\lambda}-B_2e^{-l_1/\lambda}\right]\\ B_1&=\frac{1}{2\cosh(l_1/\lambda)}\left[(V_{bix}-k_1)e^{-l_1/\lambda}-A_2e^{-l_1/\lambda}+B_2e^{-l_1/\lambda}\right]\end{aligned}\right\} \tag{5.30}$$

$$\left.\begin{aligned}A_2&=\frac{1}{2\sinh(l_g/\lambda)}\left[-(V_{bif}-k_1)e^{-l_g/\lambda}-(k_2-k_1)\cosh(l_2/\lambda)e^{-l_g/\lambda}+(V_D-k_3)+(k_3-k_2)\cosh(l_3/\lambda)\right]\\ B_2&=\frac{1}{2\sinh(l_g/\lambda)}\left[(V_{bif}-k_1)e^{-l_g/\lambda}-(k_2-k_1)\cosh(l_2/\lambda)e^{-l_g/\lambda}-(V_D-k_3)-(k_3-k_2)\cosh(l_3/\lambda)\right]\end{aligned}\right\} \tag{5.31}$$

$$\left.\begin{aligned} A_3 &= \frac{1}{2\cosh\left(l_3/\lambda\right)}\left[\left(V_{dix}-k_3\right)e^{-l_3/\lambda}+A_2e^{-l_3/\lambda}-B_2e^{-l_3/\lambda}\right] \\ B_3 &= \frac{1}{2\cosh\left(l_3/\lambda\right)}\left[\left(V_{dix}-k_3\right)e^{-l_3/\lambda}-A_2e^{-l_3/\lambda}+B_2e^{-l_3/\lambda}\right] \end{aligned}\right\} \quad (5.32)$$

, where, $V_{bix}=V_{bif}-Q_1l_{sx}^2$; $\quad V_{dix}=V_{bif}+V_{ds}-Q_1l_{dx}^2$ (5.33)

On solving the simultaneous equations obtained based on the conditions (5.26) and (5.27), we got the following equations carrying the unknown parameters l_{sx} and l_{dx}.

$$\cosh\left(l_1\right)l_{sx}^2+2\lambda\sinh\left(l_1\right)l_{sx}^2+Q\left(v_2-v_1\cosh l_1\right)=l_{dx}^2 \quad (5.34)$$

$$\cosh\left(l_3\right)l_{dx}^2+2\lambda\sinh\left(l_3\right)l_{dx}^2+Q\left(v_2\cosh l_3-v_1\right)=l_{sx}^2 \quad (5.35)$$

The extension lengths of source and drain are finally calculated from (5.34) and (5.35). We got a four-degree polynomial, given below, where x equals l_{sx}.

$$p_4x^4+p_3x^3+p_2x^2+p_1x+p_0=0; \quad x=l_{sx} \quad (5.36)$$

, where,

$p_4=a_3^2$, $\quad p_3=2a_3b_1$, $\quad p_2=b_1^2+2a_3c_4-4b_1^2/a_1^3$, $\quad p_1=2b_1c_4$,

$p_0=c_4^2-(b_1^2(1-4a_1c_2))/(4a_1^4)$,

$a_1=\cosh(l_1/\lambda)+\cosh(l_3/\lambda)$, $\quad a_2=a_1^{-1}$, $\quad a_3=a_1-a_2$,

$b_1=2\lambda\sinh((l_1+l_3)/\lambda)$,

$c_1=Q(v_2-v_1\cosh((l_1+l_3)/\lambda))$, $\quad c_2=-Q(v_2\cosh((l_1+l_3)/\lambda)-v_1)$, $\quad Q=\dfrac{2\varepsilon_{Si}}{qN_{eq}}$

$c_3=(2b_1^2-4a_1c_2)/(4a_1^2)$,

$c_4=c_1-c_3$, $\quad v_1=V_{bif}-k_1$, $\quad v_2=V_{bif}+V_{ds}-k_3$,

$V_{bif}=V_{cr}(t_{Si}/2)$ represents the effective built-in voltage at the center of the film.

5.4.2. Drain Current Modeling

The subthreshold Drain current is calculated as follows [5.61, 5.62],

$$I_{ds} = \frac{(KT) W \mu_n n_i \left[1 - e^{-V_{ds}/V_T}\right]}{\sum_{i=1}^{3} P_i(x) + \sum_{j=4}^{5} P_j(x)} \tag{5.37}$$

, where W and μ_n are considered the width of the device and the mobility of the charge carrier. To avoid the complexity of Integral Calculus in finding the different components of equation (5.37), we introduce a piecewise model in deriving the drain current as follows.

$$P_i(x) = \int_0^{l_g} \frac{dx}{F_i(x)} \tag{5.38}$$

$$\left.\begin{aligned} P_4(x) &= \int_{-l_{sx}}^{0} \frac{dx}{F_4(x)} \\ P_5(x) &= \int_{l_g}^{l_g + l_{dx}} \frac{dx}{F_5(x)} \end{aligned}\right\} \tag{5.39}$$

$$F_i(x) = \int_0^{\frac{t_{Si}-t_{cr}}{2}} e^{\frac{\phi_{u,i}(x,y)}{V_T}} dy + \int_{\frac{t_{Si}-t_{cr}}{2}}^{\frac{t_{Si}+t_{cr}}{2}} e^{\frac{\phi_{cr,i}(x,y)}{V_T}} dy + \int_{\frac{t_{Si}+t_{cr}}{2}}^{t_{Si}} e^{\frac{\phi_{l,i}(x,y)}{V_T}} dy \tag{5.40}$$

$$F_j(x) = \int_0^{\frac{t_{Si}-t_{cr}}{2}} e^{\frac{\phi_{u,j}(x,y)}{V_T}} dy + \int_{\frac{t_{Si}-t_{cr}}{2}}^{\frac{t_{Si}+t_{cr}}{2}} e^{\frac{\phi_{cr,j}(x,y)}{V_T}} dy + \int_{\frac{t_{Si}+t_{cr}}{2}}^{t_{Si}} e^{\frac{\phi_{l,j}(x,y)}{V_T}} dy \tag{5.41}$$

5.4.3. Calculation of Sensitivity and its correlation with Threshold Voltage-Shift

The ratio of threshold voltage-change to absorbed dose serves as a gauge for the RADFET's sensitivity. The surface potential for the proposed CS-JLDG MOSFET reaches its minimal value when the gate voltage meets the threshold voltage. We may determine the channel length for which the surface potential expression, for i=2, reaches its minimum value by differentiating the expression and equating the result to "zero". This is,

$$\phi_{\mathrm{m}}(x)\big|_{V_{GS}=V_{Th}} = 0 \tag{5.42}$$

According to a literature review [5.63, 5.64], the potential should be at its lowest value in the channel's midpoint. Thus, the threshold voltage is determined using the surface potential

equation, which attributes the channel's reg-2. The minimum potential value for the given channel length x_{min} is given as,

$$x_{\min} = x_m = \frac{\lambda}{2}\ln(\frac{B_2}{A_2}) \tag{5.43}$$

On substitution of (43) in (15), we have the minimum channel potential as below,

$$\psi(x_m) = \psi_{\min}(x) = \psi_{\mathrm{m}}(x) = \frac{8\varepsilon_{si}(A_2 e^{x_m/\lambda} + B2e^{-x_m/\lambda}) + 2C_{ox}t_{si}(V_{GS} - V_{FB} + qN_{f2}/C_{ox}) + q(t_{si} - t_{cr})(N_d - N_c)t_{cr}}{2(4\varepsilon_{si} + C_{ox}t_{si})} \tag{5.44}$$

Consequently, the condition calculates the threshold voltage,

$$\psi_{\mathrm{m}}(x)\big|_{V_{GS}=V_{Th}} = 0 \tag{5.45}$$

and is given as,

$$V_{Th} = V_{FB} - \left\{\frac{q\left[N_d t_{si} + (N_c - N_d)t_{cr}\right]}{2C_{ox}} + \frac{q\left[N_d(t_{si} - t_{cr})^2 + N_c(t_{si} - t_{cr})^2 t_{cr}\right]}{8\varepsilon_{si}}\right\}$$

$$- \frac{\alpha_1(qN_{f1}/C_{ox} - V_{bif}) - \alpha_2(qN_{f3}/C_{ox} - V_d) - \alpha_3 q(N_{f1} - N_{f2})/C_{ox} + \alpha_4 q(N_{f2} - N_{f3})/C_{ox} + qN_{f2}/C_{ox}}{\alpha_1 - \alpha_2 + 1} \tag{5.46}$$

The value of the unknown constants are given below,

$$\alpha_1 = \frac{e^{\mathrm{l_g}/\lambda}\sinh(x_m/\lambda)}{\sinh(\mathrm{l_g}/\lambda)}$$

$$\alpha_2 = \frac{\sinh(x_m/\lambda)}{\sinh(\mathrm{l_g}/\lambda)}$$

$$\alpha_3 = \frac{\cosh(l_2/\lambda)\cosh(x_m/\lambda)}{\sinh(\mathrm{l_g}/\lambda)}$$

$$\alpha_4 = \frac{\cosh(l_3/\lambda)\sinh(x_m/\lambda)}{\sinh(\mathrm{l_g}/\lambda)}$$

V_{Th0} is the threshold voltage of the pre-radiated device, that is,

$$V_{Th0} = V_{Th}\big|_{N_{f,i=0}} \tag{5.47}$$

and is given by,

$$V_{Th0} = V_{FB} - \left\{ \frac{q\left[N_d t_{si} + (N_c - N_d) t_{cr}\right]}{2C_{ox}} + \frac{q\left[N_d (t_{si} - t_{cr})^2 + N_c (t_{si} - t_{cr})^2 t_{cr}\right]}{8\varepsilon_{si}} \right\} - \frac{\alpha_2 V_d - \alpha_1 V_{bif}}{\alpha_1 - \alpha_2 + 1} \tag{5.48}$$

Therefore, the shift of the threshold voltage due to the irradiation phenomena is calculated as below,

$$\Delta V_{Th} = V_{Th} - V_{Th0}$$

$$\Delta V_{Th} = \frac{qN_{f1}\left\{\cosh(l_2/\lambda)\cosh(x_m/\lambda) - e^{l_g/\lambda}\sinh(x_m/\lambda)\right\}/C_{ox}}{\sinh(x_m/\lambda)(e^{l_g/\lambda} - 1) + \sinh(l_g/\lambda)}$$

$$- \frac{qN_{f2}\left\{\sinh(l_g/\lambda) + \cosh(l_2/\lambda)\cosh(x_m/\lambda) + \cosh(l_3/\lambda)\sinh(x_m/\lambda)\right\}/Cox}{\sinh(x_m/\lambda)(e^{l_g/\lambda} - 1) + \sinh(l_g/\lambda)}$$

$$+ \frac{qN_{f3}\sinh(x_m/\lambda)(1 + \cosh(l_3/\lambda))/C_{ox}}{\sinh(x_m/\lambda)(e^{l_g/\lambda} - 1) + \sinh(l_g/\lambda)} \tag{5.49}$$

The *sensitivity* of the RADFET given by *S* is defined as,

$$S = \frac{\Delta V_{Th}}{D} \tag{5.50}$$

, where *D* is the radiation dose.

The relation between the interface trap charge density due to absorbed and applied doses can be characterized by the following equation, as reported in an experimental work led by Jaksic et al. [5.65].

$$N_{f,i} = d_{11} D_i + d_{12} \tag{5.51}$$

Where d_{11} and d_{12} are the fitting parameters, and the corresponding values of the constants are,

d_{11}= 1.61x10^{10}cm^{-2}/Gy

d_{12}= 5x10^{11}cm^{-2}

On substitution of (51) and (49 in (50), we have the expression of the sensitivity as follows,

$$S = \frac{q(d_{11} + d_{12}/D_1)\left\{\cosh(l_2/\lambda)\cosh(x_m/\lambda) - e^{l_g/\lambda}\sinh(x_m/\lambda)\right\}/C_{ox}}{\sinh(x_m/\lambda)(e^{l_g/\lambda} - 1) + \sinh(l_g/\lambda)}$$

$$-\frac{q(d_{11}+d_{12}/D_2)\left\{\sinh(l_g/\lambda)+\cosh(l_2/\lambda)\cosh(x_m/\lambda)+\cosh(l_3/\lambda)\sinh(x_m/\lambda)\right\}/Cox}{\sinh(x_m/\lambda)(e^{l_g/\lambda}-1)+\sinh(l_g/\lambda)}$$

$$+\frac{q(d_{11}+d_{12}/D_3)\sinh(x_m/\lambda)(1+\cosh(l_3/\lambda))/C_{ox}}{\sinh(x_m/\lambda)(e^{l_g/\lambda}-1)+\sinh(l_g/\lambda)} \quad (5.52)$$

Equation (5.52) established a relation between sensitivity and absorbed dose.

5.5. Results and Discussions

This part verified the accuracy of our suggested model using simulated data. The suggested device is simulated numerically in three dimensions using the Silvaco Atlas device simulator [5.66]. The simulation included both the Lombardi (CVT) model, which is the comprehensive one to represent the doping, temperature, and electric field effect, and the Boltzmann statistics, default model. In addition, the movement of the charge carriers via drift-diffusion mechanisms is attributed using the concentration-dependent (CONMOB) and electric field-dependent (FLDMOB) mobility models. Additionally, Fermi-Dirac statistics with bandgap narrowing (BNG) models helped to mitigate the effects of heavy doping on the proposed device's band bending.

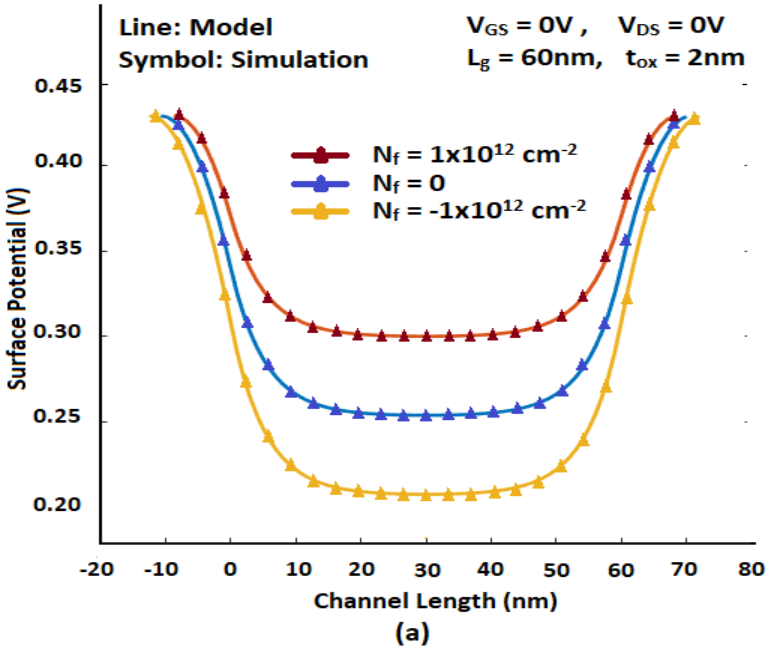
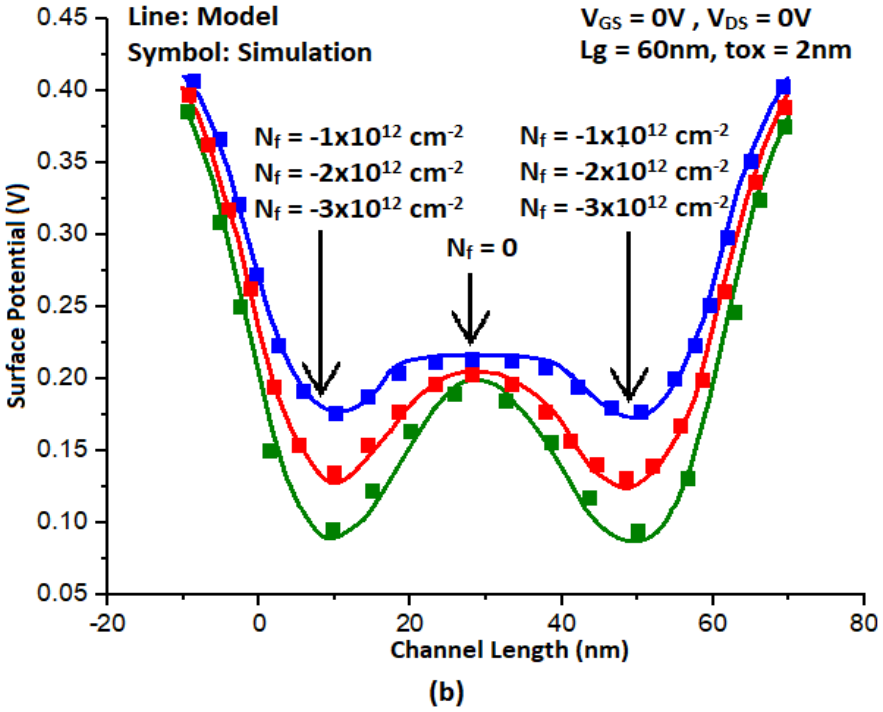


Fig 5.3 (a): Surface potential variation over the length of the channel of the C-S JLDG MOSFET due to uniform trap charge distribution is shown in Fig. 5.2(a) with the design parameters tsi=10nm, tox=2nm, tcr=8nm, lg=60nm, and Nd=5x10^{18}cm^{-3}.

Additionally, the minority carrier lifetime in recombination events is described using the Shockley-Reed-Hall (SRH) and Auger recombination models. In order to combine the effects of the interface charges and fixed oxide charges on the electrostatic behavior of the proposed RADFET device, the trap charge models are invoked in the final step. However, because the device's Si-body thickness is maintained at or above 7 nm, the quantum confinement paradigm is not employed.

We demonstrated the impact of the radiation-induced trap charges over the surface potential over the device's channel length in Fig. 5.3. Fig. 5.3(a) portrayed the potential profile of the proposed device under uniform absorption dose. The relation of effective gate voltage with trap charges is governed by the equation (5.14). The flat band voltage of the device gets increased for positive trap charges leading to a lesser effective gate voltage. Consequently, the barrier potential decreases, accumulating positive interface charges due to absorbed radiation. On the contrary, for the negative trap charges, the device's flat band voltage decreases, resulting in a hike in the effective gate voltage. Therefore, the barrier potential of the said device increases.



(b)

Fig. 5.3(b): Surface potential variation over the length of the channel of a C-S JLDG MOSFET due to non-uniform trap charge distribution is shown in Fig. 5.2(b) with design parameters tsi=10nm, tox=2nm, tcr=8nm, lg=60nm, and Nd=5x10^{18}cm^{-3}.

These underlying physics-based characteristics are demonstrated in the figure, where the proposed CS-JL MOSFET is exposed under a uniform radiation environment. Irradiation-induced negative/positive trap charges are considered for the simulations. The device is kept in unbiased condition, and the potential profiles are extracted. The radiation-induced trap charges decrease or increase the barrier potential depending upon the polarity of the charged particles, as expected. Moreover, it impacts the source/drain extension lengths demonstrated in the figure. Notably, the effect of the negative trap charges is more pronounced than that of positive ones over the device electrostatics since this condition compelled to extend more the affected areas shared by channel with source/drain. The figure shows the potential distribution over the channel for the trap charge densities of $10^{12}/cm^2$, $-10^{12}/cm^{2,}$ and no charge density.

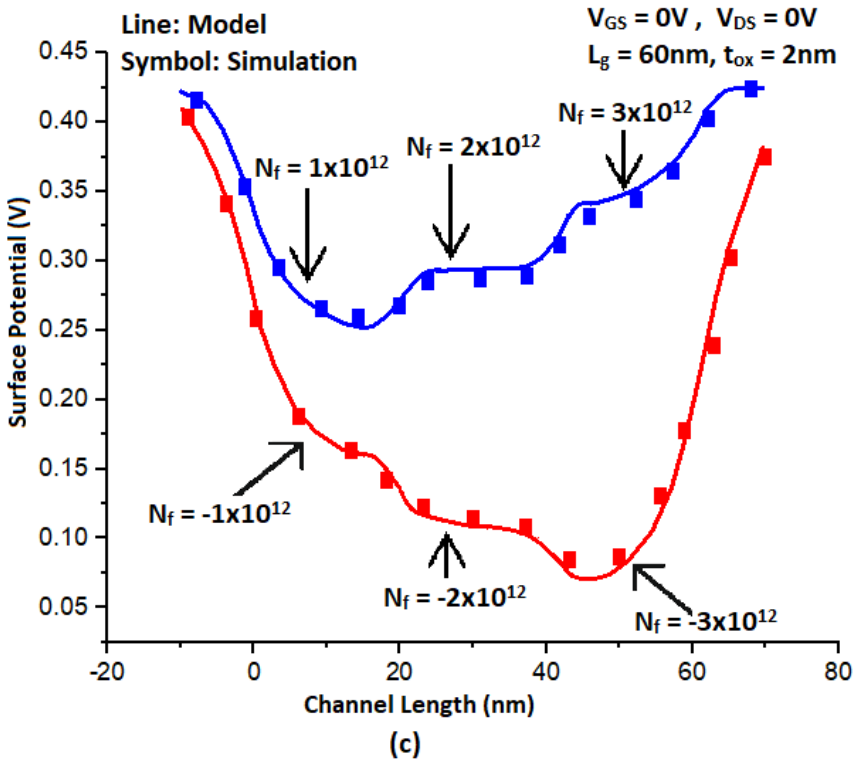


Fig. 5.3(c): Surface potential variation over the length of the channel of the C-S JLDG MOSFET due to non-uniform trap charge distribution is shown in Fig. 5.2(c) with the design parameters tsi=10nm, tox=2nm, tcr=8nm, lg=60nm, and Nd=$5x10^{18}cm^{-3}$.

Figure 5.3 illustrates the impact of the non-uniform trap charge distribution seen in figure 5.2(b) over the surface potential of the proposed RADFET sensor. The simulation incorporates negative polarity charges in order to anticipate the potential distribution of the impacted device because the influence of negative trap charges is more harmful than that of positive ones (described before). The characteristics are drawn for the charge densities $-1x10^{12}/cm^2$, $-2x10^{12}/cm^2$ and $-3x10^{12}/cm^2$ over an unbiased device. Accumulation of negative charges in

higher magnitude due to higher radiation deforms the potential profile drastically. Even the unexposed channel region (where N_f=0) gets severely affected by the neighboring affected regions, which is more dominant in the case of the higher magnitude of the interface charges. The proposed analytical model successfully captured the deformed potential profiles under the influence of the harsh radiation environment.

The proposed device's surface potential distribution is influenced by a kind of step profile of the trapped charge density (refer to Fig. 5.2(c)) is illustrated in Fig. 5.3(c). The more substantial effect of the negative trap charges than its counterpart is evident here. This is because the deformation of the curves is more detrimental affected by N_f ranging from -1x10^{12}/cm^2 to 3x10^{12}/cm^2 rather than that of by the positive trap charge densities of equivalent magnitudes.

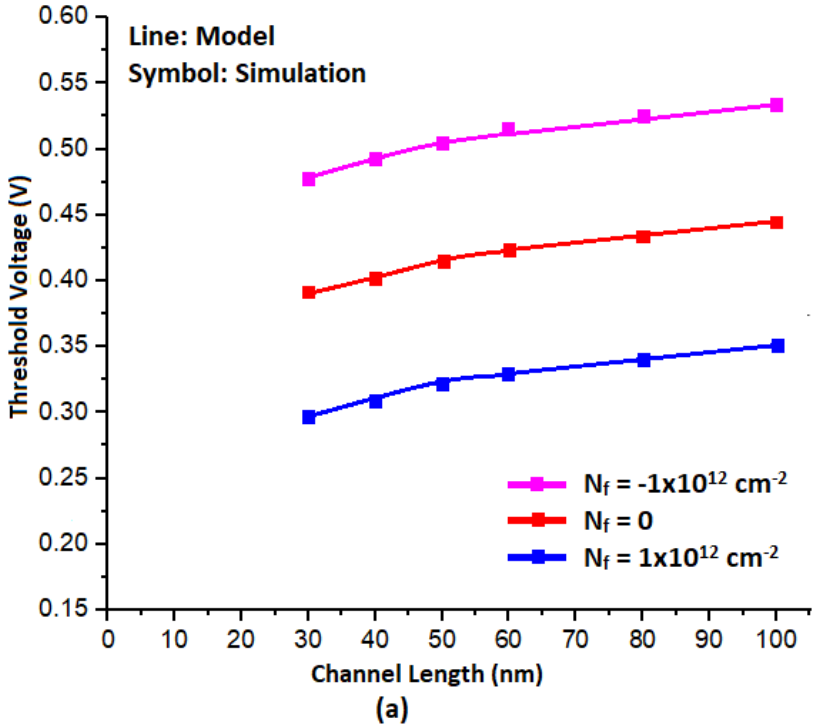


Fig. 5.4(a): Threshold voltage profile along the channel length that incorporates the effects of the trap charge brought about by absorbed radiation doses.

The threshold voltage variation due to the absorbed radiation of the proposed sensor is presented in Fig. 5.4(a). It is explained earlier how the barrier potential of the target device is reduced (increased) for irradiation-induced positive (negative) trapped charges. Consequently, the device's threshold voltage is decreased (increased) in proportion, as shown in the above figure. A higher threshold voltage is observed due to the negative accumulated interface charge

density of magnitude -1x10^{12}/cm^2 than the *zero* and 1x10^{12}/cm^2 trap charge densities. The threshold voltage roll-off of the scaled device is also noticeable. However, the appreciable changes in threshold voltage induced by the absorbed radiation doses reflect a remarkable sensitivity of our proposed C-S JLDG MOSFET-based dosimeter.

Fig. 5.4(b) captured the trapped charge-induced threshold voltage profiles for different gate oxide thicknesses of the proposed device. The states of the defect density on account of the radiation environment must be higher for thicker gate-oxide resulting in more trap charges accumulation inside the oxide and the body-oxide interface. That does raise the device's threshold voltage. As a result, it should be emphasized that a device with a thicker gate-oxide gives more sensitivity. Additionally, the induced trapped charge densities have a linear relationship with the threshold voltage fluctuation.

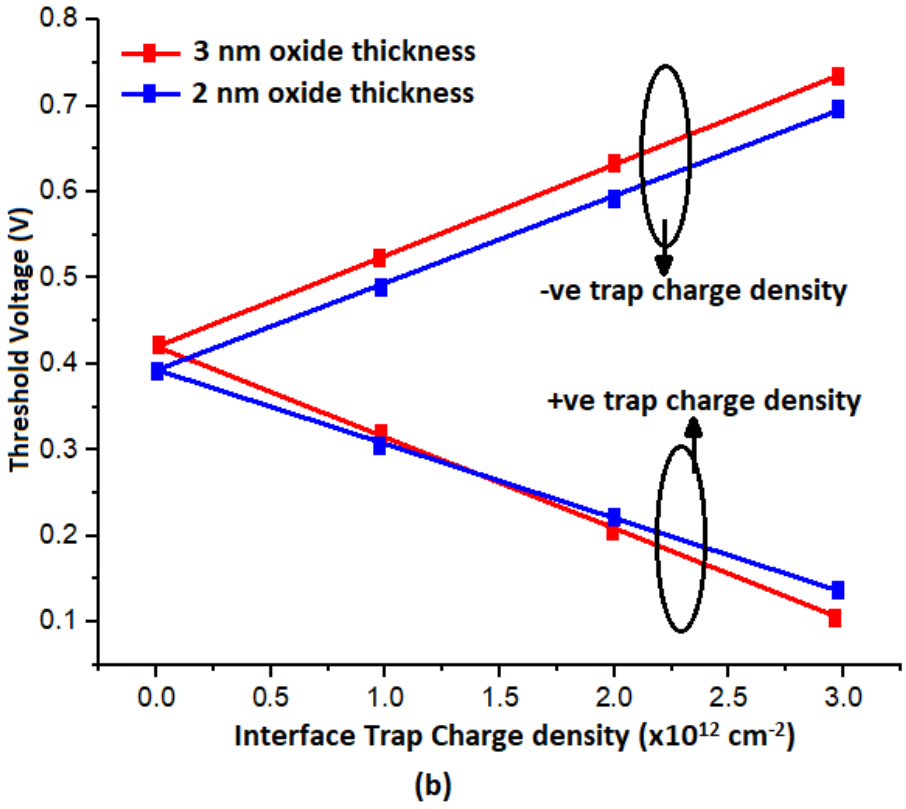


Fig. 5.4(b): Profile of variations of Threshold voltage vs. interface trap charge densities for two distinct oxide thicknesses.

A comparison of the performance of several device-based RADFET dosimeters was done in Fig. 5.4(c). As sensors, the study took into account the proposed C-S JLDG MOSFET, JL DG MOSFET, DG MOSFET and a Bulk MOSFET. The threshold voltage variations are extracted for radiation doses of *zero*, ±1x10^{12}/cm^2, ±2x10^{12}/cm^2, and ±3x10^{12}/cm^2. Sufficiently

lesser threshold voltage with a higher shift in voltage is observed for our proposed device compared to other ones.

The authors paid attention to the impact of the scalability of the core thickness over the sensitivity performance of the proposed dosimeter. Fig. 5.4(d) shows the threshold voltage profiles against the core thickness where the shell-doping concentration (N_d) is considered the third parameter. Non-linear characteristics of the threshold voltage shift are shown in the figure against the core thicknesses, where the V_{th} increases with the increase of core thickness with $N_d = 5\text{x}10^{18}/\text{cm}^3$.

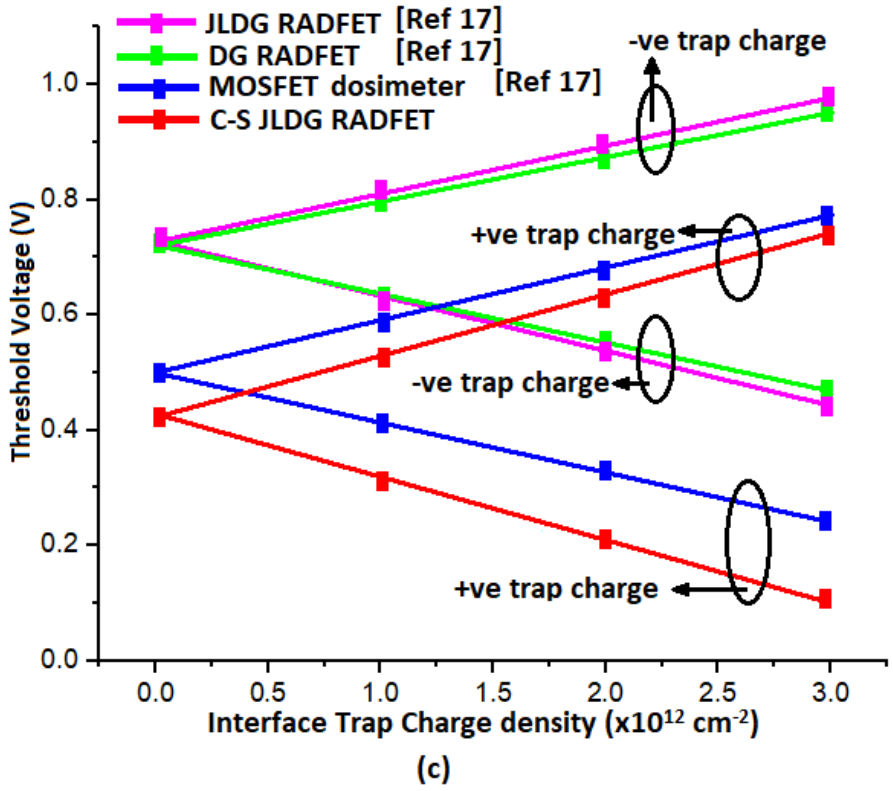


Fig. 5.4(c): Comparison of variations of Threshold voltage profile vs. interface trap charge densities for different devices under consideration in the article.

In Fig. 5.4(e), the same study is conducted for the shell-doping concentration of $2\text{x}10^{19}/\text{cm}^3$. Although the nature of the features shown in this figure is the same as before, the threshold voltage is modulated for a wide range of values by the core thickness and shell doping. Therefore, the sensitivity of the proposed dosimeter can easily be tuned from case to case by varying the core thickness with the shell-doping concentration depending upon the

application field. Therefore, it is a unique property of our proposed C-S JLDG RADFET, not reported earlier in any literature.

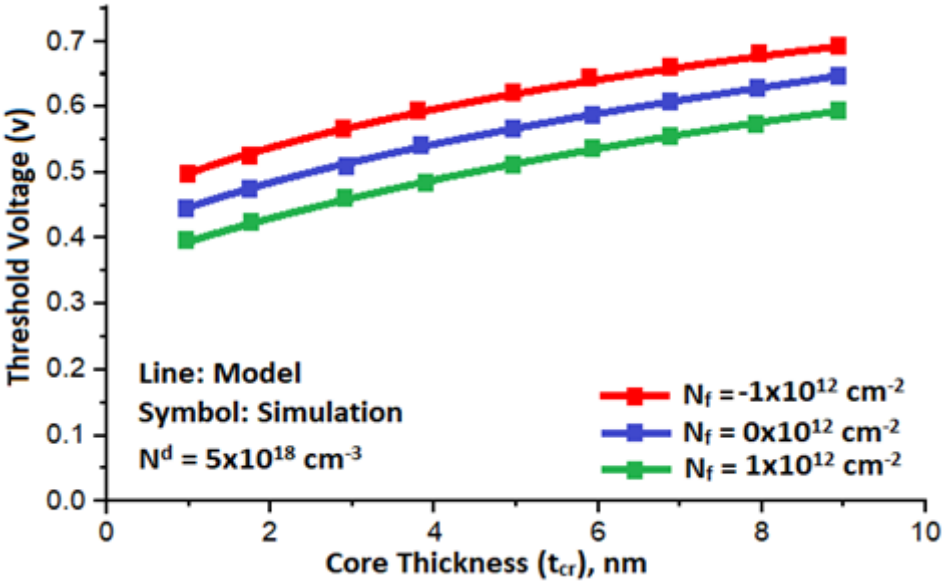


Fig. 5.4(d): Threshold voltage variation profile with N_d doping at 5 x 10^{18}/cm^3 in the shell.

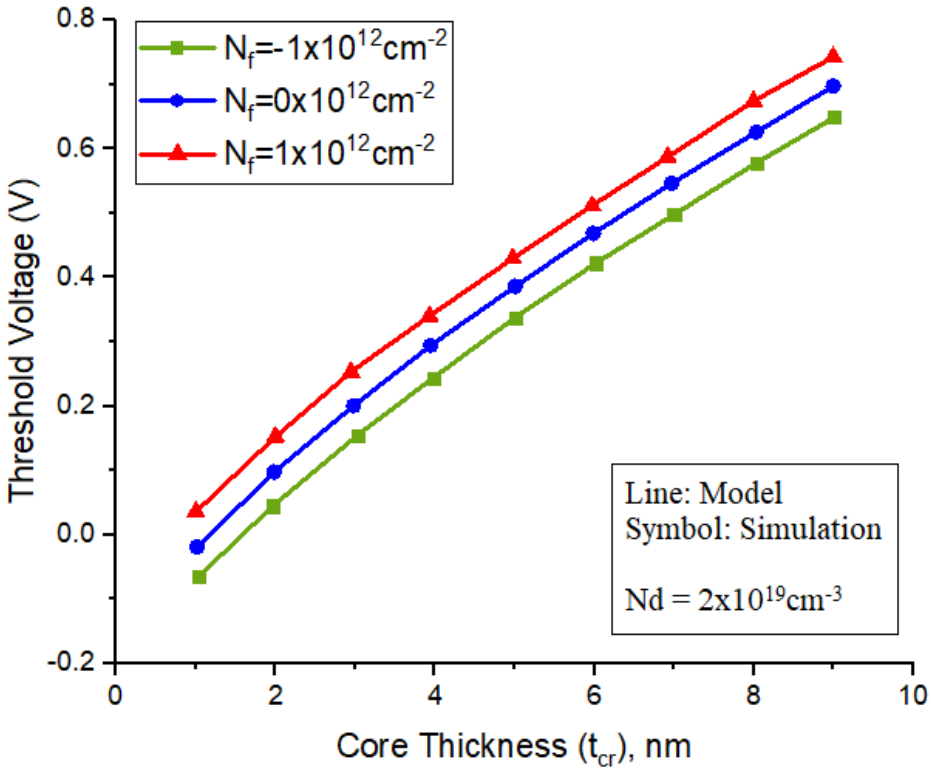


Fig. 5.4(e): Profile of changes in threshold voltage in relation to core thickness using the Nd=2x10^{19}/cm^3 shell doping.

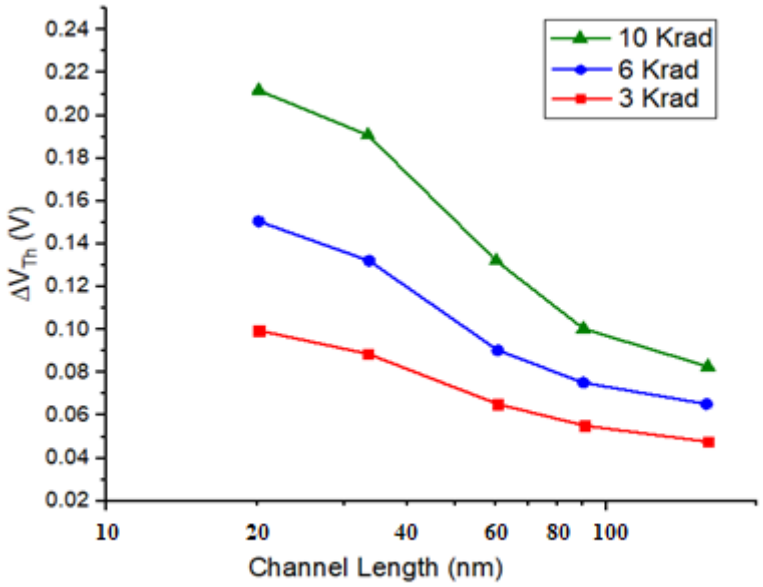


Fig. 5.4(f): Profile showing the threshold voltage shift for devices with varied gate lengths under the influence of radiation doses.

The relationship between the device's channel length and threshold voltage (Vth) for various radiation doses is shown in Fig. 5.4(f). The simulations are conducted for radiation doses of 3Krad, 6Krad, and 10Krad with varied channel lengths from 20nm to 150 nm, and the results are plotted in semi-log graphical coordinates. The nature of shift-in voltage (ΔV_{th}) is observed in the figure. The short-channel device's threshold voltage degradation, which results in a higher shift and a more sensitive device, is also noted at the same time.

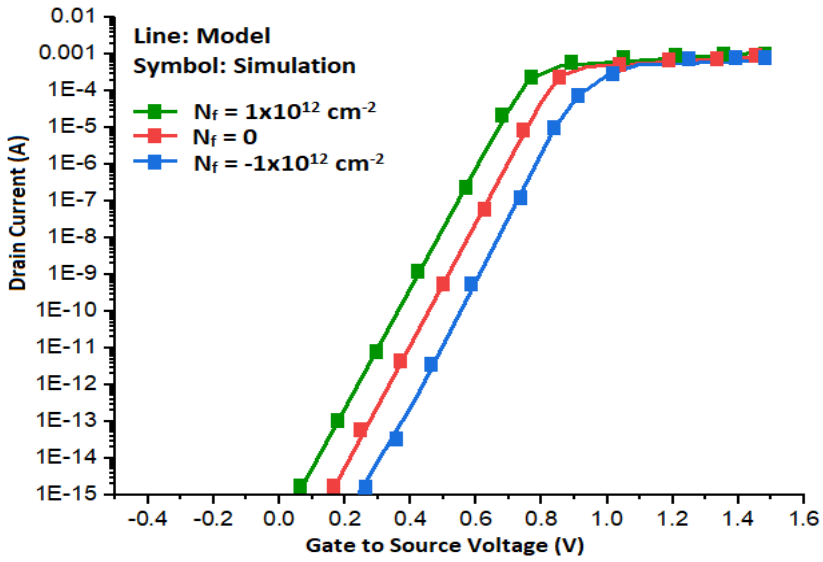


Fig. 5.5(a): I_D – V_{GS} characteristics of C-S JLDG MOSFET for negative and positive trapped charge concentrations (l_g=60nm, t_{Si}=10nm, t_{cr}=8nm, t_{ox}=2nm, N_d=5x10^{18}cm^{-3})

Through the use of the provided Fig. 5.5(a) – (c), the transfer characteristics of the suggested device under the influence of absorbed radiation are studied. The test device's channel length is 60 nm, the drain voltage is 0.5 V, and the simulation's gate voltage sweep ranges from 0 to 1.5 V.

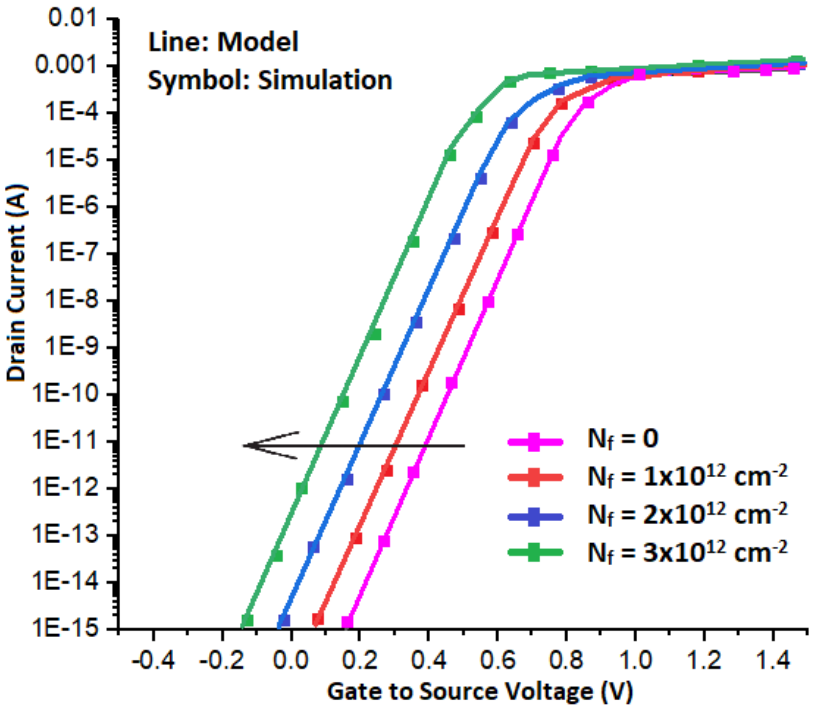


Fig. 5.5(b): I_D – V_{GS} characteristics of C-S JLDG MOSFET with variation of positive trapped charge concentrations (l_g=60nm, t_{Si}=10nm, t_{cr}=8nm, t_{ox}=2nm, N_d=5x10^{18}cm^{-3})

The drain current behavior with interface trap charge density of ±1x10^{12}/cm^2 is compared against the same with *zero* density trap charges in Fig. 5.5.

The device's barrier potential is decreased by the negative trapped charge, raising the threshold voltage. In contrast, as was discussed in the preceding section, the induced positive charges cause a decrease in the threshold voltage. Therefore, Fig. 5.5(a) represents the exact nature of current characteristics with only a change in threshold voltage, the point of voltage from which the current rises exponentially, owing to the polarity of the induced trapped charges.

The transfer properties of the aforementioned device under the impact of positive and negative trapped charge densities are explored in Figs. 5.5(b) and (c). A step increase of positive interface charge densities compelled to reduce the threshold voltage towards more

negative values. On the contrary, the induced negative interface charge densities yielded a rise in threshold voltage towards more positive values, depicted in the figures.

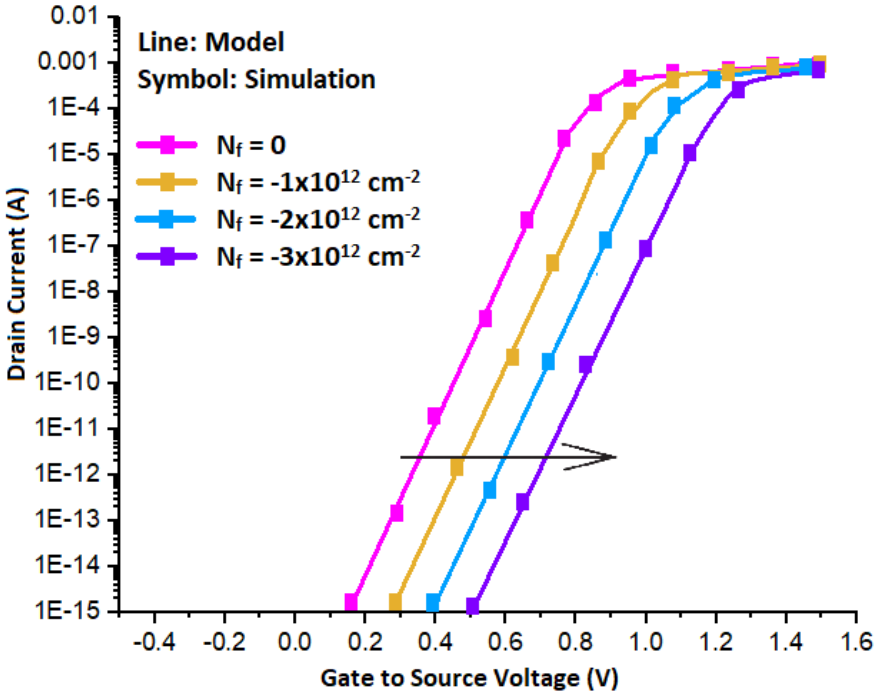


Fig. 5.5(c): I_D – V_{GS} characteristics of C-S JLDG MOSFET with variation of negative trapped charge concentrations (l_g=60nm, t_{Si}=10nm, t_{cr}=8nm, t_{ox}=2nm, N_d=5x10^{18}cm^{-3}).

The ON/OFF current ratio of the suggested device is shown in Fig. 5.6 as a measure of channel length. The study is conducted for 30nm to 100nm channel length, and results are plotted in a semi-log graph paper. An average I_{ON}/I_{OFF} ratio of about 10^{13} found for the device is entirely satisfactory, with its highest peak at 55nm channel length. Moreover, the average subthreshold swing of the device is 0.41 V. Thus, the overall electrical behavior of the proposed device justifies its potentiality in sensor applications and rugged reliability as well.

A comparison of the suggested CS JLDG MOSFET's sensitivity to that of JLDG MOSFET and Conventional Bulk MOSFET as dosimeters previously published in literature [5.11] is driven by Fig. 5.7. Each structure's sensitivity to absorbed dosages followed a linear relationship. This is also true of our suggested structure. Instead, the CS JLDG RADFET shows greater sensitivity throughout a large dose range, from 3 Krad to 3 Krad, without degrading device-level performance. Compared to the JLDG RADFET (S*ensitivity* = 1.92mV/Gy) and MOSFET dosimeter (S*ensitivity* = 1.68mV/Gy), our proposed sensor (highest S*ensitivity* of 2.02mV/Gy) emerged as a promising contender in the dosimetry applications.

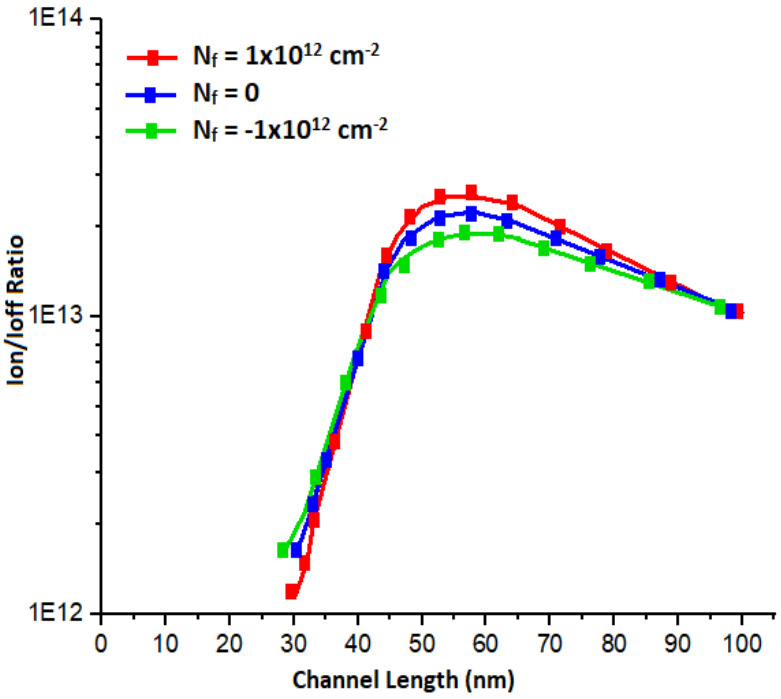


Fig. 5.6: I_{ON}/I_{OFF} ratio of the suggested device for various trap charge concentrations and channel lengths

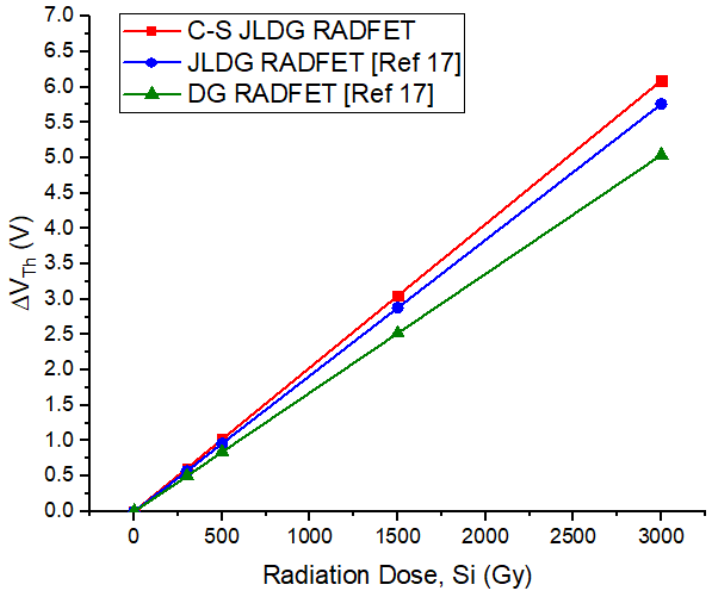


Fig. 5.7: Threshold voltage-shift profiles for the C-S JLDG RADFET (Proposed Structure), JLDG RADFET [5.17], DG RADFET [5.17], and calibrated data for the DDGAA RADFET [5.29] and Single gate RADFET [5.29] were compared against absorbed radiation doses

A table, Table 5.2 is constructed to carry out a comparative study amongst the reported MOSFET-based RADFET structures. The subthreshold swing, I_{ON}/I_{OFF} current ratio, threshold voltage, and sensitivity are regarded as the performance parameters.

Table 5.2: Comparison of the Performance of Various RADFET Dosimeters

Features	**DG RADFET [5.11]**	**JLDG RADFET [5.11]**	**CS-JLDG RADFET**
I_{ON}/I_{OFF}	$1.5x10^{9}$	$3.5x10^{12}$	$6.29x10^{12}$
SS (mV/dec)	60.4	59.7	55.6
V_{th} (V)	0.83	0.86	0.41
S (mV/Gy)	1.68	1.92	2.03

The proposed CS-JLDG RADFET exhibits superior performances compared to other contemporary dosimeters. First, the highest I_{ON}/I_{OFF} ratio order of 10^{12} is suitable for any low-power application. The subthreshold swing and the device's threshold voltage are reasonably low, empowering the structure promising for high-performance digital application. Finally, the sensitivity figure of the proposed RADFET is excellent in the similar category of dosimeters.

The proposed work has been expanded by the suggestion of a read-out circuit for the proposed CS-JLDG MOSFET-based dosimeter, which is primarily needed to measure the threshold voltage of the device. In a typical MOSFET, the initial gate voltage exhausted the mobile charges, preventing any real current from flowing across the channel. However, when the gate voltage increased and reached the threshold voltage, the channel progressively switched from the depletion-mode to the strong-inversion mode via weak inversion. As a result, the drain current flows through the channel, turning on the gadget. The V_{GS} - V_{DS} connection defines two operating areas of the on-state MOSFET. The first is the ($V_{DS} \leq V_{GS} - V_T$) linear region, while the second is the ($V_{DS} \geq V_{GS} - V_T$) saturation region [5.17]. In our published work, we proposed a diode-connected MOSFET configuration where the device's gate and source terminal are shorted to have $V_{DS} = V_{GS} = V_{OUT}$. To deliver drain current, the gate-source common terminal is connected to a variable current source (I_{DS}). Consequently, the device's transfer characteristics can be used to directly compute the threshold voltage ($I_{DS} – V_{GS}$).

One well-liked technique for determining VT from the I_{DS} - V_{GS} curve is linear extrapolation. The mathematical computation must follow these guidelines:

(i) derive $g_m = \frac{\partial\sqrt{I_{DS}}}{\partial V_{GS}}$, which the g_m-V_{GS} curve can be calculated.

(ii) At point V_{GSx}, let's say, the tangent to the g_m-V_{GS} curve intersects the V_{GS} axis.

(iii) In the saturation area, V_T is exactly equal to V_{GSx}.

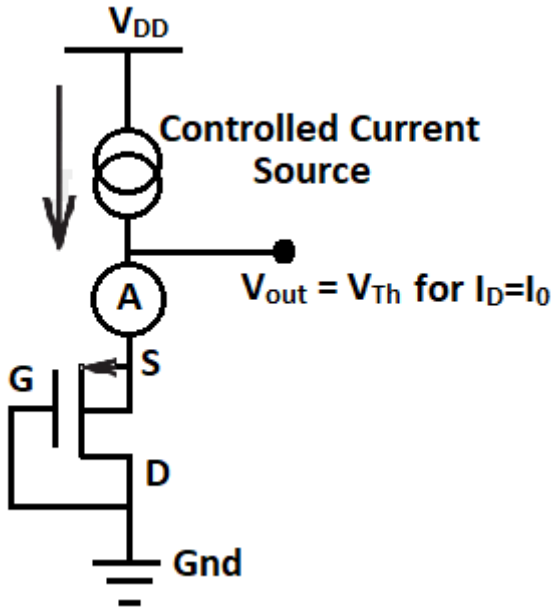


Fig. 5.8: Circuit design for the C-S JLDG RADFET's sensitivity measurement in terms of V_{Th}.

References

5.1. Biswas, M., Dey, A. & Subir Kumar Sarkar "Polyaniline Based Field Effect Transistor for Humidity Sensor." Silicon (2022**).** https://doi.org/10.1007/s12633-021-01594-3

5.2. Priyanka Saha and Subir Kumar Sarkar, "Analytical modeling of Ion sensitive broken gate TFET for pH sensing applications", IEEE Sensors Letters, Vol. 4, No.7, pp. 1-4, July 2020.

5.3. Subhashis Roy, Anup Dey, Bikram Biswas, Ayan Bhattacharya, Sudhabindu Ray, and Subir Kumar Sarkar, "Comparison of Annealing Temperature and Heterostructure Effects on ZnO Based Thin Film H2 Sensor", Sensor Letters, ASP, Vol. 17, No. 7, pp.505–510, July 2019.

5.4. D. Sen, P. Saha and Subir Kumar Sarkar, "Analysis of Dual Metal Gate Engineered SiGe/Si TFET based Biosensor: A Dielectric Modulation Approach," 2021 Devices for Integrated Circuit (DevIC), 2021, pp. 421-424, doi: 10.1109/DevIC50843. 2021. 9455889.

5.5. Priyanka Saha, Dinesh Kumar Dash and Subir Kumar Sarkar**,** "Nanowire Reconfigurable FET as Biosensor: Based on Dielectric Modulation Approach", Solid State Electronics, Elsevier, doi. 10.1016/j.sse.2019.107637, August 2019

5.6. Priyanka Saha, Pritha Banerjee, Dinesh Kumar Dash and Subir Kumar Sarkar, "Interface Trap Charge Induced Threshold Voltage Modeling of WFE High-K SOI MOSFET", Silicon, Springer, vol. 12, pp.2893-2900, doi.org/10.1007/s12633-020-00386-5, Jan 2020

5.7. Saheli Sarkhel, Navjeet Bagga and Subir Kumar Sarkar ,"A compact analytical model of binary metal alloy silicon-on-nothing (BMASON) tunnel FET with interface trapped charges", in Journal of Computational Electronics, Springer, DOI 10.1007/s10825-017-1030-7, July 2017.

5.8. Priyanka Saha, Pritha Banerjee, Dinesh Kumar Dash and Subir Kumar Sarkar, "Impact of trapped interface charges on short channel characteristics of WFE High-K SOI MOSFET" in 3rd International Conference, 2019 Devices for Integrated Circuits (DevIC)", Kalyani Government Engineering College, West Bengal, India, March 23rd-24th, 2019.

5.9. Abir Jana, Komal Kumari, Anup Dey, P.S. SreenivasReddy, Bikram Biswas, Bhaskar Gupta, Subir Kumar Sarkar, "Fabrication of P-N Heterojunction Based MoS2 Modified CuPc Nanoflowers for Humidity Sensing", Sensors and Actuator A, Elsevier, doi.org/10.1016/j.sna.2019.111574, August 2019

5.10. Sen, D., De, A., Goswami, B., Shee, Subir Kumar Sarkar, "Noise immune dielectric modulated dual trench transparent gate engineered MOSFET as a label free biosensor: proposal and investigation." J Comput Electron (2021). https://doi.org/10.1007/s10825-021-01780-x.

5.11. Avashesh Dubey, Ajay, Rakhi Narang, Manoj Saxena, and Mridula Gupta, "Modeling and Simulation of Junctionless Double Gate Radiation Sensitive FET (RADFET) Dosimeter", IEEE TRANSACTIONS ON NANOTECHNOLOGY, VOL. 17, NO. 1, JANUARY 2018.

5.12. S. Carbonetto, M. Echarri, J. Lipovetzky, M. Garcia–Inza and A. Faigón, "Temperature-Compensated MOS Dosimeter Fully Integrated in a High-Voltage 0.35 μm CMOS Process," in IEEE Transactions on Nuclear Science, vol. 67, no. 6, pp. 1118-1124, June 2020, doi: 10.1109/TNS.2020.2966567.

5.13. G. Biasi et al., "On the Combined Effect of Silicon Oxide Thickness and Boron Implantation Under the Gate in MOSFET Dosimeters," in IEEE Transactions on Nuclear Science, vol. 67, no. 3, pp. 534-540, March 2020, doi: 10.1109/TNS.2020.2971977.

5.14. B. O'Connell, C. Conneely, C. McCarthy, J. Doyle, W. Lane, and L. Adams, "Electrical performance and radiation sensitivity of stacked PMOS dosimeters under bulk bias control," *IEEE Trans. Nucl. Sci.*, vol. 45, no. 6, pp. 2689–2694, Dec. 1998.

5.15. G. Risti´c, A. Jakˇsi´c, and M. Pejovi´c, "pMOS dosimetric transistors with two-layer gate oxide," *Sens. Actuators A, Phys.*, vol. 63, pp. 129–134, 1997.

5.16. A. Enright, "The development of dual dielectrics in PMOS dosimeters," Master Thesis, National University of Ireland, Cork, Ireland, 1996.

5.17. M. Meguellati and F. Djeffal, "New dual-dielectric gate all around (DDGAA) RADFET dosimeter design to improve the radiation sensitivity," *Nucl. Instrum. Methods Phys. Res. Sect. A*, vol. 683, pp. 24–28, Aug. 2012.

5.18. W. Meile, J. Xiaoshi, C. Rongyan, L. Xi, and J.-H. Lee, "Simulation study on short channel double gate junctionless field-effect transistor," *J. Semicond.*, vol. 34, no. 3, 2013, Art. no. 034004.

5.19. Arpan De, Saptarshi Maiti and Subir Kumar Sarkar "Analytical Modelling of Symmetric Gate Underlap Quadruple Gate Multichannel Junctionless MOSFET Biosensor", Silicon, (https://doi.org/10.1007/s12633-021-01415-7).

5.20. Dipanjan Sen, Bijoy Goswami, Anup Dey, Priyanka Saha and Subir Kumar Sarkar, "Impact of Self-Heating and Nano-Gap Filling Factor on AlGaAs/GaAs Junction-Less DG-MOSFET Based Biosensor for Early Stage Diagnostics" , IEEE Region 10 Symposium (TENSYMP), 5-7th June ,2020, Dhaka, Bangladesh.

5.21. Subhramita Basak, Priyanka Saha, Subir Kumar Sarkar, "A Semi 2D Analytical Vth Model Junctionless Double Gate Nanoscale Silicon on Nothing (JLDG- SON) MOSFET", IEEE Proceedings of International Conference on Recent Advances in Engineering and Computational Sciences, March, 2014.

5.22. S. Mukhopadhyay, D. Sen, B. Goswami and Subir Kumar Sarkar**,** "Performance Evaluation of Dielectrically Modulated Extended Gate Single cavity InGaAs/Si HTFET based Label-free Biosensor Considering Non-ideal Issues," in IEEE Sensors Journal, vol. 21, issue 4, pp. 4739-4746, Feb. 2021.

5.23. Y.-J. Lee *et al.*, "High performance poly Si junctionless transistors with sub-5 nm conformally doped layers by molecular monolayer doping and microwave incorporating CO2 laser annealing for 3D stacked ICs applications," in *IEDM Tech. Dig.*, Dec. 2015, pp. 6.2.1–6.2.4, doi: 10.1109/IEDM.2015.7409638.

5.24. Nivedita Jaiswal and Abhinav Kranti, "Modeling Short-Channel Effects in Core–Shell Junctionless MOSFET," IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 66, NO. 1, JANUARY 2019.

5.25. N. Jaiswal and A. Kranti, "A Model for Gate-Underlap-Dependent Short- Channel Effects in Junctionless MOSFET," in IEEE Transactions on Electron Devices, vol. 65, no. 3, pp. 881-887, March 2018, doi: 10.1109/TED.2018.2796602.

5.26. Holmes-Siedle, Andrew G., The Use of RADFETS in Radiation Dose Measurement: Report on Three Lots Prepared for the U.S. Army. Final rept. 18 Jun 1987-18 Sep 1989; https://apps.dtic.mil/ sti/ citations/ ADA214634.

5.27. A. K. Ward, N. Blower, L. Adams, J. Doutreleau, A. Holmes-Sidle, M. Pignol, J. J. BemeronandM. Mehlem. "The Meteosat P2 Radiation Effects Experiment". Acta Astronautica, Vol 22, October 1989.

5.28. A. Holmes-Sidle and L. Adams. "RADFET. A review of the use of MOS Devices as Integrating Dosimeters". International Journal of Radiation Physics and Chemistry. Vol 28. No 2. pp 235-244. February 1986.

5.29. A. Holmes-Sidle. "Report on Proton response in CCDs". BNF-Fulmer Contract Report R1320/1. June 1991.

5.30. L. Adams, E. J. Daly, R. Harboe-Sorensen, A. G. Holmes-Siedle, A. K. Ward and R. A. Bull, "Measurements of SEU and total dose in geostationary orbit under normal and solar flare conditions," in IEEE Transactions on Nuclear Science, vol. 38, no. 6, pp. 1686-1692, Dec. 1991, doi: 10.1109/23.124163.

5.31. M. Buehler, A. Holmes-Siedle, C. Caines, C. Carmichael and D. Martin, "Stacked p-FET dosimeter for the STRV-2 MWIR detector," in IEEE Transactions on Nuclear Science, vol. 43, no. 6, pp. 2679-2686, Dec. 1996, doi: 10.1109/23.556853.

5.32. A. Kelleher, M. O'Sullivan, J. Ryan, B. O'Neill and W. Lane, "Development of the radiation sensitivity of PMOS dosimeters," in IEEE Transactions on Nuclear Science, vol. 39, no. 3, pp. 342-346, June 1992, doi: 10.1109/23.277514.

5.33. A. Kelleher, N. McDonnell, B. O'Neill, W. Lane and L. Adams, "Investigation into the re-use of PMOS dosimeters," in IEEE Transactions on Nuclear Science, vol. 41, no. 3, pp. 445-451, June 1994, doi: 10.1109/23.299782.

5.34. A. Kelleher, W. Lane and L. Adams, "A design solution to increasing the sensitivity of pMOS dosimeters: the stacked RADFET approach," in IEEE Transactions on Nuclear Science, vol. 42, no. 1, pp. 48-51, Feb. 1995, doi: 10.1109/23.364881.

5.35. A. Kelleher, W. Lane and L. Adams, "Investigation of on-chip high temperature annealing of PMOS dosimeters," in IEEE Transactions on Nuclear Science, vol. 43, no. 3, pp. 997-1001, June 1996, doi: 10.1109/23.510746.

5.36. B. O'Connell, A. Kelleher, W. Lane and L. Adams, "Stacked RADFETs for increased radiation sensitivity," in IEEE Transactions on Nuclear Science, vol. 43, no. 3, pp. 985-990, June 1996, doi: 10.1109/23.510744.

5.37. B. O'Connell, C. Conneely, C. McCarthy, J. Doyle, W. Lane and L. Adams, "Electrical performance and radiation sensitivity of stacked PMOS dosimeters under bulkbias control," in IEEE Transactions on Nuclear Science, vol. 45, no. 6, pp. 2689-2694, Dec. 1998, doi: 10.1109/23.736516.

5.38. J. R. Schwank, S. B. Roeske, D. E. Beutler, D. J. Moreno and M. R. Shaneyfelt, "A dose rate independent pMOS dosimeter for space applications," in IEEE Transactions on Nuclear Science, vol. 43, no. 6, pp. 2671-2678, Dec. 1996, doi: 10.1109/23.556852.

5.39. N. G. Tarr, G. F. Mackay, K. Shortt and I. Thomson, "A floating gate MOSFET dosimeter requiring no external bias supply," RADECS 97. Fourth European Conference on Radiation and its Effects on Components and Systems (Cat. No.97TH8294), 1997, pp. 277-281, doi: 10.1109/RADECS.1997.698909.

5.40. A. Jaksic, G. Ristic, M. Pejovic, A. Mohammadzadeh, C. Sudre and W. Lane, "Gamma-ray irradiation and post-irradiation responses of high dose range RADFETs," in IEEE Transactions on Nuclear Science, vol. 49, no. 3, pp. 1356-1363, June 2002, doi: 10.1109/TNS.2002.1039667.

5.41. A. Haran, A. Jaksic, N. Refaeli, A. Eliyahu, D. David and J. Barak, "Temperature effects and long term fading of implanted and unimplanted gate oxide RADFETs," in IEEE

Transactions on Nuclear Science, vol. 51, no. 5, pp. 2917-2921, Oct. 2004, doi: 10.1109/TNS.2004.835065.

5.42. A. Haran and A. Jaksic, "The role of fixed and switching traps in long-term fading of implanted and unimplanted gate oxide RADFETs," in IEEE Transactions on Nuclear Science, vol. 52, no. 6, pp. 2570-2577, Dec. 2005, doi: 10.1109/TNS.2005.860705.

5.43. Cheung, T., Butson, M.J. & Yu, P.K.N. Energy dependence corrections to MOSFET dosimetric sensitivity. Australas. Phys. Eng. Sci. Med. 32, 16–20 (2009). https://doi.org/ 10.1007/ BF03178623.

5.44. M. R. Shaneyfelt et al., "An Embeddable SOI Radiation Sensor," in IEEE Transactions on Nuclear Science, vol. 56, no. 6, pp. 3372-3380, Dec. 2009, doi: 10.1109/TNS.2009.2033474.

5.45. M. Wind, P. Beck and A. Jaksic, "Investigation of the Energy Response of RADFET for High Energy Photons, Electrons, Protons, and Neutrons," in IEEE Transactions on Nuclear Science, vol. 56, no. 6, pp. 3387-3392, Dec. 2009, doi: 10.1109/TNS.2009.2033060.

5.46. J. Lipovetzky, A. Holmes -Siedle, M. Garcia Inza, S. Carbonetto, E. Redin and A. Faigon, "New Fowler-Nordheim Injection, Charge Neutralization, and Gamma Tests on the REM RFT300 RADFET Dosimeter," in IEEE Transactions on Nuclear Science, vol. 59, no. 6, pp. 3133-3140, Dec. 2012, doi: 10.1109/TNS.2012.2222667.

5.47. J. Hofman, A. Holmes-Siedle, R. Sharp and J. Haze, "A Method for In-Situ, Total Ionising Dose Measurement of Temperature Coefficients of Semiconductor Device Parameters," in IEEE Transactions on Nuclear Science, vol. 62, no. 6, pp. 2525-2531, Dec. 2015, doi: 10.1109/TNS.2015.2498948.

5.48. M. S. Martínez-García et al., "Accuracy Improvement of MOSFET Dosimeters in Case of Variation in Thermal Parameters," in IEEE Transactions on Nuclear Science, vol. 62, no. 2, pp. 487-493, April 2015, doi: 10.1109/TNS.2015.2404344.

5.49. M. M. Pejovic, "Application of p-Channel Power VDMOSFET as a High Radiation Doses Sensor," in IEEE Transactions on Nuclear Science, vol. 62, no. 4, pp. 1905-1910, Aug. 2015, doi: 10.1109/TNS.2015.2456211.

5.50. Ashrafi, S., Eslami, B. Investigation of sensitivity and threshold voltage shift of commercial MOSFETs in gamma irradiation. *NUCL SCI TECH* **27,** 144 (2016). https://doi.org/10.1007/s41365-016-0149-8.

5.51. J. Hofman, A. Jaksic, R. Sharp, N. Vasovic and J. Haze, "In-Situ Measurement of Total Ionising Dose Induced Changes in Threshold Voltage and Temperature Coefficients of RADFETs," in IEEE Transactions on Nuclear Science, vol. 64, no. 1, pp. 582-586, Jan. 2017, doi: 10.1109/TNS.2016.2630275.

5.52. A. Tang, Y. Kim and M. -C. F. Chang, "Logic-I/O Threshold Comparing γ-Dosimeter in Radiation Insensitive Deep-Sub-Micron CMOS," in IEEE Transactions on Nuclear Science, vol. 63, no. 2, pp. 1247-1250, April 2016, doi: 10.1109/TNS.2016.2528219.

5.53. M. Kulhar, K. Dhoot and A. Pandya, "Gamma Dose Rate Measurement Using RadFET," in IEEE Transactions on Nuclear Science, vol. 66, no. 10, pp. 2220-2228, Oct. 2019, doi: 10.1109/TNS.2019.2942955.

5.54. K. Tamersit, "Performance Assessment of a New Radiation Dosimeter Based on Carbon Nanotube Field-Effect Transistor: A Quantum Simulation Study," in IEEE Sensors Journal, vol. 19, no. 9, pp. 3314-3321, 1 May1, 2019, doi: 10.1109/JSEN.2019.2894440.

5.55. G. Biasi et al., "On the Combined Effect of Silicon Oxide Thickness and Boron Implantation Under the Gate in MOSFET Dosimeters," in IEEE Transactions on Nuclear Science, vol. 67, no. 3, pp. 534-540, March 2020, doi: 10.1109/TNS.2020.2971977.

5.56. Meddour, A., Meddour, F. & Drid, S. Performance Enhancement of Double Graphene-Gate Junctionless Radiation Sensitive FET (DGG JL RADFET) Dosimeter: Analytical Modeling and Design Optimization. *Silicon* (2021). https://doi.org/10.1007/s12633-021-01087-3.

5.57. Tiya Dey Malakar, Suman Basu, Partha Bhattacharyya and Subir Kumar Sarkar, "Computationally Comprehensive and Efficient Generalized Poisson's Solution for Better Nanoscale SOI MOSFET", Sixth International Conference on Computational Intelligence and Communication Networks, Bhopal, 14-16 Nov., 2014.

5.58. Navjeet Bagga, Saheli Sarkhel and Subir Kumar Sarkar " Exploring the Asymmetric Characteristics of a Double Gate MOSFET with Linearly Graded Binary Metal Alloy Gate Electrode for Enhanced Performance ",IETE Journal Of Research, DOI 10.1080/03772063.2016.1176542,April,2016

5.59. Priyanka Saha, Subir Kumar Sarkar, "Drain current modeling of proposed dual material elliptical Gate-All-Around heterojunction TFET for enhanced device performance", Superlattices and Microstructures, Volume 130, 2019, Pages 194-207, ISSN 0749-6036.

5.60. Saheli Sarkhel, Navjeet Bagga and Subir Kumar Sarkar, "Compact 2D Modeling and Drain Current Performance Analysis of a Work Function Engineered Double Gate Tunnel Field Effect Transistor." Journal of Computational Electronics, Springer, Vol. 15, Issue 1, pp. 104-114, March 2016.

5.61. Priyanka Saha and Subir Kumar Sarkar,"Drain current characterization of Dielectric Modulated Split Gate TFET for bio-sensing application", Materials Science in Semiconductor Processing, Elsevier, vol. 124, 105598,Nov. 2020.

5.62. Disha Bhattacharjee, Bijoy Goswami, Dinesh Kumar Dash, Ayan Bhattacharya and Subir Kumar Sarkar," Analytical Modelling and Simulation of Drain Doping Engineered Splitted Drain Structured TFET and its Improved Performance in Subduing Ambipolar Effect", IET Circuits, Devices & Systems, DOI: 10.1049/iet-cds.2018.5261, May 2019

5.63. Priyanka Saha and Subir Kumar Sarkar, "Explicit threshold voltage modeling insight for short channel characterization of WFE Elliptical GAA strained-Si MOSFET", Journal of Electronic Materials, Springer, vol. 49, pp.7486-7494, (DOI: 10.1007/s11664-020-08503-1, September 2020.

5.64. Priyanka Saha , Pritha Banerjee, Dinesh Kumar Dash and Subir Kumar Sarkar,"Interface Trap Charge Induced Threshold Voltage Modeling of WFE High-K SOI MOSFET", Silicon, Springer,vol. 12, pp.2893-2900, doi.org/10.1007/s12633-020-00386-5, Jan 2020

5.65. A. Jaksic, G. Ristic, M. Pejovic, A. Mohammadzadeh, C. Sudre and W. Lane, "Gamma-ray irradiation and post-irradiation responses of high dose range RADFETs," in IEEE Transactions on Nuclear Science, vol. 49, no. 3, pp. 1356-1363, June 2002, doi: 10.1109/TNS.2002.1039667.

5.66. ATLAS: 2-D Device Simulator, SILVACO Int., Santa Clara, CA, USA, 2013.

5.67. J. R. Schwank et al., "Radiation Effects in MOS Oxides," in IEEE Transactions on Nuclear Science, vol. 55, no. 4, pp. 1833-1853, Aug. 2008, doi: 10.1109/TNS.2008.2001040.

5.68. Lutz, G., Klanner, R. (2020). Solid State Detectors. In: Fabjan, C., Schopper, H. (eds) Particle Physics Reference Library. Springer, Cham. https://doi.org/10.1007/978-3-030-35318-6_5.

CHAPTER 6

Performance Comparison of Proposed PSO Variant with Firefly Algorithm in Optimization of Global Routing

6.1. Introduction

With the advancement of VLSI technology, the downscaling of transistors leads to complex design, architecture and fabrication processes of modern Integrate Circuits (IC). In addition, it drastically increases the packaging density and consequently the routing complexity. In the sub-nanometer regime, electronic circuits' performance has been dominated by interconnect delay and the existing gate delay as well. Various surveys pointed out that the gate delay, local interconnect delay, global interconnect delay with and without repeaters are prime concerns regarding circuits' performance. It is also noted that below 250nm technology node gives rise to the interconnect delay over the gate delay. Therefore, interconnect delay plays a significant role in the overall system's performance.

In the VLSI design flow, routing [6.1, 6.2] takes place after floor planning and placement during the Physical Design phase. The total routing of a system materializes in two steps: global routing [6.3, 6.4] followed by detailed routing. Global routing optimizes the total interconnect lengths. This optimization problem is modeled through the famous Rectilinear Minimal Stainer Tree (RMST) problem [6.5] of graph theory, an NP-complete problem that can hardly be solved in a polynomial-time frame. Therefore, swarm intelligence [6.6-6.9], a meta-heuristic approach [6.10, 6.11], is used to address this problem. This approach was first introduced by G. Beny and J. Wang [6.12] in 1989. The social behavior of natural agents like a flock of birds, school of fish, hard of bees, and ants was modeled to achieve some global optima within a reasonable time frame for any stochastic optimization problems. Two such popular meta-heuristics algorithms are PSO (Particle Swarm Optimization) [6.13] and FA (Firefly Algorithm) [6.14-6.17].

In this paper-work, two algorithms based on weighted PSO have been proposed. The first one, the Self-Adaptive acceleration coefficient PSO (PSO-SAAC), acceleration coefficients are tuned for a local search and global search mechanism to enhance the property of the searching procedure and smooth converging rate. Furthermore, another novel approach is adopted where the concept of the genetic algorithm is hybridized with the PSO by including a component associated with a breading factor in the position update characteristic equation of PSO. In addition to the above two variants of PSO, PSO with constriction factor (PSO-C) are compared with the Firefly algorithm, the most recently introduced meta-heuristic, on a

common platform of optimization of VLSI global routing. Further, all the algorithms are tested in varied distribution topologies of terminal nodes on a defined search space.

6.2. Literature Survey

The pioneering work on Particle swarm Optimization is reported by Kennedy and Eberhart in the year of 1995. The authors, a social psychologist and an electrical engineer, introduced an optimizer to solve non-linear continuous functions [6.18]. The merit of the optimization lies in its simplicity and easy implementation with few lines of computer codes. It hardly requires any advanced mathematical operators and significant computational load, i.e., extensive memory and high speed. Previously, Reynolds [6.19] and Heppner and Grenander's [6.20] works were reported in simulating the synchronous behavior of the flock of birds moving towards a definite direction without colliding with each other. Moreover, E.O.Wilson, a sociobiologist [6.21], investigated the nature of fish schooling while searching for food. It was observed that birds and fishes control their physical movements while roaming for their food and mates. In humans, this nature is cognitive mear the adjustment of the physical proximity. Particle swarm optimization has a keen relationship with evolutionary computing. Instead, it lies somewhere in between genetic algorithms and evolutionary mechanisms. It is worthy to say it as a stochastic process. The optimization function, p_{best} and g_{best}, is close to the *crossover* function in genetics. The concept of the fitness function works like evolutionary algorithms.

A comparison between Particle Swarm Optimization (PSO) and Genetic algorithm (GA) was made by Eberhart and Shi in [6.22]. PSO, regarded as evolutionary computation, had been modeled by Kennedy and Eberhart [6.23, 6.24]. The proposed work emphasized the parameters-based performances improvement of both algorithms. PSO is attributed to optimizing the collision probabilities of a flock of birds roaming in a synchronizing manner. On the other hand, selection, crossover and mutation are foundations of GA. Therefore, an extensive analysis was performed to improve one algorithm's performance by sharing the virtue of the other one in the reported work.

Kennedy and Eberhart reported a modified Particle Swarm Optimization algorithm [6.25] applicable for discrete binary problem space. Many real-world problems can be modeled through discrete functions. They are set in a discrete space with a distinct and quantized level of variables. Moreover, combinatorial problems need to be implemented through floating point

systems. Altogether, binary two-valued functions were required as a component of optimizers in solving the problems stated above. The work assumed a hypercube as a search space where a particle's movement was limited between nearer nodes and furthest corners by hopping a number of bits. The velocity of a particle is a function of time varied with each iteration. The proposed model was tested through De Jong's (1995) suite of five test functions to evaluate the optimizer's performance. The tests were run 20 times with 20 populations and 6.0 Vmax, which revealed the binary model of PSO extremely flexible and robust.

Eberhart and Shi carried out a review work in 2001 [6.26] on the development, applications and resources of PSO from the perspective of engineering and computer science. Their report enlightened the potential application areas like human compulsion analysis, load stabilization in the power grid and optimization of the product mixture. The algorithm was built to find an optimized solution to any problem by modulating each particle's velocity to its g_{best} and p_{best} value with each time step. Moreover, each particle might move towards its best solution, l_{best}, by hopping through local topological neighborhood nodes. A magnificent work done by Clerc [6.27] described a constriction factor to achieve faster convergence. Inertia weight, another deciding factor defined by Eberhart and Shi [6.28] essentially required for tracking and optimizing dynamic systems. The proposed optimization model is efficient and popular due to its very few parameters to modulate in obtaining solutions.

A detailed study has been conducted [6.29] on the influence of topologies on the performance matrices of PSO. In general, PSO can be modeled as the trajectory vectors of each population element in a defined search space. The success of the model lies in finding global best or local best values, depending on the role of neighboring particles. The global best value is the best solution found by any population element, whereas two neighboring particles on either side (considering the ring topology) mainly influence the local best value. Studies found that the information flow in a social network gets dominated by a factor '*k,'* where *k* is the number of neighbors, and a clustering factor '*c*.' However, experiments found that the PSO algorithm is a function dependent tool, where population having fewer connections performs better in a multimodal environment. In contrast, populations with dense connections perform well in unimodal problem spaces. The reported work was carried out with heterogeneous populations having different topological characteristics.

Significant work was reported [6.30] on constructing a Particle Swarm Optimization model to control the Petri net (Time Petri net) and Multi-Agent system (MAS). A proposed TPN

comprises a set of contracts to be fulfilled among the Holonic manufacturing system (HMS) agents. Therefore, TPNs must be active to complete the processing of orders. Moreover, conflicts that occur due to a lack of resources need to be resolved by TPNs. Feasibility tests were conducted by accomplishing commitments to check the activeness of TPNs. Therefore, the use of planning and control concepts, on the one hand, and predictability & stability with flexibility & fault tolerance, on the other hand, are the keys to the successful order supply starting from manufacturing. Nevertheless, the proposed model of PSO is compatible with the logistics and scheduling problems in an aggressive environment and fruitfully delivered a solution platform for computer applications with PSO.

An adaptive PSO is reported [6.31] to optimize component placement in Printed Circuit Boards (PCBs). And at the same time, the problem includes assigning the types of components best fitted to the feeders. The work aimed to optimize the total traveling distance and, therefore, the total traveling time, including the time to change the head nozzles. The assembly time of PCBs got affected by two decisions : (i) allotment of reels on feeder racks' slots and (ii) sequencing the pick-&-palce (PAP) operation [6.32], which are NP-hard combinatorial problems of discrete types [6.33]. Moreover, assignment and sequencing are highly correlated and hardly be solved concurrently. Therefore, researchers considered these two different problems to solve. Therefore, to optimize the PCB assembly time and the scheduling time of multi-head PAPs, the authors introduced an Adaptive PSO (APSO) in three successive phases, viz. head allotments algorithm, reel grouping optimization followed by swarm intelligence. The proposed approach successfully minimizes the assembly time of components placement on the PCB board.

A noble binary PSO algorithm has been proposed [6.34] where the velocity vector has been redefined. The conventional PSO algorithm was formulated based on the updations of the velocity vector of each particle in a swarm. The vector was calculated based on the current velocity and the best position already explored by individual particles or by the influence of the g_{best} position achieved by the swarm itself. In binary PSO, respective particles' positions are represented by '0' and '1'. Then the changed positions are represented by the complements of previous position values. In the binary variant of PSO, the values that correspond to the particles' positions signify the probability that a particle may change its state or not. The proposed work redefined the particles' velocity value as the probability of changing the state of a particle from its previous state to a complementary state. This new interpretation refined

the rate of change of bits of particles. The modifications also include the previous direction and state in formulating the algorithm. The proposed approach experimented through suitable test benches finds satisfactory results.

A power network comprises a significant number of levels and parameters that may be considered a highly non-linear system with noise-induced uncertainties. The proposed work presented [6.35] a thorough survey of power system applications and optimization techniques based on the Particle Swarm Optimization algorithm. PSO is an evolutionary computational-based approach, hardly influenced by the non-linearity and size of the problem. Nevertheless, it can generate optimal solutions for many stochastic problems, where analytical computation may be next to impossible. Therefore, PSO might effectively be used in versatile areas of optimization problems of power systems. Moreover, the algorithm has certain advantages over other evolutionary techniques of the same class : (i) it possesses fewer parameters to tune, (ii) it involves flexible memory allocations, and (iii) it achieves solutions keeping the diversity of the swarm intact [6.36]. Therefore, the proposed work inferred a detailed review of the PSO algorithm, its foundation, topologies & varients, and its applications in the arena of optimization problems related to power systems.

Economic dispatch (ED) [6.37] is a pivotal module in operating a power system. It is a kind of optimization problem involved with optimal power output generators by all power units, having the constraint of total fuel cost. Notably, the total generated power should equal the system's demand, including the total network loss (transmission loss). Therefore, each unit's generation should be optimized according to a defined rating. It is regardless to mention that the non-linearities of the generation units comprising ramp rate limits, prohibited zones, and non-convex cost functions need to be considered in optimizations. PSO, in this context, might be an appropriate tool due to its low computational time with a higher convergence rate. Therefore, the work proposed a hybrid optimization algorithm combined with Fuzzy logic and Nelder – Mead algorithm with PSO to solve the ED problem with valve-point effect. The concept introduces a dynamically tuned inertia weight and learning factors in PSO based on Fuzzy logic. The Fuzzy adapted PSO (FAPSO) worked as an excellent optimizer tool approaching the g_{best} solution, followed by the NM algorithm continued its local search process concurrently.

Optimization problems related to electric power systems have always been diversified due to their complex nature of objective functions with many constraints. The work [6.38] carried out a detailed survey highlighting the PSO application areas related to electric power systems. The problems include linear, integer, non-linear and mixed-integer types of constraints to be solved. PSO, a kind of general-purpose optimizer, merely needs modifications to be implemented in a variety of applications. Since power system modules are involved in calculating non-linear functions to evaluate each candidate, PSO has been a powerful problem-solving tool in this field.

PSO was conceptualized by the collective behavior of birds, fishes and other social organisms aimed to survive and continue their daily hood. An upgraded PSO variant is reported in [6.39], where the conventional PSO model got muted through quantum mechanical theories. The research demonstrated a quantum-based PSO (QPSO) with a mutation operator of Gaussian nature. The approach accelerated the convergence rate of the algorithm bypassing the premature convergence limited to local optima. The work carried out two case studies, revealing the proposed algorithm's efficacy in terms of fast convergence and higher precision of results.

With the advancement of the traditional PSO algorithm, Kirareyaz et al. [6.40] delivered two novel ideas to reform the native structure of PSO particles. Initially, it keeps finding the positional and dimensional optima for a high dimensional and multimodal sear space with unknown dimensions. Still, the MD PSO suffers from premature convergence. Therefore, as a solution, a fractional global best formation technique (FGBF) has been modeled that artificially creates a fractional g_{best} particle potentially inherited as a better guide for the successive stages of solutions. The model was successfully implemented in the fields of non-linear function minimization and data clustering.

The work [6.41] reported a variant of PSO functioning in a dynamic environment. The challenges for the proposed algorithm in a dynamic environment are old memory and diversity loss of individual particles, which affects the search process. Therefore, it is required to either re-evaluate the memory or erase it to overcome the said problem. In re-evaluation, memory content would be verified in each stage, while each particle would replace its current location by erasing the previous memory. In addition, a tracking and restoring mechanism should be run to deal with the diversity losing mechanism.

Nápoles et al. presented a constricted PSO algorithm [6.42] named Particle Swarm Optimization with random sampling in a variable neighborhood (PSO-RSVN), capable of detecting premature converging state and, therefore, eliminating that in obtaining the solution. Traditional PSO suffers from premature solutions while getting stuck to the local optima. Thereafter, the proposed algorithm chose some random samples from neighborhoods for dispersing the swarm as and when stagnation occurs. The algorithm has experimented with nine well-known benchmarked functions, which justified its efficacy in finding global optima within a stipulated timing budget.

Shola et al. focused on resolving the Machine time scheduling problem [MTSP] in their proposed work [6.43]. Generally, the Monte-Carlo simulation was one of the best choices to deal with such problems. However, the authors proposed finding the starting time of each machine cycle considering the time is a stochastic one, defined by the normal distribution function. A hybrid algorithm using PSO with constriction and mutation factor had been proposed to handle the problem, which generated outstanding results in this regard.

Jordehi and Jasni published a review article [6.44] on parameter selection to modulate the computational behavior of PSO. The survey discussed vividly all the possible setting parameters' values for all potential applications of PSO, drawing an entire guideline for future research personnel working in the optimization domain.

The flashing light of fireflies may be modeled as an objective function of any optimization problem [6.45]. The flashlight pattern amongst fireflies during communication makes it possible to construct a new algorithm. The light produced by the bio-luminance process delivers two primary functions: (*i*) to make necessary communications to attract mating partners and (*ii*) to attract potential prey. As the light intensity is inversely proportional to the distance, its strength gets weaker with increased physical distances. Therefore, the pattern (or frequency) and the intensity of the flashing light are two major parameters in modeling the social behavior of fireflies. The article, presented by Yang, intensely covers entire concepts, models, operators, variants, and application fields, laying a path for future researchers in the optimization field.

Work is reported by Yang [6.46] on the Firefly Algorithm suitable for multimodal optimization. The work, starting with the formulation of the algorithm, proceeds to a comparative study of Particle Swarm Optimization with other pertinent algorithms. The observation revealed that the Firefly algorithm is more competent than PSO for multimodal

optimization functions. Moreover, it is realized that PSO is a subset of FA, as demonstrated in the paper. Nevertheless, FA possesses some relevance to the bacterial foraging algorithm (BFA). In FA, attractiveness is modeled as the objective functions and monotonic decay of attractiveness with distance. In contrast, the same attractiveness in BFA is a function of both fitness and distance. However, FA is proven more versatile in terms of attractiveness leading to higher mobility and better exploration of the search space.

The work reported [6.47] a successful Firefly algorithm (FA) implementation in non-linear optimization problems with many constraints. Standard benchmarked functions are validated first. Therefore, new test functions with singularity and stochastic components are generated to further implement the Firefly algorithm in the unconstrained stochastics domain. Better global solutions to the pressure vessel design optimization were found, which justified the potentiality of the FA than PSO in terms of problem-solving capacity.

Metaheuristics are among the most powerful algorithms in solving Global optimization problems, especially regarding NP-hard problems. In addition, various surveys reported that many biological agents' flight behavior exhibited the classical nature of Leύy flights. Therefore, the work [6.48] has formulated a Firefly-Leύy flight hybrid algorithm (LFA) to compare its merits with other pertinent algorithms. The findings of the work revealed that PSO might perform better in finding Global optima than the Genetic algorithm (GA). Still, LFA outperforms both PSO and GA in terms of efficiency, consistency, convergence rate and precision. Furthermore, LPA was proved more competent to handle NP-hard Global optimization problems. Further improvements may be accomplished by considering the sensitivity of various characteristic parameters of the proposed algorithm.

A novel two-stage hybrid optimization method, known as the Eagle strategy, was proposed by Yang and Deb [6.49]. Since some non-linearities and probabilistic events always exist in real-world problems, objective functions of related algorithms are formulated considering the system noise and constraints. Therefore, stochastics optimization tools need to be explored to solve those problems. Thus, the work formulated a metaheuristic named Eagle strategy incorporating the Leύy walk with the Firefly algorithm to solve NP-hard problems effectively. The performance of the proposed algorithm was compared with PSO and other competent algorithms to explore its merits in finding Global optima. The results show better accuracy and convergence rate of the proposed algorithm than PSO. Therefore, this hybrid approach

effectively handled many engineering optimization problems involving intrinsic inhomogeneities and uncertainties.

The convergence rate of the Firefly algorithm based on suitably selected parameters was analyzed by Arora and Singh [6.50]. The analysis has been carried out to explore the dynamic behavior of fireflies in discrete-time systems. The results provide exclusive guidelines for suitable parameter selection to get fast convergence. Furthermore, three sets of experiments with five benchmarked functions were involved in testing the potentiality of the proposed model. As a result, better results have been obtained with improved convergence speed at the cost of the robustness of the proposed algorithm.

The performance of the Firefly algorithm has been evaluated through clustering, which is a recommended data analysis technique. The work [6.51] compared the FA performances with PSO and ABC (Artificial Bee Colony). The algorithm was tested with nine standard methods and thirteen well-known benchmark functions. Like other metaheuristics, the performance of FA depends on the swarm size and number of iterations. Therefore, the clustering challenge of 13 benchmark functions has been involved in the test process. With the partial clustering strategy, FA successfully computes all problem sets in obtaining better solutions. The results revealed that FA is an efficient, reliable, and robust optimization technique even effective for clustering problems.

A binary Firefly algorithm is implemented to decipher encrypted messages for crypto-analysis [6.52]. The proposed algorithm considered light-intensity, distance, attractiveness, and position upgradation for fitness evaluation. The method of encryption analysis involves the Merkle-Hellman Knapsack cipher. A performance comparison has been made between FA and GA in this context. The results exhibited that FA outperforms GA even for a higher population size. Therefore, the proposed algorithm evolved as a potential contender for the crypto-analysis of Knapsack Cipher.

A work [6.53] is reported on deploying the Firefly algorithm to identify hardware and software faults in parallel and distributed systems. System-level fault diagnosis involved the collective output of all test patterns for the given set of test models. The task was an NP-hard combinatorial problem, difficult to find solutions in a polynomial-time frame. Therefore, it required metaheuristics to obtain feasible solutions. The paper-work proposed a novel approach, including binary encoding with adaptive light absorption coefficients (motivated by PSO in many cases) to accelerate the search process. In the proposed strategy, each binary

agent is attracted by every other agent with greater fitness value, encouraging diversified solutions through a corporate search process. Moreover, the proposed process delivered accelerated convergence with lesser storage capacity. Therefore the proposed model ensures effective solutions in fault identification of a distributed system with better competency than PSO and GA.

The work [6.54] proposed a Firefly-variant in a mono-alphabetical substitution cipher encryption process. The process is defined by replacing each letter of a given test with some predefined scheme, which uses linguistic statistical data. The proposed strategy of FA introduced operators of mutation and crossover, like GA, in solving problems. The results exhibit an exact prediction of the given character of the text. The optimum swarm size was considered 35, over and below which the prediction degrades. Nevertheless, observations justified the excellent potential of the proposed algorithm even for a large volume of texts.

Conventional Otsu's method is commonly used in segmentation but suffers from increased execution time for multiple thresholds. Therefore, the paper-work [6.55] proposed a Firefly, modulated by maximum-variance intra-clustering to handle this problem. The approach efficiently finds threshold values of optimization problems. Notably, the number of thresholds has a negligible impact on the algorithm's time complexity. The results justified the proposed model as more effective and accurate than Otsu and recursive Otsu methods.

6.3. Problem Statement

6.3.1. Global Routing in VLSI Physical Design

In VLSI physical design, the global routing takes place after floorplanning and placement of the circuit blocks for a given module. The routing comprises of interconnections between different blocks and pins in an electronic system/subsystem. The process is primarily defined by: (i) the netlist, (ii) the timing budget for the critical nets, and (iii) the RC delay of the metal layers and vias. The global routing aims to minimize the interconnect lengths maintaining the timing budget and performance of ICs intact. It is the initial step of routing, defining the list of regions to be interconnected, avoiding any intersection of wires and without any specific geometric layout of interconnects. The process involving thousands of pins with multimodal connections is computationally hard. Therefore, it requires a trade-off between 100 percent

routability and wire length minimization. Thus, the objective function of the global routing problem is treated as an NP-complete problem.

6.3.2. Rectilinear Steiner Tree Problem

In graph theory, the Minimum Spanning Tree (MST) of a given graph resolves into Rectilinear Stainer Tree (RST). MST of a graph has been formed by interconnecting the given vertices. The optimum weight of the graph is the sum of the weights of all the edges of the tree. Therefore, some intermediate vertices should be tactfully introduced in the MST to form RST, which would have reduced total weight. The added nodes, incorporated to minimize edges' total cost (resembles interconnects), are known as Steiner points, and the tree is called Steiner tree. It is proved by Garey and Johnson that the Rectilinear Minimum Steiner Tree (RMST) is an NP-complete problem, and to compute this in polynomial time is hardly exists.

In the context of global routing, RST is an efficient tool in wire length minimizations of VLSI circuits. The tool can effectively determine the minimum length of the interconnects for a given set of terminals. However, certain constraints, noise, power, electro-migration, signal integrity, packaging density, skew, inductance, reliability, etc., are likely to interfere with the objective functions in finding exact solutions. Therefore, the length of the non-critical nets still retains its importance in wire length optimizations.

6.4. Proposed Algorithms and Psudo Codes

6.4.1. Particle Swarm Optimization (PSO)

6.4.1.1. Operators and Proposed Model

A. Velocity Clamping

Particle's velocity, an important parameter of PSO algorithm, is the step size of swarm in each iteration. With each time step, the particles adjust their velocity & move in every direction in the problem space. If the velocity is too high, the exploration quality of the particle become high & at the same time the particle may quickly leave the boundary of the search space and diverge. On a contrary if velocity is low, the movement of particles is restricted over a small boundary and it becomes trapped in a local optima. Hence, it is required to maintain a balance

in between exploration & exploitation by setting a parameter V_{max} , given by $V_{max}= (X_{max} - X_{min}) / k$. The empirical value of k is set 2 in this work.

B. Inertia Weight

Inertia Weight (w) was further introduced to replace V_{max} to control the momentum of the particle in evaluating the updated velocity. It is introduced to control the exploration and exploitation abilities of the swarm so that the algorithm converges more effectively over time. Hence the basic PSO equation is modified as follows:

$$\left.\begin{aligned} V_{i,\,t+1} &= V_{i,\,t} + c_1 * r_1 * \left(p_{best} - X_{i,\,t}\right) + c_2 * r_2 * \left(g_{best} - X_{i,\,t}\right) \\ X_{i,\,t+1} &= X_{i,\,t} + V_{i,\,t+1} \end{aligned}\right\} \quad (6.1)$$

$$V_{i,\,t+1} = w * V_{i,\,t} + c_1 * r_1 * (p_{best} - X_{i,\,t}) + c_2 * r_2 * (g_{best} - X_{i,\,t}) \quad (6.2)$$

- If w=1: Then (6.1) is same as basic PSO.
- If w > 1: Then the velocity will increase over time and the particles will hardly be able to change their direction.
- If w < 1: Particles can quickly change their direction influenced by p_{best} and g_{best} values.
- If w = 0: Particles move without any knowledge of previous velocity.

Usually the inertia weight w is chosen depending upon the size of the search space. A high value of w is required for complex high dimensional problem space and small value for small dimensional search space.

The inertia weight can be varied by (6.3), where s is the population size, D is the Dimension size and R is relative quality of each solution normalized to [0,1].

$$w = [3 - \exp(-s/200) + (\frac{R}{8} * D)^2]^{-1} \quad (6.3)$$

C. Constriction Factor

The PSO algorithm is updated to replace the inertia weight w & max velocity V_{max} by a new parameter χ , known as constriction factor. This factor, introduced by Clerc [13], is extremely important to control the exploration & exploitation trade-off ensuring a smooth convergence of algorithm**.** Equation (6.1) gets modified as (6.4).

$$V_{i,\,t+1} = \chi * [V_{i,\,t} + \Phi_1 * (p_{best} - X_{i,\,t}) + \Phi_2 * (g_{best} - X_{i,\,t})] \quad (6.4)$$

$$\text{and, } \chi = \frac{2}{\left[2 - \phi - \sqrt{\phi^2 - 4\phi}\right]} \quad (6.5)$$

Here $\phi = \phi_1 + \phi_2$, $\phi_1 = c_1 * r_1$ and $\phi_2 = c_2 * r_2$. Typically using the value of $\phi = 4.1$ the value of χ comes out be 0.729. Hence $\chi * w = 0.729 * w < w$, implies that the particles quickly change their direction influenced by p_{best} and g_{best} with guaranteed convergence. Both $(p_{best} - X_{i,t})$ and $(g_{best} - X_{i,t})$ are multiplied by 2*0.729=1.458. In most of the cases, these values are chosen for better stability and convergence.

D. Acceleration Coefficient

1. SELF TUNED

In this algorithm PSO-ST (6.3), the acceleration constants both c_1 and c_2 are decreased linearly over each time step in the range of 2 to 1.49. At the start, the algorithm is initialized with $c_1=c_2=2$. By this tuning of linear decrement, both exploration and exploitation abilities of the swarm can be kept smooth for velocities updating and can provide a fast convergence to the algorithm. This algorithm proves to be efficient to get optimal result with high convergence rate.

2. PROPOSED SELF ADAPTATION

An algorithm PSO-SAAC is proposed where the two acceleration constant parameters c_1 and c_2 have been varied in such a manner that they got better control over the trade-off in between global exploration and local exploitation. The algorithm starts with highest exploration and lowest exploitation abilities of swarm, which have been gradually changed in every time step over the whole iteration process. Hence the particles of the swarm able to spread all over the search space uniformly, influenced by the social component of the velocity vector at the first phase of experiment. As the cognitive component outrun the social component in the next phase of the experiment, the swarm carry out the local search process based on the evaluated results of the Global search process in order to find out the best local optima. Over the entire searching process this self adaptive mechanism can be effective in generating lowest g_{best} value and thereby enhancing the optimization rate.

E. Proposed PSO with Mutation

A novel algorithm proposed where we have incorporated the essence of Genetic Algorithm in PSO. The algorithm after consuming some time steps starts with selection of swarms from current generation in the first phase. The swarms with high fitness probability get selected where the probability of selection factor is $\frac{f_j}{\sum_{j=1}^{N} f_j}$, where N is the population size. The high

fitness factor is extracted from the selected pool generating a mutant in the second phase. This enhanced knowledge of high fitness property is induced in the position vector (6.1) to evolve a new generation of swarms causing mutation in PSO. The proposed position vector in (6.6) is given below.

$$X_{i,\,t+1} = (\psi X_{i,\,t} + \xi) + V_{i,\,t+1} \qquad (6.6)$$

Where ψ is the randomization factor and ξ is the mutant fitness factor.

6.4.1.2. Pseudo Code of Proposed Model of PSO

The pseudo-code of the PSO algorithm is given below:

```
Initialize the population count (n) and maximum number of
iterations (max_it).
Set iter = 1 (here iter = current iteration count)
Initialize the position vector (xi,j) and velocity
vector(vi,j) of each particle xi.(i= 1,2…n)
Find the best position of each particle (pb) and the group(gb).
While (iter<max_it)
      iter = iter + 1
      for i = 1 to n
        Modify the velocity and then position vector of
        particle xi,j using equation (3.5) and (3.6)respectively
      End for
      Find the new best position of each particle (pb) and
      the group (gb).
End while
End
```

6.4.2. Firefly Algorithm (FA) characteristics

6.4.2.1. Operators and Proposed Models

The optimization mechanism in FA is characterised with the attraction phenomenon and the relative position of the individual fireflies. The fitness of the solution is determined by the locations of the fireflies and global optimisation is revealed by searching the best location in the problem space. Here two important factors are involved: the variation of light intensity and the formulation of attractiveness. It is assumed for simplicity that the attractiveness of a firefly is determined by its brightness which in turn is associated with the objective function. The higher is the brightness, the better is the location and more and more fireflies will be attracted

to that direction. If the brightness value all fireflies are equal, the fireflies will move randomly in the search space. The mathematical model of the firefly algorithm is given below.

As the brightness of a firefly depends upon distance, hence it is a function of x, denoted by I(x). The attractiveness β is relatively dependent upon the judgement of other fireflies. Hence, it will vary with the distance between two fireflies. Light intensity depends on the absorption coefficient of the media. So attractiveness will also vary with the varying degree of absorption. The light intensity I(r) varies according to the inverse square law in (6.7).

$$I(r) = \frac{I_s}{r^2} \tag{6.7}$$

Where, I_s is the intensity at the source. For a medium with a fixed light absorption coefficient γ, the light intensity I will vary with the distance r.

$$I = I_o e^{-\gamma r} \tag{6.8}$$

Where, I_o is the initial light intensity. In order to avoid the singularity at r = 0 in the expression, the combined effect of both the inverse square law and absorption can be approximated as the following Gaussian form.

$$I(r) = I_o e^{-\gamma r^2} \tag{6.9}$$

A firefly's attractiveness is proportional to the light intensity seen by adjacent fireflies. So the attractiveness β of a firefly can be obtained by (6.11)).

$$\beta = \beta_o e^{-\gamma r^2} \tag{6.10}$$

Where, β_o is the attractiveness at r = 0. It is often faster to calculate$1/(1 + r^2)$ than an exponential function. So the above function, if necessary, can be approximated as

$$\beta = \frac{\beta_o}{1+\gamma r^2} \tag{6.11}$$

Characteristic distance is the distance r (=Γ= 1/root(γ)) over which the attractiveness changes significantly from β_o to $\beta_o e^{-1}$ for (6.11) and $\beta_o/2$ for (6.12) . From (6.12), it is seen that the parameter γ characterizes the attractiveness, and its value is important in determining the speed of the convergence. Theoretically γ Є [0, ∞) but in actual practice, γ O(1) is determined by the characteristic length Γ of the system to be optimized. Thus, it typically varies from 0.1 to 10 for most of the cases. The distance between any two fireflies i and j at x_i and x_j, respectively is the Cartesian distance.

$$r_{i,j} = \|x_i - x_j\| = \sqrt{\sum_{k=1}^{d}(x_{ik} - x_{jk})^2} \tag{6.12}$$

Where $r_{i,j}$ is the k^{th} component of the spatial coordinate x_i of i^{th} firefly. In two dimensional case, $r_{i,j}$ is given by (6.13).

$$r_{i,j} = \sqrt{(x_i - x_j)^2 + (y_i - y_j)^2} \tag{6.13}$$

The movement of the firefly i, attracted to another more attractive (brighter) firefly j, is determined by (6.14).

$$x_i = x_i + \beta_o e^{-\gamma r_{i,j}^2}\left(x_j - x_i\right) + \alpha \epsilon_i \qquad (6.14)$$

Here, the second term is due to the attraction and the third term is randomization with α being the randomization parameter. ϵ is a vector of random numbers being drawn from a Gaussian distribution or uniform distribution. In our algorithm ϵ_i is implemented by (rand − ½) where rand is a random number generator uniformly distributed in [0, 1] and we take β_o =1 and $\alpha \in [0, 1]$.

6.4.2.2. Pseudo Code of Firefly

Pseudo code of the Firefly algorithm is given below:

```
Initialize the population count (N) and maximum number of
iterations (max_it).
Set iter = 1 (here iter = current iteration count)
Initialize some random position of fireflies (xi) equal to
the population count(i= 1.2…N).
Determine the light intensity of each firefly.
while (iter<max_it)
      for i = 1 to N
       for j = 1 to N
        If firefly j is brighter than firefly i
            Move firefly i to firefly j by eqn (3.16)
        Else
            Move the firefly i randomly in search space

      End if
        Vary attractiveness of each firefly i with
        distance using eqn 3.14
        Evaluate the intensity of new solution.
       End for
      End for
      iter = iter + 1
End while
End
```

6.5. Experimental Setup

In global routing, the total wire length of an Integrated Circuit has been optimized in order to obtain the maximum performance of the chip. Therefore, the solution to the problem can be considered as finding the least cost MRST from a graph model. Generally, a grid graph model is assumed as the experimental setup in implementing the algorithms. Hence, the entire routing region is hypothetically represented by a grid graph, *G= (V, E),* where the total area is divided

into many adjacents cells, as depicted in Fig. 6.1. Furthermore, each cell is considered as a vertex (*Vi*) and the edge connecting two vertices (*Vi* and *Vj*) is known as *Eij*. Therefore, the objective is to find the least cost stainer tree out of the modeled graph to yield the global routing solution for the multimodal net.

The position vectors of the swarms are assumed by either '0' or '1' value to implement the discrete PSO or Firefly algorithms in a two-dimensional search space. The search space is modeled by a two-dimensional grid graph (2-D matrix) with each node referred to each element of the swarm. The position vector of each particle upgrades itself relied on the probabilistic value following the sigmoid function (6.15). In the next time step, the position vector (bit value) gets complemented with the conditional probabilistic value greater than 50%.

$$s(t) = \frac{1}{1+e^{-t}} = \begin{cases} \to 1, t \to \infty \\ = \frac{1}{2}, t = 0 \\ \to 0, t \to -\infty \end{cases} \qquad (6.15)$$

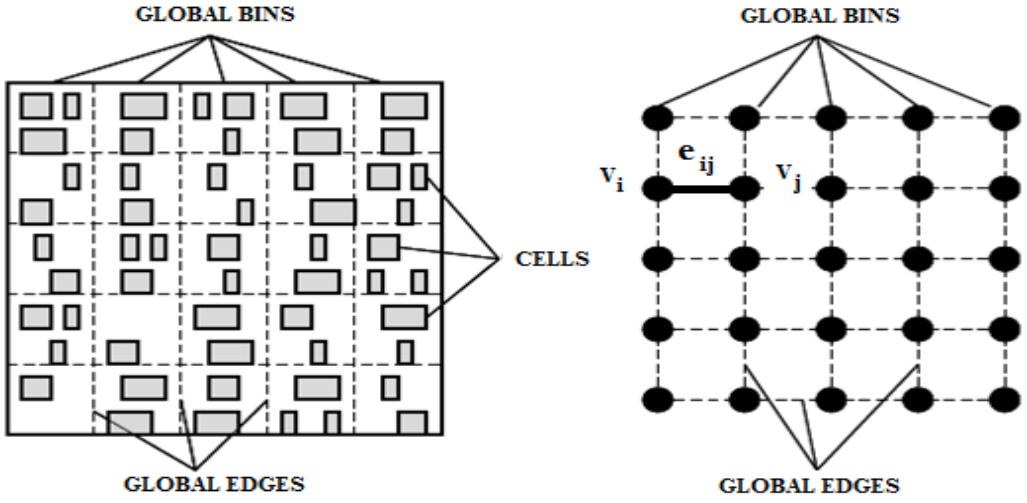


Fig. 6.1: Representation of routing region layout in a grid graph.

Therefore, three coordinate sets have been assumed on a two-dimensional 100x100 search space. Furthermore, the nodes to be interconnected have been spread over the search space following different distribution topologies for in-depth experimental purposes. There are 15 terminal points with different coordinated for the experiments. The distribution topologies include uniform, clumped, and bivariate, graphically presented in Fig. 6.2, 6.3 and 6.4, respectively. Each experiment was run thirty times for a defined set of coordinate values and

topologies. The population size of 100 with a maximum of 75 iterations is set for the experiments.

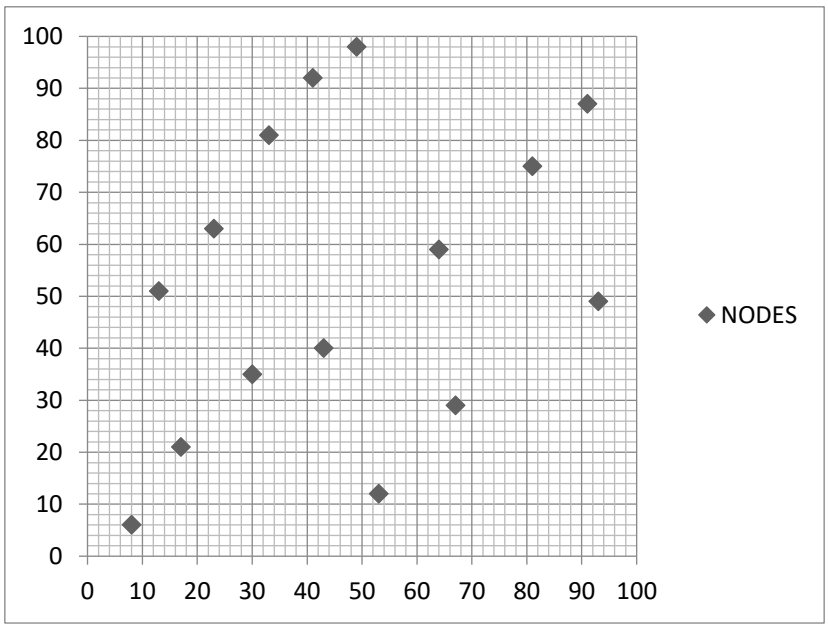


Fig. 6.2: SET 1: Nearly Uniform distribution of terminal nodes on 100x100 search space.

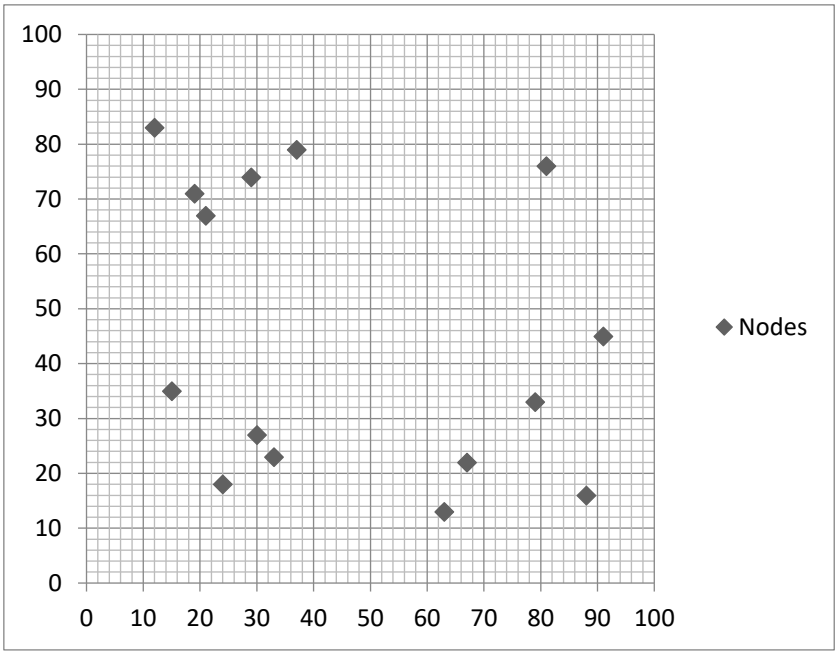


Fig. 6.3: SET 2: Clumped distribution of terminal nodes on 100x100 search space.

6.6. Results and Discussions

6.6.1. Experiment 1

The proposed PSO-ST (6.3), PSO-SAAC and PSO-W have experimented with three defined coordinated sets. First, the minimum and the average cost of the Steiner tree are calculated through 25 times simulation process of respective variants of the algorithm. This implies the minimum and average interconnect lengths found by the algorithms. The results of average global best and minimum global best are enlisted in Table 6.1 for performance comparison.

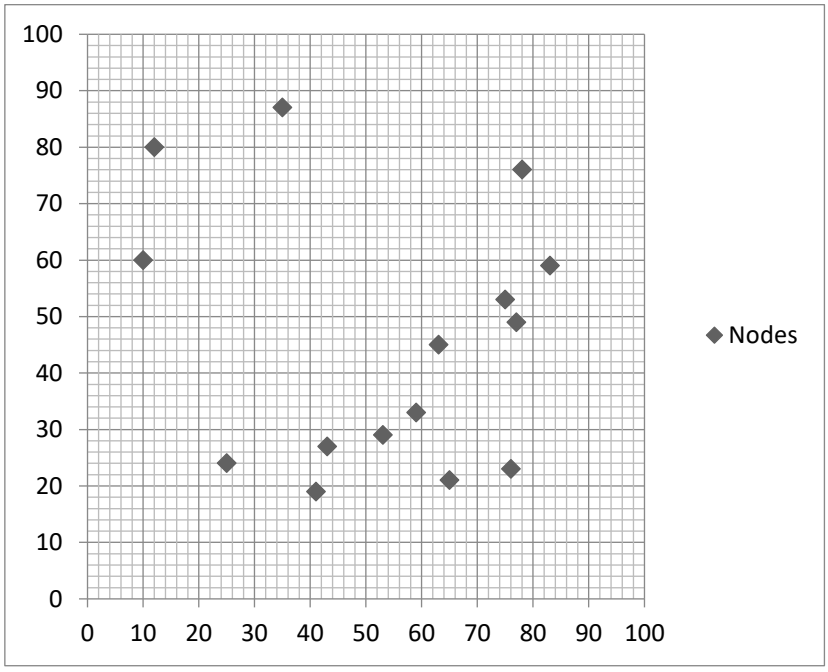


Fig. 6.4: SET 3: Bivariate distribution of terminal nodes on 100x100 search space.

TABLE 6.1: COMPARISON OF PSO-SAAC WITH PSO-W AND PSO-ST

TEST	g_{best} value	PSO-W	PSO-ST	PSO-SAAC
SET-1	Average	354.5	348.4	341.7
	Minimum	350	343	338
SET-2	Average	286.3	283.4	287.5
	Minimum	283	279	284
SET-3	Average	256.7	254.9	257.3
	Minimum	253	253	255

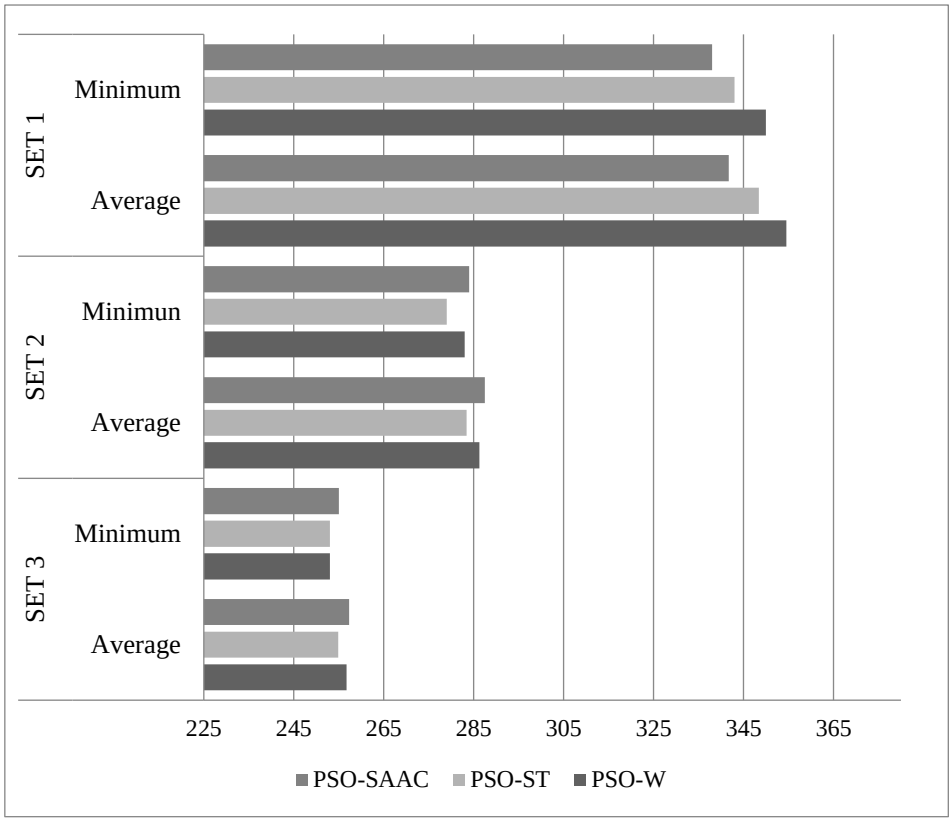


Fig. 6.5: Comparison of proposed PSO variants with existing PSO-W on varied distribution of terminal nodes

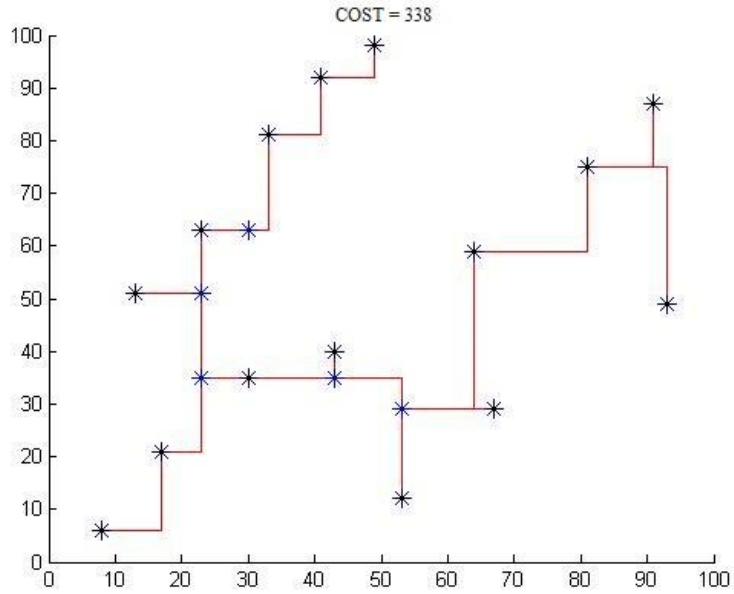


Fig. 6.6: Minimum 'cost' Steiner Tree obtained for PSO-SAAC in Set 1

The proposed PSO-SA algorithm performs best compared to its competitors in the case of uniform distribution. Furthermore, the model finds minimum interconnect lengths of 338 for

the given SET-1 data. Finally, the models are simulated through MATLAB and presented in Fig. 6.6. The bar chart given in Fig. 6 can be analyzed graphically that for clumped and bivaraite distribution, self-tuned acceleration constant controlling mechanism for PSO-ST outruns the other two algorithms. The PSO-ST algorithm provides the lowest interconnect lengths of 279 and 253 for random pin distribution profiles, depicted in Fig. 6.7 and Fig. 6.8. The average interconnects length parameters got better solutions through the proposed acceleration tunned variant of PSO.

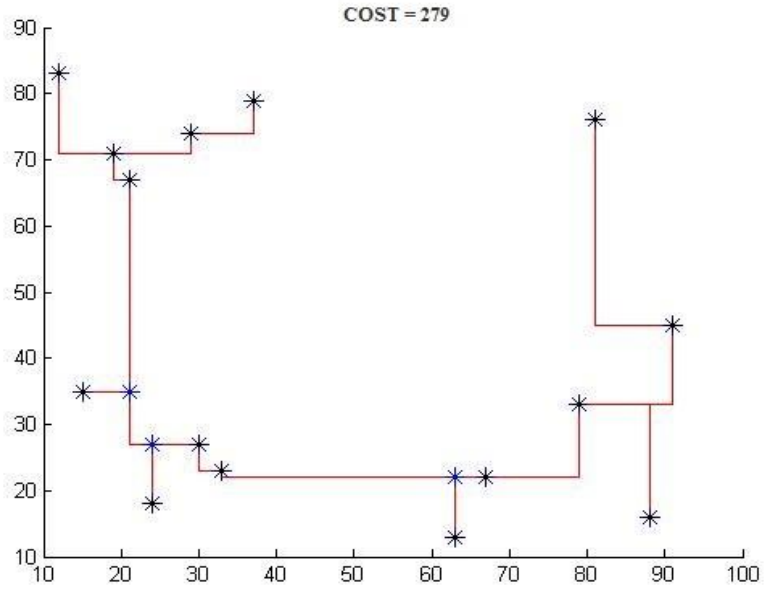


Fig. 6.7: Minimum 'cost' Steiner Tree obtained for PSO-ST in Set 2

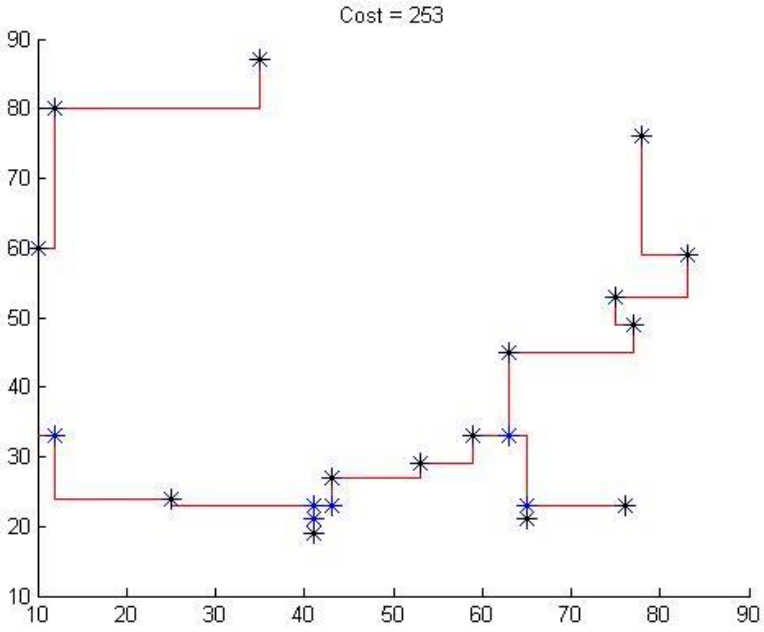


Fig. 6.8: Minimum 'cost' Steiner Tree obtained for PSO-ST in Set 3

Therefore, it is evident (from Fig. 10) that PSO-SA outperforms the rest two algorithmic models in a uniformly distributed environment. In contrast, PSO-ST effectively reduces the cost of RSMT (Rectilinear Steiner Minimal Tree) for the other two setup models. Therefore, the RSMT problem of graphs can be effectively managed and thereby the interconnect length is reduced to a great extent.

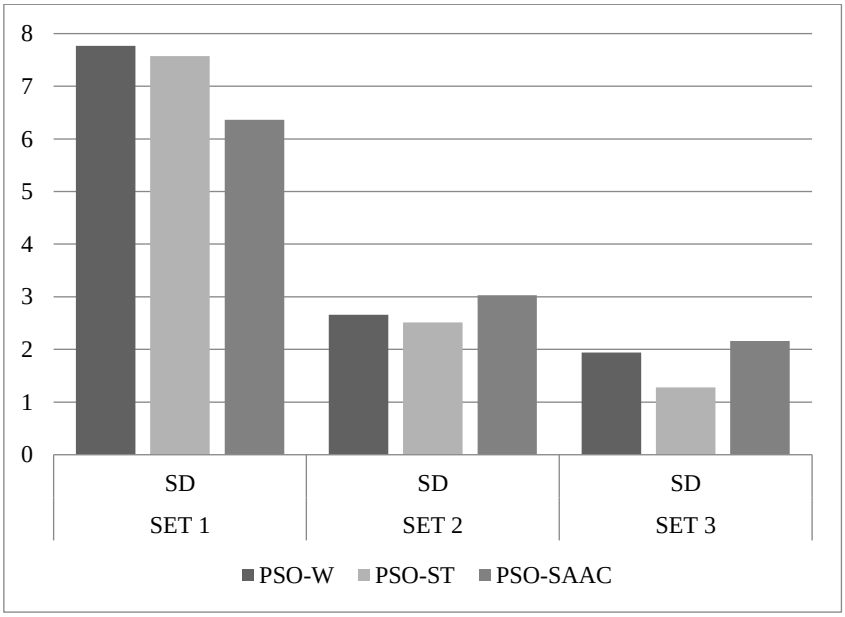


Fig. 6.9: The standard deviation of Average cost for the PSO variants.

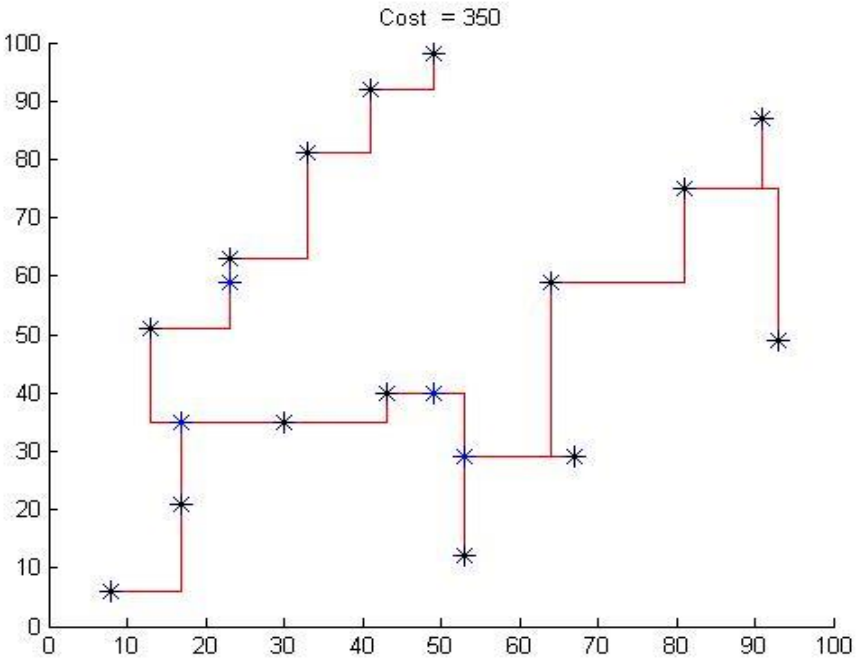


Fig. 6.10: Minimum 'cost' Steiner Tree obtained for PSO-W in Set 1

The standard deviations(SD) of the results of all experiments have been depicted in Fig.6.9. PSO-SA has the lowest SD value for SET-1 and PSO-ST possesses the lowest SD value for SET -2 and 3. The results imply that the self-adaptive model of PSO outperforms in uniform distribution platforms. In contrast, the self-tuned model of PSO outperforms in randomly distributed platforms in terms of consistent outputs.

6.6.2. Experiment 2

In the second set of experiments, the discrete PSO (DPSO) with constriction factor (PSO-C), Firefly algorithm (FA) and the proposed PSO with mutation algorithm [PSO-MU] have been tested for the defined coordinate sets. The results of all algorithms' minimum interconnect cost, average cost, and average execution time are recorded in Table 6.2. In addition, the MATLAB simulated results of RMST (Minimum Rectilinear Spanning Tree) generated for respective algorithm models are presented in Fig. 6.10, 6.11, 6.12, and 6.13.

TABLE 6.2: COMPARISON OF PSO-MU WITH FA AND OTHER PSO VARIENTS

Test	g_{best} value	PSO-W	PSO-C	FA	PSO-MU
SET 1	**Average**	354.5	350.4	337.3	336.8
	System Time	52.825	101.51	501.94	85.48
	Minimum	350	348	329	329
SET 2	**Average**	286.3	285.45	271.6	271.4
	System Time	55.35	57.65	428.69	76.06
	Minimum	283	283	265	264
SET 3	**Average**	256.7	256	253.8	250.4
	System Time	49.05	86.01	455.73	66.96
	Minimum	253	254	247	248

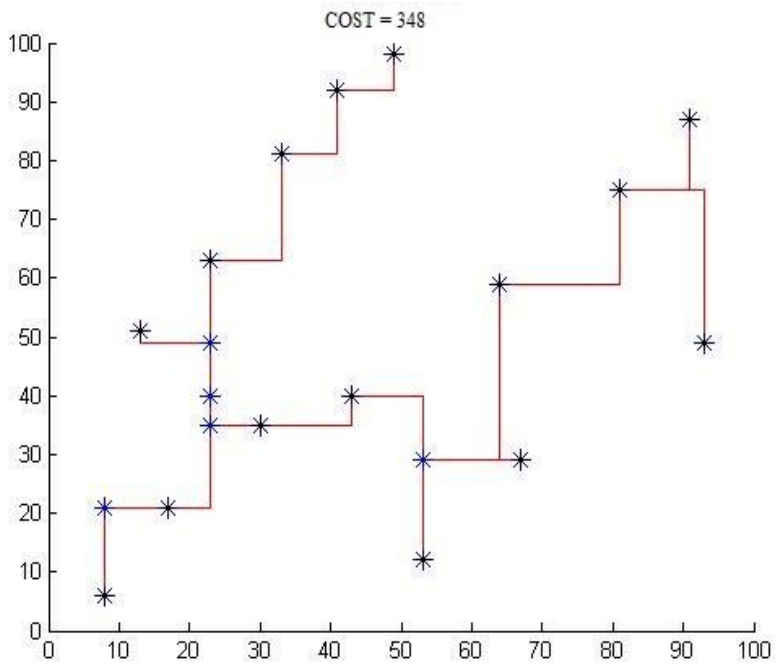


Fig. 6.11: Minimum 'cost' Steiner Tree obtained for PSO- C in Set 1

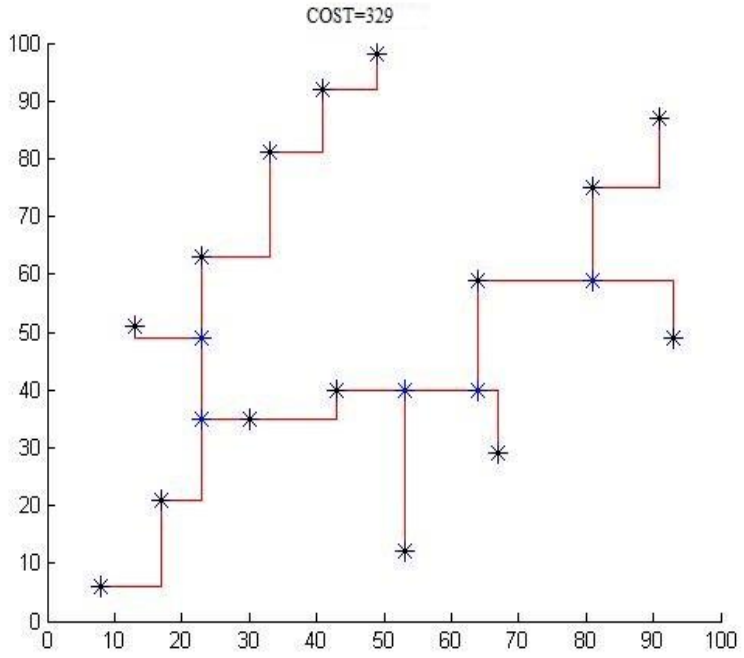


Fig. 6.12: Minimum 'cost' Steiner Tree obtained for FA in Set 1

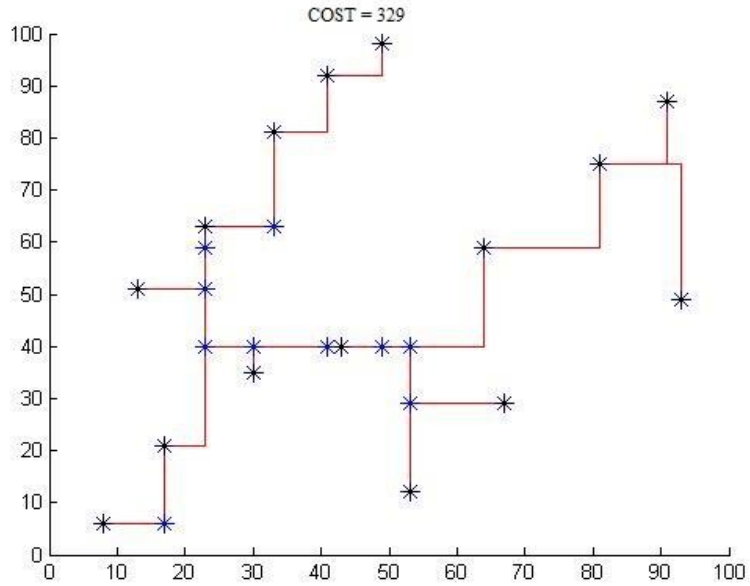


Fig. 6.13: Minimum 'cost' Steiner Tree obtained for PSO-MU in Set 1

Comparative performance analysis has been pictorially depicted in Fig. 15 to find the best performer among the proposed algorithms. The proposed PSO-MU and Firefly algorithm (FA) delivers the least minimum g_{best} value and minimum mean value as well for all the defined coordinate sets. This implied that PSO-MU and FA outperform the rest two variants in terms of optimization, precision and convergence.

For Coordinate Set 1, the 'global best' value obtained by PSO –MU and FA is 329, but the execution time of the FA algorithm is much greater than PSO-MU. The runtime of FA is found to be 501.94 compared to 85.48 for our proposed PSO-MU algorithm. This implies that our proposed algorithm meets the performance of the conventional FA algorithm while reducing the Timing budget.

TABLE 6.3: STANDARD DEVIATION OF THE g_{best} VALUES

TEST	g_{best} value	PSO-W	PSO-C	FA	PSO-MU
Test-1	SD	7.77	0.71	5.41	5.65
Test-2	SD	2.66	2.25	4.76	3.56
Test-3	SD	1.94	1.88	4.12	3.83

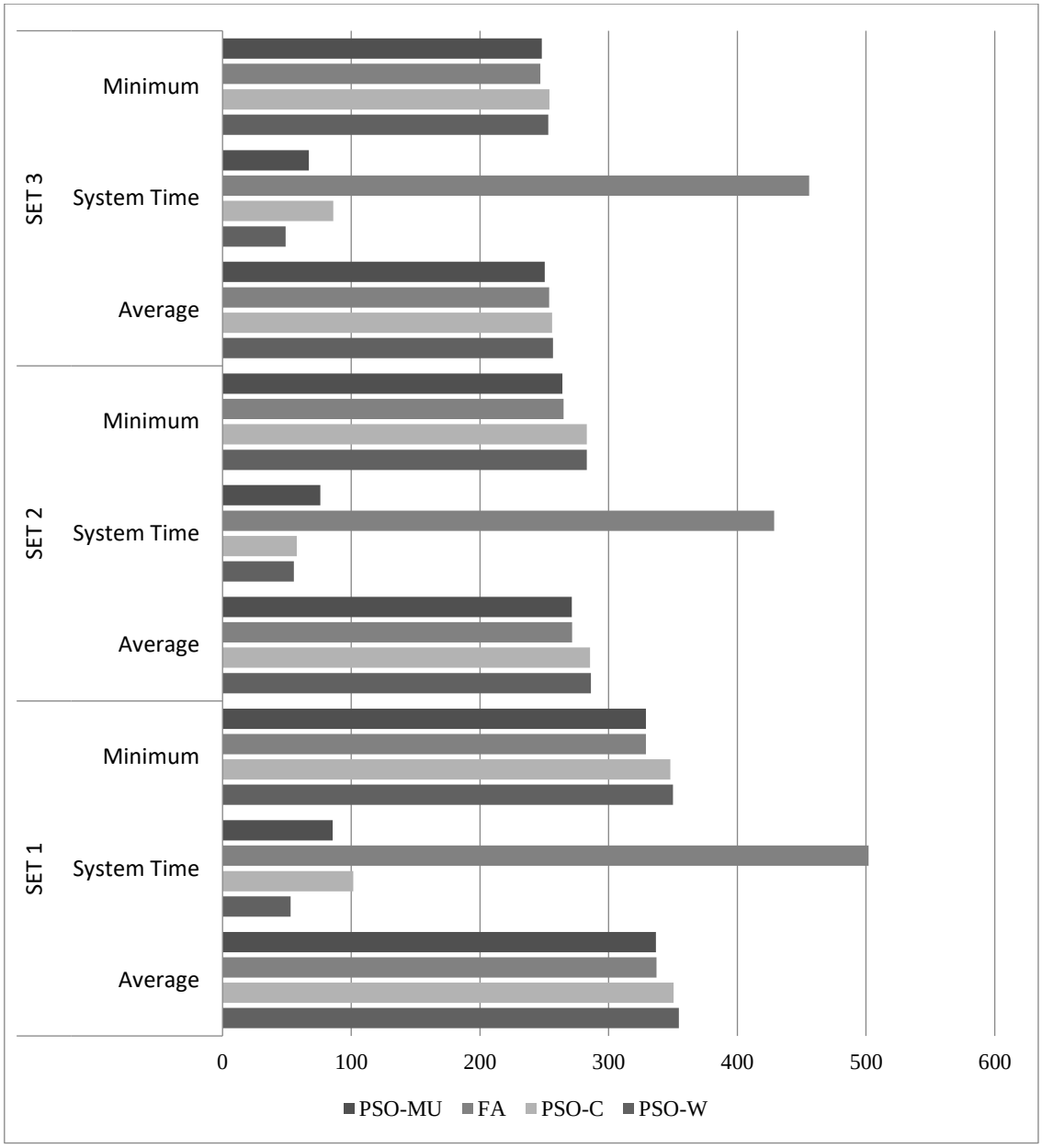


Fig. 6.14: Comparison of proposed PSO-MU with PSO-W, PSO-C, and FA.

The standard deviation (SD) values for defined coordinate sets and are derived to analyze the consistency of the proposed algorithms. From Table III, the SD value of PSO-C is 0.71, 1.88 and 2.25 for the three coordinate sets. All these values are small compared to that of PSO-W and FA. This ensures the robustness of the proposed PSO-C at the cost of time complexity of the system, irrespective of search space topologies. Therefore, PSO-C generates a higher value of interconnection cost and system execution time than PSO-W and conventional FA; it

exhibits the algorithm's robustness throughout all varied distribution topologies of the terminal nodes.

Reference

6.1. Abhinandan Khan, Pallabi Bhattacharya and Subir Kumar Sarkar," A Swarm Based Global Routing Optimization Scheme", International Conference On Advances In Electrical Engineering (ICAEE'2014), 9-11 January, 2014.

6.2. Subhrapratim Nath, Pinaki Prasad Guha Neogi, Jamuna Kanta Sing and Subir Kumar Sarkar, "VLSI Routing Optimization based on modified Constricted PSO with Iterative RLC Delay model" IEEE International Conference on Current Trends towards Converging Technologies, Coimbatore, India. March 1-3, 2018.

6.3. 2S. Nath, A. Shankar, R. Sarkar, S. Banerjee, J. K. Sing and Subir Kumar Sarkar, "Minimizing Wirelength with Bend Reduction using Gradient Descent PSO Hybrid in VLSI Global Routing," 2021 Devices for Integrated Circuit (DevIC), 2021, pp. 401-405, doi: 10.1109/DevIC50843.2021.9455851.

6.4. Suvrajit Manna, Udit Sharma, Tyajodeep Chakrabarti and Subir Kumar Sarkar, "Efficient VLSI routing Optimization employing Discrete Differential Evolution Technique", ReTIS 2015, 9-11 July, 2015.

6.5. J.-M. Ho, G. Vijayan, and C.K. Wong, "New algorithms for the rectilinear Steiner tree problem", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 1990, pp. 185-193.

6.6. Subhrapratim Nath, Swarnava Sarkar, Rabiraj Bandyopadhyay and Subir Kumar Sarkar**,** "A New Optimization Algorithm Based on Physarum BioNetwork for VLSI Global Routing",in5th International Conference on 'Computing, Communication and Sensor Network',CCSN2016,24-25 December, 2016,Kolkata, India.

6.7. Pallabi Bhattacharya ,Abhinandan Khan, Souvik Sarkar and Subir Kumar Sarkar," An Artificial Bee Colony Optimization Based Global Routing Technique ",International Conference On Control ,Instrumentation, Energy, Communication(CIEC 14) Organized By Department Of Applied Physics, University Of Calcutta, IEEE Kolkata Section, 31st January to 2nd February, 2014.

6.8. Subhrapratim Nath, Swarnava Sarkar, Rabiraj Bandyopadhyay and Subir Kumar Sarkar, "A New Optimization Algorithm Based on Physarum BioNetwork for VLSI Global Routing",in5th International Conference on 'Computing, Communication and Sensor Network',CCSN2016,24-25 December, 2016,Kolkata, India.

6.9. Tapas Chakrabarti, Tyajodeep Chakrabarti, Udit Sharma and Subir Kumar Sarkar, "Extraction of Efficient Electrical Parameters of SolarCell using Firefly and Cuckoo Search Algorithm", in IEEE-7th India 'International Conference on Power Electronics' (IICPE) 2016, 17th-19th November, Thapar University, Punjab, India, Volume: IEEE Xplore.

6.10. Subhrapratim Nath and Subir Kumar Sarkar, "Metaheuristics-based routing optimisation, balanced workload distribution and security strategy in IoT environment" International Journal of Advanced Intelligence Paradigms, Inderscience,Vol 9, Issue 1, https://doi.org/10.1504/IJAIP.2021.114586, April, 2021.

6.11. Subhrapratim Nath, Avik Kumar Chakravarty,Subinoy Ghosh and Subir Kumar Sarkar,"Invasive Weed Optimization Approach to VLSI Routing",IEEE International Conference on Devices for Integrated Circuits (DEVIC-17), Kalyani Govt. Engg. College, 23-24 March, 2017.

6.12. G. Beni and J. Wang, Swarm intelligence in cellular robotic systems. In NATO Advanced Workshop on Robots and Biological Systems, Il Ciocco, Tuscany, Italy, 1989.

6.13. Abhinandan Khan, Sulagna Laha and Subir Kumar Sarkar, "A Novel Particle Swarm Optimization approach for VLSI Routing", IEEE International Advance Computing Conference, Dr. A.K Garg Institute, Ghaziabad, 22-23 February, 2013.

6.14. Subhrapratim Nath, Avik Chackravarty, Sudipta Ghosh and Subir Kumar Sarkar, " FPGA Placement Optimization using Firefly Algorithm", published in Advances in Industrial Engineering and Management, vol. 6, no. 2, 2017, pp. 97-102, EISSN:2222-7067.

6.15. Subhrapratim Nath, Abhijit Paul, Rupam Banerjee, Swarnabja Bhaumik, Jamuna Kanta Sing and Subir Kumar Sarkar,"Optimizing FANET Routing Using a Hybrid Approach of Firefly Algorithm and ACO-Lévy Flight", in IEEE VLSI Device Circuit And System (VLSI DCS), 18-19 July 2020, Kolkata, India, DOI: 10.1109/VLSIDCS47293.2020.9179956.

6.16. Subhrapratim Nath, Rupam Banerjee, Swarnanja Bhaumik, Tuhin Karmakar, Jamuna Kanta Sing, Subir Kumar Sarkar "A Hybrid approach of ACO-Lévy flight and Firefly Algorithm in optimizing FANET Routing" International Seminar Cum Research Colloquium On Mems based Sensors and Smart Nanostructured Devices (MSSND 2019), Jadavpur University, Kolkata, 27-28 December 2019.

6.17. Subhrapratim Nath, Samriddha Banik, Arnab Seal and Subir Kumar Sarkar,"Optimizing MANET routing in AODV : An Hybridization approach of ACO and Firefly Algorithm" in 2nd IEEE 'International Conference on Research inComputational Intelligence and Communication Networks' (ICRCICN – 2016) ,organized by RCCIIT, September 2016.

6.18. James Kennedy, and Russell Eberhart, "Particle swarm optimization," in *Proc. Neural Networks*, 1995, vol. 4, pp. 1942-1948.

6.19. Reynolds, C. W. (1987). Flocks,herds and schools: a distributed behavioral model. *ComputerGraphics*,21(4):25-34

6.20. Heppner,F. and U. Grenander (1990). A stochastic nonlinearmodel for coordinated bird flocks. In *S* . Krasner, Ed., The *Ubiquity of Chaos.* AAAS Publications, Washington, DC.

6.21. Wilson, E.O. (1975). *Sociobiology: The new synthesis.* BelknapPress, Cambridge,hlA

6.22. Russell C. Eberhart and Yuhui Shi, "Comparison between genetic algorithms and particle swarm optimization," in *Evolutionary Programming VII*, 1998, pp.611-616

6.23. Eberhart, R. C., Dobbins, R. W., and Simpson, P. K. (1996), Computational Intelligence PC Tools, Boston: Academic Press.

6.24. Eberhart, R. C., and Kennedy, J. (1995), A new optimizer using particle swarm theory, Proc. Sixth International Symposium on Micro Machine and Human Science (Nagoya, Japan), IEEE Service Center, Piscataway, NJ, 39-43.

6.25. J. Kennedy, and R.C. Eberhart, "A discrete binary version of the particle swarm algorithm," in *Proc. Systems, Man, and Cybernetics, 1997. Computational Cybernetics and Simulation.* 1997, Orlando, pp.4104-4108

6.26. Russell C. Eberhart, and Yuhui Shi, "Particle swarm optimization: developments, applications and resources," in *Proc. Evolutionary Computation, 2001*, Seoul, pp. 81-86.

6.27. Clerc, M. (1 999). The swarm and the queen: towards a deterministic and adaptive particle swarm optimization. P roc. I999 Congress on Evolutionary Computation, Washington, DC, pp I95 1- 1957. Piscataway, NJ: IEEE Service Center.

6.28. Eberhart, R. C., and Shi, Y. Tracking and optimizing dynamic systems with particle swarms. Proc. Congress on Evolutionary Computation 2001, Seoul, Korea. Piscataway, NJ: IEEE Service Center.

6.29. Kennedy J, Mendes R (2002) Population structure and particle swarm performance. in *Proc. Of Congress on Evolutionary Computation*. 2. pp.1671–1676.

6.30. Fuqing Zhao, Qiuyu Zhang and Yahong Yang, "A Scheduling Holon Modeling Method with Petri Net and its Optimization with a Novel PSO-GA Algorithm," in *Proc. CSCWD '06*, 2006, pp.1-6.

6.31. Y. M. Chen & C. T. Lin. (2007). A particle swarm optimization approach to optimize component placement in printed circuit board assembly. *The International Journal of Advanced Manufacturing Technology*. *35(5-6),* pp. 610-620.

6.32. Ball MO, Magazine MJ (1988) Sequencing of insertions in printed circuit board assembly. Oper Res 36(2):192–201.

6.33. Laarhoven PV, Zijm W (1993) Production preparation and numerical control in PCB assembly. Int J Flex Manuf Syst 5(3):187–207.

6.34. Mojtaba Ahmadieh Khanesar, Mohammad Teshnehlab, and Mahdi Aliyari Shoorehdeli, "A novel binary particle swarm optimization," in *Control & Automation, 2007. MED'07. Mediterranean Conference on,*2007, pp.1-6.

6.35. Y. Valle, G. Venayagamoorthy, S. Mohagheghi, J.-C. Hernandez, R. G. Harley, (2008).Particle swarm optimization: basic concepts, variants and applications in power systems. *IEEETrans. on Evolutionary Computation,* 12(2), pp. 171–195.

6.36. A. P. Engelbrecht, "Particle swarm optimization: Where does it belong?," in *Proc. IEEE Swarm Intell. Symp.*, May 2006, pp. 48–54

6.37. Taher Niknam, (2010). A new fuzzy adaptive hybrid particle swarm optimization algorithm for non-linear, nonsmooth and non-convex economic dispatch problem. *Applied Energy*. 87(1). pp. 327-339.

6.38. M. R. Al Rashidi, and M. E. El-Hawary. (2009, Aug). A Survey of Particle Swarm Optimization Applications in Electric Power Systems. *Evolutionary Computation, IEEE Transactions on*. *13(4)*. pp. 913-918.

6.39. Leandro dos Santos Coelho. (2010). Gaussian quantum-behaved particle swarm optimization approaches for constrained engineering design problems. *Expert Systems with Applications*. . *37*(2), pp.1676-1683.

6.40. Serkan Kiranyaz, Turker Ince, Alper Yildirim, and Moncef Gabbouj. (2010, Apr). Fractional Particle Swarm Optimization in multidimensional search space. *Systems, Man, and Cybernetics, Part B: Cybernetics, IEEE Transactions on. IEEE*. . *40(2)*. pp. 298-319.

6.41. T. M. Blackwell, Particle swarm optimization in dynamic environments. In S. Yand, Y. Ong, and Y. Jin (eds.), Evolutionary computation in dynamic environments, Springer, Berlin, 2007,pp. 29–49.

6.42. G. Nápoles, I. Grau, and R. Bello, (2012). Constricted Particle Swarm Optimization based algorithm for global optimization. *Polibits*. . *(46)*, pp. 05-11.

6.43. M. A. Shohla, A. A. El-sawy, M. Nofal, and S. F. El-Zoghdy. Using Hybrid Particle Swarm Optimization to solve Machine Time Scheduling Problem with Random Starting Time. *International Journal of Computer Science Issues*. *9(5)*. pp. 322-327.

6.44. A. Rezaee Jordehi, and J. Jasni. (2013). Parameter selection in particle swarm optimization: a survey. Journal of Experimental & Theoretical Artificial Intelligence. . 25(4). pp. 527-542.

6.45. X. S. Yang, Firefly algorithm, Nature-Inspired Metaheuristic Algorithms (2008). Pp.79-90.

6.46. X. S. Yang, Firefly algorithms for multimodal optimization, in: Stochastic algorithms: foundations and applications, Springer, 2009, pp. 169-178.

6.47. X. S. Yang, (2010) .Firefly algorithm, stochastic test functions and design optimisation, International Journal of Bio-Inspired Computation .2 (2) .pp.78-84.

6.48. X. S. Yang, Firefly algorithm, levy flights and global optimization, in: Research and Development in Intelligent Systems XXVI, Springer, 2010, pp.209-218.

6.49. X. S. Yang, S. Deb, Eagle strategy using levy walk and firefly algorithms for stochastic optimization, Nature Inspired Cooperative Strategies for Optimization (NICSO 2010) (2010) 101-111.

6.50. Chai-Ead, P. Aungkulanon, and P. Luangpaiboon. "Bees and firefly algorithms for noisy non-linear optimization problems," in Proc. IMECS 2011, 2011, Hong Kong.

6.51. J. Senthilnath, S. N. Omkar, and V. Mani. (2011). Clustering using firefly algorithm: Performance study. Swarm and Evolutionary Computation. . 1(3). pp. 164-171.

6.52. S. Palit, S. Sinha, M. Molla, A. Khanra, M. Kule, A cryptanalytic attack on the knapsack cryptosystem using binary firefly algorithm, in: Computer and Communication Technology (ICCCT), 2011 2nd International Conference on, IEEE, 2011, pp. 428-432.

6.53. R. Falcon, M. Almeida, A. Nayak, Fault identification with binary adaptive fireflies in parallel and distributed systems, in: Evolutionary Computation (CEC), 2011 IEEE Congress on, IEEE, 2011, pp. 1359-1366.

6.54. J. Luthra, S. Pal, A hybrid firefly algorithm using genetic operators for the cryptanalysis of a monoalphabetic substitution cipher, in: Information and Communication Technologies (WICT), 2011World Congress on, IEEE, 2011, pp. 202-206.

6.55. Hassanzadeh, Tahereh, Hakimeh Vojodi, and A. M. E. Moghadam. "An image segmentation approach based on maximum variance intra-cluster method and firefly algorithm." Natural Computation (ICNC), 2011 Seventh International Conference on. Vol. 3. IEEE, 2011.

CHAPTER 7

Conclusions and Future Scope of the Work

7.1. Conclusion

The continuous evolution of CMOS technology has been procured through the aggressive downscaling of semiconductor devices. The uninterrupted miniaturization of MOSFETs through process technology for high packaging density, better performance and low power consumption gave rise to detrimental short channel effects (SCEs), for which the device performance got severely deteriorated. Multiple issues have arisen in scaled MOSFETs, particularly in sub-100nm technology nodes. After fifty years of aggressive downsizing, as the conventional scaling hits insurmountable physical barriers, a radical departure from conventional technology, materials and device geometry is mandatory to sustain the scaling theory for the next decade. At the same time, the backend VLSI design needs to be taken care of as the layout complexity increases day by day with the exponential growth of packaging density of modern performance-aware integrated circuits.

The main goal of the research has been to explore some non-conventional devices, precisely Tunnel Field Effect Transistors (TFET) and Junctionless Transistors (JL FET), to eradicate the deleterious ancillary issues with progressive scaling trend. Therefore, several innovative strategies involving multigate geometries, hetero gate material, and lateral channel engineering are exploited to investigate the degree of the betterment of device performances in comparison to contemporary structures. Moreover, the performance of the proposed device as a circuit element has been examined on device-circuit frameworks focused on dedicated application fields. The outcomes of the reported device structures, presented here, are relied on extensive

analytical modeling, which is further compared with relevant simulated data obtained from the device simulator to corroborate the accuracy of the derived models. Further, the objective of the thesis incorporated the evaluation of the performance matrices of Particle Swarm Optimization (PSO) and Firefly Algorithm (FA) in optimizing the interconnect length under the global routing phase of VLSI physical design. Thus, the dissertation aimed to attain even better circuit performance by addressing the routing issues related to complex layout designs of modern VLSI circuits.

Chapter 3 presented the impacts of body thickness over the electrostatic characteristics of a graded channel-tri metal-double gate Tunnel Field Effect Transistor with stacked gate oxide architecture (GC-TMDG-SO-TFET). Channel engineering has been implemented through three profiles of abrupt channel doping in decreasing order along the channel from source to drain side. Work function engineering has been deployed with a Tri-metal gate along with double gate architecture for better electrostatic controls over carrier transportation. Stack oxide is used to evade the short channel effects (SCEs) like hot carrier effect, impact ionization, etc., to restrict the premature saturation of drain current and avoid gate leakage while sustaining the device scalability. Young's parabolic approximation method with suitable boundary conditions has been applied to solve Poisson's equation of surface potential in the channel region. Therefore, the tunneling generation rate is integrated over source-channel junction area to derive the drain current expression. Finally, a comparative study is made of the proposed device with two different body thicknesses, 5nm and 8nm, respectively. The results of the analytical model are verified against the simulation results of the SILVACO TCAD device simulator. The proposed model demonstrates the impact of the graded channel as a potential barrier in the channel region to reduce leakage current in the OFF and ON states as well. High doping concentration at the junction of source and channel boosts band-to-band tunneling, consequently reducing subthreshold slope. Proper choice of work function for the gate electrodes gives better results in terms of I_{ON}/I_{OFF} ratio and SS. The stack gate structure provides better gate control over the channel region with lesser leakage current. The GC-TMDG-SO-TFET performed well at low drain voltage (~0.5V) with the input voltage, i.e., V_{GS} of about 0.5V. The I_{on} is about 0.1mA range and I_{OFF} is quite lower than femto-ampere with an I_{ON}/I_{OFF} ratio is 10^{11} and sub-threshold swing (SS) of 40mV/decade at room temperature 300K. The simulated data supports the results of analytical modeling, endorsing its accuracy and precision. The model agrees with the simulation results of the proposed device structure up to 50nm gate length. Beyond that, the short channel effects dominate the actual device performances, and more engineering techniques

need to incorporate to subdue those effects. The Quantum model has not been used in our work. That could have been explored for future works.

The second section of Chapter 3 explored a spacer-induced hetero-dielectric double gate p-n-p-n Tunnel Field Effect Transistor (S-HD-DG p-n-p-n TFET) with enhanced performance matrices. The channel engineering has been incorporated by implanting a shallow n-type region with high doping at the source side junction of the channel. The structure is then modified by introducing hetero-gate dielectric materials as gate oxides. Here, high-k material (HfO_2) at the source side and low-k (SiO_2) material at the drain side have been used to control the electric fields along the channel with a balanced proportion in order to upgrade the electrostatic characteristics of the device. Moreover, high-k spacers have been deposited at the ends of the metal gate for further improvements of the device characteristics. Hafnium dioxide (HfO_2) and Titanium Dioxide (TiO_2) have been tested as spacers to examine possible performance changes. Using Young's parabolic approximation, the analytical surface potential model has been derived from 2D Poisson's equation. Therefore, electric fields are derived by differentiating the potential equations. Kane's local tunneling model is finally used to calculate the drain current. The analytical model is then corroborated by the simulation data extracted from the SILVACO ATLAS device simulator. Both the analytical and simulation processes incorporate the effect of interface trap charges at the oxide–substrate interface. The length through which the trap charges are considered to be present is known as damaged length and is denoted by L_d in the chapter. The existence of the damaged length is considered on both sides of the channel.

The work has been carried out through two sets of experiments, as mentioned earlier in the chapter. From the first set of experiments, it is derived that high-k spacer oxide (like HfO_2) at the drain side with p-n-p-n TFET structure (structure 3) provides reasonable ON (~0.1 mA range) and OFF current (~fA range) with ON/OFF current ratio of 10^{11}. The subthreshold swing of this device is poor, i.e., 58.5 mV/decade, which is just below the 60mV/decade (theoretical limit of MOS devices at room temperature), but this device produces excellent subdued ambipolar conduction up to -1.0V of V_{GS}. It could be a potential candidate for digital VLSI applications.

In the second set of experiments, the hetero-oxide drain-sided high-k spacer induced p-n-p-n TFET architecture (structure 6) exhibits an excellent subthreshold swing (SS) of 18.37mV/decade with a very high ON/OFF current ratio of 10^{14} with OFF current at atto-ampere (10^{-18}) range. The performance comparison is enlisted in Table 3.2 in detail. Though structure 3 outperforms structure 6 in the context of subdued ambipolarity, this structure can still suppress

ambipolarity up to -0.5V of V_{GS}. Therefore, structure 6 is one of the most potential contenders in low standby power VLSI applications.

The prime motive of Chapter 4 has been to develop a device-circuit framework to explore the circuit performance of the proposed TFET device. In the work, a 2-D analytical model of a hetero-junction (Ge-Si) Tunnel Field Effect Transistor (HTFET) with stack gate oxide has been developed. Bandgap engineering is incorporated to enhance the device's performance by introducing Germanium as source material and Silicon as channel and drain material. A generic modeling approach is followed to calculate the surface potential, electric field and drain current, considering the depletion charges in the Silicon channel. Accurate computations are accomplished in obtaining the characteristics in the subthreshold region, whereas a compensation technique is adopted to derive the characteristics in the superthreshold region (due to not including the accumulation charge) to validate the results with the ATLAS device simulator. Quantum mechanical effects have not been considered as the thickness of the substrate is restricted to 10nm, for which the band energies are assumed to be continuous. The derived model thoroughly examined the device electrostatics in terms of energy band, surface potential, electric field and drain current. The proposed optimized device geometry delivers exceptionally low OFF current (order of 10^{-18} A/um), reasonably high ON current ($5x10^{-5}$ A/um), a steep sub-threshold slope (20 mV/decade) followed by an excellent ON-OFF current ratio (order of 10^{13}) compared to the similar kind of hetero-structures.

Therefore, device parameters are extracted to generate the Verilog-A model file through a look-up table method for circuit simulations. Then, the resistive inverter circuit of the proposed device is implemented and simulated with the Mentor Graphics circuit simulator to obtain the power consumption, propagation delay and power-delay product. The proposed circuit performances are finally compared with the resistive CMOS inverter of 45nm technology node.

Last but not the least, our proposed work is compared with some state-of-art technologies to prove its supremacy in digital applications. The power dissipation of a single-stage adiabatic inverter is computed and compared with a conventional CMOS inverter, for which a performance matrix called "energy gain" is defined. The energy gain is defined as the percentage of the ratio of dissipated power of an adiabatic inverter with the CMOS inverter. We have computed the energy gain for our work with the circuit parameters and physical conditions kept the same as the abovementioned work and tabulated the performance matrices for two sample voltages, given in Table 4.5.

The device performances are recorded in Tables 4.3 and 4.3. The proposed device emerged as an excellent one for digital application in terms of lower subthreshold slope, higher ON/OFF current ratio and shallow leakage current. Moreover, with a very low threshold voltage, even lesser than 0.1 V, the proposed device emerged as a suitable replacement for MOSFET in a CMOS-like digital circuit. The circuit performances are analyzed and compared in terms of power dissipation, propagation delay and power-delay product (PDP). The output responses are enlisted in Table 3.4., which exhibits that the inverter circuit based on the proposed hetero-junction tunnel FET outperforms the CMOS inverter in terms of power dissipation, propagation delay and power-delay product (PDP). Moreover, it is clear from Table 4.5 that the "energy gain" of our work is quite satisfactory compared to the previous work since the HTFET-based inverter consumed below 20% of the power that is consumed by the CMOS inverter. On the contrary, it is observed that the adiabatic inverter consumed more or less 30-35% of the power that is consumed by the CMOS inverter with similar design parameters.

Since all the experiments are carried out with the device geometry of 10 nm body thickness and 40 nm gate length, it is worthy of mentioning as concluding remarks that the device and circuit performances could have been even better with lower device dimensions though issues related to quantum mechanical effects and short channel effects need to be taken care off in those cases.

Chapter 5 paid attention to developing an analytical model of JL DG MOSFET with the core-shell structure (C-S JLDG MOSFET), including uniform and non-uniform radiation-induced trapped charges effect to evaluate the radiation response and the sensitivity of the device. The analytical models involve surface potential, drain current, threshold voltage, and subsequent sensitivity calculation in terms of threshold voltage shift. A considerable increase in the interface charge density across the gate oxide and interface states across the silicon channel/oxide interface of MOSFET is perceived due to the energy deposition from ionization radiation. Therefore, radiation-induced potential distribution, a shift in threshold voltage, and subsequent change in drain current of the device are demonstrated here based on the derived model to validate its radiation sensing feature. Moreover, the sensitivity is calculated through the ratio of threshold voltage-shift to applied dose, where the interface trap charges are correlated with the radiation dose relied in an experimental study. Notably, the proposed work measured the sensitivity for a wide range of applied doses. Finally, the findings from the analytical model got validated against the simulated data extracted using 3D numerical simulation through the SILVACO Atlas device simulator.

The observations find that the core-shell JL structure has better controllability over the gate and is more immune to short channel effects than other contemporary planner structures. As a result, it exhibits a better threshold voltage shift under absorbed irradiation. As a result, our RADFET evolves with some exceptional electrical characteristics with improved sensitivity compared to works of a similar kind reported in contemporary pieces of literature. The recorded sensitivity of the proposed device is 2.03mV/Gy, followed by a threshold voltage of 0.41V, a subthreshold swing of 55.6mV/dec, and an I_{ON}/I_{OFF} ratio of $6.29x10^{12}$ when exposed to radiation ambiance. Furthermore, the device has manifested a linear response in sensitivity property, measured for a wide range of radiation doses, from 30Gy to 3,000 Gy. The fabrication of Core-Shell Junctionless structure is quite feasible now with the modern day's advanced process technology. The derived model incorporating the radiation effects can be thus applied in circuits to predict the radiation exposed device performance. The analytical results also bear a close resemblance to the simulated data, verifying its accuracy. Therefore, we can suggest the proposed RADFET dosimeter as a potential contender compatible with the VLSI integrated circuit with the incentive towards further experimental exploration of it as a sensor device.

Chapter 6 is dedicated to the performance improvement of VLSI circuits by sorting out the routing complexity in backend design. The related work proposed two novel approaches based on the Particle Swarm Optimization algorithm to solve the global routing problem in VLSI domain. At the same time, the performance of the Firefly Algorithm, which is relatively a new metaheuristic than PSO, has been tested for the routing problem. Finally, a comparative study is made among the abovementioned algorithms along with the other three variants of PSO, which have already been established as good routing algorithms in VLSI design. Experiments are conducted to examine the optimization property, rate of convergence, computational time, and robustness of the algorithms and how the algorithms work efficiently in problem space with different distributive topologies.

The results demonstrated that from the perspective of problem spaces, topologically different, the overall performance of PSO-ST [12] is very satisfactory, whereas PSO-SAAC performed best in a nearly uniform distributed problem space. It is also observed that the performance of PSO-C, PSO-MU, and FA is independent of the varied distribution of problem space. Moreover, the new algorithm FA has the best optimization power and has the demerits of maximum computational time, whereas the performance of the proposed algorithm PSO-MU maintains a balance between the optimization and convergence rate. Finally, although

PSO-MU was consistent in random problem space, PSO-C emerged as the best algorithm in the context of robustness.

Hence the work pointed out the individual merits and demerits of the algorithms, best suited for solving the wire-length minimization problem of global routing. It was expected that in the context of optimization, FA outruns PSO, but it is also established that the model of hybridization with some older algorithms can compete with the performance of some newer ones and can do even better. Therefore, the global routing problem in VLSI can be efficiently handled by modern metaheuristics and algorithms developed by hybridizing different swarm intelligence. It is noteworthy that the speed-aware VLSI circuit performance significantly depends on the wire length minimization techniques in the routing phase.

7.2. Future Scope of the Work

The dissertation encompasses all the possible state-of-art technological aspects, including frontend and backend VLSI design aiming to improve the performances of modern integrated circuits. However, there is still some room for potential improvements and possible extensions of the respective works, which may be highlighted for future scope, as follows:

1. Quantum mechanical phenomena are predominant at sub-10nm technological nodes. However, as the ITRS roadmap predicts the futuristics device dimensions below the 10nm, it will be essential to consider the quantum effect in characterizing the electrostatics of next-generation devices. Therefore, the quantum correction models will be considered in the simulation process and side-by-side in analytical modeling for subsequent validation of analytical results with the simulation data. Moreover, 2-D Poisson-Schrödinger solver must be incorporated to secure more accurate results.

2. It has become a general practice to derive the drain current expression of the Tunnel Field Effect Transistor by using Kane's local tunneling model. Whereas the non-local tunneling models are more accurate in this regard, though handling the mathematical complexity is a great concern. With the increasing development of TFET structures, deploying non-local BTBT and line tunneling concepts is recommended while formulating the drive current.

3. There are many nonlinearities observed in terms of glitches, inaccurate voltage levels, etc., in output responses of the CMOS-like inverter circuit made of TFET device. Therefore, it is the technology's call to refine the Verilog-A modeling by suitably incorporating the capacitive model to characterize the device electrostatics accurately. Furthermore, the circuit model

should also be reconstructed to eliminate the impure responses caused by device parasitic elements.

4. Global routing has been a challenging area for researchers looking forward to the performance optimization of VLSI circuits. Swarm intelligence has always been an intelligent tool to handle the complexity of the routing process. However, there are very few works reported exploring metaheuristics in wire length optimization. Moreover, hybridization is an essential and effective concept of merging more than one algorithm together, in order to acquire even better results. Therefore, enough scopes are there to implement hybridized evolutionary computations in the global routing phase to improve the circuit performance in terms of power and speed.