Nanoscale III-V Compound Semiconductor Field Effect Transistors for High Performance Analog and Logic Applications

Thesis submitted

by

Sumedha Dasgupta

Doctor of Philosophy (Engineering)

Department of Electronics & Telecommunication Engineering

Faculty Council of Engineering & Technology

Jadavpur University,

Kolkata, India

2023

JADAVPUR UNIVERSITY
KOLKATA-700032, INDIA

INDEX NO.140/17/E

1. Title of the thesis: **Nanoscale III-V Compound Semiconductor Field Effect Transistors for High Performance Analog and Logic Applications**

2. Name, Designation & Institution of the Supervisor/s:

Dr. Chandrima Mondal
Assistant Professor,
Department of Electronics & Telecommunication Engineering
Jadavpur University,
Kolkata-700032, India

“Statement of Originality”

I, **SUMEDHA DASGUPTA** registered on **29.3.17** do hereby declare that this thesis entitled “**Nanoscale III-V Compound Semiconductor Field Effect Transistors for High Performance Analog and Logic Applications**” contains literature survey and original research work done by the undersigned candidate as part of Doctoral studies.

All information in this thesis have been obtained and presented in accordance with existing academic rules and ethical conduct. I declare that, as required by these rules and conduct, I havefully cited and referred all materials and results that are not original to this work.

I also declare that I have checked this thesis as per the “Policy on Anti Plagiarism, Jadavpur University, 2019”, and the level of similarity as checked by iThenticate software is **1%**.

Signature of Candidate: Sumedha Dasgupta

Date : 9/11/23

Certified by Supervisor:(Signature with date, seal)

Chandrima Mondal
09.11.2023
DR. CHANDRIMA MONDAL
Kolkata-700032

CERTIFICATE FROM THE SUPERVISOR

This is to certify that the thesis entitled "**Nanoscale III-V Compound Semiconductor Field Effect Transistors for High Performance Analog and Logic Applications**" submitted by **Smt. SUMEDHA DASGUPTA**, who got her name registered on **29.3.17** for the award of Ph.D. (Engg.) degree of Jadavpur University is absolutely based upon her own work under the supervision of **Dr. CHANDRIMA MONDAL** and that neither her thesis nor any part of the thesis has been submitted for any degree/ diploma or any other academic award anywhere before.

Chandrima Mondal 09.11.2023

Signature of the Supervisor and date with Office Seal

DR. CHANDRIMA MONDAL
Professor
Department of Electronics and Telecommunication Engineering
Jadavpur University
Kolkata-700032

PUBLICATION OF THE AUTHOR

JOURNAL PUBLICATIONS

[1] **Sumedha Dasgupta**, Chandrima Mondal and Abhijit Biswas,"Role of grooving angle of 14-nm InAs quantum well for improvement of analog/RF and linearity performance," IET circuits Devices and Systems, October, 2019.https://doi.org/10.1049/iet-cds.2019.0064

[2] **Sumedha Dasgupta**, Chandrima Mondal and Abhijit Biswas, "Effect of temperature and channel thickness on digital and analog performance of InAs Quantum Well nMOSFETs," Microsystems Technologies, pp.1-7,October, 2019.https://doi.org/10.1007/s00542-019-04657-z

CONFERENCE PUBLICATIONS

[1] **Sumedha Dasgupta**, Chandrima Mondal and Abhijit Biswas, "Effect of Grooving Angle on Analog Performance of InGaSb Quantum Well p-MOSFET," Codec 2023, Accepted.

[2] **Sumedha Dasgupta**, Chandrima Mondal and Abhijit Biswas,"Impact of Channel Thickness on Single –Event Transient in InAs quantum-well n-MOSFETs," in Proceedings of IEEE Calcutta Conference (Calcon), pp. 71-74, 2022. ISBN: 978-1-6654-6241-9

[3] **Sumedha Dasgupta**, Chandrima Mondal and Abhijit Biswas, "Reduction of Harmonic Distortion of 14-nm InAs quantum well nMOSFET for high DC to AC conversion and high voltage gain," 4th IEEE Electron Devices Technology and Manufacturing (EDTM) Conference Proceedings of Technical Papers, Malayasia, pp. 28-31,April,2020.ISBN: 978-1-7281-2539-8

[4] **Sumedha Dasgupta**, Chandrima Mondal and Abhijit Biswas, "Effect of temperature on digital and analog performance of InAs Quantum Well n-MOSFETs," in Proc. 6th International Conference on Microelectronics, Circuits and Systems (MICRO 2019), Kolkata, pp. 72-77, 2019.ISBN : 81-85824-46-4

[5] **Sumedha Dasgupta**, Chandrima Mondal and Abhijit Biswas,"Impact of Channel Thickness of Nanoscale InAs on insulator MOSFETs for Analog/RF Circuit Applications," in Proc. 4th International Conference on Electronics and Communication Engineering (ICIECE), Hyderabad, pp. 383-387, 2015 ISBN: 973-93-85100-41-3

COMMUNICATED

Sumedha Dasgupta, Chandrima Mondal and Abhijit Biswas, "Radiation Resilience and Performance Analysis of InAs Quantum Well n-MOSFETs with Varied Groove Angles"

Acknowledgement

I would like to express my sincere gratitude to all those people who have helped me in my journey towards my PhD degree.

First, I would like to sincerely thank our Head of the Department, Prof. Manotosh Biswas and Prof. Ananda Shankar Chowdhury, Prof. Sheli Sinha Chaudhuri , Prof. P. Venkateswaran and all other respected PRC committee members for allowing me to do my research work in the Department of Electronics & Telecommunication Engineering, Jadavpur University.

I would like to express my deepest gratitude to my supervisor Dr. Chandrima Mondal (Jadavpur University) for her constant guidance, support and encouragements towards fulfillment of my thesis work. I would like to express my heartfelt gratitude to Prof. Abhijit Biswas (University of Calcutta) for his invaluable suggestions during my work.

I would like to acknowledge RUSA 2.0 for providing financial support through project bearing Ref no.R-11/759/19 dated 27/06/2019 and SMDP-C2SD project sponsored by DeitY, Government of India.

Finally, I would like to thank my family for all their love, support and sacrifice and their consistent encouragement that contributed significantly to my academic work and I dedicate my work to them in the most sincere way I can do. And, this endeavor definitely would not have been possible without the constant help of my lab mates.

Sumedha Dasgupta
9/11/23

Jadavpur University
Kolkata-700032

(Sumedha Dasgupta)

ABSTRACT

CMOS technology utilizing high-mobility InAs based channels is expected to be one of the promising devices for high-performance and low-power analog circuits in the future. Low effective mass of InAs makes mobility of electrons in InAs to be about 20 times that of Silicon at room temperature making it applicable for high speed applications. However, the most important critical issue faced with InAs based devices is the problem of leakage current. But, device/process/integration technologies of InAs based n-MOSFETs for meeting this requirement for future node MOSFETs are being continuously explored.

Moreover, keeping pace with the development of III-V CMOS technology and the search to get newer materials through combinations of III-V compound semiconductors, thin-body InGaSb semiconductors are emerging out as the choice channel material for designing high mobility p-channel MOSFETs with improved OFF -state characteristics.

The present work deals with the device physics and design of thin-body InAs based on-insulator structure as well as with quantum-well n-MOSFET structure having raised source-drain architecture. This also includes a study on the device performance of thin-body InGaSb based quantum well p-MOSFET having raised source-drain architecture. A detailed investigation of the analog and digital as well as linearity performance of InAs n-MOSFET and InGaSb p-MOSFET has been made. The effect of variation of channel thickness and angle of grooving on the analog parameters viz. transconductance (g_m), output conductance (g_d) tranconductance efficiency factor (g_m/I_D), device gain (g_m/g_d) in a wide temperature range of 150 K to 300 K has been studied. Digital performance parameters like on current (I_{ON}), off current (I_{OFF}), I_{ON}-I_{OFF} ratio and intrinsic delay within the same temperature range has also been well explored.

Apart from device level analysis, the author has performed the circuit level analysis also to understand the linearity analysis of the circuit built with device. Distortion characteristics, extracted by integral function method (IFM) in terms of second and third order harmonic distortions (HD_2 and HD_3) and also total harmonic distortion (THD) of common-source amplifier built with InAs quantum-well n-MOSFET with varying groove angle has been studied.

Research on radiation effects in the category of single event effects on InAs quantum well n-MOSFET with raised source- drain architecture in the presence of Neon, Krypton and Xenon ions has also been explored by the author. This study relates to the changes caused in the output response of a device by an energetic particle, striking the middle of the device channel. Transient response analysis, total collected charge, charge collection efficiency, full width at half maximum (FWHM), rise time and pulse width with respect to changed angle of grooving and channel thickness are included in this study.

TABLE OF CONTENTS

LIST OF TABLES

Chapter 5: Enhancing Radiation Resilience in InAs Quantum Well n-MOSFETs through Optimized Groove Geometry and Channel Thickness: A Study of Single Event Transients under Varied Bias Conditions

LIST OF FIGURES

Fig. 3.19 : Variation of ON-current with temperature for different values of t_{ch} viz. 5 nm ,8 nm and 10 nm of InAs quantum well n-MOSFET for V_{DS}=0.8 V and L_{ch} = 14 nm.

Fig. 3.20: Variation of OFF-current with temperature for different values of t_{ch} viz. 5 nm ,8 nm and 10 nm of InAs quantum well n-MOSFET for V_{DS}=0.4 V and L_{ch} = 14 nm.

Fig. 3.21:2-D electron concentration profile in the channel under the gate for device (a) t_{ch}=5nm and T=300K (b) t_{ch}=5nm and T=150K (c) t_{ch}=10nm and T=300K (d) t_{ch}=10nm and T=150 K of InAs quantum well n-MOSFET at V_{DS} = 0.4V and V_{GT}= 0.4V for L_{ch}=14nm.The left and right sides indicate source and drain ends, respectively.

Fig. 3.22:2-D effective electric field profile in the channel under the gate for device (a) t_{ch}=5nm and T=300K (b) t_{ch}=5nm and T=150K (c) t_{ch}=10nm and T=300K (d) t_{ch}=10nm and T=150K of InAs quantum well n-MOSFET at V_{DS} = 0.4V and V_{GT}= 0.4V for L_{ch}=14nm.The left and right sides indicate source and drain ends, respectively.

Fig. 3.23 : Plot of I_{ON}/I_{OFF} with temperature for different values of t_{ch} viz. 5 nm ,8 nm and 10 nm of InAs quantum well n-MOSFET for V_{DS}=0.8 V and L_{ch} = 14 nm.
Fig.4.24: Plot of Intrinsic Delay with temperature for different values of t_{ch} viz. 5 nm ,8 nm and 10 nm of InAs quantum well n-MOSFET for V_{DS}=0.8 V and L_{ch} = 14 nm.

Fig. 3.25: Transfer characteristics at T=300K as a function of V_{GT} for different values of t_{ch} viz. 5 nm , 8 nm and 10 nm of InAs quantum well n-MOSFET for V_{DS}=0.4 V and L_{ch} = 14 nm.

Fig. 3.26:Variation of (a) transconductance (g_m)with respect to V_{GT} at T=300K (b) Peak values of transconductance (g_m) with respect to temperature of InAs quantum well n-MOSFET at V_{DS} = 0.4V for L_{ch}=14nm.

Fig. 3.27: Variation of (a) output conductance (g_d)with respect to V_{GT} at T=300K (b) output conductance (g_d)with respect to temperature of InAs quantum well n-MOSFET at V_{DS} = 0.4V for L_{ch}=14nm.

Fig. 3.28:Variation of (a) transconductance generation factor (g_m/I_D)with respect to V_{GT} at T=300K b Peak values of transconductance generation factor with respect to temperature of InAs quantum well n-MOSFET at V_{DS} = 0.4V for L_{ch}=14nm.

Fig. 3.29:Variation of (a) intrinsic gain with respect to V_{GT} at T=300K (b) Peak values of intrinsic gain with respect to temperature of InAs quantum well n-MOSFET at V_{DS} = 0.4V for L_{ch}=14nm.

Fig. 3.30: Simulated transfer characteristics with respect toVGT for InGaSb quantum well p-MOSFET with Lch = 14 nm and tch = 5 nm and θ varying from 40^0 to 90^0 at V_{DS} =- 0.5 V.

Fig. 3.31:2-D electric field distribution for (a)θ= 40^0 (b)θ= $90^0$and 2-D carrier distribution for (c)θ= 40^0 and (d) θ= 90^0 for InGaSb quantum well p-MOSFET with L_{ch} = 14 nm and t_{ch} = 5 nm

architecture. The gate length (L_G) or channel length (L_{ch}) beneath HfO_2 is 14 nm with L_{SD} as the spacing between the source and drain regions at the top of the device and θ as the angle of grooving.

Fig. 5.2: Simulated transient current at V_{GS} = 0.0 V and V_{DS} = 0.5 V for InAs quantum well n-MOSFET with L_{ch} = 14 nm and t_{ch} varying as 4 nm, 7 nm and 10 nm.

Fig. 5.3: Total collected charge for the total duration of radiation and charge collection efficiency at V_{GS} = 0.0 V and V_{DS} = 0.5 V for InAs quantum well n-MOSFET with L_{ch} = 14 nm and varying t_{ch} from 4 nm to 10 nm.

Fig. 5.4: (a): FWHM and time taken to attain the steady-state after peak-in time (b): Rise time and pulse width of radiation at V_{GS} = 0.0 V and V_{DS} = 0.5 V for InAs quantum well n-MOSFET with L_{ch} = 14 nm and varying t_{ch} from 4 nm to 10 nm.

Fig. 5.5: Simulated drain current for θ = 40° at (a) V_{GT} = -0.2 V and (b) V_{GT} = 0.3 V (c) maximum change in the drain current due to radiation at V_{DS} = 0.5 V for InAs quantum well n-MOSFET with t_{ch} = 5 nm, L_G = 14 nm, and θ varying as 40°, 60°, 70° and 90° under the influence of Neon, Krypton and Xenon ions.

Fig. 5.6: 2-D electron concentration for (a) θ= 40° under effect of Ne (b) θ= 40° under effect of Kr (c) θ= 40° under effect of Xe (d) θ= 90° under effect of Ne (e) θ= 90° under effect of Kr (f) θ= 90° under effect of Xe at V_{GT} = -0.2 V and V_{DS} = 0.5 V within the time span of t=0 ns and 0.6 ns for InAs quantum well n-MOSFETs with t_{ch} = 5 nm, L_G = 14 nm.

Fig. 5.7: 2-D electron concentration for (a) θ= 40° under effect of Ne (b) θ= 40° under effect of Kr (c) θ= 40° under effect of Xe (d) θ= 90° under effect of Ne (e) θ= 90° under effect of Kr (f) θ= 90° under effect of Xe at V_{GT} =0.3 V and V_{DS} = 0.5 V within the time span of t=0 ns and 0.6 ns for InAs quantum well n-MOSFETs with t_{ch} = 5 nm, L_G = 14 nm.

Fig. 5.8: (a) Total collected charge and (b) charge collection efficiency during the span of radiation with respect to V_{GT} at V_{DS} = 0.5 V for θ varying as 40°, 60°, 70° and 90°for InAs quantum well n-MOSFETs with t_{ch} = 5 nm, L_G = 14 nm under the influence of Neon, Krypton and Xenon ions .Filled symbols represent the influence of Neon, half-filled symbols represent the influence of Krypton, and open symbols represent the influence of Xenon. Rectangle, Circle, Triangle and diamond symbols are used to represent grooving angle of 40°, 60°, 70° and 90°, respectively.

Fig. 5.9: (a) FWHM (b)Time taken to reach steady state after peak-in time with respect to V_{GT} at V_{DS} = 0.5 V for InAs quantum well n-MOSFET with t_{ch} = 5 nm, L_G = 14 nm. Filled symbols represent the influence of Neon, half-filled symbols represent the influence of Krypton, and open symbols represent the influence of Xenon. Rectangle, Circle, Triangle and diamond symbols are used to represent grooving angle of 40°, 60°, 70° and 90°, respectively.

CHAPTER-1

INTRODUCTION

Extensive research and immense development in the field of nanotechnology has created the pathway for the evolution of III-V compound semiconductors, like InAs, InP, GaAs, InSb etc. replacing the conventional Silicon to enable low power and high speed electronics. Many noteworthy features of III-V materials, especially their high electron mobility and lower bandgap are exploited to fabricate high performance MOSFET devices.Various novel architectures like on-insulator structure, asymmetric source-drain structure, raised source-drain structure using III-V channel materials with advanced high-k dielectrics like HfO_2, ZrO_2 are now widely examined in order to study analog, digital and RF performances.Of all these new materials, CMOS technology utilizing high-mobility InAs based n-channels and InGaSb based p-channels are expected to be the promising devices for high-performance and low-power logic in the future.

A detailed literature survey on recent advances on InAs channel n-MOSFET and a short survey on InGaSb based p-MOSFET for modern era has been presented in this chapter.

BACKGROUND

Integrated-circuits (IC) technology has undergone through unmatched technological and economical progress. Nowadays, the field of electronics is identified by extreme low weight and volume, low power consumption, low cost and reliability. The driving force behind the ascent of electronics is “miniaturization” [1.1]. Miniaturization of the fundamental building blocks of electronics has proved to be highly beneficial for the microelectronic industry. Positioning of

large number of transistors on a single chip has become possible due to this concept of miniaturization. This in turn has increased the functionality and has reduced the cost of large variety of integrated circuits. Thus, the major advantages gained as a result of transistor scaling include low cost of manufacturing, increased speed, low power consumption and the ability to perform multiple tasks simultaneously.

Today, the semiconductor industry is mainly dominated by low power metal oxide semiconductor field-effect transistor (MOSFET) which was first fabricated in Bell laboratory in 1962. The development of the semiconductor industry which is primarily driven by low cost and improved performance is nowadays governed by the reducing feature size of its fundamental building block – MOSFET [1.2].

The metal–oxide–semiconductor field-effect transistor (MOSFET) (as shown in Fig. 1.1) is a semiconductor device, widely used for switching and amplifying electronic signals. It has an insulated gate (hence also called IGFET) whose voltage controls the conductivity of the carriers within the device. One unique attribute of this transistor is that its logic characteristics improve when its dimensions are reduced. Because of small sizes, MOSFET can be designed and fabricated in a single chip and thus it has become a core of integrated circuit. [1.3-1.4].

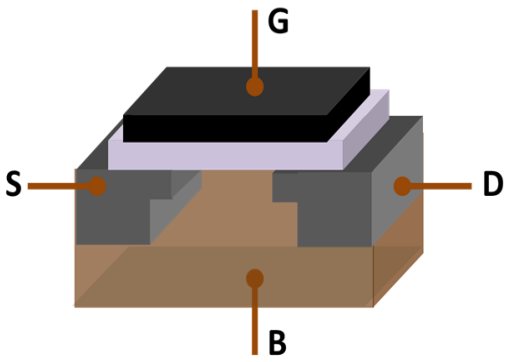


Fig. 1.1: MOSFET showing gate (G), body (B), source (S) and drain (D)

1.1 Introduction to scaling and Moore's law

1.1.1 Moore's law-application in recent trends

The tremendous progress achieved on the scaling of Silicon-based large-scale-integrated circuits (LSIs) technology in the past four decades is driven by Moore's law, which predicted that the transistor density would double every 18 months. This law is the driving force behind the tremendous advancement of the semiconductor industry. [1.5-1.8].

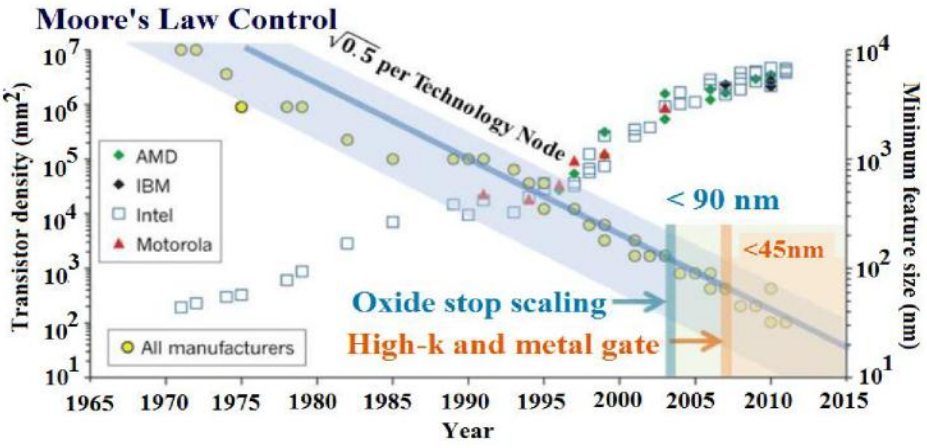


Fig. 1.2: The evolution of transistor gate length (minimum feature size) and the density of transistors in microprocessors over time [1.6]

For instance, Figure 1.2 shows that between 1970 and 2011, the gate length of MOSFETs shrank from 10μm to 28nm (yellow circles; y axis, right), and the number of transistors per square millimetre increased from 200 to over 1 million (diamonds, triangles and squares show data for the four main microprocessor manufacturers; y axis, left). This has also improved the operating frequency of the microprocessors. This is mainly achieved by scaling the transistors following the scaling rule proposed by Robert Dennard et al. [1.9] .The scaling trend of transistors is still evident today and the schedule in which the transistor density increases (2 × every 18 months) is still generally recognized by the roadmap made by the industry.

1.1.2 Scaling of MOSFET

Keeping pace with Moore's Law, MOSFET miniaturization has enormously helped the microelectronic industry in terms of low cost of manufacturing, increased speed, low power consumption and the ability to perform multiple tasks simultaneously [1.10-1.15]. However, there are certain limitations on the scaling of conventional MOSFET (a) limitation of voltage scaling due to the power concern (b) constraints in the reduction of the thickness of gate oxides and (c) controlled reduction of channel length due to increased leakage current. These negative effects of scaling are called "short-channel effects" [1.16-1.20]. These effects mainly includes reduction in the threshold voltage, drain induced barrier lowering (DIBL), hot carrier effect, impact ionization effect, mobility degradation, carrier velocity saturation and channel length modulation[1.21-1.26]. To combat these effects, novel materials and architectural changes are now being introduced. To increase the control of gate over the channel, multi-gate structure using high-k gate dielectrics is adopted. To further reduce the supply voltage, one of possible solutions is to adopt small bandgap, high-mobility channel material such as III-V materials for low power-consumption and to boost the drive current.

1.2 Material Alternative to Silicon

With the spectacular advancement in nanotechnology, high-mobility channel materials combined with innovative architectures are nowadays examined widely as an alternative to Silicon to enable low-power and high speed electronics. For this, III-V compound semiconductors are now being considered as the alternative channel materials which are combined with high-k dielectric material and several novel architectures for future nanoscale devices.[1.27-1.45].Of them, the most important ones are InAs, GaAs, InP, GaP and AlAs.

Table I covers the comparative analysis of the different parameters of conventional Silicon and III-V materials at T=300K. It is evident from Table I that effective electron mass in III-V semiconductors is much low compared to Silicon (Si) and thus have high electron mobility. This increases the ON-current of these semiconductors. Also, being direct semiconductors, III-V semiconductors are used both for electronic and optoelectronic purposes and thus system-on-chip technology can be achieved. However, as the effective mass is low in III-V semiconductors, density of states is low which limits the drain current. Also, dielectric constant is high which increases short channel effects.

Table I: Comparative analysis of the parameters of conventional Silicon and III-V materials at T=300K

PARAMETER	**InAs**	GaAs	InP	Ge	Si
Type	**Direct**	Direct	Direct	Indirect	Indirect
Bandgap (eV)	**0.35**	1.42	1.35	0.66	1.12
Effective mass of electrons	**$0.023m_o$**	$0.063\ m_o$	$0.08\ m_o$	$0.041m_o$	$0.98m_o$
Electron mobility ($cm^2/V.s$)	**40000**	8500	4600	3900	1500
Hole mobility ($cm^2/V.s$)	**500**	400	150	1900	450
Dielectric constant	**14.8**	13.1	12.1	16	11.9

m_o= rest mass of electron = 9.1×10^{-31}Kg

1.3 InAs as the choice channel material for n-MOSFET for this work

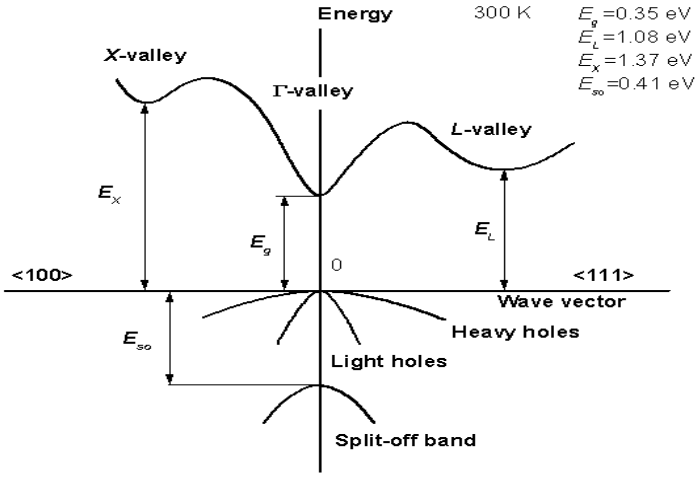


Fig.1.3: Bandstructure of InAs at T=300K

Amongst the binary III-V semiconductors, InAs exhibits the highest electron mobility of 40,000 $cm^2/V.s$ at room temperature, which is,for instance, twenty times higher than in Si, making it suitable for high speed applications. Moreover, the lower energy gap (E_g = 0.35 eV at T=300K) of InAs allows supply voltage scaling enabling such devices suitable for low power applications. Also, being direct semiconductor, InAs finds applications both in electronic and optoelectronic fields. InAs is also preferred because of it's large Bohr radius (34 nm) which makes heavy quantization possible at sub-20-nm thicknesses. As mean free length is about 150 nm, so InAs can well be used as ballistic transistors. Thus, InAs due to its excellent transport and physical properties has become an intriguing choice as a channel material for high speed, low power devices [1.46-1.54].

1.3.1 Issues of using InAs as the channel material

Despite the outstanding electron transport properties in InAs, it suffers from a couple of disadvantages. The lower value of density of states in such a material, which arises due to lighter

effective mass of electrons, limits the drain current [1.28]. Moreover, InAs exhibits a larger amount of leakage current due to low energy bandgap.

1.3.2 Recent Advances made in InAs channel MOSFETs to combat the issues

1.3.2.1 Device design

To increase the gate control of the channel and reduce short channel effects, several researchers are adopting bandgap engineering and novel architectures like on-insulator structures, inclusion of vertical spacers between the channel and the N^+ S/D, nanowires etc. OFF state characteristics like leakage current, subthreshold swing are highly improved using these structures. Some researchers have also performed 3-D simulations on single-gate (SG), double-gate (DG), and gate-all-around (GAA) InAs BTBT transistors with different dimensions to study the subthreshold and ON-current characteristics.

Takei *et al.* have explored the effect of body thickness (5-13 nm) of InAsOI NMOS with a channel length of 200 nm (Fig. 1.4) on the bandgap, leakage currents, subthreshold slope, transconductance and gate delay. The results show that with channel thickness reduction from 13 nm to 5 nm, bandgap of the devices increases from 0.4eV to 0.54eV for which OFF current decreases from 1500 nA/ μm to 4 nA/ μm and subthreshold swing changes from 180 mV/decade to 115 mV/decade due to enhanced gate coupling efficiency. However, due to this scaling, there is a compromise in peak value of transconductance which changes from 1.72 mS/μm to 0.65 mS/μm and also in gate delay (= $C_{ox}.V_{DD}/I_{ON}$) [1.55].

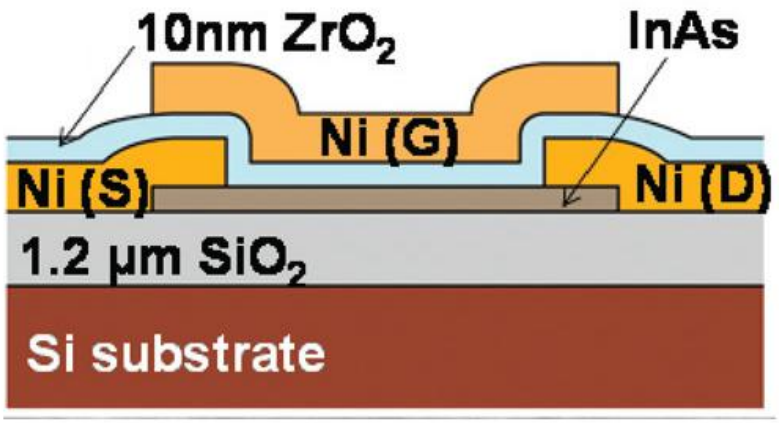


Fig.1.4: Cross-sectional schematic of the top-gated InAs XOI FETs [1.55]

Source-to-drain tunneling is becoming a major issue in sub 10-nm channel, especially while using III-V material due to low effective masses. Dutta *et al*. have worked on the concept of thickness dependent effective mass and bandgap [1.56] and using that, they have demonstrated that in extremely thinned InAs and InSb devices, with decrement in channel thickness, there is increment in effective mass and bandgap (Fig. 1.5). They have also shown that as channel thickness decreases, there is also decrement in the energy separation in the L and X valley minimas from Γ valley minimum which helps in multivalley transport thus reduces the unwanted source drain tunneling.

Lee *et al*. [1.57] has reported a novel architecture of raised source/drain InAs/$In_{0.53}Ga_{0.47}As$ channel MOSFETs by placing a vertical undoped spacer using intrinsic $In_{0.53}Ga_{0.47}As$ between the channel and the N^+ source/drain (Fig. 1.6).The introduction of the spacer improves OFF-state characteristics at a high drain bias (V_{DS}) but does not have significant effect on ON-current. They have reported that such a device with 4.5 nm thick InAs channel layer, 8 nm thick spacer and 55 nm channel length displays peak g_m of 2.4 mS/µm, 96mV/dec SS and 130mV/V DIBL at V_{DS}=0.5V.

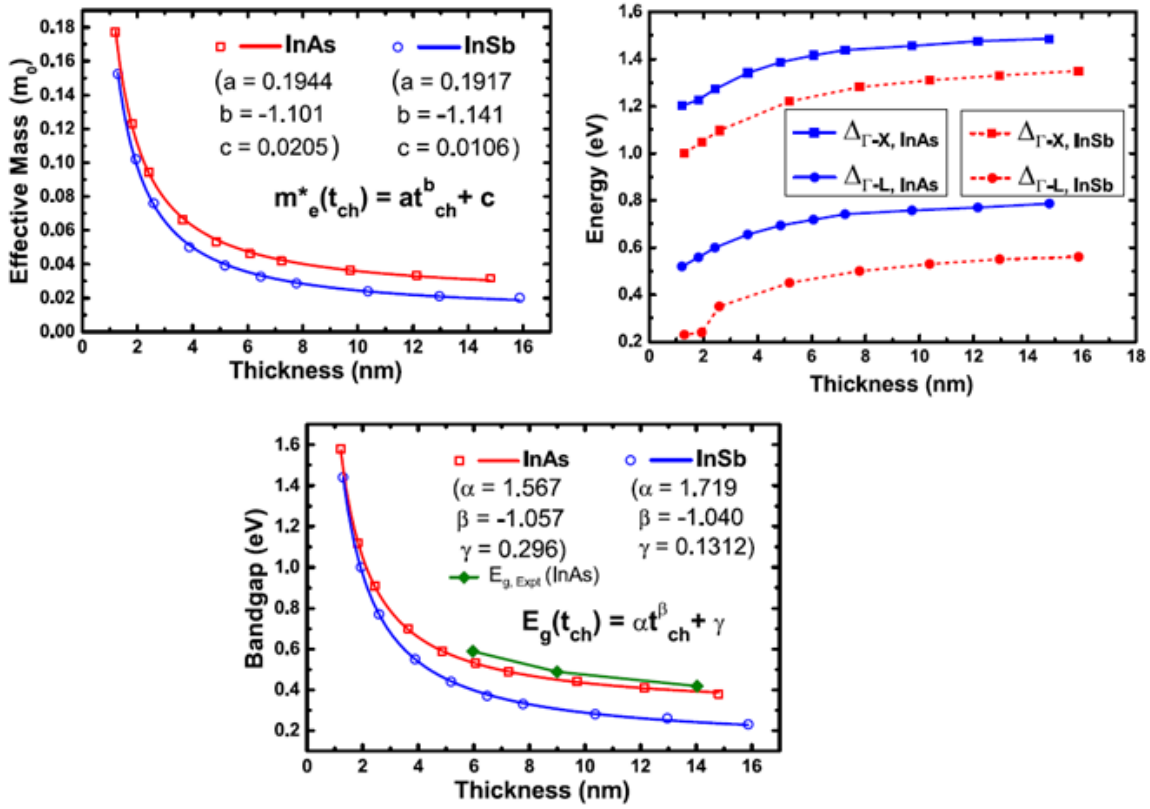


Fig. 1.5: Dependency of Effective Mass interband energy and bandgap energy with thickness in InAs and InSb [1.56]

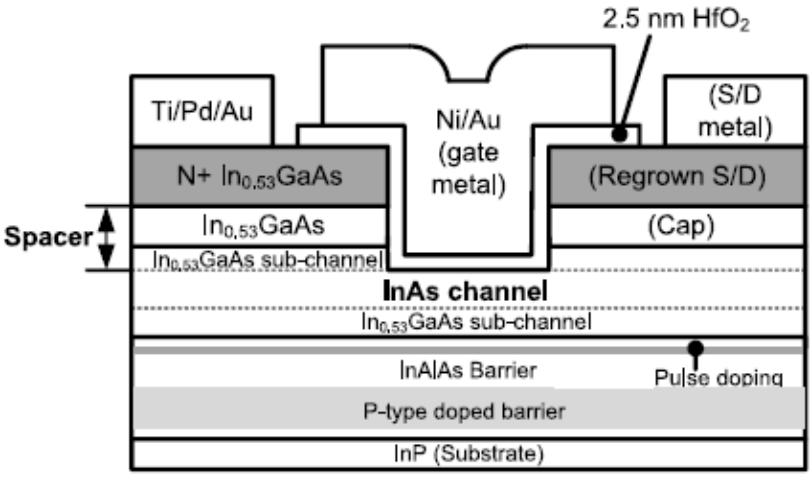


Fig.1.6: Device structure with vertical spacer [1.57]

The concept of subchannel has been used to increase carrier transport and electron confinement in the channel. Delta doping is used to supply carriers to S/D access region, to improve subthreshold swing and reduce parasitic R_{SD}. [1.58] shows carrier density as a function of gate potential for various delta doping in InAs quantum well MOSFET. Delta doping of $1x10^{12}/cm^2$ results in both low R_{SD} and excellent electrostatic control.

Furthermore in 2014, Lee and his group demonstrated that devices with thick vertical spacer thickness shows only moderate improvement at V_{DS} = 0.1 V but improves the FET performances in the high-field region at all gate lengths. Devices with t_{ch}=5nm and L_g= 1 μm show subthreshold swing of 68.86 mV/dec and 66.07 mV/dec at V_{DS} =0.1V whereas the values are 79 mV/dec and 71.32 mV/dec at V_{DS}=0.5V for t_{spacer}=2nm and 15nm, respectively [1.59].

Semiconductor nanowires (NWs) are very useful for high-performance nanoelectronics [1.60-1.65]. InAs based NWs are becoming very promising mainly because of their high electron mobility.

To study the effect of increased gate control on channel, Gerhard Klimeck and his group [1.66] performed 3-D simulations on Single-gate, Double-gate, and Gate-all-around InAs BTBT transistors with varied dimensions using an atomistic full-band Schrödinger–Poisson solver. Nowadays, tunnel FETs (TFETs) are also studied widely. InAs based TFETs are gaining importance through optimization of structure and parameters like doping concentration and supply voltage. Also, to establish InAs TFETs as a potential logic gate, their high-frequency properties are also studied.[1.67]

1.3.2.2 Surface/interface treatment

Use of high-k materials on Silicon MOSFETs brought new dimensions to III-V study. Research in this domain has highlighted the fact that III–V MOS interfaces suffer from the problem of

high density of interface states and interface defects. So, to improve the quality of the interface, atomic layer deposition (ALD) and forming gas anneal (FGA) techniques for high-k gate dielectric on a III-V substrate are adopted which shows drastic improvement in subthreshold characteristics and ON/OFF current ratio[1.68-1.71] as shown in Fig. 1.7. Some researchers have also worked on the effect of substrate orientation to improve the interface charge density [1.72-1.76].

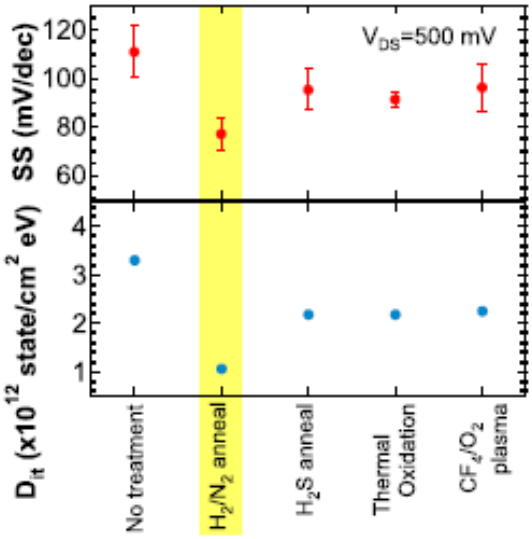


Fig.1.7: Average SS and extracted D_{it} of XOI FETs as a function of different surface/interface treatments [1.68]

1.3.2.3 Non-parabolicity, ballistic nature and intersubband transition of InAs

Researches are being carried out to study the impact of band structure on deeply scaled III–V devices. The results show that in InAs, during strong quantum confinement, the parabolic effective mass model with bulk effective masses is no longer valid and the conduction band nonparabolicity factor comes into play [1.56] which is to be considered for ultra-thin bodies. J. Wagner *et al*. included this effect of nonparabolicity in the study intersubband excitations in

InAs/A1Sb QW's and they found good agreement with theoretical predictions including nonparabolicities [1.77-1.79].

Some group has also projected that InAs can potentially be used as ballistic transistors because of its relatively long bulk electron mean free path (λ=150 nm).[1.80-1.82]

Zeng *et al.* has also demonstrated the function of a gate controlled InAs based tunneling diode with multiple subband contributions [1.83].

1.3.2.4 Parasitic Resistance

Another factor that becomes prominent with the scaling of devices is the existence of the parasitic resistance. The large RS/D will become a serious concern if it is not optimized, as it could limit the ON-state performance of InAs transistors [1.84]. For further improvement of device performance, proper control of this factor is important.

1.3.2.5 Use of InAs to study effect of radiation on device performance

Study of III-V based device performance under effect of environmental radiation is a growing concern in the semiconductor industry. InAs based devices are nowadays explored to know the drain current pattern under radiation effects so as to build up radiation-tolerant circuits which can be used in hostile environments [1.85-1.98].

1.3.2.6 Use of InAs in optical field

Marshall *et al* has presented a systematic study the findings of which have made InAs to make its application in optical communications [1.99-1.104]. On examining various factors like impact

ionization, avalanche multiplication and excess noise in InAs diodes, they have confirmed InAs based “electron avalanche photodiode” to be highly desirable in the field of optics.

1.4 A short survey on InGaSb as the choice channel material for p-MOSFET for this work

One of the dominating challenges in III-V materials, is to maximize the hole mobility in *p*-channel FETs for the design of complementary circuits. In 2010, M.G. Ancona *et al.* conducted numerical modeling to study p-channel FETs with InSb, GaSb and InGaSb channels. They concluded that InGaSb devices provide the best balance of speed and power dissipation for the design of complementary circuits and for low power and high speed applications [1.105]. Bennett et al. also used InGaSb as the channel material for making p-MOS for the design of complementary circuits that can operate at extremely low power. They have studied the effect of strain on effective mass and mobility of InGaSb, the strain of which has been controlled by adjusting the composition. For $In_{0.23}Ga_{0.77}Sb$, effective mass is $0.101m_o$ and mobility at T=300K is $870cm^2/V.s$. These values for $In_{0.41}Ga_{0.59}Sb$ are $0.096\ m_o$ and $1170\ cm^2/V.s$, respectively [1.106]. Alam *et al.* in 2015, studied the ballistic nature of InGaSb XOI n-FET for gate length of 15nm and have found that the drain current increases almost by three times when the channel thickness is reduced from 5 to 3 nm. They have also studied the effect of interface trap states and surface roughness on the device performance. They have concluded that the surface roughness effects the OFF-characteristics greatly but it’s effect on the ON-state is relatively small. Also, by considering the density is in the order of $10^{12}\ eV^{-1}\ cm^{-2}$, the impact of interface states can be compensated. The threshold voltage, SS, and DIBL- all these parameters reduce with the channel thickness highlighting the fact that the performance of thinner channel is better in all aspects.[1.107] S.H. Kim and his group studied the mobility characteristics of

GaSb/InGaSb/GaSb quantum well structure which showed excellent electrical properties in terms of OFF-current, subthreshold swing and effective mobility through optimized insulating barrier and improved interface quality with InGaAs passivation layer [1.108]. III−V electronics also faces the problem of lattice mismatch while integrating high mobility complementary transistors on the same substrate. In 2012, Ali Javey and his group have addressed this problem and they have succeeded in integrating 13 nm thick InAs and 7 nm thick InGaSb layers to make them work as enhancement-mode n- and p- MOSFETs, respectively. As a proof of layout, they also designed CMOS NAND and CMOS NOR logic with the fabricated one. [1.53]

1.5 Motivation of present work

From the literature survey, it is understood that there is a need to develop appropriate models for MOS devices with various architectures using III-V channel materials with advanced high-k dielectrics in order to evaluate analog, digital and RF performances. InAs is specifically ideal for III-V material due to its high electron mobility and also the possibility of heavy quantization at sub-20-nm thicknesses. As mean free length is about 150 nm, so InAs can well be used as ballistic transistors. Also, the combination of narrow band gap and high electron mobility property make InAs suitable for low power, high speed applications. Again, by changing composition, the mobility of holes in InGaSb can be made almost equal to 1500cm^2/V.s at room temperature. Hence, UTB-based InAs/InGaSb MOSFETs on the Si CMOS platform can be strong device structures at more advanced technology nodes.

1.6 Scope of the present work

From the study of the history and the detailed review report, it can be concluded that various novel architectures and many measures are now being explored to improve device

characteristics. However, the present work mainly deals with the device physics and design of thin-body InAs based quantum-well n-MOSFET structure having raised source-drain architecture with varied groove angle. Though raised source-drain architecture has been reported earlier, improvement of device parameters with the variation of the grooving angle is not being reported yet. This work covers a detailed investigation of the analog and digital parameters, linearity performance as well as the radiation tolerance of InAs based n-MOSFET having raised source-drain architecture with varied groove angle and also the analog performance of InGaSb based p-MOSFET having similar architecture.

1.7 Organization of thesis

Chapter 2: Various physics and models that are used in the work are included in this chapter. A detailed review about the various models like mobility model, scattering model, generation and recombination model, transport model are covered in this part. Temperature and thickness dependency of these models are clearly discussed. Physics related to the work on single-event transient effect on device parameters are also included in this chapter. Several fitting parameters of these models are also listed here.

Chapter 3: In this chapter, a comprehensive investigation towards the logic and analog performances of several MOSFET structures over a wide range of temperature and channel thickness is included. Several structures included in this chapter are 30 nm channel length InAs-on-insulator n-MOSFET, one 14 nm channel length quantum well InAs based n-MOSFET with raised source/drain architecture and also one 14 nm channel length quantum well InGaSb based p-MOSFET with raised source/drain architecture. The channel thickness of all these structures is varied in the range of 5 nm to 25 nm. The effect of temperature varying from 300 K down to 150

K is also being considered here. Different digital parameters such as ON-current, OFF-current, their ratio and intrinsic delay and also analog/RF performances in terms of transconductance (g_m), output conductance (g_d), transconductance generation factor (g_m/I_D) ,intrinsic voltage gain (g_m/g_d), unity gain cut-off frequency (f_T) and maximum frequency of oscillation (f_{max}) are reported in this chapter.

Chapter 4: This chapter contains investigation about the effect of variation of the grooving angle (Θ) viz. 20^0 to 90^0, on the analog and linearity performance of 14 nm InAs channel quantum well n-MOSFET having channel thickness of 5 nm and featuring a 2 nm $In_{0.53}Ga_{0.47}As$ layer as the vertical spacer between the channel and N^+ S/D and also on a common-source amplifier circuit made with such a device. Further, the impact of varied channel thickness, viz. 3nm, 6 nm and 8nm on the analog and harmonic distortion parameters for such a device is also included in this chapter. Device parameters that are studied includes transfer characteristics, transconductance (g_m), output conductance (g_d), transconductance efficiency factor (g_m/I_D), intrinsic voltage gain (g_m/g_d) and harmonic distortion parameters such as second and third order harmonic distortions (HD_2 and HD_3) and also total harmonic distortion (THD).

Chapter 5: This chapter covers single-event transient effect of Neon, Krypton and Xenon on the device performance of InAs quantum well n-MOSFET with the angle of grooving varying from 40^0 to 90^0 and channel thickness varying as 4 nm, 7 nm and 10 nm at the channel length of 14 nm. Device performance parameters that are included are total collected charge, charge collection efficiency, full width half maximum (FWHM), pulse width and rise time. High energy ion is considered to be incident in the middle of the channel (other sensitive regions are not being considered) whose effect on the said parameters are studied.

Chapter 6: Finally, the thesis is summed up in the concluding chapter, highlighting the key features of the proposed quantum well device with raised source/drain architecture.

REFERENCES

[1.1] J. S. Kilby, "Invention of the Integrated Circuits," *IEEE Trans. Electron Devices,* vol. 23, p.p 648, 1976. https://doi.org/10.1109/T-ED.1976.18467.

[1.2] D. Kahng, "A Historical Perspective on the Development of MOS Transistors and Related Devices," *IEEE Trans. Electron Devices,* vol. 23 p.p 655, 1976. https://doi.org/ 10.1109/T-ED.1976.18468.

[1.3] T. Sakurai, and A. Richard Newton, "A Simple MOSFET Model for Circuit Analysis," *IEEE Trans. Electron Devices*, vol.38, no.4, pp.887-894,1991.https://doi.org/ 10.1109/16.75219.

[1.4] C. H.Wann, K.Noda, T. Tanaka,M. Yoshida, and C. Hu, "A Comparative Study of Advanced MOSFET concepts," *IEEE Trans. Electron Devices,* vol.43, no.10, pp.1742-1753,1996. https://doi.org/10.1109/16.536820.

[1.5] R.Chau, B. Doyle, S. Datta, J. Kavalieros, K. Zhang, "Integrated nanoelectronics for the future," *Nature Materials,* vol.6, no. 11, pp.810–812,2007. https://doi.org/10.1038/nmat2014.

[1.6] H. Iwai, "Roadmap for 22 nm and beyond,"*Microelectron. Eng*, vol. 86, pp.1520–1528 2009. https://doi.org/10.1016/j.mee.2009.03.129.

[1.7] G.E. Moore ,"Progress in digital integrated circuit," *IEDM Tech. Dig*, pp.11,1975.

[1.8] M. Bohr, "A 30 year retrospective on Dennard's MOSFET scaling paper," *IEEE SSCS Newsletter*, vo.12, no.1,pp. 11-13,2007.

[1.9] R.W. Keyes, "The Impact of Moore's Law," *Solid State Circuits Society Newsletter,* vol. 11, pp. 25-27,2006. https://doi.org/10.1109/N-SSC.2006.4785857.

[1.10] D. E. Liddle,"The Wider Impact of Moore's Law," *IEEE Solid-State Circuits Newsletter*, vol.11, no.3, pp. 28-30,2006. https://doi.org/10.1109/N-SSC.2006.4785858.

[1.11] R. H. Dennard, F. H. Gaensslen, H. H. Yu, V. L. Rideout, E. Bassous, A. R. Leblanc,"Design of ion-implanted MOSFET's with very small physical dimensions," *IEEE Journal of Solid-State Circuits*, vol. SC-9, no.5, pp. 256-267,1974. https://doi.org/10.1109/JSSC.1974.1050511.

[1.12] W. Haensch, E. J. Nowak, R. H. Dennard, P. M. Solomon, A. Bryant, O. H. Dokumaci, A. Kumar, X. Wang, J. B. Johnson, and M. V. Fischetti, "Silicon CMOS devices beyond scaling," *IBM Journal of Research and Development*, vol. 50, No. 4.5, pp. 339-361, 2006. https://doi.org/10.1147/rd.504.0339.

[1.13] J. R.Brews, W. Fichtner, E. H.Nicollian, S. M. Sze," Generalized guide for MOSFET miniaturization," *IEEE Electron Device Lett.*, vol.1, no. 1, pp. 2-4, 1980. https://doi.org/10.1109/EDL.1980.25205.

[1.14] D. J. Frank, R. H. Dennard, E. Nowak, P. M. Solomon, Y. Taur, and H.S. Philip Wong ,"Device scaling limits of Si MOSFETs and their application Dependencies,"*Proceedings of IEEE*, vol.89, no.3,pp. 259–288,2001. https://doi.org/10.1109/5.915374.

[1.15] O. Semenov, A.Vassighi, M.Sachdev, A.Keshavarzi, C. F.Hawkins, "Effect of CMOS Technology Scaling on Thermal Management During Burn-In," *IEEE Transactions on Semiconductor Manufacturing*, vol.16, no.4, pp.686-695,2003.https://doi.org/ 10.1109/TSM.2003.818985.

[1.16] T. Yuan, D. A. Buchanan, C. Wei, D. J. Frank, K. E. Ismail, L. Shih-Hsien, G. A. Sai-Halasz, R. G. Viswanathan, H. J. C. Wann, S. J. Wind, and W. Hon-Sum, "CMOS Scaling into the Nanometer Regime", Proceedings of the IEEE, vol.85, pp. 486-504,1997. https://doi.org/10.1109/5.573737.

[1.17] S.M. Sze, "Physics of Semiconductor Devices", New York, Wiley, 1981.

[1.18] T. Ghani, K. Mistry, P. Packan, S. Thompson, M. Stettler, S. Tyagi, and M. Bohr, "Scaling Challenges and Device Design Requirements for High Performance Sub-50 nm Gate Length Planar CMOS Transistors,"*Symposium on VLSI Technology*, pp. 174-175, 2000. https://doi.org/10.1109/VLSIT.2000.852814.

[1.19] Semiconductor Industry Association, "National Technology Roadmap for semiconductor," *Asutin, Texas: Sematech Inc.*, 1997

[1.20] Y. Taur, "CMOS design near the limit of scaling," *IBM Journal of Research and Development*, vol. 46, no. 2.3, pp. 213-222, 2010. https://doi.org/10.1147/rd.462.0213.

[1.21] M. Schulz, "The end of the road of Silicon," *Nature*, vol. 399, no. 24, pp. 729-730,1999. https://doi.org/10.1038/21526.

[1.22] M. Bohr, "Moore's Law in the Innovation Era," In Proc: *SPIE*, vol. 7974, pp.797402-1-8, 2011. https://doi.org/10.1117/12.883462.

[1.23] C.W. Pearce, and D.S. Yaney,"Short channel effects in MOSFETs," IEEE Electron Device Letters, vol. EDL-6, no. 7,pp. 326-328, 1985.https://doi.org/ 10.1109/EDL.1985.26143.

[1.24] D. Duarte, N. Vijaykrishnan, Mj. Irwin, H.S. Kim, and G. McFarland, " Impact of Scaling on the Effectiveness of Dynamic Power Reduction Schemes," *Proceedings of the*

IEEE International Conference on Computer Design: VLSI in Computers and Processors (ICCD'02), 2002. https://doi.org/10.1109/ICCD.2002.1106798.

[1.25] Y, Bin, C.H.J. Wann, E.D. Nowak, K. Noda, and H.Chenming, "Short-channel effect improved by lateral channel-engineering in deep-submicronmeter MOSFET's," *IEEE Transactions on Electron Devices*, vol.44, no.4, pp.627-634, 1997. https://doi.org/10.1109/16.563368.

[1.26] M. Shur,"Physics of Semiconductor Devices,"Prentice Hall, Englewood Cliffs, NJ,1990.

[1.27] T. Ytterdal, S. H.Kim,K. Lee, and T. A.Fjeldly,"A new approach for modeling of current degradation in hot electron damaged LDD N-MOSFETs," *IEEE Trans. Electron Devices, ED*. vol.42, pp.362–364,1995. https://doi.org/10.1109/16.370054.

[1.28] J.A.delAlamo,"Nanometer-scale electronics with III-V compound semiconductors,"*Nature*,vol.479, no.17, pp.317-323,2011.https://doi.org/ 10.1038/nature10677.

[1.29] I.Vurgaftman, J.R. Meyer, and L.R. Ram-Mohan,"Band parameters for III–V compound semiconductors and their alloys,"*Journal of Applied Physics*, vol.89, no.11, 2001. https://doi.org/10.1063/1.1368156.

[1.30] R. Chau, S. Datta, and A. Majumdar, "Opportunities and Challenges of III-V Nanoelectronics for Future High-Speed, Low-Power Logic Applications," *IEEE Compound Semiconductor Integrated Circuit Symposium, CSIC '05*, 2005. https://doi.org/ 10.1109/CSICS.2005.1531740.

[1.31] A.Lubow, S. I. Beigi, and T. P. Ma, "Comparison of drive currents in metal-oxide-semiconductor field-effect transistors made of Si, Ge, GaAs, InGaAs, and InAs

channels," *Applied Physics Letters*, vol. 96, 122105 ,2010. https://doi.org/ https://doi.org/10.1063/1.3367708.

[1.32] K. L. Low, Y.C. Yeo, and G. Liang, "Ultimate Performance Projection of Ultrathin Body Transistor Based on Group IV, III-V, and 2-D-Materials,"*IEEE Transactions on Electron Devices*, vol. 63, no.2, pp.773-780, 2016. https://doi.org/10.1109/TED.2015.2508815.

[1.33] U. P.Gomes, Y. K. Yadav, S. Chowdhury , K.Ranjan, S.Rathi, and D.Biswas,"Prospects of III-Vs for logic applications," *Journal of Nano and Electronic Physics*, vol. 4 no.2,2012.

[1.34] S.Oktyabrsky, and P.Ye, "Fundamentals of III–V Semiconductor MOSFETs," Edited volume, Springer, NY, USA ,2010.

[1.35] P. D.Ye, "Main determinants for III-V metal-oxide-semiconductor field-effect Transistors. *J. Vac. Sci. Technol. A*, vol.26,no.4, pp.697–704,2008. https://doi.org/10.1116/1.2905246.

[1.36] Y. Q. Wu, Y. Xuan, T. Shen, P. D.Ye, Z.Cheng, and A.Lochtefeld, "Enhancement mode InP n-channel metal-oxide-semiconductor field-effect-transistors with atomic-layer deposited Al_2O_3 dielectrics," *Appl. Phys. Lett*, vol.91, no.2, 2007. https://doi.org/10.1063/1.2756106.

[1.37] Y.Wu, P.Ye, G. Wilk, and B. Yang,"GaN metal-oxide-semiconductor field effect transistorwith atomic layer deposited Al_2O_3 as gate dielectric," *Mater. Sci. Eng. B*, vol.135**,** no.3,pp. 282–284, 2006. https://doi.org/10.1016/j.mseb.2006.08.020.

[1.38] X. Jiang, Q. Xiong, S. Nam, F.Qian, Y. Li, and C. M. Lieber, "InAs/InP radial nanowire heterostructures as high electron mobility devices," *Nano Lett.*,vol.7, pp.3214-3218,2007. https://doi.org/10.1021/nl072024a.

[1.39] R.Terao, T.Kanazawa, S. Ikeda, Y.Yonai, A. Kato, and Y. Miyamoto,"InP/InGaAs composite MOSFETs with regrown source and Al2O3 gate dielectric exhibiting maximum drain current exceeding 1.3 mA/μm,"*Appl. Phys. Exp.*, vol.4, no.5, 054201 ,2011. https://doi.org/ 10.1143/APEX.4.099202.

[1.40] M.Radosavljevic, B. C. Kung,S. Corcoran, G.Dewey, M. K.Hudait, J. M.Fastenau, J.Kavalieros, W. K. Liu, D.Lubyshev, M. Metz, K.Millard, N.Mukherjee, W.Rachmady, U.Shah, and R.Chau ,"Advanced high-k gate dielectric for high performance short channel In0.7Ga0.3As quantum; well field effect transistor on silicon substrate for low power logic applications," in *Proc IEDM Tech. Dig*., pp.319-322, 2009. https://doi.org/10.1109/IEDM.2009.5424361.

[1.41] J. Robertson, and B.Falabretti, "Band offsets of high-k gate oxide on III–VSemiconductors,"*J. Appl. Phys*., vol. 100, no.1, 014111-1-8, 2006. https://doi.org/10.1063/1.2213170.

[1.42] M, Jiongjiong, E Lind, and L-E Wernersson,"Asymmetric InGaAs/InP MOSFETs With Source/Drain Engineering," *IEEE Electron Device Letters*, vol. 35, no.5, pp.515-517,2014. https://doi.org/10.1109/LED.2014.2308925.

[1.43] S. Tewari, A. Biswas, and A. Mallik,"Impact of a Spacer Layer on the Analog Performance of Asymmetric InP/InGaAs nMOSFETs," *IEEE Transaction on Electron Devices*,vol. 63, no. 6, pp. 2313-2320,2016. https://doi.org/ 10.1109/TED.2016.2548518.

[1.44] D. Han, D. C. Ruiz , A. M. Arabhavi , O. J. S. Ostinelli , and C. R. Bolognesi , "High-Speed Steep-Slope GaInAs Impact Ionization MOSFETs (I-MOS) With SS = 1.25 mV/dec—Part II: Dynamic Switching and RF Performance, **"** *IEEE Transactions on Electron Devices*, vol. 69, no. 7, pp. 3549-3556, 2022.https://doi.org/ 10.1109/TED.2022.3171739.

[1.45] S. Baskaran, R. Saravana, V. Saminathan, R. Poornachandran, N. Mohan, and V. Janakiraman ,**"**Impact of High-K and Gate-to-Drain Spacing in InGaAs/InAs/InGaAs-based DG-MOS-HEMT for Low-leakage and High-frequency Applications," *IETE Journal of Research*, 2021. https://doi.org/10.1080/03772063.2021.1929517.

[1.46] P.Paramasivam, N.Gowthaman, and V. M. Srivastava," Design and Analysis of InP/InAs/AlGaAs Based Cylindrical Surrounding Double-Gate (CSDG) MOSFETs With La_2O_3 for 5-nm Technology," *IEEE Access*, vol.9, pp.159566-159576,2021. https://doi.org/ 10.1109/ACCESS.2021.3131094.

[1.47] G. Sujatha, N. Mohankumar, R. Poornachandran, R. Saravana, G.S. Mishra, V. Mahesh,and M. Arunkumar, "Noise Characterization of InAs Based Composite Channel DG -MOSHEMT with Different Gate Dielectrics," *Silicon*, vol.14, pp. 1925–1933,2022. https://doi.org/10.1109/EDKCON.2018.8770495.

[1.48] T. -W. Kim and J. A. del Alamo, "Injection velocity in thin-channel InAs HEMTs," *IPRM - 23rd International Conference on Indium Phosphide and Related Materials*, pp. 1-4, 2011.

[1.49] N. Kharche, G. Klimeck, D. -H. Kim, J. A. del Alamo and M. Luisier, "Performance analysis of ultra-scaled InAs HEMTs," *IEEE International Electron Devices Meeting (IEDM)*,pp.1-4,2009. https://doi.org/ 10.1109/IEDM.2009.5424315.

[1.50] S. Mookerjea, and S.Datta, “Comparative Study of Si, Ge and InAs Based Steep Subthreshold Slope Tunnel Transistors for 0.25V Supply Voltage Logic Applications,”*66th Device Research Conference (DRC)*. pp. 47-48, 2008.

[1.51] S.R.Mehrotra ,M. Povolotskyi, D.C. Elias, T. Kubis, J.J.M. Law, J.W.Rodwell,and G. Klimeck, “Simulation Study of Thin-Body Ballistic n-MOSFETs Involving Transport in Mixed Γ-L Valleys,” *IEEE Electron Device Letters*,vol.34, no.9,pp. 1196-1198,2013. https://doi.org/ 10.1109/LED.2013.2273072.

[1.52] H. Ko ,K. Takei, R. Kapadia,S. Chuang, H. Fang, W. L, Paul, K. Ganapathi, E. Plis, H.S. Kim, S-Y. Chen, M. Madsen, C. F. Alexandra, Y.L. Chueh , S. Krishna, S. Salahuddin ,and A. Javey ,“Ultrathin compound semiconductor on insulator layers for high-performance nanoscale transistors,” *Nature*, vol. 468 , no.11, pp.286-289, 2010. https://doi.org/ 10.1038/nature09541.

[1.53] J. Nah, H. Fang, C. Wang, K. Takei, M.H. Lee, E. Plis, S. Krishna, and A. Javey, “III−V Complementary Metal−Oxide−Semiconductor Electronics on Silicon Substrates,” *Nano Letters*,vol.12,pp.3592−3595,2012. https://doi.org/10.1021/acs.nanolett.5b02936.

[1.54] B.Markman, S. T. Suran Brunelli, M. Guidry, L. Whitaker and M. J. W. Rodwell, "Lg = 40nm Composite Channel MOS-HEMT Exhibiting f_τ = 420 GHz, f_{max} = 562 GHz," *Device Research Conference (DRC)*, pp. 1-2, 2021. https://doi.org/ 10.1109/DRC52342.2021.9467208.

[1.55] K. Takei, S. Chuang, H. Fang, R. Kapadia, C-H. Liu, J. Nah, H.S.Kim, E. Plis, S. Krishna, Y-L Chueh,and A. Javey, “Benchmarking the performance of ultrathin body InAs-on-insulator transistors as a function of body thickness,” *Applied Physics Letters.*, vol. 99, 103507,2011. https://doi.org/10.1063/1.3636110.

[1.56] T. Dutta, S. Kumar, P. Rastogi, A. Agarwal, and Y.S. Chauhan,"Impact of Channel Thickness Variation on Band structure and Source-to-Drain Tunneling in Ultra-Thin Body III-V MOSFETs," *Journal of Electron Devices Society*, vol. 4, no.2, 2016. https://doi.org/10.1109/JEDS.2016.2522981.

[1.57] S. Lee, C-Y. Huang, D.C. Elias, J.J.M. Law, V. Chobpattanna, S. Kramer , B.J.Thibeault, W. Mitchell, S. Stemmer, A.C. Gossard, and M.J.W. Rodwell, "High performance raised source/drain InAs/$In_{0.53}Ga_{0.47}As$ channel metal-oxide semiconductor field-effect-transistors with reduced leakage using a vertical spacer," *Applied Physics Letters*, vol.103, 233503, 2013. https://doi.org/10.1063/1.4838660.

[1.58] T.-W.Kim, R.J.W.Hill, C.D.Young, D.Veksler, L.Morassi, S.Oktybrshky, J. Oh, C. Y. Kang,D.-H. Kim, J.A.del Alamo, C.Hobbs, P.D.Kirsch, and R.Jammy," InAs quantum-well MOSFET (L_g=100nm) with record g_m, f_T and f_{max}," VLSI Technology(VLSIT), 2012. https://doi.org/ 10.1109/VLSIT.2012.6242520.

[1.59] S.Lee, C.Y. Huang, D.C. Elias,B.J.Thibeault, W. Mitchell, V.Chobpattana, S. Stemmer, A.C.Ossard, M.J.W.Rodwell, "Highly scalable raised source/drain InAs quantum well MOSFETs exhibiting I_{ON} = 482μA/μm at I_{OFF}=100 nA/μm and V_{DD}=0.5 V,"*IEEE Transaction on Electron Devices*, vol.35, no.6, pp. 621-623, 2014. https://doi.org/10.1109/LED.2014.2317146.

[1.60] T. Bryllert, L. E.Wernersson, L. E. Froberg, and L. Samuelson, "Vertical high-mobility wrap-gated InAs nanowire transistor," *IEEE Electron Device Letters*,vol.27, no.5,pp. 323-325,2006. https://doi.org/ 10.1109/LED.2006.873371.

[1.61] Q.Hang, F. Wang, P. D.Carpenter, D.Zemlyanov, D.Zakharov, E. A.Stach, W. E.Buhro, andD. B.Janes,"Role of molecular surface passivation in electrical transport

properties of InAs nanowires," *Nano Letters*,vol.8, pp.49–55 ,2008. https://doi.org/10.1021/nl071888t.

[1.62] E.Lind, A. I.Persson, L. Samuelson, and L. E.Wernersson, **"**Improved subthreshold slope in an InAs nanowire heterostructure field-effect transistor," *Nano Letters*, vol.6, pp.1842–1846,2006. https://doi.org/10.1021/nl052468b.

[1.63] A.C.Bleszynski, F.A. Zwanenburg, R. M.Westervelt, A. L.Roest, E. P. A.Bakkers, and L. P.Kouwenhoven, "Correlating the Nanostructure and Electronic Properties of InAs Nanowires,"*Nano Letters*,vol.7, pp.2559– 2562, 2007. https://doi.org/10.1021/nl904053j.

[1.64] A.C. Ford, J. C.Ho,Y. L. Chueh, Y. C. Tseng, Z. Fan, J. Guo, J. Bokor, and A. Javey,"Diameter-Dependent Electron Mobility of InAs Nanowires," *Nano Letters*, vol.9, no.1, pp.360-365, 2009. https://doi.org/10.1021/nl803154m.

[1.65] A.Konar, J. Mathew, K. Nayak, M. Bajaj, R.K. Pandey, S. Dhara, K. V. R. M.Murali, and M. Deshmukh,"Carrier Transport in High Mobility InAs Nanowire Junctionless Transistors," *Nano Letters*, vol.15, no.2, 2015. https://doi.org/10.1021/nl5043165.

[1.66] M. Luisier,and G. Klimeck,"Atomistic Full-Band Design Study of InAs Band-to-Band Tunneling Field-Effect Transistors," *IEEE Electron Device Letters*, vol.30,no.6, pp.602-604 2009. https://doi.org/ 10.1109/LED.2009.2020442.

[1.67] G.Doornbos, M. Holland, G. Vellianitis, M. J. H. Van Dal, B. Duriez, R. Oxland, A. Afzalian, T-K Chen, G. Hsieh, M. Passlack , and Y-C Yeo , "High-Performance InAs Gate-All-Around Nanowire MOSFETs on 300 mm Si Substrates, " *Journal of Electron*

Devices Society, vol. 4, no.5, pp. 253-259,2016.https://doi.org/ 10.1109/JEDS.2016.2574203.

[1.68] K.Takei, R. Kapadia,H. Fang,E. Plis, S. Krishna, and A. Javey, "High quality interfaces of InAs-on-insulator field-effect transistors with ZrO_2 gate dielectrics," *Applied Physics Letters.*,vol.102, 153513 ,2013. https://doi.org/10.1063/1.4802779.

[1.69] K.Takei, R. Kapadia, Y. Li ,E. Plis, S. Krishna,and A.Javey,"Surface Charge Transfer Doping of III−V Nanostructures,"*J. Phys.Chem. C* ,vol. 117, pp.17845−17849,2013. https://doi.org/10.1021/jp406174r.

[1.70] A.C. Ford, C.W. Yeung, S. Chuang, H.S. Kim, E. Plis, S. Krishna, C. Hu, Chenming and A. Javey, "Ultrathin body InAs tunneling field-effect transistors on Si substrates," *Applied Physics Letters*,vol. 98, 113105,2011. https://doi.org/10.1063/1.3567021.

[1.71] S-W.Wang, T. Vasen, G. Doornbos, R. Oxland, S-W. Chang, X. Li ,R.C.Guerrero,M.Holland,C- H. Wang, M. Edirisooriya, J. S. R.Ramirez, P.Ramvall, S. Thoms, D.S. Macintyre,G.Vellianitis,G. C. H. Hsieh, Y- S. Chang, K.M. Yin, Y-C. Yeo, C.H. Diaz, H.D.R. Carlos, I. G. Thayne, and M. Passlack, "Field-Effect Mobility of InAs Surface Channel n-MOSFET With Low D_{it} Scaled Gate-Stack," *IEEE Transactions on Electron Devices*,vol.62 no.8, pp.2429-2436,2015. https://doi.org/ 10.1109/TED.2015.2445854.

[1.72] K. Sumita, K. Toprasertpong, M. Takenaka and S. Takagi, "Subband Engineering by Combination of Channel Thickness Scaling and (111) Surface Orientation in InAs-On-Insulator nMOSFETs," *IEEE International Electron Devices Meeting (IEDM)*, pp. 2.5.1-2.5.4,2020. https://doi.org/ 10.1109/IEDM13553.2020.9371995.

[1.73] K. Sumita, C. -T. Chen, K. Toprasertpong, M. Takenaka and S. Takagi, "Optimum Design of Channel Material and Surface Orientation for Extremely-Thin-Body nMOSFETs under New Modeling of Surface Roughness Scattering," *IEEE International Electron Devices Meeting (IEDM)*, pp. 18.3.1-18.3.4,2021. https://doi.org/ 10.1109/IEDM19574.2021.9720715.

[1.74] K. Sumita, K. Toprasertpong, M. Takenaka and S. Takagi, "Proposal and Experimental Demonstration of Ultrathin-Body (111) InAs-On-Insulator nMOSFETs With L Valley Conduction," *IEEE Transactions on Electron Devices*, vol. 68, no. 4, pp. 2003-2009, 2021. https://doi.org/10.1109/TED.2021.3049455.

[1.75] C. H. Wang, G.Doornbos,G.Astromskas , G.Vellianitis, R.Oxland, M. C.Holland, M. L.Huang, C. H.Lin, C. H. Hsieh, Y. S.Chang, T. L. Lee , Y. Y. Chen, P.Ramvall, E. Lind,W. C.Hsu, L.-E.Wernersson , R.Droopad, M.Passlack, and C. H.Diaz, "High-k dielectrics on (100) and (110) n-InAs: Physical and electrical characterizations,"*AIP Advances*, vol.4, 047108 2014. https://doi.org/10.1063/1.4871187.

[1.76] Y. Liu, N. Neophytou, G. Klimeck, and M.S. Lundstrom,"Band-Structure Effects on the Performance of III–V Ultrathin-Body SOI MOSFETs," *IEEE Transactions on Electron Devices*, vol. 55, no.5, pp.1116-1122, 2008. https://doi.org/10.1109/TED.2008.919290.

[1.77] J. Wagner, J. Schmitz, F. Fuchs, J.D. Ralston, and P. Koidl, "Intersubband transitions in InAs/A1Sb quantum wells studied by resonant Raman scattering," *Physical Review B*,vol.51, no.15,1995. https://doi.org/10.1103/PhysRevB.51.9786.

[1.78] D. C. Larrabee, G. A.Khodaparast, J.Konoa, K. Ueda, Y. Nakajima,M.Nakai, S.Sasa, M.Inoue, K. I.Kolokolov,J. Li, and C. Z.Ning, "Temperature dependence of intersubband transitions inInAs/AlSb quantum wells,"*Applied Physics Letters*, vol. 83, no.19, 2003. https://doi.org/10.1063/1.1626264.

[1.79] E. Halpern, A.Henning,H.Shtrikman, R. Rurali, X. Cartoixa, Y. Rosenwaks,"Room Temperature Observation of Quantum Confinement in SingleInAs Nanowires," *Nano Letters*,vol.15,pp. 481−485,2015. https://doi.org/10.1021/nl503809c.

[1.80] A.Rahman, G. Klimeck and M. Lundstrom, "Novel channel materials for ballistic nanoscale MOSFETs-bandstructure effects," *IEEE International Electron Devices Meeting, IEDM Technical Digest*,2005. https://doi.org/10.1109/IEDM.2005.1609421.

[1.81] S. Chuang Q.Gao, R.Kapadia, A.C. Ford, J. Guo, and A. Javey, "Ballistic InAs Nanowire Transistors," *Nano Letters*, vol.13, pp. 555−558, 2013. https://doi.org/10.1021/nl3040674.

[1.82] A.C. Ford, S. B. Kumar, R. Kapadia, J.Guo, and A. Javey, "Observation of Degenerate One-Dimensional Sub-Bands in Cylindrical InAs Nanowires," *Nano Letters,* vol. 12, pp.1340−1343, 2012. https://doi.org/10.1021/nl203895x.

[1.83] Y. Zeng, C-I. Kuo,R. Kapadia, C.Y. Hsu, A.Javey, and C. Hu, "Two dimensional to three dimensional tunneling in InAs/AlSb/GaSb quantum well heterojunctions," *Journal Of Applied Physics,* vol.114,024502 ,2013. https://doi.org/10.1063/1.4812563.

[1.84] K. Takei, H. Fang, S. B. Kumar, R. Kapadia, Q. Gao, M. Madsen ,H.S. Kim, C.H. Liu,Y.L. Chu, E. Plis, S. Krishna, H.A. Bechtel, J. Guo ,and A. Javey, "Quantum Confinement Effects in Nanoscale-Thickness InAs Membranes,"*Nano Letters,*vol.11, pp. 5008–5012 ,2011. https://doi.org/10.1021/nl2030322.

[1.85] V. Ramachandran, R. A. Reed, R. D. Schrimpf, D. McMorrow, J. Brad Boos, M. P. King, E. X. Zhang,G. Vizkelethy, X. Shen, and S. T. Pantelides, "Single-Event Transient Sensitivity of InAlSb/InAs/AlGaSb High Electron Mobility Transistors," *IEEE Transactions on Nuclear Science*, vol. 59, no. 6, pp. 2691-2696, 2012. https://doi.org/ 10.1109/TNS.2012.2223716.

[1.86] V. F.Cavrois, P. Paillet, D. McMorrow, A. Torres,M. Gaillardin, J. S. Melinger, A. R. Knudson, A. B. Campbell,J. R. Schwank,G. Vizkelethy, M. R. Shaneyfelt,K. Hirose, O. Faynot, C. Jahan, and L. Tosti,"Direct Measurement of Transient Pulses Induced by Laser and Heavy Ion Irradiation in Deca-Nanometer Devices," *IEEE Transactions on Nuclear Science*, vol. 52, pp. 2104-2113,2005. https://doi.org/ 10.1109/TNS.2005.860682.

[1.87] D. McMorrow, J. Warner, S.DasGupta, V. Ramachandran, J.B.Boos, R. Reed, R. Schrimpf, P. Paillet, V.F. Cavrois, J. Baggio, S. Buchner, F. El-Mamouni, M. Raine, and O. Duhamel, ,".Novel Energy-Dependent Effects Revealed in GeV Heavy Ion-Induced Transient Measurements of Antimony-Based III-V HEMTs," *IEEE Transactions on Nuclear Science*, vol. 57, pp. 3358-3365,2010. https://doi.org/ 10.1109/TNS.2010.2086487.

[1.88] Todd Weatherford, and W.T.Anderson, "Historical Perspective on Radiation Effects in III-V Devices," *IEEE Transactions on Nuclear Science*,vol.50.pp.704-710,2003. https://doi.org/ 10.1109/TNS.2003.813124.

[1.89] J. H. Warner,D. McMorrow, S. Buchner, J.B. Boos, N.J.H. Roche,P. Paillet, M. Gaillardin, E. Blackmore, M. Trinczek,V. Ramachandran,R. A. Reed, and R. D.

Schrimpf,"Proton-Induced Transient Charge Collection in GaAs and InAlSb/InAs-Based FETs," *IEEE Transactions on Nuclear Science*, vol.60, pp.2651-2659,2013. https://doi.org/ 10.1109/TNS.2013.2261091.

[1.90] M. Barth, H. Lieu, J. H. Warner, B. R. Bennett, J. B. Boos, D. McMorrow, N. Roche, P. Paillet, M. Gaillardin, and S. Datta,"Single Event Measurement and Analysis of Antimony Based n-Channel Quantum-Well MOSFET With High- Dielectric," *IEEE Transactions on Nuclear Science*, vol. 62, no. 6, pp. 2807-2814, 2015. https://doi.org/ 10.1109/TNS.2015.2498905.

[1.91] M. Barth, A. Kumar, J. H. Warner, B. R. Bennett, J. B. Boos, C. D. Cress, N.J.-H. Roche,M. Raine, M. Gaillardin, P. Paillet,D. McMorrow, K. Saraswat, and S. Datta, "Single-Event Measurement and Analysis of Antimony-Based p-Channel Quantum-Well MOSFETs with High-k Dielectric," *IEEE Transactions on Nuclear Science*, vol. 64, no. 1, pp. 434- 440, 2016. https://doi.org/10.1109/TNS.2016.2637923.

[1.92] F.F.Komarov, O.V. Milchanin, I.N. Parkhomenko, L.A.Vlasukova, N.S. Nachaev, V.A. Skuratov, and V.N. Yuvchenko,"Influence of the Irradiation with High-Energy Xe Ions on the Structure and Photoluminescence of Silicon and Silica with InAs Nanoclusters,"*Journal of Engineering Physics and Thermophysics*, vol. 92, pp. 508–515 ,2019. https://doi.org/10.1007/s10891-01901958-y.

[1.93] A.Elwailly , J. Saltin, M. Gadlage,and H. Wong, "Radiation Hardness Study of L_G = 20 nm FinFET and Nanowire SRAM Through TCAD Simulation," *IEEE Transactions on Electron Devices*, vol.68, pp.2289-2294,2021. https://doi.org/ 10.1109/TED.2021.3067855.

[1.94] Y. M. Aneesh, S. R. Sriram, K. R. Pasupathy and B. Bindu, "An Analytical Model of Single-Event Transients in Double-Gate MOSFET for Circuit Simulation," *IEEE Transactions on Electron Devices*, vol. 66, no. 9, pp. 3710-3717,2019. https://doi.org/ 10.1109/TED.2019.2926883.

[1.95] M. Zerarka, P. Austin, A. Bensoussan, F. Morancho, and A. Durier," TCAD Simulation of the Single Event Effects in Normally-off GaN Transistors after Heavy Ion Radiation," *IEEE Transactions on Nuclear Science*, vol. 64 , no.8, pp.2242-2249, 2017. https://doi.org/10.1109/TNS.2017.2710629.

[1.96] K. Ni, "Single Event Transient And Total Ionizing Dose Effects On III-V MOSFETs for SUB-10 nm Node CMOS,"[dissertation]. Dept. Elect. Eng., Graduate School of Vanderbilt University, Nashville, Tennessee, 2016.

[1.97] V. Ramachandran, "Single-Event Mechanisms in InAlSb/InAs/AlGaSb High Electron Mobility Transistors,"[dissertation] Dept. Elect. Eng., Graduate School of Vanderbilt University, Nashville, Tennessee, 2013.

[1.98] J. E. Turner, "Atoms, Radiation, and Radiation Protection," third ed. WILEY-VCH Verlag GmbH & Co. KGaG, Germany, 2007.

[1.99] J. P. R. David, and C. H. Tan, "Material considerations for avalanche photodiodes,"*IEEE J. Sel. Topics Quantum Electron*, vol.14, no.4, pp.998–1009 ,2008. https://doi.org/ 10.1109/JSTQE.2008.918313.

[1.100] R. J. McIntyre," Multiplication noise in uniform avalanche diodes," *IEEE Transactions on Electron Devices*, ED-13, no.1, pp.164–168,1966. https://doi.org/10.1109/T-ED.1966.15651.

[1.101] R. B. Emmons, “Avalanche-photodiode frequency response,” *Journal Of Applied Physics*,vol.38, no.9, pp.3705–3714,1967. https://doi.org/10.1063/1.1710199.

[1.102] J.C. Campbell, “Recent advances in avalanche photodiodes,” *IEEE J. Sel. Topics Quantum Electron*, vol.10, no.4, pp.777–787, 2004. https://doi.org/10.1109/JSTQE.2004.833971.

[1.103] A.R.J. Marshall,J. P. R. David, and C.H. Tan,“Impact Ionization in InAsElectronAvalanche Photodiodes,” *IEEE Transactions on Electron Devices*,vol.57, no.10,pp. 2631-2638,2010. https://doi.org/10.1109/TED.2010.2058330.

[1.104] A.R.J. Marshall, C. H.Tan, M. J.Steer, and J. P. R. David,“Electron dominated impact ionization and avalanche gain characteristics in InAs Photodiodes,” *Applied Physics Letters*, vol.93, 111107 ,2008. https://doi.org/10.1063/1.2980451.

[1.105] M.G. Ancona , B.R. Bennett, and J.B. Boos, “Scaling projections for Sb-based p-channel FETs”, Solid-State Electronics, vol. 54, pp.1349–1358,2010. https://doi.org/10.1016/j.sse.2010.06.022

[1.106] B.R.Bennett, M.G. Ancona, G. Mario,J.B. Boos, B.V. Shanabrook, “Mobility enhancement in strained p-InGaSb quatum wells.,” Applied Physics Letters, vol. 91, 042104,2007. https://doi.org/10.1063/1.2762279

[1.107] Md. N. K. Alam, Md. S. Islam, Md. G. Kibria, and Md. R. Islam, “On the Ballistic Performance of InGaSb XOI FET: Impact of Channel Thickness and Interface States,” *IEEE Transactions on Electron Devices*, vol. 62, no. 6, pp. 1855-1861, 2015. http://doi.org/10.1109/TED.2015.2420102.

[1.108] S.H. Kim , I. Roh, J-H. Han, D-M Geum ,S. K. Kim, S. S. Kang, H.-K. Kang, W. C. Lee, S. K. Kim, D. K. Hwang, Y. H. Song , and J. D. Song, “High Hole Mobility and

Low Leakage Thin-Body (In)GaSb p-MOSFETs Grown on High-Bandgap AlGaSb," Journal of Electron Devices Society, vol.9, pp.42-48,2021. http://doi.org/10.1109/JEDS.2020.3039370

CHAPTER-2

Details of Physics and Models incorporated in the work

In this chapter, the author has described in details the various concepts of physics and the different models of the numerical device simulator, SILVACO ATLAS, that have been used to investigate the various aspects of MOSFET devices. The models developed from different physics based equations are modeled using various model parameters, the values of which are either extracted or calculated from different literatures and then fed into the simulator to structure the devices. To authenticate the simulation framework, the author has validated the characteristics of all the simulated structures with some experimentally reported results.

2.1 Introduction

Numerical simulation of electronic devices is an integral part of the semiconductor industry. The characteristics and the performance of new designs can be evaluated and studied with device simulation well before going through the manufacturing cycles. Semiconductor device modeling uses models for the behavior of the devices based on fundamental physics of the devices and also includes the creation of compact circuit models that capture the electrical behavior of such devices. Reliable numerical simulators provide robust outputs that are sufficient to accurate a device model. A large part of ongoing research and development of emerging devices like MOSFET depends on the outcome of numerical simulators.

In the present work, the author has used two-dimensional numerical device simulation using SILVACO ATLAS [2.1] to obtain the device characteristics of different semiconductor

structures and to get an idea about the internal processes and mechanisms that govern the device operation**.** SILVACO ATLAS has a vast library of various models that run successfully to provide the structure and the characteristics of the devices. This work covers the effects of temperature, channel thickness, angle of grooving and radiation on the digital, analog, RF and linearity performances of InAs based on-insulator and quantum well n-MOSFETs and InGaSb based quantum well p-MOSFET. Various models used for this purpose are temperature and concentration dependent low field mobility model, parallel electric field dependent model, scattering model, different tunneling and generation/recombination models, drift-diffusion transport model with inclusion of quantum effect for thin body devices. Also, the dependency of bandgap, effective mass and non-parabolicity factor on changes of temperature and channel thickness are well incorporated in the simulator after reviewing the respective literatures. The details of all these above discussed physics and models are covered in this chapter.

The chapter is organised as follows: In the section 2.2, the detail description of the physics and models used to investigate the effect of channel thickness and grooving angle on the device performance of InAs based n-MOSFET and InGaSb based p-MOSFET is given. This is followed by Section 2.3 which has the detailing of the models used to incorporate the effect of the changes of temperature in the device performance of InAs based quantum well n-MOSFET. Then, section 2.4 covers the concepts of physics incorporated in the simulation to study the effect of radiation on InAs based quantum well n-MOSFET. Finally, section 2.5 has the model calibration part of the work.

2.2 Models used to investigate the effect of channel thickness and grooving angle on the device performance of InAs based n-MOSFET and InGaSb based p-MOSFET

With the progress in ITRS roadmap, the device dimensions are being scaled down greatly. In bulk materials, the electronic properties are governed by continuous energy bands. However, when the dimensions of a material are reduced to the nanoscale, the behaviour of electrons becomes restricted, and discrete energy levels, called quantum states, are formed due to the phenomenon called quantum confinement. With scaling, the available quantum states become increasingly discrete, and their energy difference increases. This results in an increase in the band gap of the scaled devices compared to the bulk material [2.2-2.3] This variation of bandgap with the reduced channel thickness (t_{ch}) in InAs channel is incorporated using

$$E_g\,(t_{ch}) = \alpha {t_{ch}}^{\beta} + \gamma \tag{2.1}$$

where α =1.567, β= -1.057 and γ = 0.296 following [2.2].

In extremely confined channels, use of parabolic effective mass approach (m^*) is no longer valid as m^* increases with confinement .This effect of variation of effective mass of electrons (m^*) with channel thickness in InAs MOSFETs is introduced using

$$m^*(t_{ch}) = a{t_{ch}}^{b} + c \tag{2.2}$$

where a=0.1944, b= -1.101 and c= 0.0205 [2.2].

In narrow-gap materials, the approximation of parabolic conduction band does not hold good. The non-parabolicity of the conduction band is significant for such materials. So, the nonparabolicity of the conduction bands in terms of nonparabolicity factor (α) is introduced whose dependency on bandgap and electron effective mass is given as

$$\alpha = \frac{1}{E_g}(1 - \frac{m^*}{m_0})^2 \quad (2.3)$$

where, m_0 is the rest mass of electrons [2.4].

However, the bandgap and the effective mass of holes for InGaSb p-MOSFET are directly taken from the literature survey [2.5].

Table I shows the thickness dependent values of bandgap, effective mass, and non-parabolicity factor for InAs and InGaSb based MOSFETs at T=300 K.

Table I: Summary of thickness dependent parameters of InAs and InGaSb based channels used in simulation at T=300K

Parameter (Unit)	**Values of the parameters for channel thickness of 5 nm**	
	InAs	**InGaSb x:0.41**
Band gap (eV)	0.58	0.45
Effective mass (m^*)	0.053 (of electrons)	0.26 (of holes)
Non-parabolicity factor(eV^{-1})	1.54	1.21

Following are the different models from the ATLAS library that the author has used for the simulation of the structures.

2.2.1 Mobility models

2.2.1.1 Analytic Model

Low field analytic mobility model [2.6-2.9] has been used to specify the concentration and temperature dependent low field mobilities following

$$\mu_{LF}(N,T) = \mu_{min} + \frac{\mu_{max}(300K)+(\frac{300K}{T})^{\theta 1} - \mu_{min}}{1+(\frac{N}{N_{ref}(300K)(\frac{T}{300K})^{\theta 2}})^{\lambda}} \quad (2.4)$$

Here, N is the total impurity concentration in /cm^3 and T is temperature in Kelvin, μ_{max} and μ_{min} represent the mobility saturation at lowest and highest doping concentration, respectively(in cm^2/V.s), N_{ref} denotes the reference doping concentration at which mobility reduces to half of μ_{max} value,θ_1, θ_2 and λ are the fitting parameters.

All the extracted analytic mobility parameters used in InAs and InGaSb channel at T= 300 K are given in Table II.

Table II: Analytic mobility parameters for InAs and InGaSb based channel material used in simulation at T=300K

Parameters (unit)	**InAs (electrons)**	**InGaSb (holes)**
μ_{min} (cm^2/V.s)	1000	153.1
μ_{max} (cm^2/V.s)	34,000	823.75
N_{ref} (300K) (/cm^3)	1.1×10^{18}	7.77×10^{17}
λ	0.32	0.629
Θ_1	1.57	1.76
Θ_2	3	2.78

2.2.1.2 Parallel electric field dependent mobility/Saturation velocity model

When the magnitude of the electric field becomes significant, the velocity of the carriers start to get saturated. Analytic model takes into account the low field effects while this model helps to

get a smooth transition from low field to high field behavior. To incorporate this effect, the following equation is considered.

$$\mu_n(E) = \mu_{no}\left(\frac{1}{1+\left(\frac{\mu_{no}E}{v_{satn}}\right)^{\beta_n}}\right)^{\frac{1}{\beta_n}} \quad (2.5)$$

$$\mu_p(E) = \mu_{po}\left(\frac{1}{1+\left(\frac{\mu_{po}E}{v_{satp}}\right)^{\beta_p}}\right)^{\frac{1}{\beta_p}} \quad (2.6)$$

Here, E is the parallel electric field, μ_{no} and μ_{po} are the low field mobility for electrons and holes, respectively. β_n and β_p are the mobility parameters for electrons and holes, respectively, having the values as 2 and 1. v_{satn} and v_{satp} are the saturation velocity for electrons and holes, respectively. v_{satn} for InAs is taken as 0.9×10^7 cm/s [2.10] and v_{satp} in InGaSb is 8×10^6 cm/s. [2.5]

2.2.2 Scattering model

Carrier scattering has a damping effect on mobility. To incorporate carrier-carrier scattering contribution to mobility, Conwell-Weisskopf model [2.11] is invoked following

$$\mu_{CCS} = \frac{D.Conwell.\left(\frac{T}{300}\right)^{\frac{3}{2}}}{\sqrt{pn}\left(\ln\left(1+\frac{F.Conwell.\left(\frac{T}{300}\right)^{2}}{pn^{\frac{1}{3}}}\right)\right)} \quad (2.7)$$

where *p* and *n* are hole and electron concentration, respectively . *D. Conwell* and *F. Conwell* are the model parameters taking the values as 1.04×10^{21} $(cm.V\cdot s)^{-1}$ and 7.452×10^{13} cm^{-2}, respectively and T is the lattice temperature.

This mobility is then combined with other enabled low field mobility models to give the overall mobility (μ_n/μ_p) for electrons/holes using Matthiessen's rule:

$$\frac{1}{\mu_n} = \frac{1}{\mu_{no}} + \frac{1}{\mu_{CCS}} \tag{2.8}$$

$$\frac{1}{\mu_p} = \frac{1}{\mu_{po}} + \frac{1}{\mu_{CCS}} \tag{2.9}$$

Here, μ_{CCS} is the mobility obtained from this model.

2.2.3 Recombination/generation model

Carrier generation and recombination are the processes in which the semiconductor material tries to return to the equilibrium state from the non-equilibrium one. Following recombination and generation models are used in this work to simulate InAs and InGaSb MOSFETs.

2.2.3.1 Shockley-Read -Hall (SRH) recombination model

This model is used in the simulation to consider the effect of phonon transitions through the traps or defects within the forbidden gap of the semiconductor. This model is modeled as [2.12-2.13]

$$R_{SRH} = \frac{pn - {n_i}^2}{\tau_{p0}\left[n + n_i exp\left(\frac{E_t}{KT_L}\right)\right] + \tau_{n0}\left[p + n_i exp\left(\frac{-E_t}{KT_L}\right)\right]} \tag{2.10}$$

where E_t is the difference between the trap energy level and intrinsic Fermi level, considered as 0 as it corresponds to most efficient recombination center. τ_{n0} and τ_{p0} are the carrier lifetimes, considered in the order of 10^{-6}s for InAs [2.14] and in the order of 10^{-9} s for InGaSb [2.15] .Here, *p* and *n* are hole and electron concentration, respectively, T_L is the lattice temperature in Kelvin, n_i is the intrinsic carrier concentration.

2.2.3.2 Auger recombination model

Auger recombination is a non-radiative process where the excess energy from the electron-hole recombination is transferred to electrons or holes that are subsequently excited to higher energy states within the same band instead of giving off photons. This model is introduced using [2.16]

$$R_{Auger} = AUGN(pn^2 - nn_i{}^2) + AUGP(np^2 - pn_i{}^2) \quad (2.11)$$

where *AUGN* and *AUGP* are the Auger coefficients. These coefficients are considered in the order of 10^{-26} and 10^{-25} cm^6/s at T=300K for InAs and InGaSb, respectively. [2.14, 2.17] Here, *p* and *n* are hole and electron concentration, respectively and n_i is the intrinsic carrier concentration.

2.2.3.3 Radiative recombination model

This recombination dominates in narrow bandgap material. In this type, the electron from the conduction band directly recombines with hole in the valence band and in doing so releases photon energy which is equal to the bandgap energy of the semiconductor. This model is used as [2.1]

$$R_{np}^{opt} = C_C^{opt}(np - n_i^2) \quad (2.12)$$

where the radiative recombination coefficient C_C^{opt} is considered in the order of 10^{-11} cm^3/s for InAs [2.14] and in the order of 10^{-10} cm^3/s InGaSb.

2.2.3.4 Selberherr's Impact Ionization model

Impact ionization is the phenomenon by which energetic carriers traveling in a material loses energy and generates other carriers. This effect is introduced through Selberherr's Impact Ionization model following [2.16]

$$\propto_n = A\exp[-(\frac{B}{E})^C] \quad (2.13)$$

Here, E is the electric field in the direction of current and the constants A, B and C for InAs are $5.16x10^5$ cm^{-1}, $2.52x\ 10^6$ Vcm^{-1} and 0.25, respectively. [2.18] These coefficients for InGaSb are $2.75x10^5$ cm^{-1}, $1.89x\ 10^5$ Vcm^{-1} and 1.17, respectively. [2.19]

2.2.4 Tunneling model

Tunneling of carriers from valence band to conduction band occur through traps or defects at high electric fields. This tunneling can also occur due to local band bending at high field. All these have effect on the current calculation of the device. To incorporate these effects in simulation, the following models are used in the simulation. [2.20-2.21]

2.2.4.1 Band-to band tunneling

When the electric field within the semiconductor is sufficiently high, local bending of bands occur which allow electrons to tunnel, by internal field emission, from valence band to conduction band, leading to the generation of an additional electron in conduction band and hole in valence band. This generation rate is given by

$$G_{BBT} = D\ BB.A\ E^{BB.GAMMA}\exp(-\frac{BB.B}{E}) \quad (2.14)$$

where E is the magnitude of electric field, D is the statistical factor considered as 1. The other factors are calculated following

$$BB.A = \frac{q^2\sqrt{(2\times Mass.Tunnel\times m_0)}}{h^2\sqrt{E_g(300)}} \quad (2.15)$$

$$BB.B = \frac{\pi^2 E_g(300)^{\frac{3}{2}}\sqrt{\frac{Mass.Tunnel\times m_0}{2}}}{qh} \quad (2.16)$$

$$BB.GAMMA = 2$$

where *Mass.Tunnel* is the effective mass, m_o is the rest mass of electron, $E_g(300)$ is bandgap of the material at T=300 K, q is the electronic charge.

2.2.4.2 Trap Assisted Tunneling

At high electric fields, tunneling of electrons from the valence band to the conduction band through trap or defect states have an important effect on the current. Trap-assisted tunneling is modeled by including appropriate enhancement factors (Γ_n^{DIRAC} and Γ_p^{DIRAC}) in the trap lifetimes. These enhancement factors modify the lifetimes (Γ_n and Γ_p) to include the effects of phonon-assisted tunneling. The model is modeled by:

For donar like traps, the recombination term is given by

$$R_D = \frac{pn-n_i^2}{\frac{\tau_n}{1+\Gamma_n^{DIRAC}}[p+DEGEN.FAC\times n_i \exp\left(\frac{E_i-E_t}{KT_L}\right)+\frac{\tau_p}{1+\Gamma_p^{DIRAC}}[n+\frac{1}{DEGEN.FAC}\times n_i \exp\left(\frac{E_t-E_i}{KT_L}\right)} \quad (2.17)$$

For acceptor like traps, the recombination term is given by

$$R_A = \frac{pn-n_i^2}{\frac{\tau_n}{1+\Gamma_n^{DIRAC}}[p+\frac{1}{DEGEN.FAC}\times n_i \exp\left(\frac{E_i-E_t}{KT_L}\right)+\frac{\tau_p}{1+\Gamma_p^{DIRAC}}[n+DEGEN.FAC\times n_i \exp\left(\frac{E_t-E_i}{KT_L}\right)} \quad (2.18)$$

where *DEGEN.FAC* is the degeneration factor of the trap level used to calculate the density, considered as 1.Here, p and n are hole and electron concentration, respectively and n_i is the intrinsic carrier concentration, T_L is the lattice temperature in Kelvin, K is the Boltzmann's constant.

The field-effect enhancement terms are given by

$$\Gamma_n^{DIRAC} = \frac{\Delta E_n}{KT_L}\int_0^1 \exp(\frac{\Delta E_n}{KT_L} \times u \times K_n \times u^{\frac{3}{2}})du \quad (2.19)$$

$$\Gamma_p^{DIRAC} = \frac{\Delta E_p}{KT_L}\int_0^1 \exp(\frac{\Delta E_n}{KT_L} \times u \times K_p \times u^{\frac{3}{2}})du \quad (2.20)$$

where u is the integration variable, ΔE_n and ΔE_p are tunneling energy range for electrons and holes, respectively. K_n and K_p are given by

$$K_n = \frac{4}{3}\frac{\sqrt{2\times m_o \times Mass.Tunnel\times \Delta E_n^3}}{3\times q\times h\times |E|} \quad (2.21)$$

$$K_p = \frac{4}{3}\frac{\sqrt{2\times m_o \times Mass.Tunnel\times \Delta E_p^3}}{3\times q\times h\times |E|} \quad (2.22)$$

where *Mass.Tunnel* is the effective mass, m_0 is the rest mass of electron, h is Planck's constant, K is Boltzmann's constant, q is electronic charge.

2.2.5 Carrier statistics and Transport model

Fermi-Dirac statistics is being used to control the distribution of carriers within solids. Electrons within a semiconductor obey Fermi-Dirac statistics which says that the probability (*f(E)*) of finding an electron in state with energy E is given by

$$f(E) = \frac{1}{1+\exp(\frac{E-E_F}{KT})} \quad (2.23)$$

where *K* is the Boltzmann's constant, T is the absolute temperature and *EF* is the Fermi level.

To incorporate the effect of confinement of carriers in nanoscale devices, the drift-diffusion transport model of carriers is used along with the density gradient model with a quantum correction factor. This is given by [2.22-2.23]

$$J_n = qD_n\nabla n - qn\mu_n\nabla(\varphi - \Lambda) - \mu_n n(KT\nabla(lnn_i) \quad (2.24)$$

$$J_p = -qD_p\nabla p - qp\mu_p\nabla(\varphi - \Lambda) + \mu_p p(KT\nabla(lnn_i) \quad (2.25)$$

where J_n and J_p are the current densities foe electron and hole, respectively, q is the electronic charge, p and n are hole and electron concentration, respectively, D_p and D_n are the diffusion coefficients for holes and electrons, respectively, μ_p and μ_n are hole and electron mobility, respectively, n_i is the intrinsic carrier concentration, T is the temperature in Kelvin, K is the Boltzmann's constant.

Λ is the quantum correction potential given by

$$\Lambda = -\frac{\gamma h^2}{12m}[\nabla^2 logn + \frac{1}{2}(\nabla logn)^2 \quad (2.26)$$

where γ is the fit factor and h is Planck's constant.

2.2.6 Numerical implementation

For powerful initial guess strategies, small-signal techniques that can converge at all frequencies and also to have proper iterations, Newton and Block numerical techniques are also adopted in the simulation.

2.3 Models used to incorporate the effect of the changes of temperature in the device performance of InAs based n-MOSFET

The temperature dependent models that are included in the simulation are as follows:

2.3.1 Universal Energy Bandgap model

The temperature dependence of the bandgap [2.24-2.25] is modeled in the simulation using

$$E_g = E_{g0} - \frac{\alpha T^2}{(T+\beta)} \quad (2.27)$$

Here , E_{g0} is bandgap at T=0 K, α and β are the material dependent factors. The extracted parameters E_{g0} , α and β are considered as 0.415 eV, 0.276 meV/K and 83 K, respectively for InAs .

2.3.2 Temperature dependent Effective Mass

The author has included the variation of effective mass of electrons (m^*) with temperature (T) following

$$m^*(T) = \frac{m^*(300)}{E_g(300)} E_g(T) \tag{2.28}$$

where $m^*(300)$ and $E_g(300)$ are electron effective mass and bandgap at T=300K, respectively [2.4,2.26]

2.3.3 Temperature Dependence of Electron Affinity

The electron affinity of a semiconductor gets affected by the change of lattice temperature which is modeled in Atlas by making it a fraction of the temperature dependence of the bandgap [2.1]. The default value of the fraction ($\mathrm{CHI}.E_g.\mathrm{TDEP}$) is 0.5.

$$\chi(\mathrm{T}) = \chi(300) - \mathrm{CHI}.E_g.\mathrm{TDEP} \times (E_g(T_L) - E_g(300)) \tag{2.29}$$

where $\chi(300)$ and $E_g(300)$ are electron affinity and bandgap at T=300 K, T_L is the lattice temperature.

2.3.4 Temperature Dependence of Saturation Velocity

Saturation velocity of carriers do depend on temperature [2.10]. This dependency is incorporated using

$$v_{sat}(T) = \frac{v_{sat}(300)}{(1-A)+A.(\frac{T}{300})} \quad (2.30)$$

Here, A is the temperature coefficient that reflects the temperature dependence of saturation velocity of various materials and $v_{sat}(300)$ is the saturation velocity of electrons at T=300 K. These parameters for InAs channel are considered as 0.43 and 0.9×10^7 cm/s, respectively.

2.3.5 Incomplete Ionisation model

To incorporate the effect of freezing out of dopants at low temperature, incomplete ionization model has been used.

2.3.6 Temperature Dependent Recombination model

2.3.6.1 Temperature Dependent Shockley-Read-Hall (SRH) recombination model

Shockley-Read-Hall (SRH) recombination model with temperature dependence electron and hole lifetimes is used as: [1]

$$\tau_n = \tau_{n0}(\frac{T}{300K})^{LT.\tau_n.} \quad (2.31)$$

Here, τ_{n0} is SRH lifetime for electrons , considered in the order of 10^{-6} s. [2.14]

The fitting parameters $LT.\boldsymbol{\tau_n}$ is considered as 1.

2.3.6.2 Temperature Dependent Auger and Radiative recombination model

Temperature dependent Auger coefficients and Radiative recombination coefficients at any other temperature apart from room temperature are fitted in the simulation following [2.14]

2.4 Physics incorporated to study radiation effect on InAs based quantum well n-MOSFET

Semiconductor-based devices nowadays find many applications in harsh radiation environments such as space, atomic research centers, and radiation physics laboratories. The study of the device performance under the effect of radiation is a rising trend in the semiconductor industry. Of the several methods that cover up this study of radiation, the category of single-event transient effect is being considered in this work.

To study this radiation effect on the performance of the device, the device is assumed to be exposed to high-energy, fast moving ion particle. In this work, it is considered that when this fast moving heavy energetic ion traverses through the medium of the device, it maintains one Gaussian irradiation track with a narrow radius of 5 nm, width of 120 ps (t_c) and the time the radiation reaches its peak value time is considered as 600 ps (t_0) [2.27]. This ion track with respect to time (*T(t)*) and space (*R(r)*) is represented by [2.1]

$$T(t) = \frac{2\exp\left(-\left(\frac{t-t_0}{t_c}\right)^2\right)}{t_c\sqrt{\pi}erfc\left(-\frac{t_0}{tc}\right)} \tag{2.32}$$

$$R(r) = exp\left(-\frac{r}{RADIUS}\right)^2 \tag{2.33}$$

This ion interacts with the electrons of atoms of the material or medium and this interaction excites or ionizes the atoms, leading to an energy loss of the traveling ion. This linear rate of energy loss or linear rate of energy transfer (LET) to the medium is called Mass Stopping Power given by [2.28]

$$LET = -\frac{dE}{dx} \times \frac{1}{\rho} \tag{2.34}$$

where ρ and $\frac{dE}{dx}$ are the density and stopping power of the medium.

In SILVACO, this theoretically calculated LET value for a particular medium and for a particular radiating ion is incorporated in terms of amount of generated charge by that particular ion within that particular medium using the conversion factor (X) for that medium. This conversion factor (X) is calculated as $X = \frac{q \times \rho}{E_{eh}}$, where E_{eh} is electron-hole pair creation energy of the medium/material and q is electronic charge. [2.27]

In this work, the incident ion energy is considered as 9.3 MeV/amu for 3 different testing ions viz. Neon, Krypton and Xenon. Table III shows the conversion of energy that is transferred to InAs layer of thickness 5 nm by these radiating ions to the generated charge within that layer.

Table III: Conversion of energy to the generated charge within InAs layer of thickness 5 nm

Incident ions	Incident energy (MeV)	LET (MeV.cm^2/mg)	Generated charge (pC/µm)
Neon	187.58	2.58	0.129
Krypton	771.9	33.45	1.67
Xenon	1227.39	75.52	3.77

These ions while traversing through the device, lose energy across each layer of the device. So, incident energy and LET values for each layer with varied thicknesses are calculated in details in Chapter 5.

2.5 Model calibration

With the proper inclusion of all the above discussed physics and models in the simulation, the author has validated the characteristics of the simulated InAs-on-insulator (InAsOI) n-MOSFET structure with the experimentally reported result of InAsOI n-MOSFET structure having channel thickness of 13 nm and channel length of 2.85 µm. [2.29] .The author has also calibrated the proposed quantum well structure by comparing the transfer characteristics and the variation of transconductance (g_m) with respect to gate voltage (V_{GS}) with the experimental results of InAs

quantum well n-MOSFET featuring t_{ch}= 5 nm and L_{ch}= 18 nm with angle of grooving (θ) as 40^0 [2.30]. The results of validation, the details of which are given in the following chapter, show that the simulated data matches quite well with the experimental results reported which certainly verifies the simulation framework for the proposed MOSFET structures.

REFERENCES

[2.1] *ATLAS users' manual: device simulation software*' (Silvaco Int., Santa Clara, CA, USA, 2014), available at http://www.silvaco.com

[2.2] T. Dutta, S. Kumar, P. Rastogi, A. Agarwal, and Y.S. Chauhan, " Impact of Channel Thickness Variation on Bandstructure and Source-to-Drain Tunneling in Ultra-Thin Body III-V MOSFETs," *Journal of Electron Devices Society*, vol.4, no.2, pp.66-71,2016. https://doi.org/10.1109/JEDS.2016.2522981.

[2.3] K. Takei, S. Chuang, H. Fang, R.Kapadia, C-H. Liu, J. Nah, H.S. Kim, E. Plis, S. Krishna, Y.L. Chueh, and A. Javey, "Benchmarking the performance of ultrathin body InAs-on-insulator transistors as a function of body thickness," *Applied Physics Lett.*,vol.99,no.10, pp.103507-1-3, 2011. https://doi.org/10.1063/1.3636110.

[2.4] R. A. Stradling, and R. A. Wood, "The temperature dependence of the band-edge effective masses of InSb, InAs and GaAs as deduced from magneto phonon magneto resistance measurements," Journal of Physics C: Solid State Physics, vol. 3, no.5, pp. 94-99.1970.

[2.5] M.G. Ancona , B.R. Bennett, and J.B. Boos, “Scaling projections for Sb-based p-channel FETs”, Solid-State Electronics, vol. 54, pp.1349–1358,2010. https://doi.org/10.1016/j.sse.2010.06.022

[2.6] D. M. Caughey and R. E. Thomas, "Carrier mobilities in silicon empirically related to doping and field," in *Proceedings of the IEEE*, vol. 55, no. 12, pp. 2192-2193, 1967. https://doi.org/ 10.1109/PROC.1967.6123.

[2.7] M. Sotoodeh, A.H. Khalid, and A.A. Rezazadeh, “Empirical low-field mobility model for III–V compounds applicable in device simulation codes,”*J. Appl. Phys.*, vol. 87,no.6, pp.2890-2900, 2000. https://doi.org/10.1063/1.372274.

[2.8] E. Vadiee, Y Fang, C. Zhang, A. M. Fischer, J. J. Williams, E. J. Renteria, G. Balakrishnan, and C. B. Honsberg, “Temperature dependence of GaSb and AlGaSb solar cells,” Current Applied Physics, vol.18, pp.752-761, 2018. https://doi.org/10.1016/j.cap.2018.03.007

[2.9] R. Vaillon, J.-P. Pérez,C. Lucches, D. Cakirogl, P-O. Chapuis, T. Taliercio, and E. Tournié, “Micron-sized liquid nitrogen-cooled indium antimonide photovoltaic cell for near-field thermophotovoltaics,”*Optics Express*, vol. 27, no. 4 , pp.11-24,2019. https://doi.org/10.1364/OE.27.000A11

[2.10] R. Quay, C. Moglestue, V. Palankovski, and S. Selberherr, “A temperature dependent model for the saturation velocity in semiconductor materials,” *Materials Science in Semiconductor Processing*, vol.3, pp.149-155, 2000. https://doi.org/10.1016/S1369-8001(00)00015-9.

[2.11] T. P. McLban, and E. G. S. Paigb, "A Theory Of The effects of carrier-carrier scattering on mobility in semiconductors," *J. Phys. Chm. Solids*, vol. 16, pp.220-236,1960. https://doi.org/10.1016/0022-3697(60)90152-9

[2.12] W. Shockley, and W.T. Read, "Statistics of the Recombination of Holes and Electrons", *Phys. Rev.*, vol.87, pp.835-842,1952.https://doi.org/10.1103/PhysRev.87.835

[2.13] R. N. Hall, "Electron-Hole Recombination in Germanium," *Phys. Rev.* , vol.87, pp.387,1952 .https://doi.org/10.1103/PhysRev.87.387

[2.14] B. V. Olson, E. A. Kadlec, J. K. Kim, J. F. Klem, S. D. Hawkins, and E. A. Shaner, "Intensity- and Temperature-Dependent Carrier Recombination in InAs/$InAs_{1-x}Sb_x$ Type-II Superlattices," *Physical Review Applied*, vol. 3, 044010-1-12 ,2015. https://doi.org/10.1103/PhysRevApplied.3.044010

[2.15] R. G. Bedford, G. Triplett, D. H. Tomich, S. W. Koch, J. Moloney, and J. Hader," Reduced auger recombination in mid-infrared semiconductor lasers," *Journal Of Applied Physics*, vol. 110, 073108-1-6 ,2011. https://doi.org/10.1063/1.3646552

[2.16] S. Selberherr, Analysis and Simulation of Semiconductor Devices, 1st edition, Springer Vienna, 1984. https://doi.org/ 10.1007/978-3-7091-8752-4

[2.17] J. Piprek, Semiconductor Optoelectronic Devices: *Introduction to Physics and Simulation*, 1st edition, Academic Press Inc, 2003, Pages 49-82. https://doi.org/10.1016/B978-0-08-046978-2.50028-4.

[2.18] A.R. J. Marshall, C. H. Tan, M. J. Steer and J. P. R. David, "Electron dominated impact ionization and avalanche gain characteristics in InAs Photodiodes," *Applied Physics Lett*, vol. 93, pp.111107-1- 111107-3,2008. https://doi.org/10.1063/1.2980451

[2.19] E. Jamil, "Analytical modeling and characterization for avalanche photodiodes," Doctor of Philosophy, Engineering, Optical Science Engineering, The University of New Mexico, Albuquerque, New Mexico, July, 2017.

[2.20] G. A. M. Hurkx, D. B. M. Klaassen, and M. P. G. Knuvers, "A new recombination model for device simulation including tunneling," *IEEE Trans. Electron Dev.*, vol. 39 ,no.2, pp.331-338,1992. https://doi.org/10.1109/16.121690.

[2.21] G. A. M. Hurkx, C. D. Graaff, W. J. Kloosterman, and M. P. G. Knuvers , "A new analytical diode model including tunneling and avalanche breakdown," *IEEE Trans. Electron Devices*,vol.39,no.9,pp. 2090–2098,1992. https://doi.org/ 10.1109/16.155882.

[2.22] J.R. Zhou, and D.K. Ferry, "Simulation of Ultra-small GaAs MESFET Using Quantum Moment Equations," *IEEE Trans. Electron Devices,* vol. 39, pp.473-478, 1992.

[2.23] A. Wettstein, A. Schenk, and W. Fichtner, "Quantum Device-Simulation with the Density Gradient Model on Unstructured Grids", *IEEE Trans. Electron Devices* , vol. 48, no. 2, pp.279-283,2001.

[2.24] Y.P. Varshni , "Temperature dependence of the energy gap in semiconductors.," *Physica* ,vol. 34,pp.149–154,1967. https://doi.org/10.1016/0031-8914(67)90062-6.

[2.25] I. Yeo, J. D. Song, and J. Lee, "Temperature-dependent energy band gap variation in self-organized InAs quantum dots," Applied Physics Letters, vol. 99, 151909-1-3,2011. https://doi.org/10.1063/1.3651492.

[2.26] M. Oszwaldowski, and M. Zimpel, "Temperature dependence of intrinsic carrier concentration and density of states effective mass of heavy holes in InSb," *J. Phys. Chem. Solids*, vol. 49, no.10, pp. 1179-85,1988. https://doi.org/10.1016/0022-3697(88)90173-4.

[2.27] M. Barth, H. Lieu, J. H. Warner, B. R. Bennett, J. B. Boos, D. McMorrow, N.

Roche, P. Paillet, M. Gaillardin and S. Datta, “Single Event Measurement and Analysis of Antimony Based n-Channel Quantum-Well MOSFET With High- Dielectric,” *IEEE Transactions on Nuclear Science*, vol.62, pp.2807-2814,2015..https://doi.org/10.1109/TNS.2015.2498905

[2.28] John Evan Turner, Atoms, Radiation, and Radiation Protection, third ed. WILEY-VCH Verlag GmbH & Co. KGaG, Germany.2007.

[2.29] J. Nah , H. Fang ,C. Wang ,K. Takei ,M.H. Lee ,E. Plis , S. Krishna , and A. Javey , “ III–V complementary metal-oxide-semiconductor electronics on silicon substrates.,” *Nano Letters* , vol. 12, no. 7, pp. 3592–3595,2012. https://doi.org/10.1021/nl301254z.

[2.30] S. Lee, C.-Y. Huang, D.C. Elias, B.J. Thibeault, W. Mitchell, V. Chobpattana, S. Stemmer, A.C. Ossard, and M.J.W. Rodwell, “Highly scalable raised source/drain InAs quantum well MOSFETs exhibiting I_{ON} = 482μA/μm at I_{OFF}=100 nA/μm and V_{DD}=0.5 V,” *IEEE Electron Device Lett*, vol.35, no.6,pp. 621-23, 2014. https://doi.org/ 10.1109/LED.2014.2317146.

CHAPTER - 3

Effect of Temperature, Channel Thickness and Grooving Angle on Digital and Analog performance of different structures of InAs and InGaSb Field Effect Transistors

In this chapter, the author has studied the effect of change of temperature, channel thickness and angle of grooving on the analog and digital performance of InAs based on-insulator and quantum well n-MOSFET structures and InGaSb based quantum well p-MOSFET structure. The author has structured the devices in SILVACO ATLAS platform and simulated them after incorporating the physics and the models discussed in the previous chapter. All these models are calibrated by comparing the characteristics of the simulated devices with some experimentally reported results to authenticate the simulation framework.

3.1 Introduction

With advancement in nanotechnology, group III-V materials are slowly getting wide acceptance over conventional Silicon. In this work, the author has chosen InAs as the material of study for n-MOSFET because of its very low effective mass which is about 46 times less compared to Silicon at 300 K. Due to this, the electron mobility in InAs increases by almost 20 times compared to that in Silicon. Also, the bandgap of InAs at T=300 K is about 0.35 eV while it is 1.1 eV for Silicon. For this low bandgap, InAs can work at low V_{DD} and has low threshold voltage. Also, unlike Silicon, InAs is one direct semiconductor which enables InAs to have both electronic and optoelectronic applications. [3.1- 3.10].However, due to its narrow bandgap feature, OFF-current is very high. Also, due to low effective mass of electrons, there are low

density of states which limit the drain current. However, in this part of work, the author has also considered InGaSb as the channel material for quantum well p-MOSFET mainly because of its high hole mobility compared to Silicon [3.11-3.15].

To enhance the performance of nanoelectronic devices, several novel architectures like thin-channel devices, on-insulator structures, asymmetric source/drain structures, raised source/drain structures are being explored nowadays.

Among the many factors that govern the performance of the device, temperature plays a crucial role. [3.16-3.27] Both mobility and carrier concentration that determines the conductivity of a semiconductor are temperature dependent parameters. Years back in 1967, Y.P. Varshni proposed the relationship of the dependency of energy bandgap of semiconductors on temperature [3.16].In 2009, A.C. Ford *et. al.* showed in their paper the effect of surface roughness scattering on mobility degradation of InAs nanowire at low temperature [3.18]. In 2013, N. Gupta and her group showed that effective electron mobility in InAs nanowire increases in the temperature range of 30 K to 50 K and above 50 K, mobility decreases [3.20]. In 2000, R. Quay *et. al.* presented a model showing the temperature dependence of saturation velocity of elementary binary and alloyed semiconductors [3.25].So, the changes in temperature affect the speed, power and reliability of the system. Structurally, the angle of grooving (θ) which controls the effect of electric field on the channel also plays an important role in the performance of the device. S. Lee *et. al.* in 2013 and 2014 showed that with the inclusion of vertical spacer between channel and source/drain, there is significant improvement in OFF-state characteristics without having significant impact in on-state [3.9-3.10]. Also, thinning of channel thickness is the state-of the art trend which is followed to improve the OFF-state characteristics of the devices. K. Takei and his group in 2011 has shown reduction in OFF current with decrease in channel

thickness of InAs-on-insulator transistor [3.3]. In 2016, T. Dutta *et. al.* modelled equations to evaluate the variation of effective mass and bandgap on channel thickness of InAs and InSb MOSFETs [3.7].Md.N.K. Alam and his group in 2015 showed the betterment of the OFF-state and ON-state characteristics of InGaSb-on-insulator n-MOSFET with the variation of channel thickness.[3.28]In 2017, J. Lin *et. al.* showed the strong impact of channel thickness on the device characteristics of self-aligned InGaAs quantum well n-MOSFET.[3.29]

In this chapter, the author has discussed how the change of temperature, channel thickness and angle of grooving affect the digital and analog performance of the device. Parameters like bandgap, carrier concentration, non-parabolicity factor as well as effective mass, electron affinity, saturation velocity, threshold voltage are some of the important temperature and channel thickness dependent parameters of the device which control the device performance .Thus, temperature and channel thickness change influence various material and transport properties which ultimately affect the current-voltage characteristics of the device. Also, the change of the effect of electric field on the channel with changes in grooving angle is incorporated in this work.

In this chapter, first the author has made a comprehensive investigation towards the analog/RF performances of 30 nm channel length InAsOI (on-insulator) n-MOSFETs at T=300K with the channel thickness varying from 5 nm to 25 nm [3.30]. Then, the author has studied the logic and analog performances of 14 nm channel length InAs quantum well n-MOSFETS with raised source/drain architecture with the channel thickness in the range of 5 – 10 nm in the temperature range of 150K to 300 K [3.31-3.32]. Here, the author has also included effect of variation of the angle of grooving (θ) on the analog performance of InGaSb based 14nm channel length p-

MOSFET with raised source/drain architecture with the channel thickness of 5 nm and θ varying from 40^0 to 90^0 at T= 300 K [3.31].

This chapter is organised as follows: In the section 3.2.1 InAsOI structure with the device parameters are given followed by InAs quantum well n-MOSFET with parameter specification in section 3.2.2. This section is followed by the structure of InGaSb quantum well p-MOSFET in section 3.2.3. The various models and the simulation schemes that are used are incorporated in section 3.3. This section also covers the validation of the developed model with simulation results and experimental data for both on-insulator and quantum well structures. After that results from the model and the respective comparative analysis are presented in section 3.4 and 3.5, respectively. Finally this chapter is summarised in section 3.6.

3.2 Device Structure

3.2.1 InAsOI n-MOSFET

The top gated InAsOI n-MOSFET with fabrication steps shown in Fig. 3.1. The device is having a channel length of 30nm and has ZrO_2 as the gate dielectric and SiO_2 as the buried oxide layer (BOX). The summary of the material specifications is given in Table I.

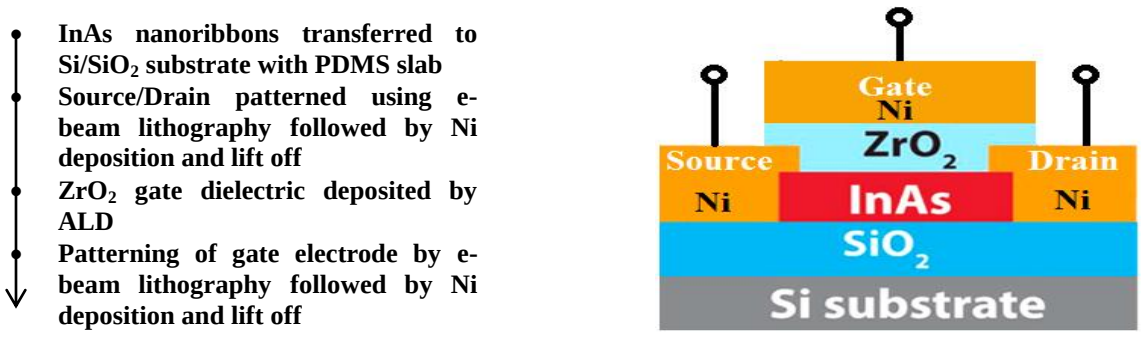


Fig. 3.1: Fabrication steps and schematic structure of a top gated InAsOI NMOS with ZrO_2 as the gate dielectric. Nickel is used for the gate material and also for source and drain contacts.

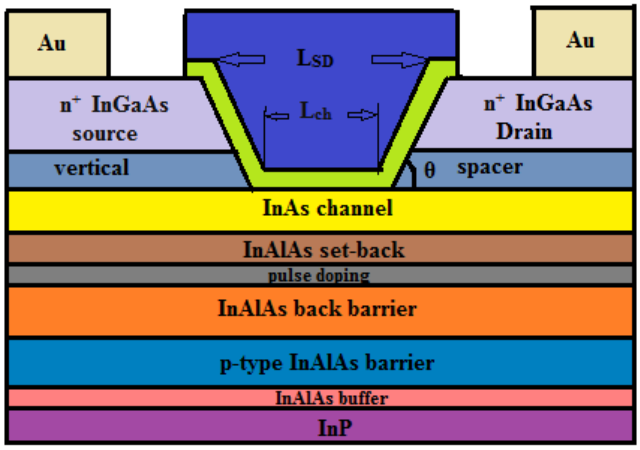
Table I: Dimensions of various material layers of InAsOI n-MOSFET shown in Fig. 3.1.

Material	Parameters	Values
InAs (channel material)	Channel length (L_{ch})	30nm
	Channel Thickness(t_{ch})	5nm - 25nm
ZrO_2 (gate dielectric)	Dielectric constant	22
	Thickness	4nm
SiO_2 (buried oxide layer)	Dielectric constant	3.9
	Thickness	0.1 μm
Nickel (gate metal)	Work function	5.1eV

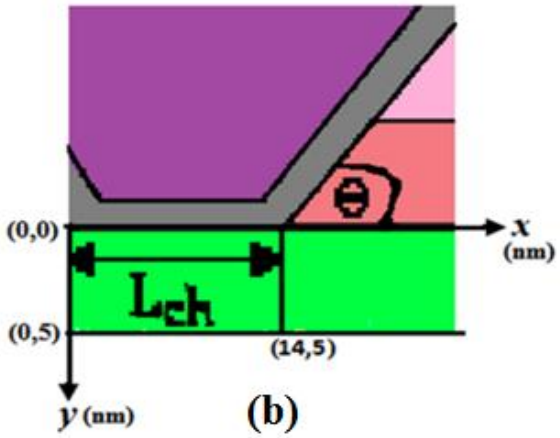
3.2.2 InAs quantum well n-MOSFET

14-nm channel length InAs quantum well n-MOSFETs featuring $In_{0.53}Ga_{9.47}As$ spacer layers between the channel and n^+ source/drain with angle of grooving (θ) is shown in Fig. 3.2(a) with the fabrication steps. Fig. 3.2(b) portrays more clearly the dimensions of device structure. The actual gate length is the distance between the vertical spacers following [3.10]. It is equal to the channel length (14 nm) which is the length of the InAs material making a direct contact with the gate dielectric as portrayed in Fig. 3.1(a) and (b). This length (L_{ch}) and the distance between the source and drain gold (Au) contacts remain fixed at 14 nm and 406 nm, respectively for all devices with all grooving angles. However, the distance between source and drain terminals (L_{SD}) changes from 183 nm to 14 nm as the angle of grooving (θ) increases from 40^0 to 90^0. The summary of the various material layers with their respective thickness and doping is given in Table II and the various material specifications are given in Table III.

- **Different layers of InAlAs , InAs channel layer and InGaAs cap layer formed on InP by solid source molecular beam epitaxy**
- **Groove angle defined with dummy gate patterned using HSQ based e-beam lithography**
- **Native oxide etched in dilute HCl**
- **Vertical spacer and N^+ S/D formed using MOCVD technique**
- **Device irregularities, dummy gates, cap layer, extra layer of InAs removed by etching**
- **HfO_2 gate dielectric deposited by ALD. Angular dimension (θ) and L_{SD} maintained using coordinate geometry**
- **Post forming gas annealing, Ni gate and Au S/D formed**



(a)



(b)

Fig. 3.2 (a) Fabrication steps and cross-sectional view of InAs channel quantum well n-MOSFET with L_{ch} as the channel length, L_{SD} as the upper spacing between the source and drain terminals and θ as the angle of grooving. (b)Expanded view showing L_{ch} and Θ clearly.

Table II: Dimensions of various material layers of InAs quantum well n-MOSFET shown in Fig. 3.2

Layer (symbol)	Material	Thickness unit	Doping (type)
Buffer	InAlAs	50 nm	-
Barrier	InAlAs	250 nm	$1\times10^{17}/cm^3$ (p-type)
Back Barrier	InAlAs	100 nm	-
Pulse doping	InAlAs	2 nm	$1\times10^{12}/cm^2$ (n-type)
Setback	InAlAs	5 nm	-
Channel Thickness (t_{ch})	InAs	Varied in the range of 5 – 10 nm	-
Vertical spacer	InGaAs	2 nm	$1\times10^{15}/cm^3$ (n-type)
Source and drain	InGaAs	60 nm	$4\times10^{19}/cm^3$ (n-type)
Channel length (L_{ch})	InAs	14 nm	
Channel width (W)	InAs	1 µm	
Gate oxide thickness	HfO_2	3 nm	

Table III: Material specifications of different layers of InAs quantum well n-MOSFET shown in Fig. 3.2

Material	Mole Fraction x	Electron Affinity (eV)	Bandgap (eV)	Ref
$In_x Al_{1-x} As$	0.52	4.66	1.5	[3.34]
$In_x Ga_{1-x} As$	0.53	4.5	0.74	

3.2.3 InGaSb quantum well p-MOSFET

Fig. 3.3 shows the cross-sectional view of InGaSb quantum well p-MOSFET, the specifications of which are detailed in Table IV, other material specifications remaining same as Table III.

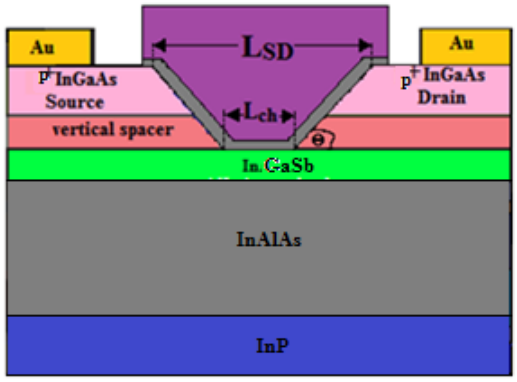


Fig.3.3. Cross-sectional view of InGaSb channel quantum well p-MOSFET with raised source/drain architecture.

3.3 Simulation set-up and model validation

As already discussed, the author has used SILVACO ATLAS [3.35] as the numerical device simulator. For the simulation of the device structures, the author has employed the following models, the details of which are already been discussed in the previous chapter. For mobility of the carriers, both concentration and temperature dependent low field analytic mobility model and also the high field mobility model which includes the effects of lateral electric field and saturation velocity are incorporated in the simulation [3.36, 3.14]. To capture effects of carrier-carrier scattering on mobility, Conwell-Weisskopf model is employed [3.37]. To include the process of generation and recombination of carriers, both non-radiative as well as radiative recombination models together with impact ionization model are being used [3.38-3.41].

Table IV: Dimensions of various material layers of InGaSb quantum well p-MOSFET shown in Fig. 3.3.

Layer (symbol)	Material	Thickness unit	Doping (type)
Buffer	InAlAs	50 nm	-
Barrier	InAlAs	250 nm	$1\times10^{17}/cm^3$ (n-type)
Back Barrier	InAlAs	100 nm	-
Pulse doping	InAlAs	2 nm	$1\times10^{12}/cm^2$ (p-type)
Setback	InAlAs	5 nm	-
Channel Thickness (t_{ch})	InGaSb	5 nm	-
Angle of grooving(θ)	-	Varied from 40° to 90°	
Vertical spacer	InGaAs	2 nm	$1\times10^{15}/cm^3$ (p-type)
Source and drain	InGaAs	60 nm	$4\times10^{19}/cm^3$ (p-type)
Channel length (L_{ch})	InGaSb	14 nm	
Channel width (W)	InGaSb	1 µm	
Gate oxide thickness	HfO_2	3 nm	

The concept of tunneling of carriers is covered through tunneling models like band-to-band tunneling model and trap assisted tunneling model [3.42-3.43]. The distribution of carriers is also being considered through Fermi-Dirac analysis. To include quantum effects in carrier transport, drift and diffusion process of current flow is used along with the density gradient model. Physics related to the effect of change of temperature on bandgap, effective mass and saturation velocity as well as temperature dependent recombination models are well integrated in the simulation [3.44-3.46] .To substantiate the use of the physics and models in the simulated structures, the

author has validated the characteristics of both on-insulator and quantum well structures with some experimentally reported results.

The author has compared the transfer characteristics obtained from the simulation of InAsOI structure with the reported experimental results [3.4] featuring InAsOI n-MOSFET structure having channel thickness of 13 nm and channel length of 2.85 μm on 1.6 μm thick SiO_2 layer with 10 nm thick ZrO_2 as the top gate dielectric for two different values of the supply voltage as shown in Fig. 3.4. It is very clear that the simulated transfer characteristics match quite well with the experimental characteristic curves reported in [3.4] for the two different supply voltages. This fact ensures the validity of the models used in the simulation set-up for obtaining terminal characteristics of InAs on insulator devices.

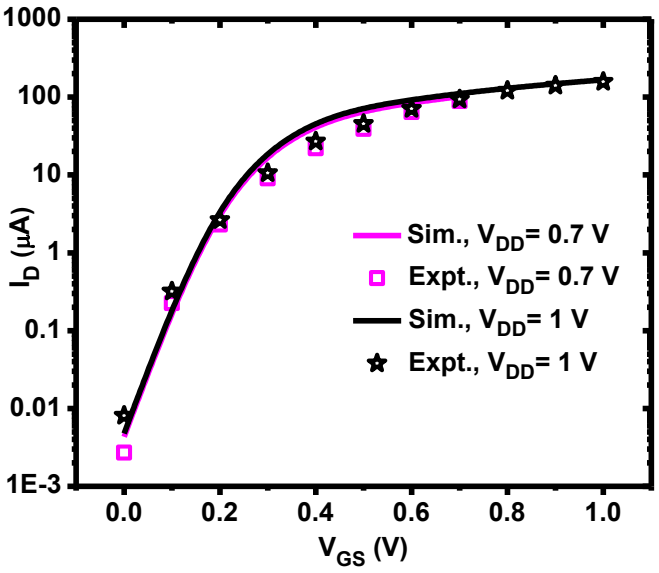


Fig.3.4: Comparison of simulation and experimental transfer characteristics of InAs NMOS having channel length of 2.85μm and channel thickness of 13 nm for two different values of supply voltage V_{DD} = 0.75 V and 1 V, respectively. Symbols represent experimental data [3.4] whereas the continuous line represents the simulation results.

During the calibration of the quantum well structure, the author has compared the simulated transfer characteristics and the variation of transconductance (g_m) with respect to gate voltage

(V_{GS}) with the experimental results of InAs quantum well n-MOSFET having t_{ch}= 5 nm and L_{ch}= 18 nm with angle of grooving (θ) as 40^0 [3.10]. From Fig. 3.5,it can be found out that the simulated data matches well with the experimental results reported in[3.10] which certainly validates the simulation framework for quantum well MOSFET.

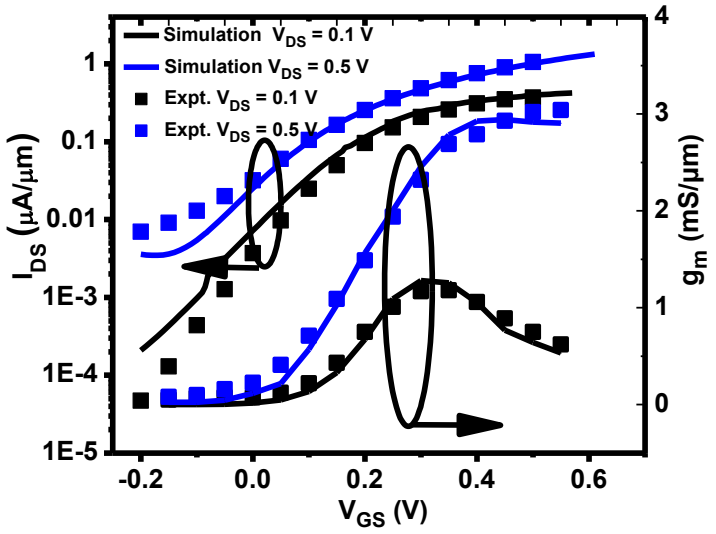


Fig. 3.5:Comparison of simulation and experimental results of transfer characteristics (primary axis) and transconductance (secondary axis) of InAs quantum well n-MOSFET for V_{DS} = 0.1 V and V_{DS} = 0.5 V. Symbols represent experimental data [3.10] whereas the continuous line represents simulation results.

3.4 Results and Discussions

3.4.1 Impact of channel thickness on analog/RF performance of InAs on-insulator n-MOSFET

The variation of drain current (I_D) as a function of gate overdrive voltage (V_{GT}) is shown in Fig. 3.6 in linear and logarithmic scales for InAsOI NMOS devices having five different thicknesses viz. 5 nm, 7 nm, 15 nm, 20 nm and 25 nm at channel length of 30 nm and compared with Si NMOS device with channel thickness of 5 nm. At a fixed value of gate overdrive voltage, InAsOI MOS device with the channel thickness of 25 nm exhibits largest drain current due to

increased number of inversion carriers with the increase in channel thickness. The lowest drain current is obtained for SOI NMOS device with channel thickness of 5 nm because of its low electron mobility as compared to InAsOI devices.

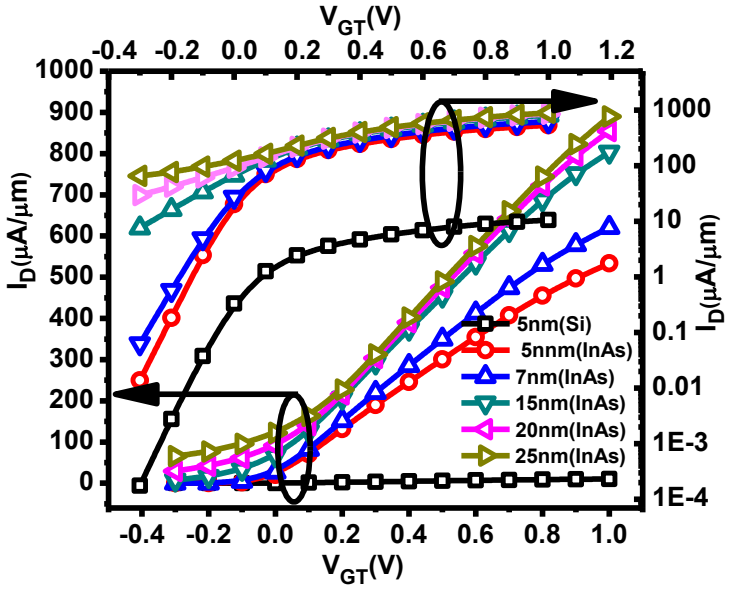


Fig. 3.6: Transfer characteristics of InAsOI NMOS devices having five different channel thicknesses viz. 5 nm, 7 nm, 15 nm, 20 nm and 25 nm and SOI NMOS device with channel thickness of 5 nm at L_{ch} = 30 nm and V_{DS} = 0.5 V.

The transconductance (g_m) is demonstrated with V_{GT} in Fig. 3.7 for both InAsOI and SOI NMOS devices for five different channel thickness (t_{ch}) values at channel length of 30 nm. It can easily be seen from Fig. 3.7 that maximum and minimum values of g_m are observed for InAsOI device having channel thickness of 25 nm and 5 nm, respectively. This nature is commensurate with the results obtained using the relation $g_m = 2I_D/V_{GT}$.

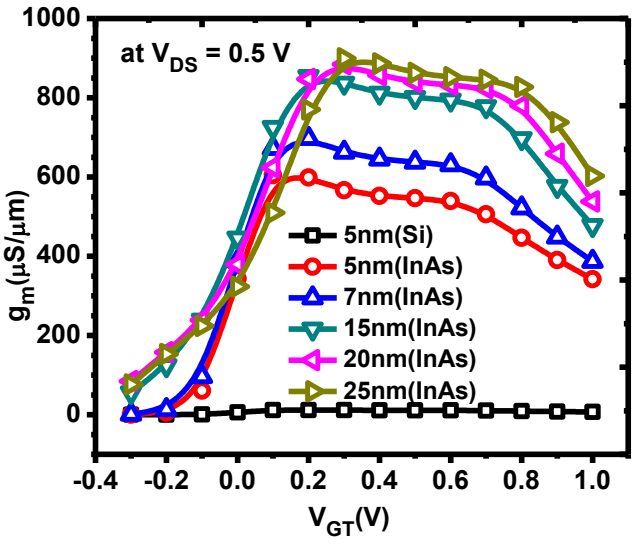


Fig. 3.7: Variations of transconductance (g_m) with respect to V_{GT} of InAsOI NMOS devices having channel thickness of 5nm, 7nm, 15nm, 20nm and 25nm and that for SOI NMOS device with channel thickness of 5 nm at L_{ch} = 30 nm and V_{DS} = 0.5 V.

Fig. 3.8 shows the variation of output conductance (g_d) with V_{GT} for different InAsOI devices and is compared with the result of 5 nm thick SOI device at channel length of 30 nm. The highest value of g_d in InAsOI device having channel thickness of 25 nm is due to the increased amount of short channel effects in such a device. The value of g_d becomes lower as the channel thickness reduces. From Fig. 3.8 it is evident that at V_{GT} = 0.5 V g_d in the InAsOI device having channel thickness of 5 nm reduces by 94 % as compared with that in InAsOI device with channel thickness of 25 nm. Fig. 3.9 compares the voltage gain A_V of the InAsOI devices with five different channel thicknesses and SOI device with channel thickness of 5 nm as a function of V_{GT}.

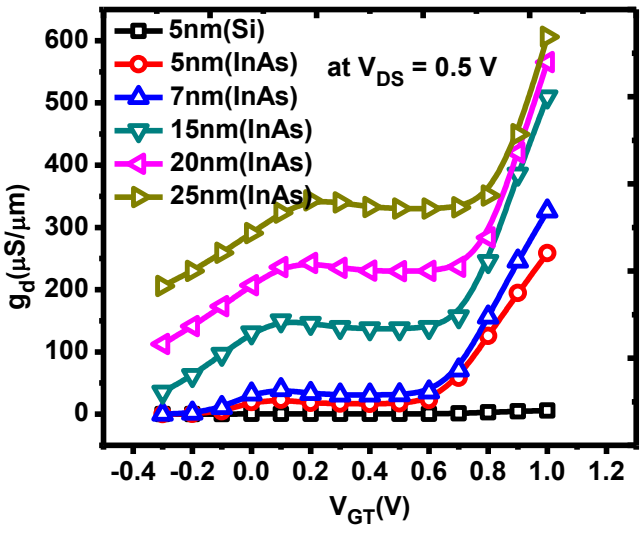


Fig. 3.8: Variations of g_d with V_{GT} for both InAsOI NMOS devices having channel thickness of 5 nm, 7 nm, 15 nm, 20 nm and 25 nm and that of SOI NMOS device with channel thickness of 5 nm at L_{ch} = 30 nm and V_{DS} = 0.5 V.

It can be easily noticed from Fig. 3.9 that the 5 nm thickened InAsOI device shows significant improvement in voltage gain compared to the other devices as the device shows considerable reduction in g_d despite partial compensation of g_m. Notably, the peak gain improves by 60% for InAsOI device with respect to SOI device for the same channel thickness of 5 nm. The transconductance generation factor or transconductance efficiency (g_m/I_D) for the InAsOI and SOI devices are almost equal at the same channel thickness of 5 nm as shown in Fig. 3.10.The transconductance efficiency for InAsOI and SOI devices remains the same as both the drain current and transconductance show the similar dependency on the channel thickness. The improvement of transconductance generation factor in the subthreshold region of operation is attributed to the significant reduction in drain current and considerable value of g_m in such a region.

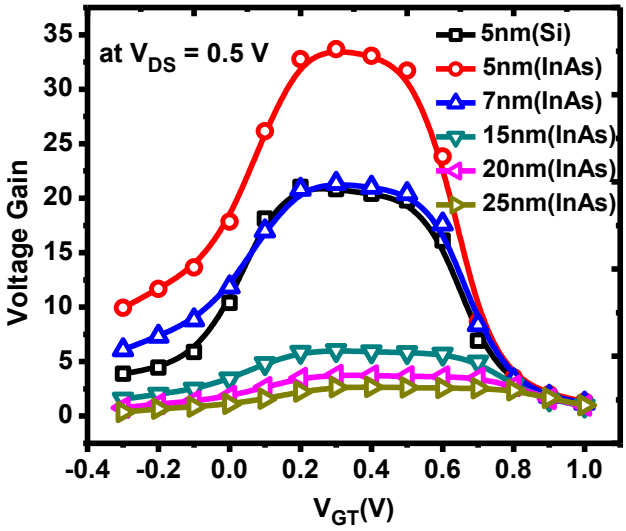


Fig. 3.9: Variations of voltage gain with respect to V_{GT} of InAsOI NMOS devices having channel thicknesses of 5 nm, 7 nm, 15 nm, 20 nm and 25 nm and that of SOI NMOS having channel thickness of 5 nm at L_{ch} = 30 nm and V_{DS} = 0.5 V.

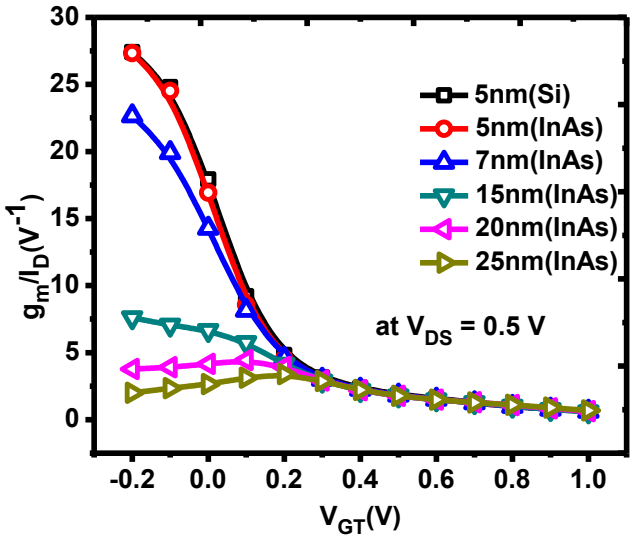


Fig. 3.10: Variations of transconductance efficiency (g_m/I_D) with respect to V_{GT} of InAsOI NMOS devices having channel thickness of 5 nm, 7 nm, 15 nm, 20 nm and 25 nm and that of SOI NMOS device with t_{ch} of 5 nm at L_{ch} = 30 nm and V_{DS} = 0.5 V.

The variation of unity-gain cut-off frequency and maximum frequency of oscillations with respect to V_{GT} for both InAsOI and SOI devices are shown in Figs. 3.11 and 3.12, respectively . The peak values of f_T and f_{max} for InAsOI devices with 25 nm channel thickness are,

respectively, 49% and 187% larger than the corresponding values for InAsOI devices with 5 nm channel thickness.

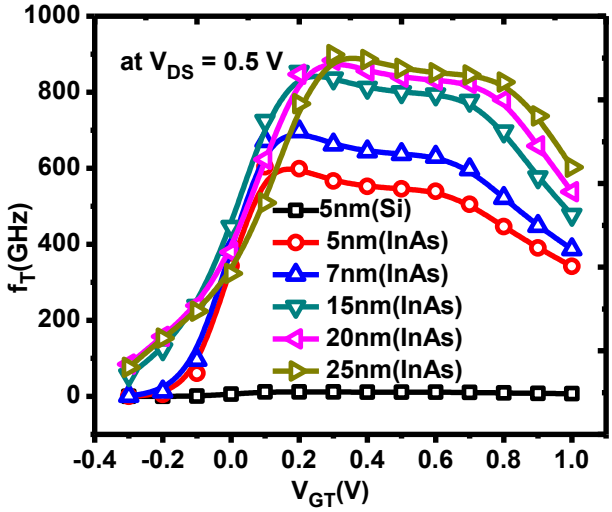


Fig. 3.11: Variation of cut-off frequency (f_T) with V_{GT} for InAsOI NMOS devices having channel thickness of 5 nm, 7 nm, 15 nm, 20 nm and 25 nm and that of SOI NMOS having channel thickness of 5 nm at L_{ch} = 30 nm and V_{DS} = 0.5 V.

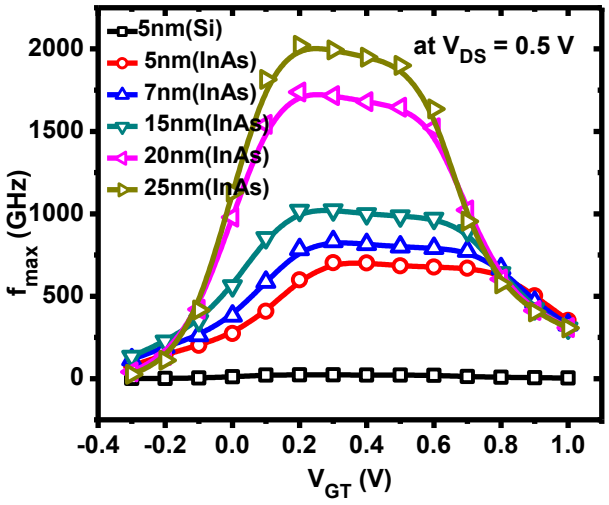


Fig. 3.12: Variations of maximum frequency of oscillations (f_{max}) with V_{GT} of InAsOI NMOS devices having channel thicknesses of 5 nm, 7 nm, 15 nm, 20 nm and 25nm and SOI NMOS having channel thickness of 5 nm at L_{ch} = 30 nm and V_{DS} = 0.5 V.

The improvement in f_T is primarily accounted for the enhanced value of g_m and that in f_{max} is due to augmented value of g_m despite partial compensation of g_d of InAsOI devices .

3.4.2 Impact of channel thickness and temperature on digital performance of InAs quantum well n-MOSFET at V_{DS} =0.5V

For InAs quantum well n-MOSFET devices having channel thicknesses in the range of 5 -10 nm and at channel length of 14 nm, the variation of drain current (I_D) with V_{GT} in both linear and log scale at T=300K is shown in Fig. 3.13. At a particular value of V_{GT}, 10 nm thick MOS device shows the maximum value of drain current mainly because of increasing number of inversion carriers with the increase in channel thickness.

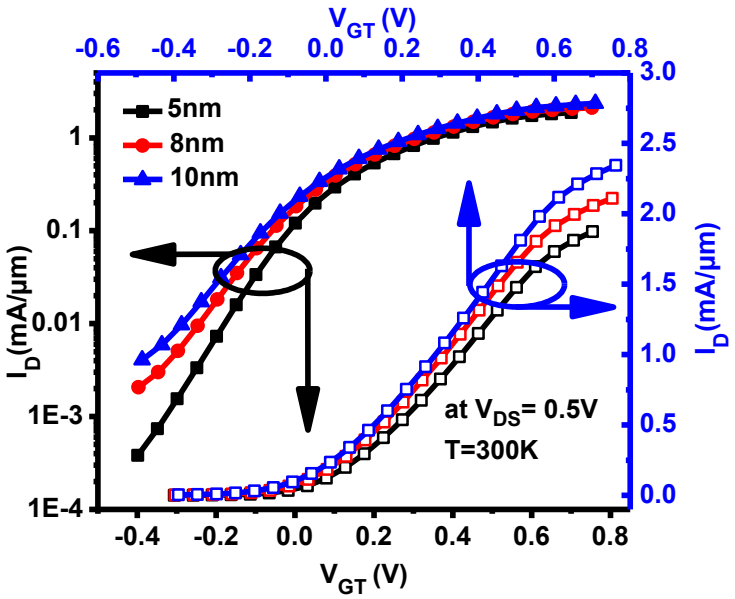


Fig. 3.13: Transfer characteristics at T=300K as a function of V_{GT} for different values of t_{ch} viz. 5 nm ,8 nm and 10 nm of InAs quantum well n-MOSFET for V_{DS}=0.5 V and L_{ch} = 14 nm.

Also, the temperature dependency of ON-current and OFF-current are shown in Fig. 3.14 & Fig. 3.15, respectively. For the entire range of temperature, ranging from 150 K to 300K, high value of ON-current (I_{ON}), calculated at V_{GS}= V_{DS}=0.5V, is observed in InAs quantum well n-MOS device having channel thickness of 10 nm. This variation of ON-current is due to increase of

electron concentration with increase of channel thickness and temperature as explained in the following.

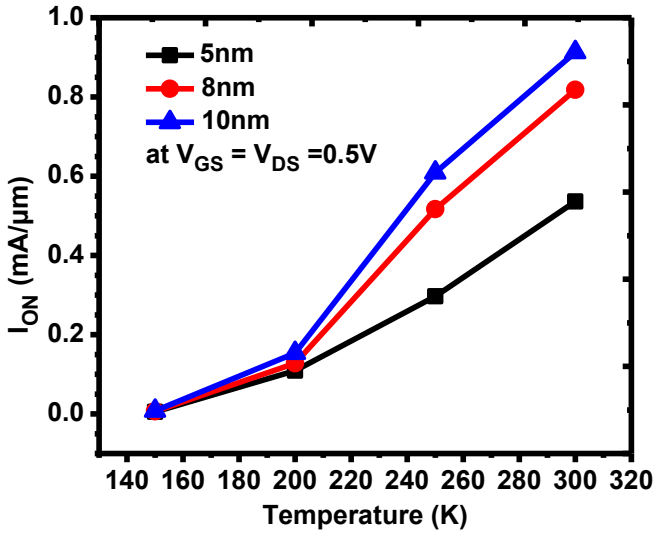


Fig. 3.14: Variation of ON-current with temperature for different values of t_{ch} viz. 5 nm ,8 nm and 10 nm of InAs quantum well n-MOSFET for V_{DS}=0.5 V and L_{ch} = 14 nm.

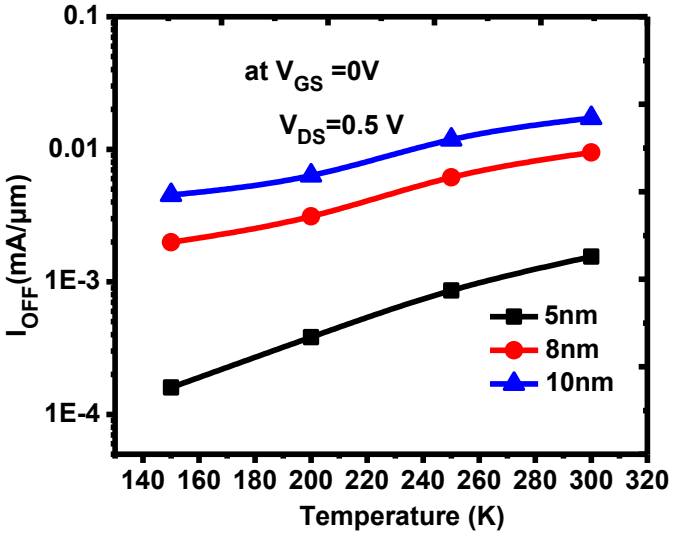


Fig. 3.15: Variation of OFF-current with temperature for different values of t_{ch} viz. 5 nm ,8 nm and 10 nm of InAs quantum well n-MOSFET for V_{DS}=0.5 V and L_{ch} = 14 nm.

2-D electron concentration distribution within the channel under bias condition of V_{GT} =0.5V and V_{DS}= 0.5V for the devices with t_{ch}=5 nm and 10 nm at T=300K and 150K are, respectively, shown in Fig. 3.16[(a)-(d)]. From the fig. it is clear that the total electron concentration in the channel increases for the larger value of t_{ch} and for higher temperature, compared to smaller t_{ch} and lower temperature under the identical bias conditions. At T=300K, towards the drain end of the channel, the electron concentration changes from 7.07×10^{18} cm^{-3} to 1.15×10^{18} cm^{-3} for t_{ch}= 5nm, while for t_{ch}=10nm, the change is from 8.7×10^{18} cm^{-3} to 1.25×10^{18} cm^{-3}. However, this variation at T=150K is within 6.3 - 1.25×10^{18} $cm^{-3}$for t_{ch}=5nm and within 8 - 1.2×10^{18} $cm^{-3}$for t_{ch}=10nm.

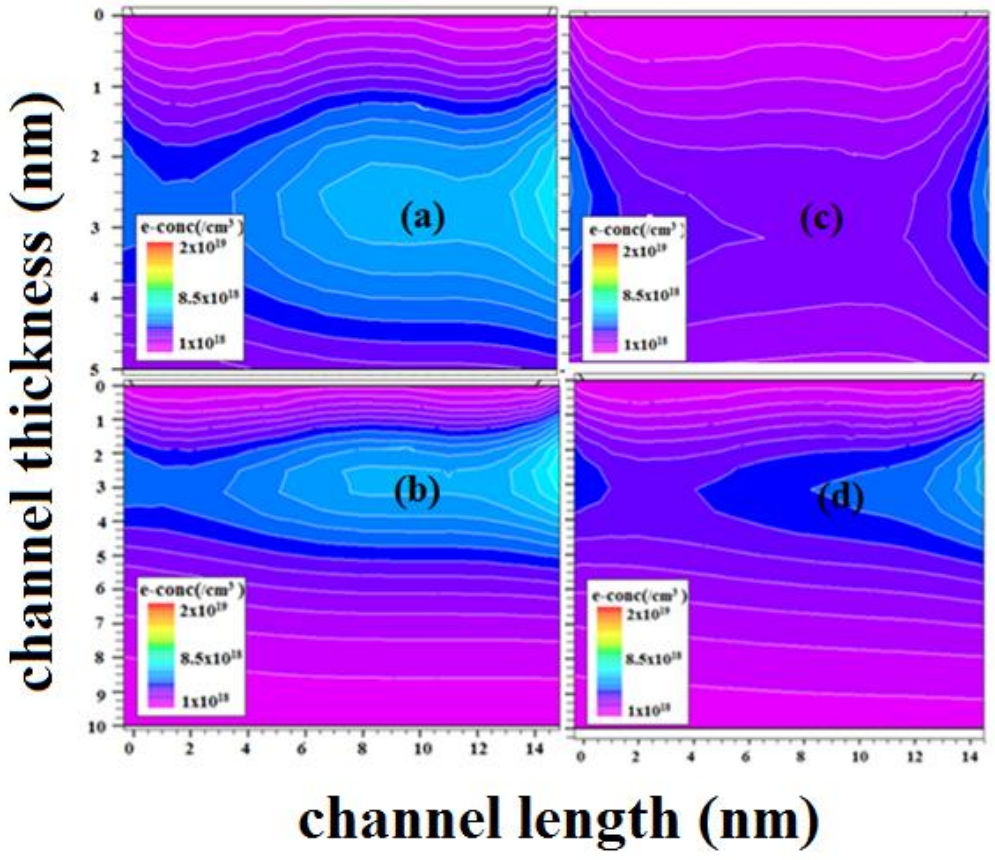


Fig. 3.16:2-D distribution of electron concentration for device (a) t_{ch}=5nm and T=300K (b) t_{ch}=10 nm and T=300 K (c) t_{ch}=5nm and T=150 K (d) t_{ch}=10nm and T=150K of InAs quantum well n-MOSFET at V_{DS} = 0.5V and V_{GT}= 0.5V for L_{ch}=14nm.

Due to the higher values of electron concentration in the channel, the highest I_{ON}, measured at $V_{GS}=V_{DS}=0.5$ V, is observed in the device with t_{ch}= 10 nm at T=300K. Thus, improvement in ON-current, for t_{ch}= 10 nm are by 70.23% and 48.86% compared to the device with t_{ch}= 5 nm at T=300K and T=150K, respectively. The values of OFF-current, measured at V_{GS}= 0 V and V_{DS}= 0.5V are shown in Fig. 3.15. The 5 nm channel thickness device is showing lower values of OFF-current for the whole range of temperature. As the bandgap of InAs channel varies inversely with channel thickness and temperature as shown in Table V, the smaller bandgap device shows lesser value of threshold voltage and hence increased subthreshold leakage current at high temperature. The lowest I_{OFF} with t_{ch}= 5 nm at 150 K comes out to be 20 times less compared to I_{OFF} at T=300K. This variation of OFF and ON current is reflected in ON-OFF current ratio as displayed in Fig. 3.17. This figure shows the highest ON-OFF current ratio of 345.95 at 300 K for 5nm InAs channel device and the lowest one of 1.74 at T=150 K for 10 nm thick channel device.

The intrinsic delay which varies inversely with ON-current, shows improvement with increasing temperature and thickness as shown in Fig.3.18. Minimum delay of 35.54 ps is obtained for 10 nm thick InAs device at 300 K whereas the highest delay of 6145.83 ps is obtained for 5 nm thick device at 150 K.

Table V: Summary of material and transport parameters of channel used in simulation and measured threshold voltage

Parameter (Unit)	Temp (K)	Value		
		10 nm	8 nm	5 nm
Band gap (eV)	300	0.43	0.46	0.58
	150	0.468	0.498	0.618
Intrinsic carrier concentration (cm^{-3})	300	5.93×10^{13}	3.67×10^{13}	4.48×10^{12}
	150	1.27×10^{9}	4.37×10^{8}	5.21×10^{6}
Electron density of states, N_c ($/cm^3$)	300	1.64×10^{17}	2.01×10^{17}	3.11×10^{17}
	150	6.57×10^{16}	7.91×10^{16}	1.21×10^{17}
Hole density of states, N_V ($/cm^3$)	300	6.6×10^{18}	6.6×10^{18}	6.6×10^{18}
	150	2.33×10^{18}	2.33×10^{18}	2.33×10^{18}
Non-parabolicity factor (eV^{-1})	300	2.16	2.0	1.54
	150	1.97	1.83	1.43
Effective mass of electrons(m_0)	300	0.035	0.04	0.0535
	150	0.038	0.043	0.057
Threshold voltage (V)	300	0.238	0.247	0.299
	150	0.3	0.308	0.316

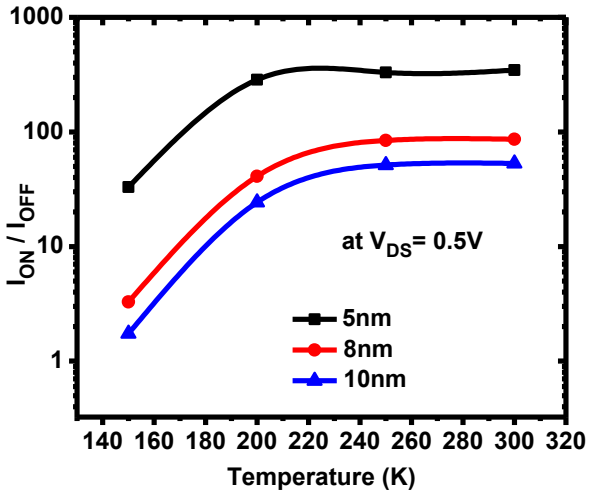


Fig.3.17: Plot of I_{ON}/I_{OFF} with temperature for different values of t_{ch} viz. 5 nm ,8 nm and 10 nm of InAs quantum well n-MOSFET for V_{DS}=0.5 V and L_{ch} = 14 nm.

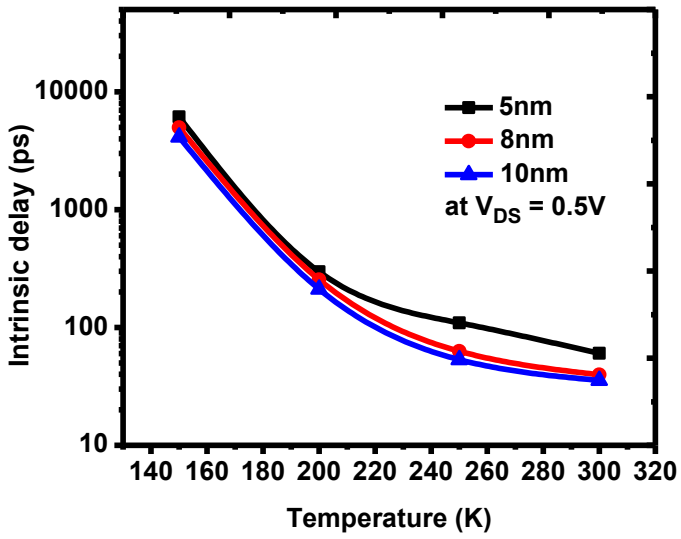


Fig. 3.18: Plot of Intrinsic Delay with temperature for different values of t_{ch} viz. 5 nm ,8 nm and 10 nm of InAs quantum well n-MOSFET for V_{DS}=0.5 V and L_{ch} = 14 nm.

3.4.3 Impact of channel thickness and temperature on digital and analog performance of InAs quantum well n-MOSFET

To further continue the work on the proposed quantum well structure, the author has raised the supply voltage to 0.8V. Under this biasing condition, the author has again studied the aforesaid logic parameters at supply voltage of 0.8 V and also studied the analog parameters at the voltage of $V_{DD}/2$ i.e. 0.4 V.

3.4.3.1 Impact of channel thickness and temperature on digital performance of InAs quantum well n-MOSFET at V_{DS} =0.8 V

The temperature dependency of ON-current and OFF-current are shown in Figs. 3.19 and Fig. 3.20, respectively. 10 nm thick InAs quantum well n-MOS device shows high value of ON-current (I_{ON}), calculated at V_{GS} = V_{DS}= V_{DD} = 0.8 V, for the entire range of temperature due to rise of carrier concentration in such a device.

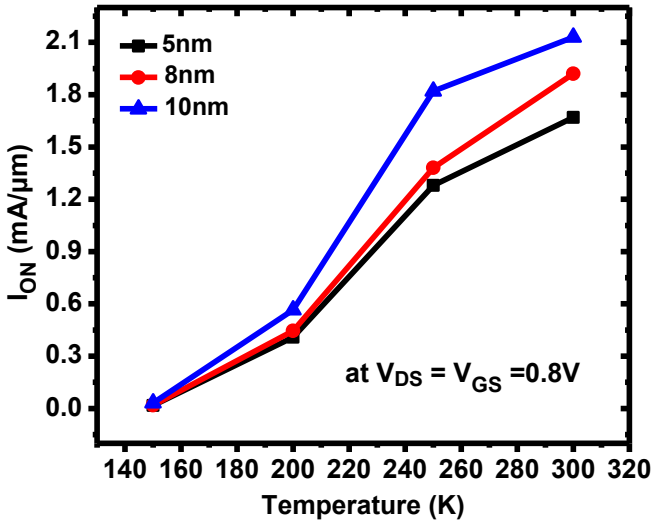


Fig. 3.19 : Variation of ON-current with temperature for different values of t_{ch} viz. 5 nm ,8 nm and 10 nm of InAs quantum well n-MOSFET for V_{DS}=0.8 V and L_{ch} = 14 nm.

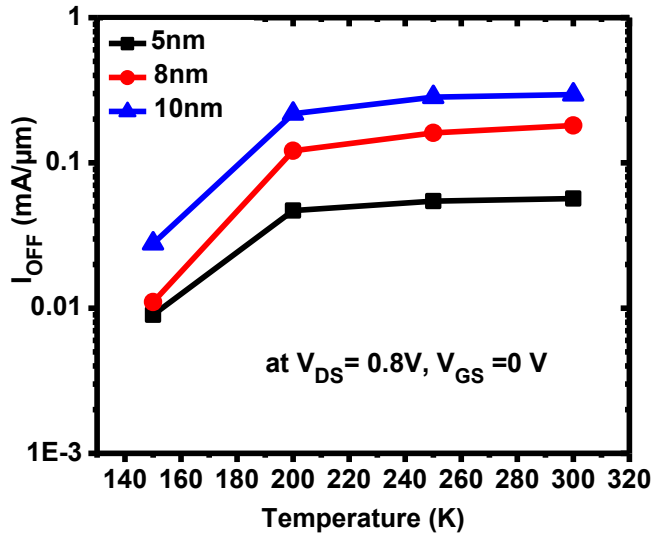


Fig. 3.20: Variation of OFF-current with temperature for different values of t_{ch} viz. 5 nm ,8 nm and 10 nm of InAs quantum well n-MOSFET for V_{DS}=0.4 V and L_{ch} = 14 nm.

The improvement of ON-current with increment in channel thickness and temperature is due to increment of electron concentration with increasing channel thickness and temperature as revealed from the following in-depth analysis. At the bias condition of V_{GT} = 0.4 V and V_{DS}= 0.4 V, the distribution of electron concentration within the channel length (L_{ch}) for 5 nm and 10 nm

thickened devices at T = 300 K and 150 K are, respectively, shown in Fig. 3.21[a–d]. Fig. 3.21[a–d] shows that under the identical bias conditions, the total electron concentration in the channel is more for a larger value of t_{ch} and for higher temperature compared to that for smaller t_{ch} and lower temperature.

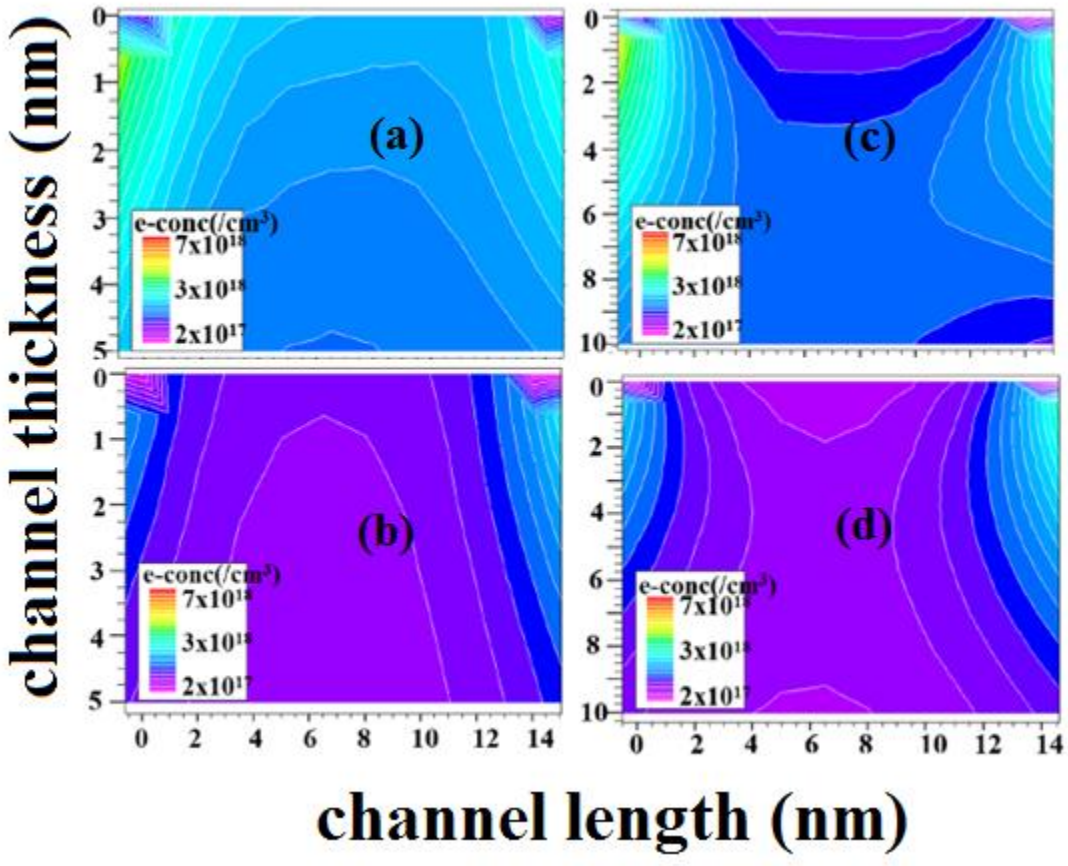


Fig. 3.21:2-D electron concentration profile in the channel under the gate for device (a) t_{ch}=5nm and T=300K (b) t_{ch}=5nm and T=150K (c) t_{ch}=10nm and T=300K (d) t_{ch}=10nm and T=150 K of InAs quantum well n-MOSFET at V_{DS} = 0.4V and V_{GT}= 0.4V for L_{ch}=14nm.The left and right sides indicate source and drain ends, respectively.

It is found that at T = 300 K, the electron concentration within the channel changes from 3×10^{18} $cm^{-3}$to 4×10^{17} cm^{-3} for t_{ch} = 5 nm whereas for t_{ch} = 10 nm, the concentration decreases from 5×10^{18} cm^{-3} to 7×10^{17} cm^{-3}. However, at T = 150 K, this change ranges between 2×10^{18}– 2×10^{17} cm^{-3} for t_{ch}= 5 nm and between 4×10^{18}–5×10^{17} $cm^{-3}$for t_{ch} = 10 nm. Also, the effective electric field profiles across the drain-end gate edge for 5 nm and 10 nm thickened devices at T=300K

and 150K at V_{GT} = 0.4 V and V_{DS}= 0.4 V are respectively, shown in Fig. 3.22[(a)-(d)] which reveals that, the effective electric field in the channel is more for a larger value of t_{ch} and for higher temperature compared to that for smaller t_{ch} and lower temperature under the identical bias conditions. While at T=300K, the effective electric field lies in the range 4×10^5-3×10^4 V/cm for the device with t_{ch} =5nm, the corresponding range increases to 6×10^5 – 5×10^4 V/cm for the device with t_{ch} =10nm. However, this variation of effective electric field at T=150K, is in the range of 3×10^5 – 2×10^4 V/cm for the device with t_{ch} =5nm and in the range of 5×10^5 – 4×10^4 V/cm for the device with t_{ch} =10nm.

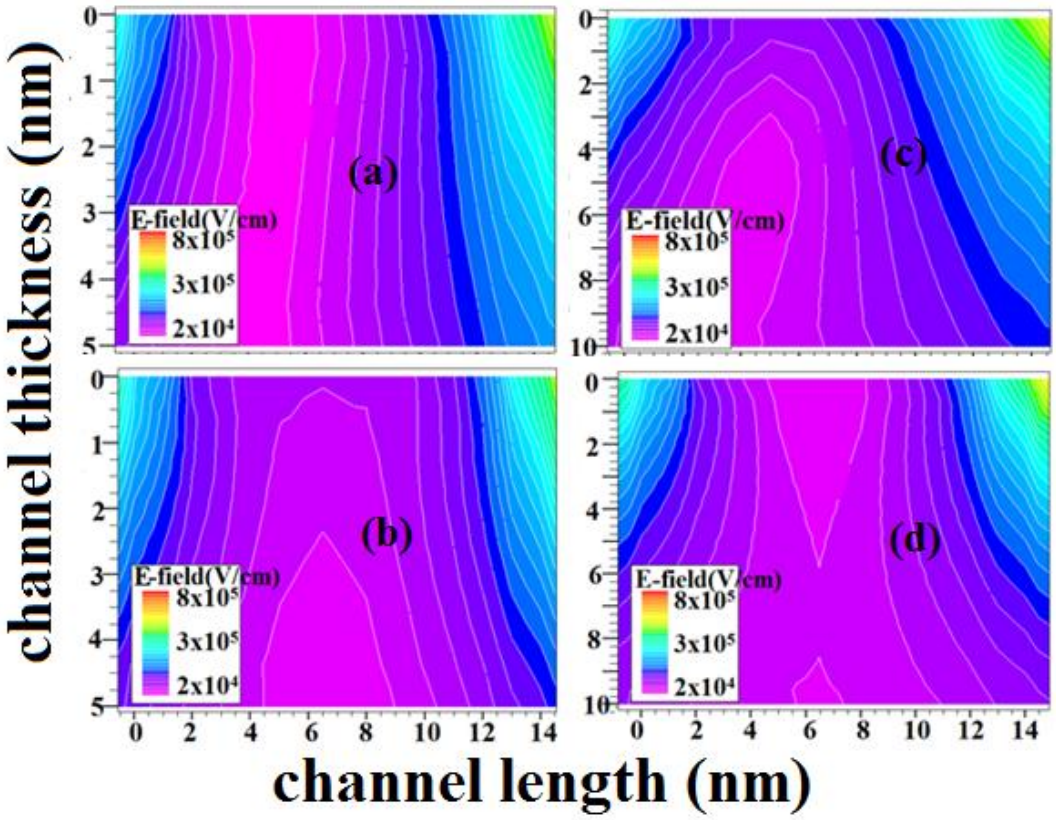


Fig. 3.22:2-D effective electric field profile in the channel under the gate for device (a) t_{ch}=5nm and T=300K (b) t_{ch}=5nm and T=150K (c) t_{ch}=10nm and T=300K (d) t_{ch}=10nm and T=150K of InAs quantum well n-MOSFET at V_{DS} = 0.4V and V_{GT}= 0.4V for L_{ch}=14nm.The left and right sides indicate source and drain ends, respectively.

Due to greater effect of electric field at higher temperature and thickened device, carriers gather sufficient energy to become free and thus concentration increases which ultimately increases

drain current. Also, as temperature and channel thickness decreases, threshold voltage increases which decreases the drain current. Thus, the ON-current improves by 27.54% and 86.98% in the wider channel device compared to the narrower one at T = 300 K and T = 150 K, respectively. Again, 5 nm channel thickness device shows lower values of OFF-current, evaluated at V_{GS} = 0 V and V_{DS} = 0.8 V, compared to the corresponding quantity for 10-nm thick channel device for the entire range of temperature as shown in Fig 3.20. I_{OFF} for the 5 nm thick device at 150 K comes out to be 6.3 times less as compared to corresponding I_{OFF} at T = 300 K. Also, as the 5 nm InAs channel device displays very low value of OFF-current at 300 K, highest ON–OFF current ratio is achieved under this condition as shown in Figure 3.23. The values of this ratio at T = 300 K and T = 150 K are 29.45 and 1.87, respectively for t_{ch} = 5 nm which decrease to 7.22 and 1.136, respectively at T = 300 K and T = 150 K for t_{ch} = 10 nm.

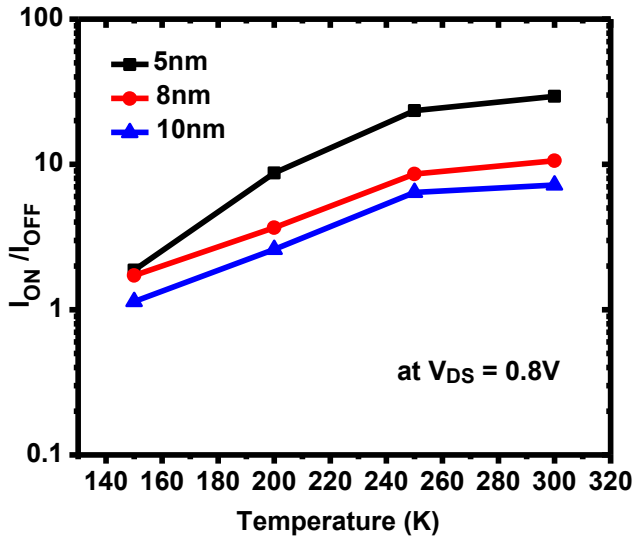


Fig. 3.23 : Plot of I_{ON}/I_{OFF} with temperature for different values of t_{ch} viz. 5 nm ,8 nm and 10 nm of InAs quantum well n-MOSFET for V_{DS}=0.8 V and L_{ch} = 14 nm.

As intrinsic delay decreases with increasing temperature and thickness, minimum value of this delay is observed in 10-nm-thick device at 300 K as shown in Fig. 3.24.These parameters

are7.62 ps and 513.45 ps respectively at T = 300 K and T = 150 K for t_{ch} = 10 nm and the values increase to 9.71 ps and 960.05 ps at T = 300 K and T = 150 K, respectively for t_{ch} = 5 nm.

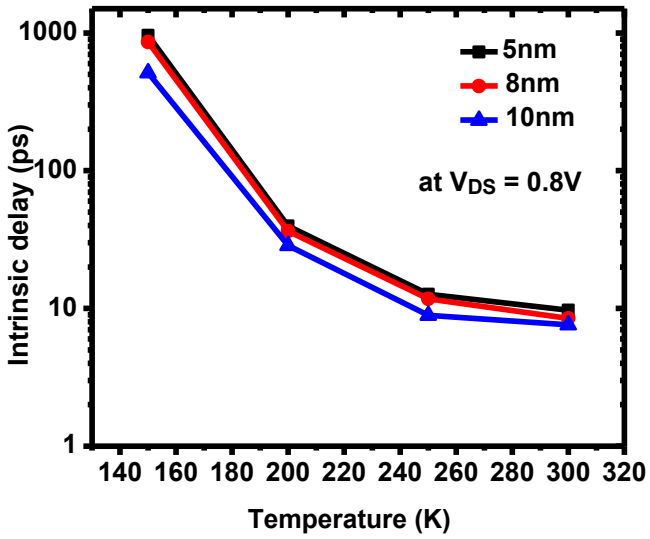


Fig.3.24: Plot of Intrinsic Delay with temperature for different values of t_{ch} viz. 5 nm ,8 nm and 10 nm of InAs quantum well n-MOSFET for V_{DS}=0.8 V and L_{ch} = 14 nm.

3.4.3.2 Impact of channel thickness and temperature on analog performance of InAs quantum well n-MOSFET at V_{DS} =0.4 V

For the same devices described in Section 3.4.3.1, the change of drain current (I_D) with V_{GT} in both linear and log scale at T = 300 K is shown in Fig. 3.25. At a particular value of V_{GT}, the highest value of drain current is for the device with t_{ch} = 10 nm. This is due to increased number of inversion carriers in such device. The variation of transconductance, g_m with V_{GT} is shown at T = 300 K in Fig. 3.26 (a) and the dependency of the peak values of g_m with temperature is shown in Fig. 3.26(b).

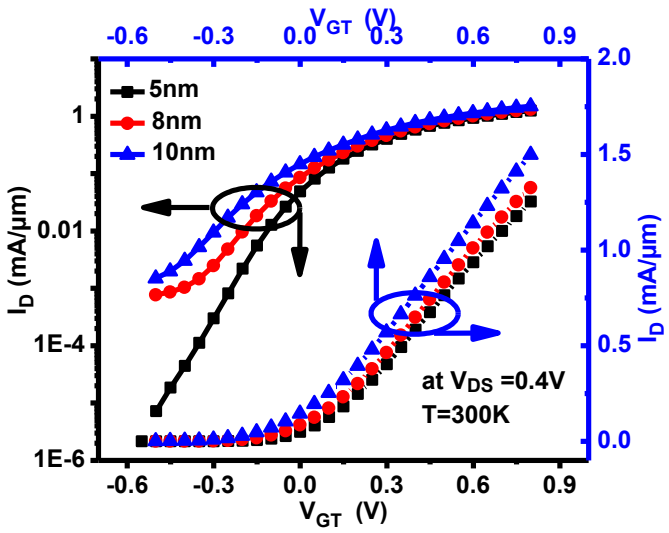


Fig. 3.25: Transfer characteristics at T=300K as a function of V_{GT} for different values of t_{ch} viz. 5 nm , 8 nm and 10 nm of InAs quantum well n-MOSFET for V_{DS}=0.4 V and L_{ch} = 14 nm.

The highest and lowest values of g_m are for the device with t_{ch} = 10 nm and 5 nm, respectively for all temperatures. This is because effective mobility of the carriers increases with temperature which ultimately improves transconductance of the device. Numerical analysis shows that at V_{GT} = 0.4 V and V_{DS}= 0.4 V the peak values of the effective electron mobility for 10 nm thick device at T = 300 K and T = 150 K are 8 $\times 10^3$ cm^2 V^{-1} $s^{-1}$and 5×10^3 cm^2 V^{-1} s^{-1}, respectively, while the corresponding values become 2.7 $\times 10^3$ cm^2-$V^{-1}s^{-1}$and 1.82×10^3 cm^2 $V^{-1}s^{-1}$ for 5 nm thick device at T = 300 K and T = 150 K, respectively. Thus, peak g_m increases by 6.75% and 27.75% for T = 300 K and T = 150 K, respectively, for the device with t_{ch}= 10 nm, compared to the device with t_{ch} = 5 nm.

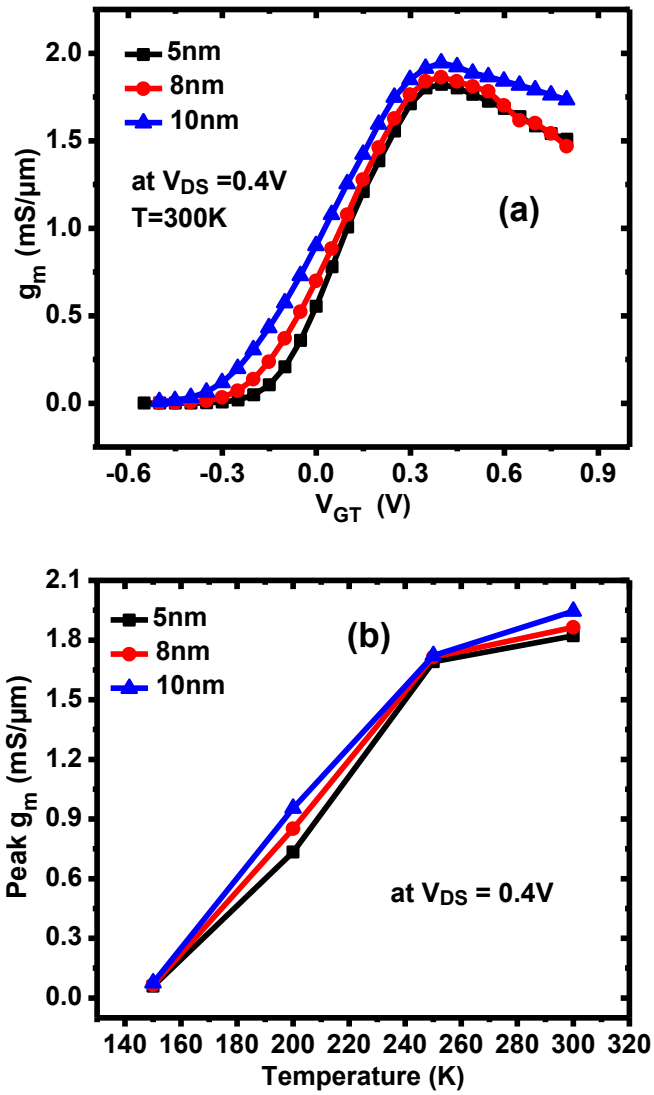


Fig. 3.26:Variation of (a) transconductance (g_m)with respect to V_{GT} at T=300K (b) Peak values of transconductance (g_m) with respect to temperature of InAs quantum well n-MOSFET at V_{DS} = 0.4V for L_{ch}=14nm.

The variation of output conductance g_d with V_{GT} with variation of channel thicknesses at T = 300 K is shown in Figure 3.27 (a) and the values of g_d for all the devices at V_{DS} = V_{GS} = 0.4 V for the entire range of temperature is shown in Fig. 3.27 (b). 10 nm thick device shows the higher value of g_d for the entire temperature range due to greater effect of vertical electric field. Numerical analysis shows that under identical bias condition (i.e. V_{GT} =0.4V and V_{DS}= 0.4V) , the peak values of vertical electric field along the channel length under the gate for the device with t_{ch}= 10

nm at T=300 K and T=150 K are 7.43×10^5 V/cm and 4.3×10^5 V/cm, respectively, while the corresponding values reduces to 3.3×10^5V/cm and 2.5×10^5 V/cm for the device with t_{ch}= 5 nm at T=300 K and T=150 K, respectively. Lesser effect of vertical field causes decrement of DIBL and hence less short channel effects in 5-nm-thick device as given in Fig. 3.27. Moreover, output current and thus output conductance increases with temperature. Thus, the value of g_d improves as the channel thickness and temperature reduces.

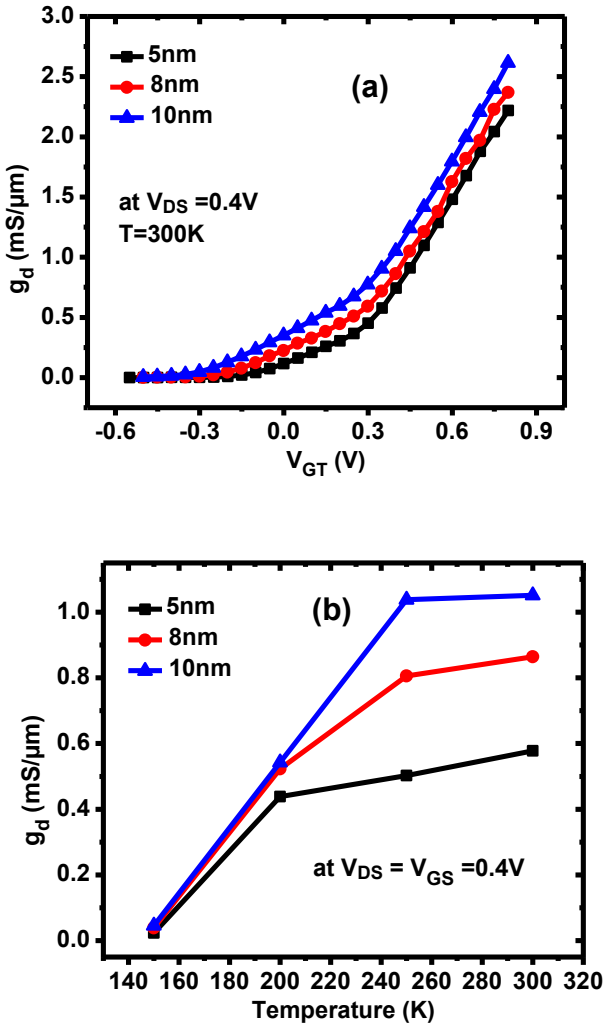


Fig. 3.27: Variation of (a) output conductance (g_d)with respect to V_{GT} at T=300K (b) output conductance (g_d)with respect to temperature of InAs quantum well n-MOSFET at V_{DS} = 0.4V for L_{ch}=14nm.

At $V_{DS} = V_{GS} = 0.4$ V, g_d for the device with t_{ch}= 5 nm reduces by 45.08% and by 49.20% at T = 300 K and T = 150 K, respectively, as compared to that with t_{ch}= 10 nm.

Fig. 3.28 (a) shows the variation of transconductance generation factor or transconductance efficiency (g_m/I_D) with respect to V_{GT} for three different channel thicknesses at 300 K

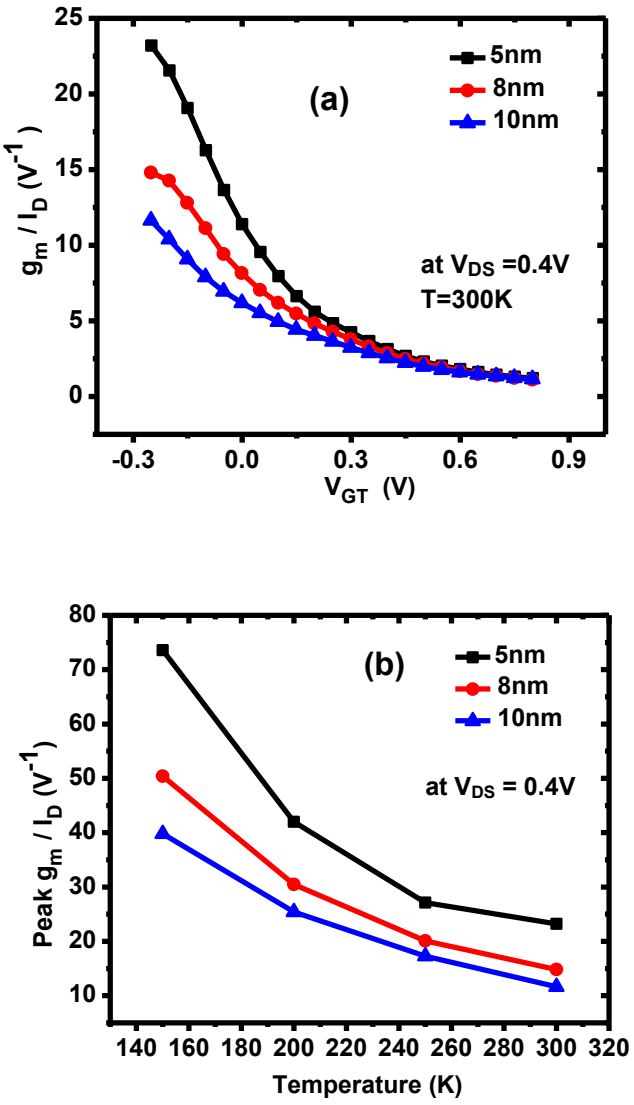


Fig. 3.28:Variation of (a) transconductance generation factor (g_m/I_D)with respect to V_{GT} at T=300K b Peak values of transconductance generation factor with respect to temperature of InAs quantum well n-MOSFET at V_{DS} = 0.4V for L_{ch}=14nm.

and its dependency on temperature is shown in Fig. 3.28(b).5 nm thickened device displays improvement of this factor in the subthreshold region of operation for all temperatures due to

considerable reduction in drain current in such a region. So, this factor improves by 99% and 84.92% for 5 nm thick device at T = 300 K and T = 150 K, respectively, as compared to that with 10 nm thick one.

The intrinsic voltage gain of these devices with different channel thicknesses at T = 300 K and the peak values at different temperatures are shown in Figure 3.29 (a) and (b), respectively.

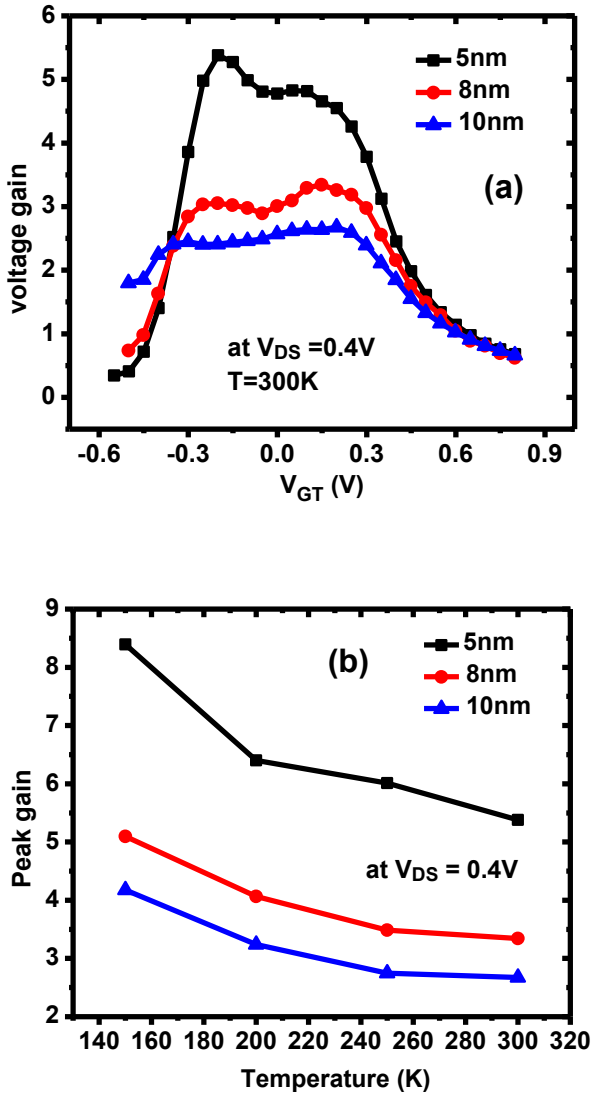


Fig. 3.29:Variation of (a) intrinsic gain with respect to V_{GT} at T=300K (b) Peak values of intrinsic gain with respect to temperature of InAs quantum well n-MOSFET at V_{DS} = 0.4V for L_{ch}=14nm.

Despite partial compensation of g_m, as g_d decreases significantly, 5 nm thickened device shows considerable improvement of this factor at all temperatures as compared to the other devices. Thus, peak gain of 5 nm thickened device improves by almost 100% at both T = 300 K and T = 150 K as compared to 10 nm thickened device.

3.4.4 Impact of angle of grooving on analog performance of InGaSb quantum well p-MOSFET

The change of drain current with respect to V_{GT} both in linear and log scale for different values of θ are shown in Fig. 3.30.It is very evident from the characteristics that the current decreases as the grooving angle decreases. This decrement is due to lesser effect of electric field and thus less lowering of source potential barrier in the narrower angled device. From the study, it is found that as θ increases from 40^0 to 90^0, the distance between the source and drain terminals (L_{SD}) decreases from 183 nm to 14 nm. For this longer source drain distance, the effect of electric field on the channel is lower in the device with $\theta = 40^0$ compared to the one with $\theta = 90^0$.

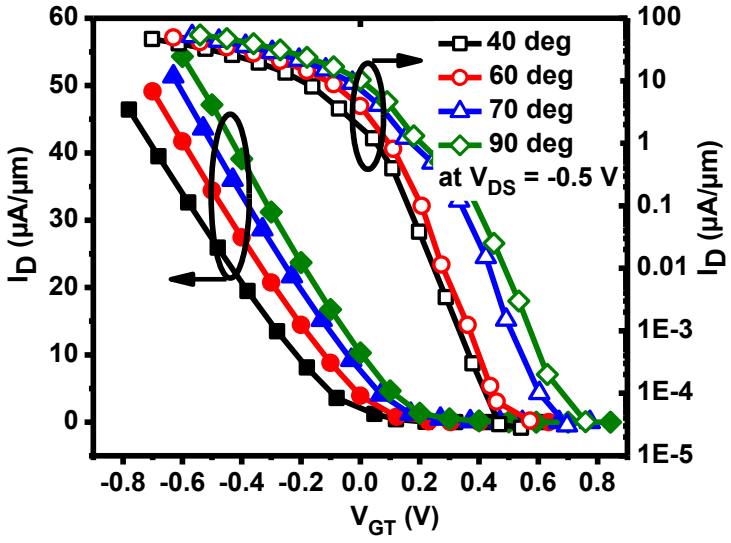


Fig. 3.30: Simulated transfer characteristics with respect toV_{GT} for InGaSb quantum well p-MOSFET with L_{ch} = 14 nm and t_{ch} = 5 nm and θ varying from 40^0 to 90^0 at V_{DS} =- 0.5 V.

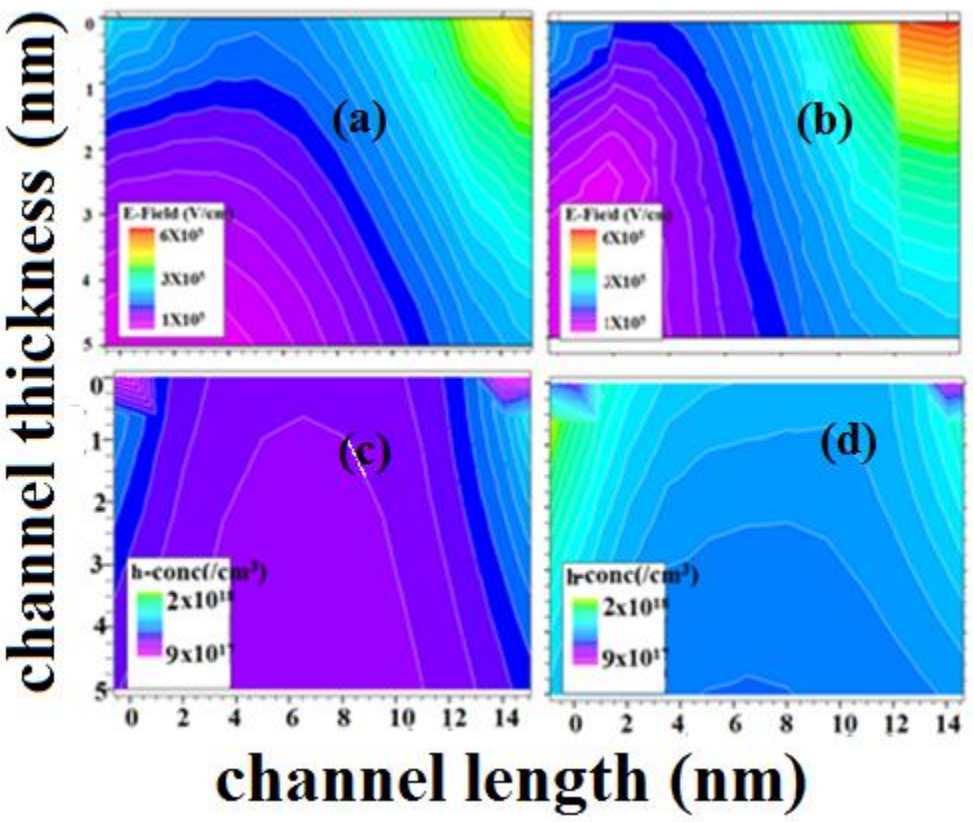


Fig. 3.31:2-D electric field distribution for (a)θ= 40^0 (b)θ= $90^0$and 2-D carrier distribution for (c)θ= 40^0 and (d) θ= 90^0 for InGaSb quantum well p-MOSFET with L_{ch} = 14 nm and t_{ch} = 5 nm at $V_{DS} = V_{GT}$ =- 0.5 V.

Fig. 3.31(a)-(b) show that the peak value of electric field across the drain end gate edge is 4.78 $\times 10^5$ V/cm for the device with θ = 40^0 which increases to 5.65 $\times 10^5$ V/cm for the device with θ = 90^0 at $V_{DS} = V_{GT}$ =-0.5 V.

This weaker effect of electric field on the smaller angled device leads to lesser reduction of potential barrier across the source and hence lesser injection of carriers into the channel. From Fig. 3.31(c)-(d),it is found that the peak carrier concentration across the drain end gate edge is 1.32×10^{18}/cm^3 for the device with θ = 40^0 which increases to 1.61×10^{18}/cm^3 for the device with θ = 90^0 at $V_{DS} = V_{GT}$=-0.5 V. Thus, the drain current at $V_{DS} = V_{GT}$=-0.5 V in lesser angled device is 1.5 times less compared to the larger angled one. Fig. 3.32 shows the variation of transconductance (g_m) with respect to V_{GT} for different grooving angle. It is evident that g_m attains

its minimum value for the device θ = 40^0. Such a variation is commensurate with the results obtained using the relation $g_m = 2I_D/V_{GT}$. The value of g_m at $V_{DS} = V_{GT} = -0.5$ V for the device with θ = 40^0 is 1.2 times less compared to the device with θ = 90^0.

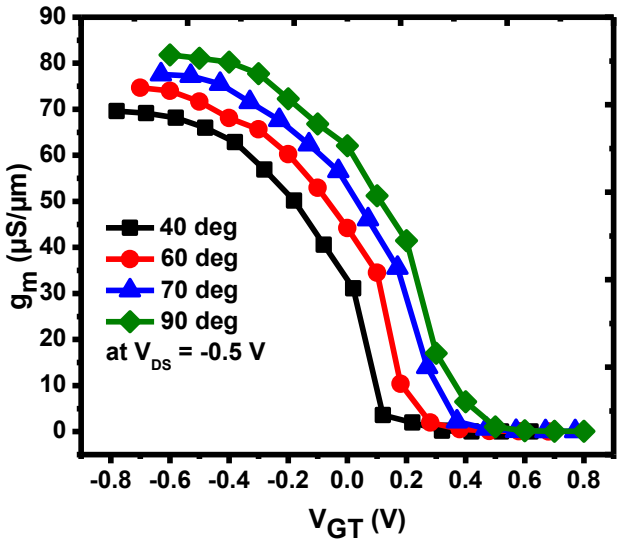


Fig. 3.32 Variation of transconductance (g_m) with respect to V_{GT} at T=300K of InGaSb quantum well p-MOSFET at V_{DS} = -0.5V for L_{ch}=14nm.

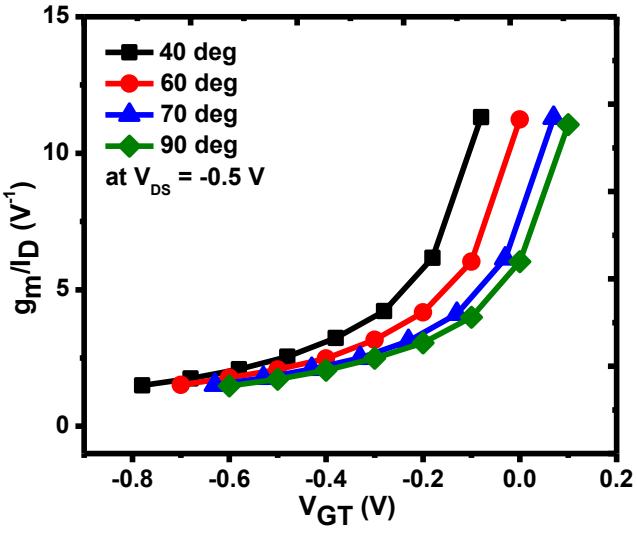


Fig. 3.33:Variation of transconductance generation factor (g_m /I_D) with respect to V_{GT} at T=300K of InGaSb quantum well p-MOSFET at V_{DS} = -0.5V for L_{ch}=14nm.

Fig. 3.33 shows the variation of transconductance efficiency factor (g_m/I_D) with respect to V_{GT}. The improvement of this efficiency factor in the subthreshold region of PMOS with $\theta = 40^0$ is due to significant reduction of current in such region. Thus, the peak value of this factor increases by 0.35% for the smaller angled device compared to the larger one.

Fig. 3.34 shows the variation of output conductance (g_d) with respect to V_{GT}. Due to larger source/drain distance in smaller angle device, the effect of electric field is less in such a device. This phenomenon leads to lesser amount of DIBL and thus lesser short channel effects in such a device. Thus, g_d decreases by 1.57 times in the smaller angled device compared to the larger one at $V_{DS}=V_{GT}=-0.5V$.

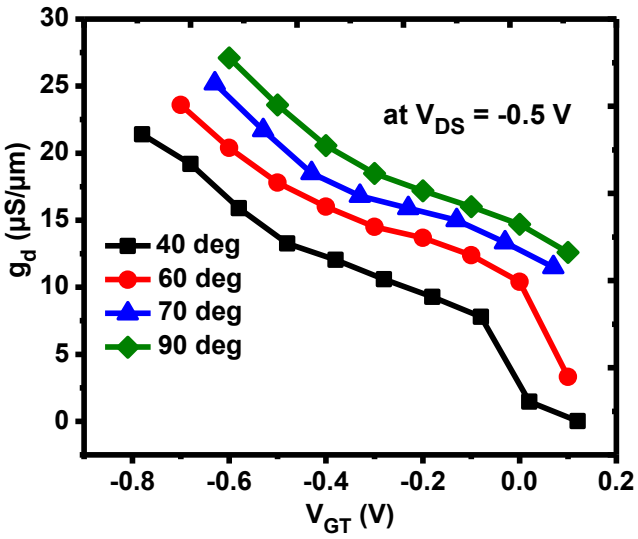


Fig. 3.34:Variation of output conductance (g_d) with respect to V_{GT} at T=300K of InGaSb quantum well p-MOSFET at V_{DS} = -0.5V for L_{ch}=14nm.

The variation of voltage gain with respect to V_{GT} is shown in Fig.3.35. It can be easily noticed that voltage gain attains considerable improvement in the device with $\theta = 40^0$ compared to the one with $\theta = 90^0$ due to significant reduction of g_d despite partial compensation in g_m. So, the peak gain improves by 1.28 times in the smaller angled device relative to the larger angled one.

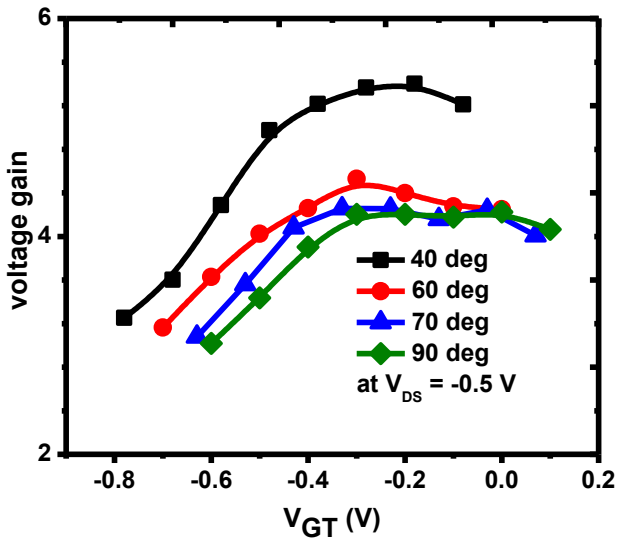


Fig. 3.35 :Variation of voltage gain with respect to V_{GT} at T=300K of InGaSb quantum well p-MOSFET at V_{DS} = -0.5V for L_{ch}=14nm.

3.5 Comparative analysis of the proposed structure with other reported structures

In Table VI, the author has made a comparative analysis of the proposed structures with other reported structures in terms of OFF current, ON-current, subthreshold slope, peak value of g_m , f_T and $f_{max.}$ From the table, it is quiet evident that the InAsOI structure with channel length of 30 nm and channel thickness of 5 nm shows considerable improvement in OFF-current with a comparable ON-current and a small compromise on the peak value of transconductance compared to other reported III-V n-MOS structures. Though SOI structure shows best result in terms of OFF-current, the ON-current and hence transconductance is greatly reduced in such structure. Moreover, the proposed device also shows remarkable results in terms of RF parameters like f_T and f_{max}, making the device suitable for RF application. Also, the proposed InAs based quantum well structure shows improvement in OFF-current and peak value of transconductance, with a compromise in ON-curent and subthreshold slope compared to InGaAs based quantum well structure. Moreover, the proposed InGaSb based quantum well p-FET

though shows compromised value in terms of subthreshold slope and ON-current compared to reported InGaSb based quantum well p-MOS, the device shows considereable improvement in terms of OFF-current.

3.6 Summary

While comparing the proposed on-insulator structure with the proposed quantum well structure, it is found that subthreshold slope and the peak value of transconductance improves by 1.09 times and 3.4 times respectively, making the quantum well structure to be more effective in the various fields of applications.From the careful analysis of InAs based quantum well n-MOSFET in digital domain, at V_{DS}= 0.5V, the author has concluded to opt for 5-nm-thick device at 250 K which offers low OFF-current of 8.5 x 10^{-4} mA/μm and high ON–OFF current ratio of 331.30 and delay of 109.43 ps with a very small compromise in ON-current. However, at the same temperature and V_{DS}=0.8 V, the values of these parameters for the said device are 0.05 mA/μm, 23.48 and 12.675 ps, respectively. Moreover, for analog performance at V_{DS}=0.4V, the author choose to consider 5-nm-thick channel device at 150 K offering lowest value of output conductance of 0.02 mS/μm, the highest value of transconductance generation factor of 73.5 V^{-1} and the highest intrinsic voltage gain of 8.39 with little compromise in terms of transconductance. The work on the impact of angle of grooving on the device performance of p-MOSFET shows that the smaller angled device shows considerable improvement in all analog parameters except transconductance. The author thus chooses to opt for the device having the angle of grooving of 40^0 and channel thickness of 5 nm showing considerable value of peak transconductance of 69 μS/μm and peak voltage gain of 5.4 with the value of output conductance of 12 μS/μm at V_{GT} = V_{DS} =-0.5 V in making circuits that can work well in analog domain.

Table VI: Comparative analysis of the proposed structures with other structures in terms of OFF current, ON current, subthreshold slope, peak value of g_m, f_T and f_{max}

Type of device with specifications	Temp (K)	I_{OFF} (mA/μm)	I_{ON} (mA/μm)	Subthreshold slope (mV/dec)	Peak g_m (mS/μm)	f_T (GHz)	f_{max} (GHz)	Ref
Self-aligned InGaAs quantum well n-MOSFET L_{ch} = 40 nm, t_{ch} =9 nm V_{DS} = 0.5 V	300	0.1	1.1	125	0.8	-	-	[3.29]
Self-aligned InAsOI n-MOSFET L_{ch} = 75 nm, t_{ch} =15 nm V_{DS} = 0.5 V	300	0.002	1.3	310	-	27	23	[3.47]
InGaAs tri-gate n-MOSFET L_{ch} = 20 nm, V_{DS} = 0.5 V	300	0.4	1.5	-	2	275	400	[3.48]
Top gated InGaSb-OI p-FET L_{ch} = 100 nm, t_{ch} =7 nm V_{DS} = -0.5 V	300	0.04	0.9	130	0.036	-	-	[3.49]
SOI TFET L_{ch} = 30 nm, t_{ch} =20 nm V_{DS} = 0.4 V	200	2×10^{-13}	1×10^{-4}	-	0.012	-	-	[3.50]
	300	2×10^{-11}	0.008	-	0.02	-	-	
InGaSb quantum well p-FET L_{ch} = 40 nm, V_{DS} = -0.5 V	300	0.01	0.2	83	-	-	-	[3.51]
InAsOI n-MOSFET L_{ch} = 30 nm, t_{ch} =5 nm V_{DS} = 0.5 V (author's work)	**300**	**1.3×10^{-5}**	**0.5**	**190**	**0.6**	**604**	**703**	**[3.30]**
InAs quantum well n-MOSFET with raised source/drain architecture L_{ch} = 14 nm, t_{ch} =5 nm, θ = 40^0, V_{DS} = 0.5 V (author's work)	**200**	**3.82×10^{-4}**	**0.12**	**169**	**0.74**	**-**	**-**	**[3.31-3.32]**
	300	**0.0015**	**0.53**	**175**	**2.09**	**-**	**-**	
InGaSb quantum well p-MOSFET with raised source/drain architecture L_{ch} = 14 nm, t_{ch} =5 nm , θ = 40^0 V_{DS} = - 0.5 V (author's work)	**300**	**3.9×10^{-4}**	**0.025**	**192**	**0.064**	**-**	**-**	**[3.33]**

REFERENCES

[3.1] T.C Harman , H.L. Goering , and A.C Beer , " Electrical properties of n-type InAs," *Phys Rev*, vol. 104, no.6, pp1562–1564,1956. https://doi.org/10.1103/PhysRev.104.1562

[3.2] A.Lubow , S. Ismail-Beigi , and T.P Ma ,"Comparison of drive currents in metal-oxide-semiconductor field effect transistors made of Si, Ge, GaAs, InGaAs and InAs channels," *Applied Physics Letters* , vol. 96, no.12, pp.122105,2010. https://doi.org/10.1063/1.3367708

[3.3] K. Takei ,S. Chuang , H. Fang , R. Kapadia , C.H.Liu ,J. Nah , H.S Kim, E. Plis,S. Krishna , Y.L Chueh , and A. Javey , " Benchmarking the performance of ultrathin body InAs-on-insulator transistors as a function of body thickness," *Applied Physics Letters*, vol.99,no.10,pp.103507,2011. https://doi.org/10.1063/1.3636110.

[3.4] J. Nah , H. Fang ,C. Wang ,K. Takei ,M.H. Lee ,E. Plis , S. Krishna , and A. Javey , " III–V complementary metal-oxide-semiconductor electronics on silicon substrates.," *Nano Letters* , vol. 12, no. 7, pp. 3592–3595,2012. https://doi.org/10.1021/nl301254z.

[3.5] K. Takei ,R. Kapadia ,H. Fang , E. Plis , S. Krishna , and A.Javey, "High quality interfaces of InAs-on-insulator field-effect transistors with ZrO_2 gate dielectrics," *Applied Physics Letters*, vol.102,no. 15,pp.153513, 2013. https://doi.org/10.1063/1.4802779

[3.6] M. Yokoyama , H. Yokoyama , M. Takenaka,and S. Takagi,"III–V single structure CMOS by using ultrathin body InAs/GaSb-OI channels on Si," *Proceedings of VLSI Tech*, p 978,2014. http://dx.doi.org/10.1109/VLSIT.2014.6894350.

[3.7] T. Dutta ,S. Kumar ,P. Rastogi,A. Agarwal ,and Y.S. Chauhan , " Impact of channel thickness variation on bandstructure and source-to drain tunneling in ultra-thin body III–V MOSFETs," *J Electron Devices Soc*, vol.4, no.2, pp.66–71,2016. https://doi.org/10.1109/JEDS.2016.2522981

[3.8] J.A. del Alamo, "Nanometer-scale electronics with III-V compound semiconductors," *Nature*, vol.479, no.17, pp.317-323, 2011. https://doi.org/10.1038/nature10677

[3.9] S. Lee, C.-Y. Huang, D. Cohen-Elias, J.M. Law, V. Chobpattanna, S. Kramer, B.J. Thibeault, W. Mitchell, S. Stemmer, A.C. Gossard, and M. J. W. Rodwell, "High performance raised source/drain InAs/$In_{0.53}Ga_{0.47}As$ channel metal-oxide semiconductor field-effect-transistors with reduced leakage using a vertical spacer," *Applied Physics Letters*,vol.103, no.23,pp.233503-1-4,2013. http://doi.org/10.1063/1.4838660.

[3.10] S. Lee, C.-Y. Huang, D.C. Elias, B.J. Thibeault, W. Mitchell, V. Chobpattana, S. Stemmer, A.C. Ossard, and M.J.W. Rodwell, "Highly scalable raised source/drain InAs quantum well MOSFETs exhibiting I_{ON} = 482μA/μm at I_{OFF}=100 nA/μm and V_{DD}=0.5 V," *IEEE Electron Device Lett*, vol.35, no.6,pp. 621-23, 2014. https://doi.org/ 10.1109/LED.2014.2317146.

[3.11] A. Nainani, Z. Yuan, T. Krishnamohan, B. R. Bennett, J. Brad Boos, M. Reason, M. G. Ancona, Y. Nishi, and K. C. Saraswat, "$In_xGa_{1-x}Sb$ channel p-metal-oxide-semiconductor field effect transistors: Effect of strain and heterostructure design," *Journal Of Applied Physics*, vol. 110, pp. 014503-1-9, 2011. http://dx.doi.org/10.1063/1.3600220.

[3.12] L. W. Guo, W. Lu, B. R. Bennett, J Brad Boos, and J. A. del Alamo, "Ultralow Resistance Ohmic Contacts for p-Channel InGaSb Field-Effect Transistors", *IEEE Electron Device Letters*, vol. 36, no. 6, pp.546-548,2015. http://dx.doi.org/10.1109/LED.2015.2421337

[3.13] Md. N. K. Alam, Md. S. Islam, Md. G. Kibria, and Md. R. Islam, "On the Ballistic Performance of InGaSb XOI FET: Impact of Channel Thickness and Interface States," *IEEE Transactions on Electron Devices*, vol. 62, no. 6, pp. 1855-1861, 2015. http://doi.org/10.1109/TED.2015.2420102.

[3.14] B. R. Bennett, M. G. Ancona, J. Brad Boos, and B. V. Shanabrook, "Mobility enhancement in strained p-InGaSb quantum wells", *Applied Physics Letters* ,vol. 91, pp.042104-1-3, 2007. https://doi.org/ 10.1063/1.2762279.

[3.15] M. Yokoyama, H. Yokoyama, M. Takenaka, and S. Takagi, " InGaSb-on-insulator p-channel metal-oxide-semiconductor field-effect transistors on Si fabricated by direct wafer bonding ," *Journal of Applied Physics*, vol. 125, 114501,2019. https://doi.org/10.1063/1.5049518.

[3.16] Y.P. Varshni ,"Temperature dependence of the energy gap in semiconductors.," *Physica*, vol. 34,pp.149–154,1967. https://doi.org/10.1016/0031-8914(67)90062-6.

[3.17] D.L. Rode , " Electron transport in InSb, InAs, and InP," *Phys Rev B*, vol.3, no.10, pp. 3287–3299,1971.https://doi.org/10.1103/PhysRevB.3.3287

[3.18] A.C. Ford ,J.C. Ho ,Y.L. Chueh, Y.C. Tseng ,Z. Fan ,J. Guo, J. Bokor, and A. Javey, "Diameter-Dependent Electron Mobility of InAs Nanowires," *Nano Lett*, vol.9,no. 1, pp. 360–365,2009. https://doi.org/10.1021/nl803154m.

[3.19] H.A. Nilsson , P. Caroff, C. Thelander, E. Lind , O. Karlstrom, and L.E. Wernersson ,"Temperature dependent properties of InSb and InAs nanowire field-effect transistors.," *Applied Physics Letters*, vol.96, no. 15,pp.153505. https://doi.org/10.1063/1.3402760.

[3.20] N. Gupta , Y. Song , G.W. Holloway, U. Sinha, C.M. Haapamaki, R.R. LaPierre, and J. Baugh, "Temperature-dependent electron mobility in InAs nanowires," *Nanotechnology*, vol. 24, no.22,pp. 225202,2013. http://doi.org/10.1088/0957-4484/24/22/225202.

[3.21] Yeo ,J. Dong Song ,and J. Lee , " Temperature-dependent energy band gap variation in self-organized InAs quantum dots," *Applied Physics Letters*, vol. 99, no.15,pp.151909,2011. http://doi.org/10.1063/1.3651492.

[3.22] A.Konar, J. Mathew ,K. Nayak, M. Bajaj, R.K. Pandey, S. Dhara, K.V.R.M .Murali,and M. Deshmukh , "Carrier transport in high mobility InAs nanowire junctionless transistors.," *Nano Lett*, vol.15,pp. 1684–1690, 2015. https://doi.org/10.1021/nl5043165

[3.23] E.M. Conwell, and M. O. Vossell, "High field transport in n-type GaAs," *Physical Review*, vol.166, no. 3, pp.797-821, 1968. https://doi.org/10.1103/PhysRev.166.797.

[3.24] R. A. Stradling, and R. A. Wood, "The temperature dependence of the band-edge effective masses of InSb, InAs and GaAs as deduced from magneto phonon magneto resistance measurements," *Journal of Physics C: Solid State Physics*,vol.3,no.5, pp.94-99,1970. https://doi.org/10.1088/0022-3719/3/5/005.

[3.25] R. Quay, C. Moglestue, V. Palankovski, and S. Selberherr, “A temperature dependent model for the saturation velocity in semiconductor materials,” *Materials Science in Semiconductor Processing*, vol.3, pp.149-155, 2000. https://doi.org/10.1016/S1369-8001(00)00015-9.

[3.26] R. Kim, U. E. Avci and I. A. Young, "Computational Study of Temperature Effects on MOSFET Channel Material Benchmarking," *IEEE Electron Device Letters*, vol. 41, no. 9, 2020,pp.1332-1335. https://doi: 10.1109/LED.2020.3012187.

[3.27] T. A. Oproglidis, T. A. Karatsori, S. Barraud, G. Ghibaudo and C. A. Dimitriadis, "Effect of Temperature on the Performance of Triple-Gate Junctionless Transistors," in *IEEE Transactions on Electron Devices*, vol. 65, no. 8, pp. 3562-3566, 2018, https://doi: 10.1109/TED.2018.2839196.

[3.28] Md. N. K. Alam, M. S. Islam, Md. G. Kibria, and Md. R. Islam, “On the Ballistic Performance of InGaSb XOI FET: Impact of Channel Thickness and Interface States,” *IEEE Transactions on Electron Devices*, vol. 62, no. 6, pp.1855-1861, 2015. https://doi.org/ 10.1109/TED.2015.2420102

[3.29] J. Lin, D. A. Antoniadis, and J. A. del Alamo, “Impact of Intrinsic Channel Scaling on InGaAs Quantum-Well MOSFETs,” *IEEE Transactions on Electron Devices*, vol. 62, no.11, pp.1-7,2017. https://doi.org/10.1109/TED.2017.2444835.

[3.30] S. Dasgupta, C. Mondal, and A. Biswas, “Impact of channel thickness of nanoscale InAs on insulator MOSFETs for analog/RF circuit applications,” *Proc. ICIECE*, Hyderabad, India, pp.383–387, 2015.ISBN:973-93-85100-41-3.

[3.31] S. Dasgupta, C. Mondal, and A. Biswas A , “Effect of temperature on digital performance of InAs quantum well nMOSFETs,” in *Proceedings of 6th international*

***conference on microelectronics, circuits and systems (MICRO),* pp 72–77, 2019. ISBN : 81-85824-46-4**

[3.32] S. Dasgupta, C. Mondal, and A. Biswas, "Effect of temperature and channel thickness on digital and analog performance of InAs Quantum Well n-MOSFETs," *Microsystem Technologies*, pp.1-7, October, 2019. https://doi.org/10.1007/s00542-019-04657-z

[3.33] S. Dasgupta, C. Mondal, and A. Biswas, "Effect of Grooving angle on the Analog Performance of InGaSb p-MOSFET," CODEC 2023, accepted.

[3.34] S. Tewari, A. Biswas, and A. Mallik, " Impact of a Spacer Layer on the Analog Performance of Asymmetric InP/InGaAs nMOSFETs," *IEEE Trans. Electron Devices*, vol.63, no.6, pp.2313-2320,2016. https://doi.org/10.1109/TED.2016.2548518.

[3.35] *ATLAS users' manual: device simulation software*' (Silvaco Int., Santa Clara,CA, USA, 2014), available at http://www.silvaco.com

[3.36] M. Sotoodeh, A.H. Khalid, and A.A. Rezazadeh, "Empirical low-field mobility model for III–V compounds applicable in device simulation codes,"*J. Appl. Phys.*, vol. 87,no.6, pp.2890-2900, 2000. https://doi.org/10.1063/1.372274.

[3.37] T. P. McLban, and E. G. S. Paigb, "A Theory Of The effects of carrier-carrier scattering on mobility in semiconductors," *J. Phys. Chm. Solids*,vol. 16, pp.220-236,1960. https://doi.org/10.1016/0022-3697(60)90152-9

[3.38] B. V. Olson, E. A. Kadlec, J. K. Kim, J. F. Klem, S. D. Hawkins, and E. A. Shaner, "Intensity- and Temperature-Dependent Carrier Recombination in InAs/InAs1−xSbx Type-II Superlattices," Physical Review Applied, vol. 3, 044010-1-12 ,2015. https://doi.org/10.1103/PhysRevApplied.3.044010

[3.39] J. Piprek, Semiconductor Optoelectronic Devices: Introduction to Physics and Simulation, 1st edition, Academic Press Inc, 2003, Pages 49-82. https://doi.org/10.1016/B978-0-08-046978-2.50028-4.

[3.40] A.R. J. Marshall, C. H. Tan, M. J. Steer and J. P. R. David, "Electron dominated impact ionization and avalanche gain characteristics in InAs Photodiodes," Applied Physics Lett, vol. 93, pp.111107-1- 111107-3,2008. https://doi.org/10.1063/1.2980451

[3.41] E. Jamil, "Analytical modeling and characterization for avalanche photodiodes," Doctor of Philosophy, Engineering, Optical Science Engineering, The University of New Mexico, Albuquerque, New Mexico, July, 2017.

[3.42] G. A. M. Hurkx, D. B. M. Klaassen, and M. P. G. Knuvers, "A new recombination model for device simulation including tunneling," IEEE Trans. Electron Dev., vol. 39 ,no.2, pp.331-338,1992. https://doi.org/10.1109/16.121690.

[3.43] G. A. M. Hurkx, C. D. Graaff, W. J. Kloosterman, and M. P. G. Knuvers , "A new analytical diode model including tunneling and avalanche breakdown," IEEE Trans. Electron Devices,vol.39,no.9,pp. 2090–2098,1992. https://doi.org/ 10.1109/16.155882.

[3.44] I. Yeo, J. D. Song, and J. Lee, "Temperature-dependent energy band gap variation in self-organized InAs quantum dots," Applied Physics Letters, vol. 99, 151909-1-3,2011. https://doi.org/10.1063/1.3651492.

[3.45] M. Oszwaldowski, and M. Zimpel, "Temperature dependence of intrinsic carrier concentration and density of states effective mass of heavy holes in InSb," *J. Phys. Chem. Solids*, vol. 49, no.10, pp. 1179-85,1988. https://doi.org/10.1016/0022-3697(88)90173-4.

[3.46] J-X. Shen, D. Steiauf,A. McAllister, G. Shi, E. Kioupakis, A. Janotti, and C. G. Van de Walle, "Impact of phonons and spin-orbit coupling on Auger recombination in InAs," Phys. Rev. B, vol.100, 155202,2019. https://doi.org/10.1103/PhysRevB.100.155202.

[3.47] C. Wang, J-C Chien, H. Fang, K. Takei, J. Nah, E. Plis, S. Krishna, A. M. Niknejad, and A. Javey, "Self-Aligned, Extremely High Frequency III-V Metal-Oxide-Semiconductor Field-Effect Transistors on Rigid and Flexible Substrates," Nano Letters, vol. 12, no.8, pp.4140-4145,2012. https://doi.org/10.1021/nl301699k

[3.48] C.B. Zota, F. Lindelöw, L.-E. Wernersson and E. Lind, "High-frequency InGaAs tri-gate MOSFETs with f_{max} of 400 GHz," *Electronics Letters*, vol. 52, no. 22, pp. 1869–1871, 2016. https://doi.org/10.1049/el.2016.3108

[3.49] K. Takei, M. Madsen, H. Fang, R. Kapadia, S. Chuang, H. S. Kim, C-H Liu, E. Plis, J. Nah, S. Krishna, Y-L Chueh, J. Guo, and A. Javey, "Nanoscale InGaSb Heterostructure Membranes on Si Substrates for High Hole Mobility Transistors," *Nano Lett*., vol.12, pp.2060−2066,2012. https://doi.org/dx.doi.org/10.1021/nl300228b

[3.50] S. Chander, S. K. Sinha , S. Kumar ,P. K. Singh, K. Baral , K. Singh, S. Jit, "Temperature analysis of Ge/Si heterojunction SOI-Tunnel FET," *Superlattices and Microstructures*,vol.110, pp. 162-170,2017. http://dx.doi.org/10.1016/j.spmi.2017.08.048

[3.51] M.G. Ancona , B.R. Bennett, and J.B. Boos, "Scaling projections for Sb-based p-channel FETs", Solid-State Electronics, vol. 54, pp.1349–1358,2010. https://doi.org/10.1016/j.sse.2010.06.022

CHAPTER - 4

Impact of Grooving Angle and Channel Thickness on Analog Performance and Linearity Analysis of 14 nm InAs Quantum Well N-MOSFET

In this chapter, the author has investigated the effect of change of grooving angle and channel thickness on the analog and linearity performance of InAs based quantum well n-MOSFET. For the analysis of the linearity performance, the author has extracted the distortion parameters from the device characteristics using Integral Function Method (IFM) technique.

4.1 Introduction

As discussed in the previous chapter, InAs is emerging as the new channel material replacing conventional Silicon mainly because of its high electron mobility and low bandgap property. There has been extensive research on InAs-based MOS devices in the literature [4.1-4.8]. Also, as mentioned earlier, that of the several architectures that are used to combat with the problem of leakage current in InAs based devices, the author has studied the raised source/drain structure where a vertical spacer is used to control the off-current. Experimental reports [4.9-4.10] show that in such structure, the effect of the drain field on the channel decreases greatly which reduces the OFF-state leakage significantly at high drain bias without considerably affecting the ON-current. The angle of grooving (Θ) also plays an important role in the performance of the device as it controls the electric field of the channel.

Nowadays, study of non-linearity is becoming a growing trend in the semiconductor industry. This analysis plays an important role in RF systems to find out whether harmonic distortions are minimal at the output or not. This analysis of harmonic distortion is of immense importance for

analog and mixed integrated circuits. Harmonic distortion is characterised by figures of merit like k^{th}-order harmonic distortion (HD_k, where k is a positive non-zero number) and total harmonic distortion (THD). Of these, the second and third-order distortions are important [4.11-4.17]. R.Salazar *et. al.* in 2008 calculated these above said traditional figures of harmonic distortions of a set n-MOSFETS of different channel lengths using Full Successive Integral Method, keeping DC voltage fixed and varying the amplitude of the input signal.[4.12] R.T. Doria and his group in 2010 studied these harmonic distortion parameters on unstrained and biaxially strained fin-shaped field-effect transistors with different channel lengths L and fin widths.[4.16]. Paul G. A. Jespers and B. Murmman in 2015 derived analytic expressions that linked MOSFETs distortions with the transistor's transconductance generation factor. [4.13] In 2020, C. A. B. de Carvalho *et. al.* studied the harmonic distortions of vertically stacked SOI nanowire with different fin widths and channel lengths. They concluded that the second-order harmonic distortion mainly dominates the harmonic distortion and it is about 30 dB larger than third order harmonic distortion.[4.17] Of the several techniques used for the extraction of distortion parameters, integral function method (IFM) stands out as it is a combination of simplicity, efficiency and accuracy and also permits the distortion extractions from DC measurements without the need of AC characterisation [4.18-4.20].

In this chapter, the author has first investigated the effect of variation of the grooving angle (Ɵ) from 20° to 90°on the analog and linearity performance of 14 nm InAs channel quantum well n-MOSFET having channel thickness of 5 nm and featuring a 2 nm $In_{0.53}Ga_{0.47}As$ layer as the vertical spacer between the channel and N^+ S/D as shown in Fig.4.1 and also on a common-source amplifier circuit made with such a device.[4.21] Further, the author has extended the work to study the impact of varied channel thicknesses, viz. 3nm, 6 nm and 8nm on the analog

and harmonic distortion parameters of a device [4.22]. The author has used integral function method (IFM) for the distortion analysis part of both these works.

This chapter is organised as follows: In the section 4.2 the device structure is given. Overview of models and validation are presented in section 4.3. The results are presented in section 4.4. Section 4.5 has a comparative analysis of the proposed device with other reported devices. Finally, this chapter is summarized in section 4.6.

4.2 Device Description

The cross-sectional view of the InAs quantum well n-MOSFET considered in this chapter is given in Fig. 4.1. The fabrication steps and the dimensions of the device remain same as explained the section 3.2.2 of the previous chapter.

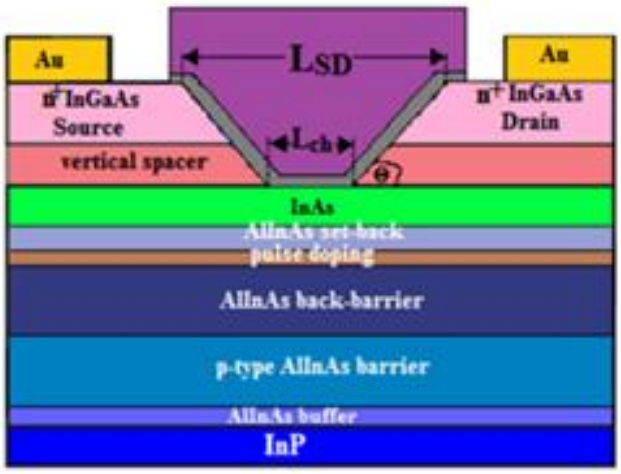


Fig 4.1: Cross-sectional view of InAs quantum well n-MOSFET having channel thickness 5 nm with L_{ch} as channel length L_{SD} as the spacing between source and drain and Θ as angle of grooving.

4.3 Simulation set-up, model calibration and validation

Models used for this work include the thickness dependent bandgap, effective mass, and non-parabolocity factor models, low and high electric field and concentration dependent mobility model, scattering model, tunneling and recombination models, carrier statistics and transport model. The physics and the parameter values of all these models are discussed in details in Chapter 2. With the incorporation of all these models, the author has first calibrated the device and the results of the calibration are then validated with the experimental results of [4.23], the details of which are given in Chapter 3.

4.4 Results and Discussions

4.4.1 Impact of grooving angle (θ) on device parameters for t_{ch} = 5 nm

The effect of varying grooving angle on the analog performance of InAs quantum well n-MOSFET with t_{ch} = 5 nm and L_{ch} =14 nm is investigated. The transfer characteristics, both in linear and log scales and the variations of transconductance (g_m), its derivative and the output conductance (g_d) with respect to gate overdrive voltage (V_{GT}), respectively for five different angles of grooving e.g., 20^0, 40^0, 60^0, 70^0 and 90^0 at V_{DS} = 0.5V are shown in Fig. 4.2[(a),(b) and (c)].

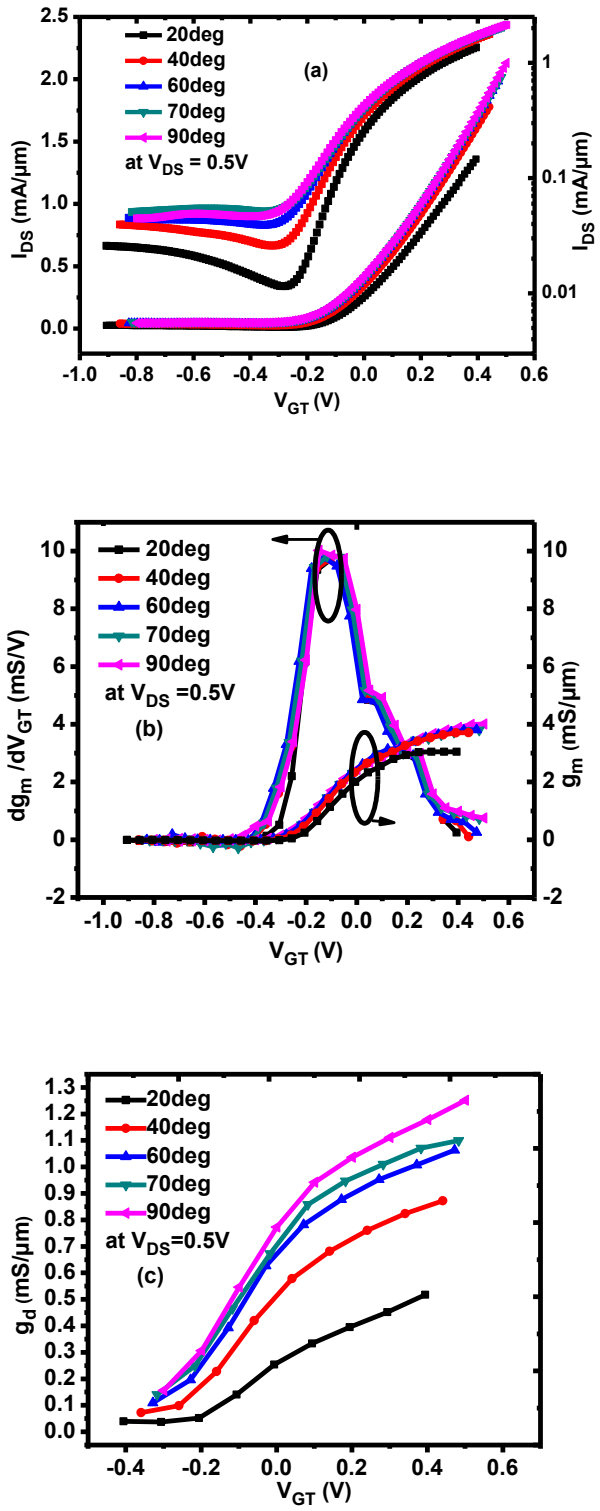


Fig. 4.2:(a)Transfer characteristics in both linear and log scale (b)variation of transconductance (g_m) and derivative of g_m (c) variation of output conductance (g_d) as a function of V_{GT} for different values of θ viz. 20^0, 40^0, 60^0, 70^0 and 90^0 of InAs quantum well n-MOSFET for V_{DS} = 0.5V and L_{ch}=14nm.

It is evident from Fig. 4.2(a) that the drain current of the devices increases with angle of grooving. This is due to increment of electron concentration with θ. The peak electron concentration at the semiconductor-oxide interface along the drain-side gate edge increases from 3.71×10^{18}/cm^{3}for 20^0 angled device to 4.8×10^{18}/cm^3 for 90^0 angled device at V_{DS}=0.5 V and V_{GT}=0.3 V. Fig. 4.3[(a) and (b)] shows the effective electric field profiles within the channel for the devices with θ = 90^0 and 20^0at the same bias condition, respectively.

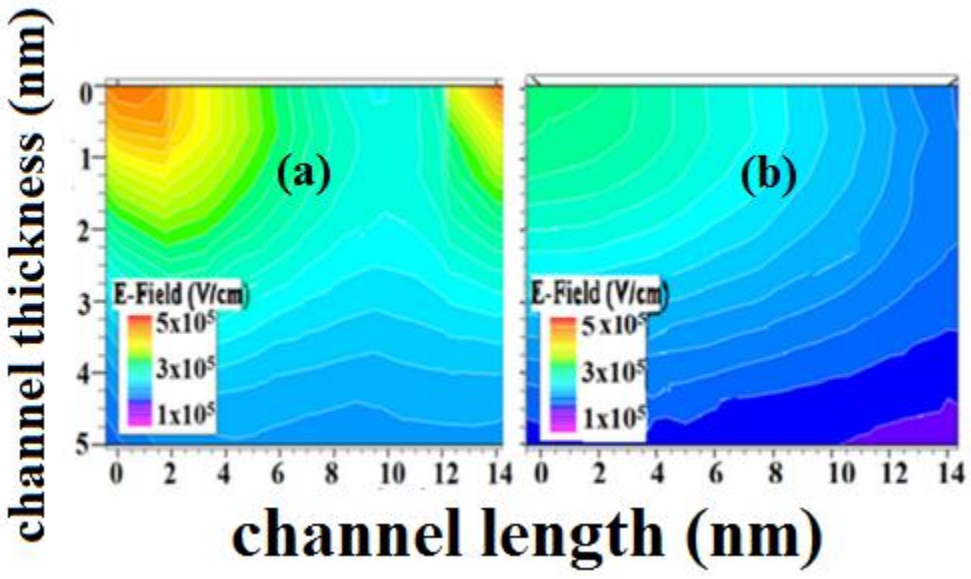


Fig.4.3: 2-D effective electric field profile in the channel under the gate length Lg with (a) θ = 90^0 (b) θ = 20^0 of InAs quantum well n-MOSFET at V_{DS} = 0.5V and V_{GT}= 0.3V for L_{ch}=14nm. The left and right sides indicate source and drain ends, respectively.

While the electric field is in the range $2.92\times10^5 - 1.51\times10^5$ V/cm for the device with θ=20^0, the corresponding range increases to 4.17×10^5-1.74×10^5 V/cm for the device with θ = 90^0. Due to greater effect of electric field in wider angled device, the source barrier lowering is more in such a device, leading to increase in concentration of carriers. Again, as transconductance shows better results with increasing effective mobility, g_m enhances with increasing angle of grooving

(as shown in Fig. 4.2(b)) as the peak effective electron mobility decreases from 425cm^2/V.s for θ = 90^0 to 380 cm^2/V.s for θ=20^0 for the same value of V_{DS} = 0.5Vand V_{GT}=0.3V and such a variation is commensurate with the results obtained using the relation $g_m = 2I_{DS}/V_{GT}$. Moreover, the distance between the source and the drain terminals (L_{SD}) shows dependency on θ i.e. L_{SD} for the device with θ = 20^0 is 406 nm which decreases to 14 nm for the device with θ = 90^0. This increased distance in smaller angled device results in a weaker effect of the drain field across the gate edges, the peak value of which changes from 3.23×10^{5}V/cm for a 90^0 angled device to 2.5×10^{5}V/cm for a 20^{0}angled device under the same bias condition as shown in Fig. 4.4 (a) and (b), respectively.

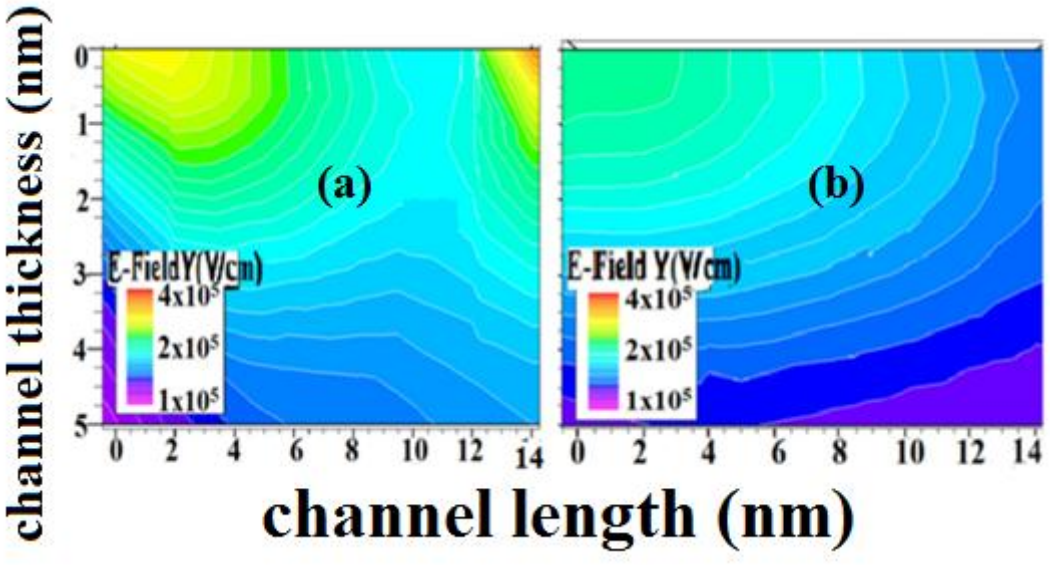


Fig. 4.4: 2-D vertical electric field distribution in the channel under the gate length L_g with (a) θ = 90^0 (b) θ = 20^0 of InAs quantum well n-MOSFET at V_{DS} = 0.5V and V_{GT} = 0.3V for L_{ch}=14nm. The left and right sides indicate source and drain ends, respectively.

This lesser effect of drain field on drain current in smaller angled device angled device leads to reduced amount of DIBL in such a device which ultimately leads to improvement in output

conductance (g_d) as shown in Fig. 4.2 (c). Thus, at $V_{DS} = V_{GS} = 0.5$ V, g_d in the device having $\theta=20^0$ improves by 67.81% compared to that with $\theta = 90^0$.

Fig. 4.5 shows the variation of transconductance efficiency (g_m/I_D) with respect to V_{GT}. The smaller angled device shows improvement of this factor in the subthreshold region of operation of the transistor due to the considerable reduction of drain current in that region,as shown in Fig. 4.2 (a). From Fig. 4.6 which compares the voltage gain (A_v) of different groove angled device with respect to V_{GT}, it can be concluded that the gain for the device with $\theta = 20^0$ shows the best results. In such a device, though there is partial compensation of g_m, there is significant reduction in g_d. Thus, the device with $\theta = 20^0$ shows improvement in the peak gain by 144% compared to the one $\theta = 90^0$.

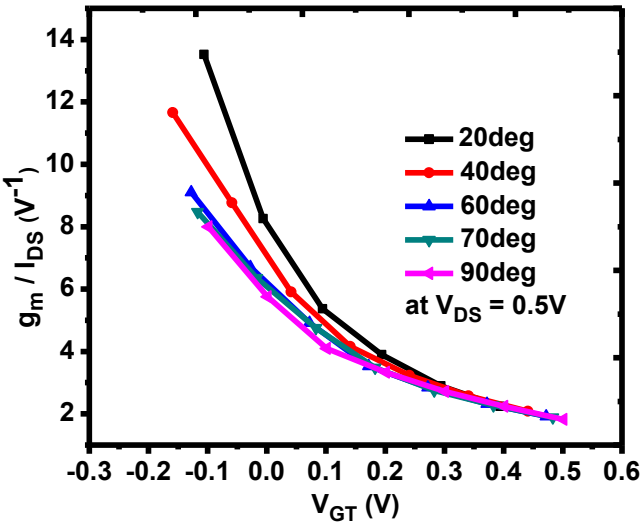


Fig.4.5: Variations of transconductance efficiency (g_m/I_d) with respect to V_{GT} at V_{DS}= 0.5V of InAs quantum well n-MOSFET with different θ viz. 20^0, 40^0, 60^0, 70^0 and 90^0 for L_{ch}=14nm.

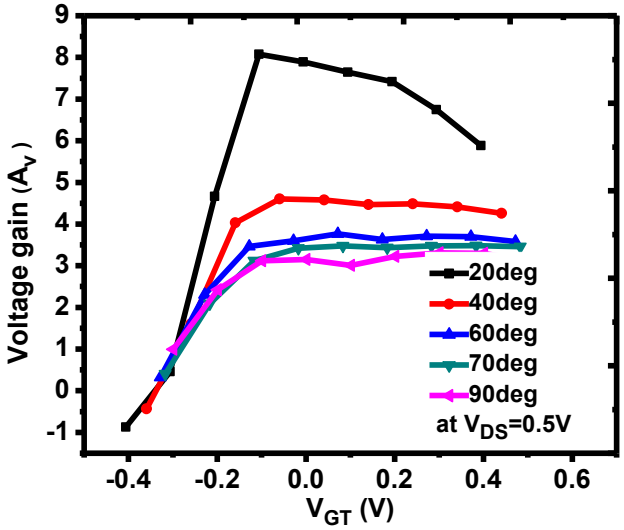


Fig.4.6: Variations of voltage gain (Av) with respect to V_{GT} at V_{DS}=0.5V of InAs quantum well n-MOSFET with different θ viz. 20^0, 40^0, 60^0, 70^0 and 90^0 for L_{ch}=14nm.

4.4.2 Harmonic Distortion analysis on a common source amplifier circuit

A common-source amplifier circuit is designed using InAs quantum-well n-MOSFET with a resistive load 1 MΩ at V_{DD}=650mV to analyze the nonlinearity of such amplifiers in terms of harmonic distortion. One 50 mV ac signal is used for the IFM analysis [4.15-4.16, 4.20] and it is superimposed on the applied dc bias V_{IN} to obtain figure of merits (FOMs) of harmonic distortion (HD) in dB. These HD parameters are studied from the voltage transfer characteristics of the circuit shown in Fig. 4.7 (a). The equations considered for the HD analysis are as follows [4.20]:

$$HD_2 = 0.5v_a \left(\frac{1}{2g_m}\right)\frac{dg_m}{dV_{GT}} \tag{4.1}$$

$$HD_3 = 0.25{v_a}^2 \left(\frac{1}{6g_m}\right) d^2\, g_m \tag{4.2}$$

$$THD = \sqrt{[(HD_2)^2 + (HD_3)^2]} \tag{4.3}$$

HD_2, HD_3, and THD denote 2nd order, 3rd order and total harmonic distortions, respectively.

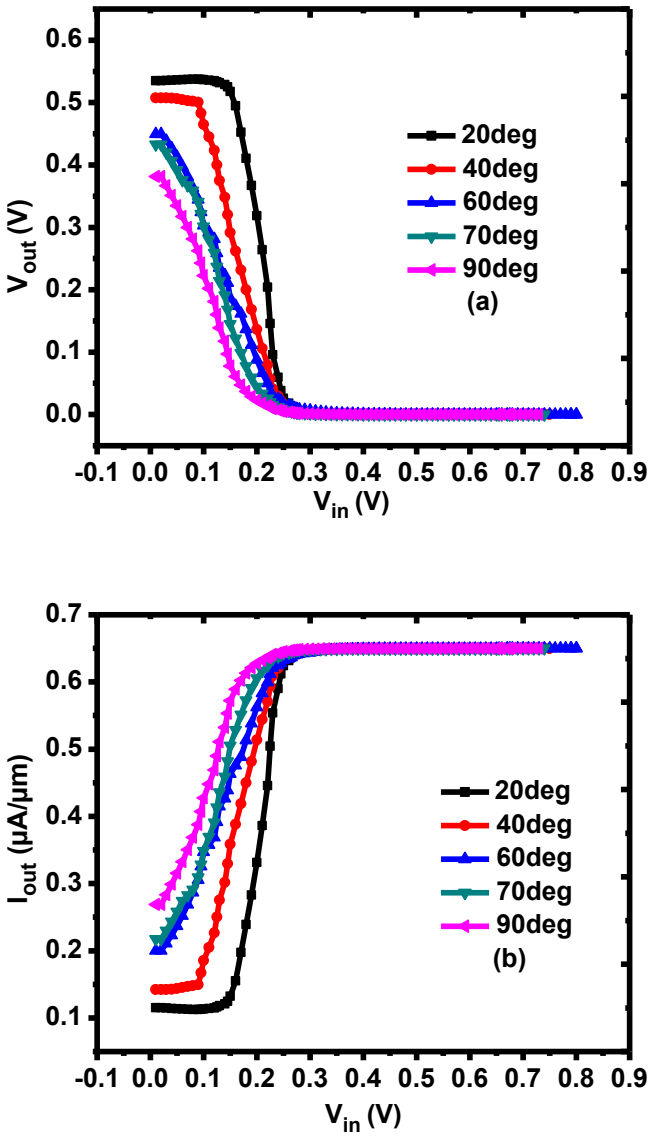


Fig. 4.7:(a)Voltage transfer characteristics (VTCs) and (b) transfer characteristics of common source amplifiers for R_L=1MΩ at V_{DD} = 650mV with varying groove angle of device viz.20^0, 40^0, 60^0, 70^0 and 90^0 and t_{ch} = 5 nm

The nature in which HD_2 varies with input voltage, as shown in Fig. 4.8, reveals that this factor has tendency to decrease in magnitude with increasing grooving angle. This trend can be explained as follows. Both g_m and its slope increase with θ (as in Fig. 4.2 (b)), but the rate of increase of g_m is higher as compared to its derivative with respect to V_{GT}. At V_{GT} = 0.3V and V_{DS} = 0.5V, g_m for 90° angled device increases by 20.66% compared to 20° one; however the

percentage increase of the slope of g_m for θ = 90° is only 4.11% compared to 20° one under the same bias condition. As HD_2 varies inversely and directly with g_m and its derivative, respectively, it shows better results for higher angled device compared to the lower angled one and thus linearity improves with increased θ. Moreover, from Table I, it can be concluded that the minimum value of HD_2 in the circuit having greater value of θ shifts to a lower V_{IN}. From the characteristics of the common source amplifier it can be concluded that for a higher θ, the output current (I_{OUT}) increases rapidly as V_{IN} increases [Fig. 4.7 (b)] for which the output voltage (V_{OUT}) decreases sharply [Fig. 4.7 (a)]. From the characteristics, it is clear that the point of maximum gain at the steepest slope of the VTC shifts towards lower V_{IN} for higher θ and thus the minimum value of HD_2 which corresponds to the point of maximum gain shifts towards the lower V_{IN} with increasing θ.

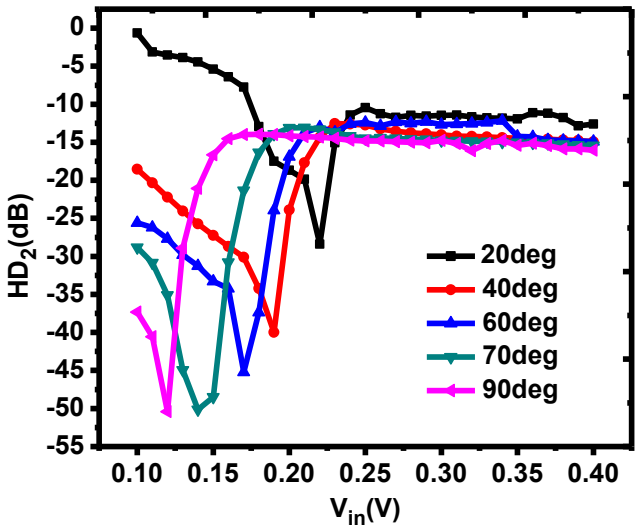


Fig.4.8: Variation of HD_2 with input voltage of a common source amplifier with R_L=1MΩ at V_{DD} = 650mV with varying groove angle of device e. g., 20^0, 40^0, 60^0, 70^0 and 90^0 and t_{ch} = 5 nm

Table I: Position of minima in HD_2 characteristics

Grooving angle (θ)	20^0	40^0	60^0	70^0	90^0
V_{in} (V)	0.22	0.19	0.17	0.14	0.12

Fig. 4.9 shows that HD_3 also improves with increased θ as this factor shows similar dependency on g_m as HD_2. Table II shows the positions of the minima in HD_3 characteristics, where the position of the first minimum refers to the point at which the current starts increasing while the second minimum corresponds to the onset of current saturation.

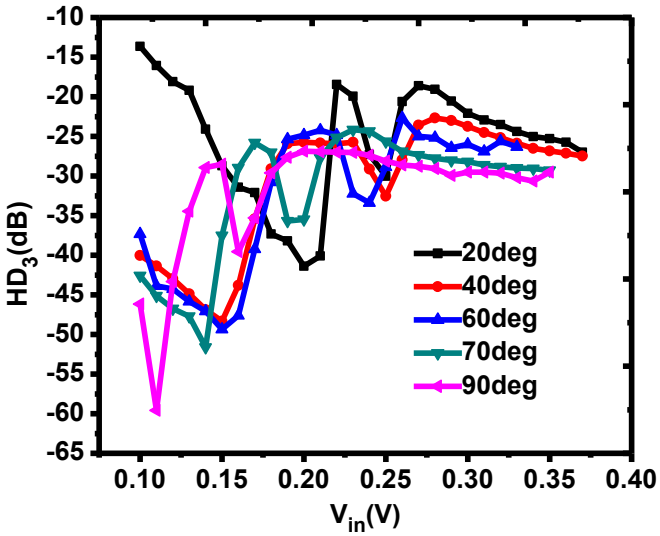


Fig.4.9: Variation of HD_3 with input voltage of common source amplifier with R_L=1MΩ at V_{DD} = 650mV for different groove angles of the device e. g., 20^0, 40^0, 60^0, 70^0 and 90^0 and t_{ch} = 5 nm

Table II: Position of minima in HD_3 characteristics

Grooving angle (θ)	V_{in} at 1st minimum(V)	V_{in} at 2nd minimum(V)
20^0	0.2	0.25
40^0	0.15	0.25
60^0	0.15	0.24
70^0	0.14	0.19
90^0	0.11	0.16

Fig.4.10 indicates that the overall Total Harmonic Distortion (THD) falls with increasing θ which improves the circuit linearity. The THD denotes distortions obtained from all harmonics and thus Fig. 4.10 indicates the summed distortions gathered from both HD_2 and HD_3.

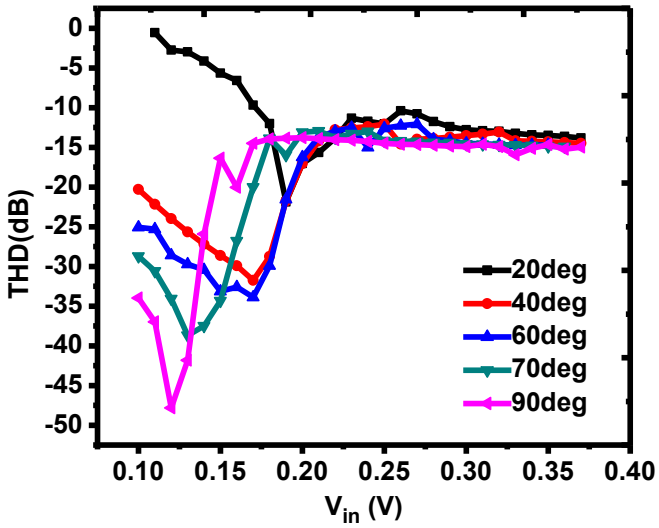


Fig.4.10:Variation of THD with input voltage of common source amplifier with R_L=1MΩ at V_{DD} = 650mV with varying θ viz.20^0, 40^0, 60^0, 70^0, 90^0 and t_{ch} = 5nm

Using the ac analysis, the change of peak gain, bandwidth and gain-bandwidth product with respect to θ are being analyzed. Fig. 4.11 shows that the peak gain decreases with increasing θ,

due to increment of g_d with increasing θ as shown in Fig. 4.2(c). Thus, the peak gain of the circuit having θ=20^0 improves by 64.2% with respect to the circuit having θ=90^0.

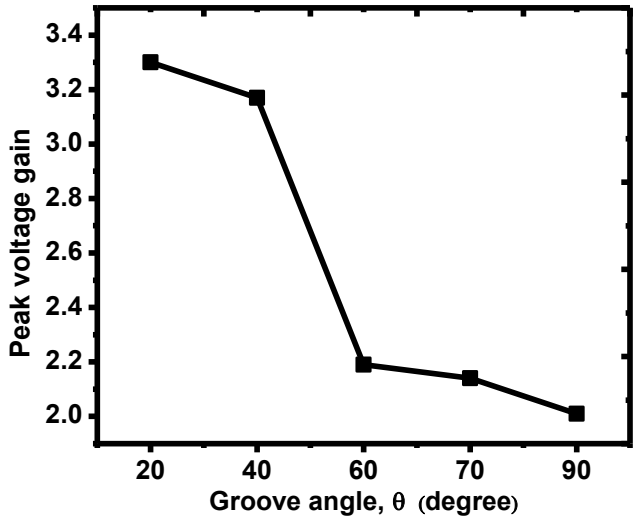


Fig.4.11: Variation of peak voltage gain of common source amplifier with R_L=1MΩ at V_{DD} = 650mV with varying groove angle of device viz.20^0, 40^0, 60^0, 70^0, 90^0 and t_{ch} = 5 nm

Fig.4.12 shows that the bandwidth of the amplifier increases with increasing θ because the

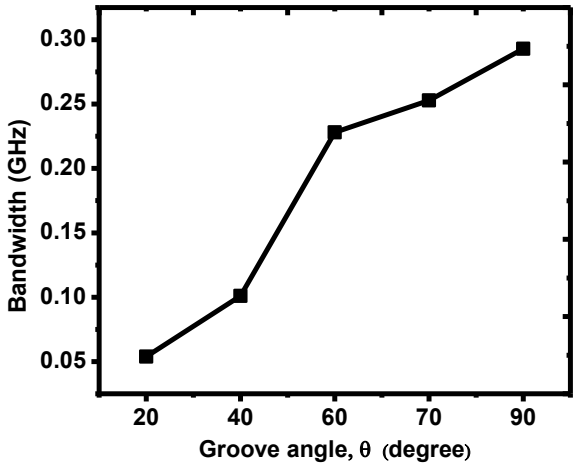


Fig. 4.12: Variation of bandwidth of common source amplifier with R_L=1MΩ at V_{DD} = 650 mV with varying groove angle of device viz.20^0, 40^0, 60^0, 70^0, 90^0 and t_{ch} = 5 nm

parasitic capacitances of the devices decrease with increasing θ, thus making higher grooving angle more suitable for high frequency applications. Fig. 4.13 demonstrates the dependency of gain-bandwidth product on θ which changes following the dependency of both gain and bandwidth on θ.

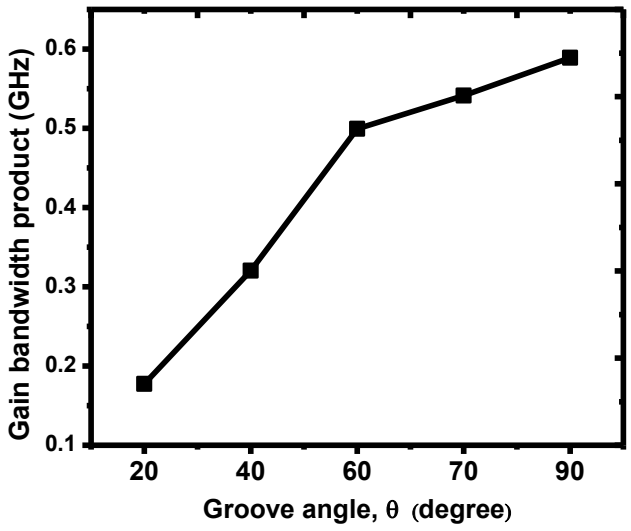


Fig. 4.13: Variation of gain-bandwidth product of common source amplifier with R_L=1MΩ at V_{DD} = 650mV with varying groove angle of device viz. 20^0, 40^0, 60^0, 70^0, 90^0 and t_{ch} = 5 nm

From this comprehensive analysis, the author has concluded that improved device and circuit-level parameters can be achieved by adjusting the angle of grooving. To add to this, the author has further carried on the studies to have an idea about the impact of channel thickness also on the device and distortion parameters. For this, the author has considered the grooved structure with varying channel thickness viz. from 3 nm to 8 nm, keeping all other device parameters as well as model same as that of the previous study.

4.4.3 Impact of channel thickness on analog parameters of the device

For the channel thicknesses in the range of 3 nm to 8 nm and at channel length of 14 nm, the change of drain current (I_D) with respect to V_{GT} both in linear and log scale is shown in Fig. 4.14.The maximum value of drain current is obtained for the device having t_{ch} = 8 nm due to increased electron concentration in such a device.

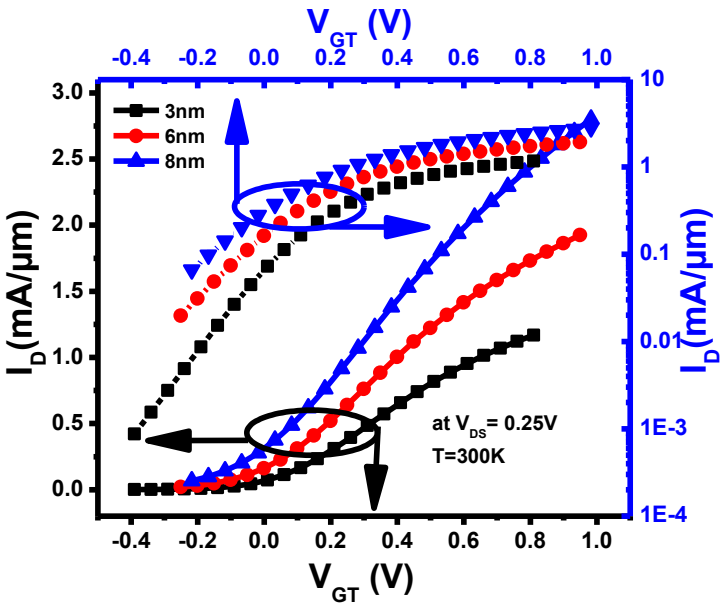


Fig. 4.14:Transfer characteristics as function of V_{GT} for different values of t_{ch} viz. 3nm, 6nm, and 8nm of InAs quantum well n-MOSFET for V_{DS} = 0.25V and L_{ch}=14nm at T=300K.

The distribution of electron concentration under identical bias condition (i.e. V_{DS} = V_{GT} =0.25V) along the channel length (L_{ch}) for the devices with t_{ch}=3 nm and 8 nm at T=300K are given in Fig. 4.15[(a)-(b)], respectively. It is clear from Fig. 4.15[(a)-(b)] that, for a larger value of t_{ch} , the total electron concentration in the channel exceeds that for smaller t_{ch} under the identical bias conditions. Notably, at V_{DS} = V_{GT} =0.25V, when t_{ch} is 3 nm, the electron concentration lies in the range of 4.17×10^{17} cm^{-3} to 1.03×10^{17} cm^{-3} but under same condition when t_{ch} is 8 nm, the concentration is from 2.95×10^{18} cm^{-3} to 2.5×10^{17} cm^{-3}. Due to the higher values of electron

concentration in the channel, the highest drain current is obtained for the device with t_{ch}= 8 nm. Thus, drain current for t_{ch}= 8 nm improves by 2.45times compared to the device with t_{ch}= 3 nm.

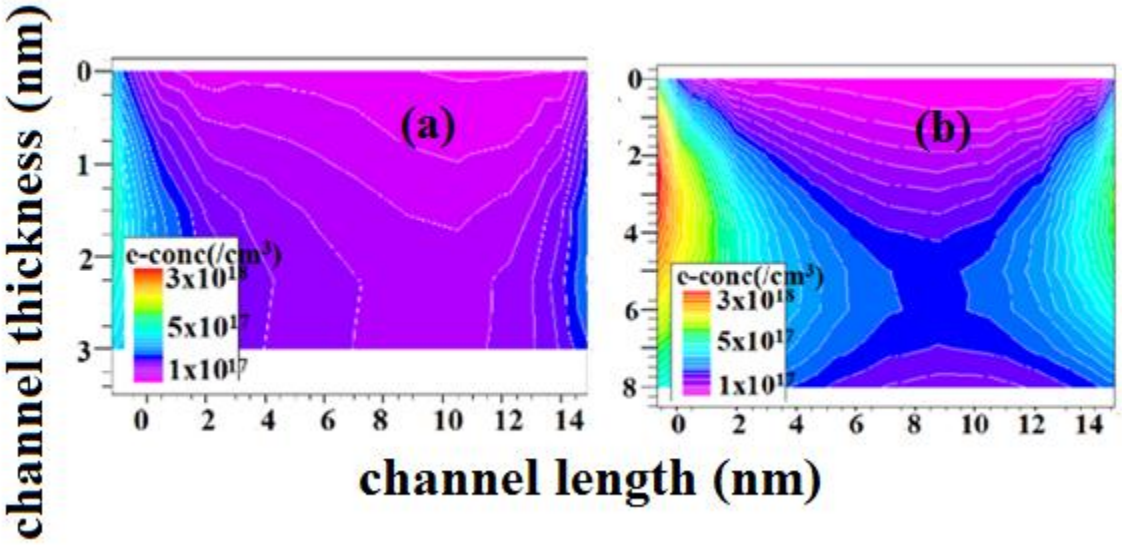


Fig. 4.15: 2-D distribution of electron concentration (/cm^3) for device (a) t_{ch}=3 nm (b) t_{ch}= 8nm of InAs quantum well n-MOSFET at V_{DS} = V_{GT} = 0.25V for L_{ch}=14nm at T=300K. The left and right sides indicate source and drain ends, respectively.

The variation of transconductance, g_m and the slope of g_m with V_{GT} at T=300K is demonstrated in Fig. 4.16 which shows the maximum and minimum values of g_m are obtained for having channel thickness of 8 nm and 3 nm, respectively. This is because effective mobility of the carriers increases with increase of t_{ch} which in turn improves transconductance of the device. Numerical analysis shows that the peak values of the effective electron mobility changes from 1.79×10^3cm^2/V.s for t_{ch}= 3 nm to 4.6×10^3cm^2/V.s for t_{ch}=8 nm at T=300K.Thus, for the device with t_{ch}=8 nm, peak g_m increases by 75.8% compared to the device with t_{ch}=3 nm.

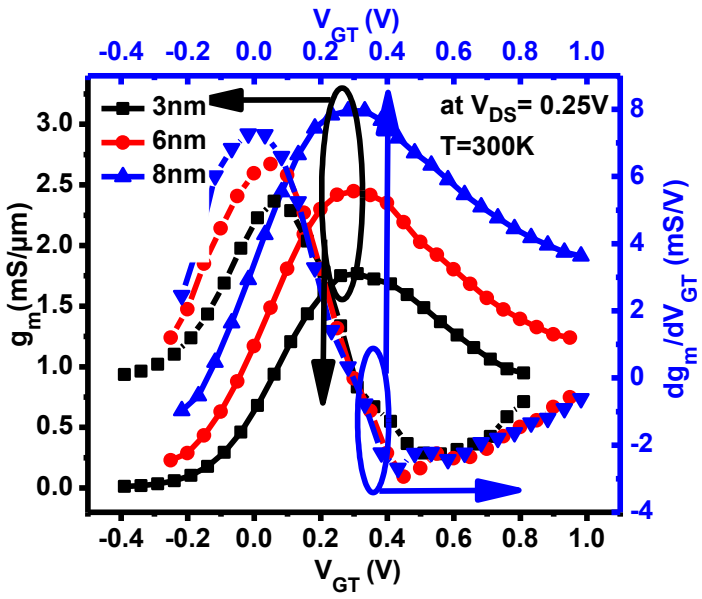


Fig. 4.16: Variation of transconductance (g_m) and the slope of g_m with respect to V_{GT} of InAs quantum well n-MOSFET with varying t_{ch} viz. 3 nm, 6 nm and 8 nm, respectively at V_{DS} = 0.25V for L_{ch}=14nm at T=300K.

Fig. 4.17 shows the variation of output conductance g_d with V_{GT} for different values of channel thicknesses at T=300K. Device with t_{ch} = 8 nm shows higher value of g_d because with increasing channel thickness, output current increases which ultimately increases the output conductance.

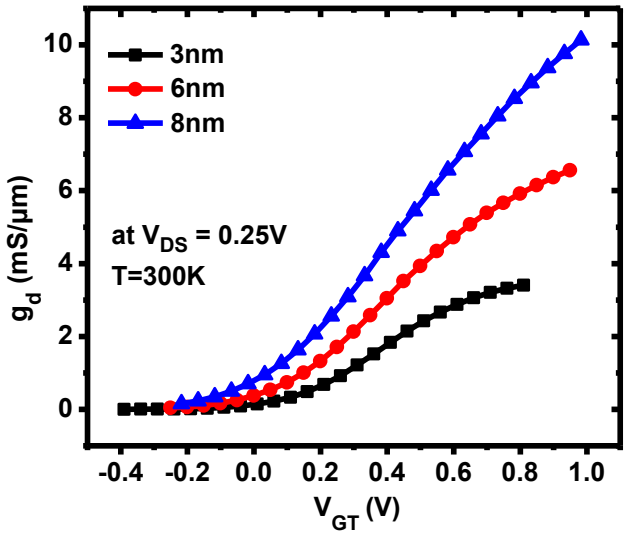


Fig. 4.17: Variation of output conductance (g_d) with respect to V_{GT} of InAs quantum well n-MOSFET with varying t_{ch} viz. 3 nm, 6 nm and 8 nm, respectively at V_{DS} = 0.25V for L_{ch}=14nm at T=300K.

So, V_{DS}=V_{GT}= 0.25 V, g_d in the device having t_{ch}=3 nm reduces by 67.7% as compared to that with t_{ch}=8 nm. Fig. 4.18 deals with the variation of the transconductance generation factor or transconductance efficiency (g_m/I_D) with respect to V_{GT} and this factor shows improved value in the device with t_{ch}=3 nm due to considerable reduction in the drain current in its subthreshold region. Thus, this factor improves by 1.93 times for the device with t_{ch}=3 nm as compared to that with t_{ch}=8 nm.

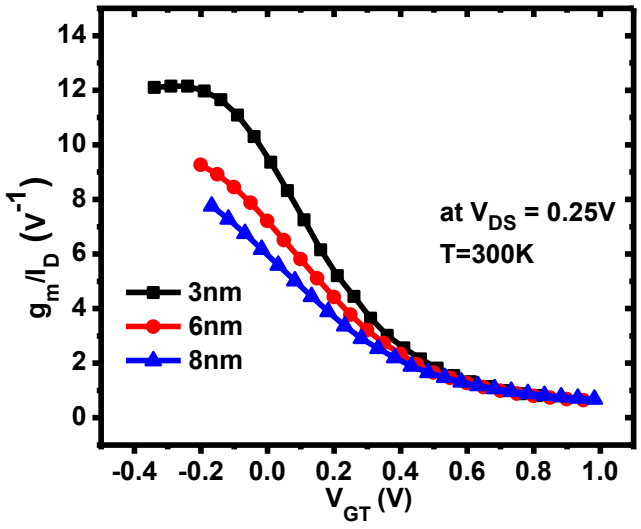


Fig. 4.18: Variation of transconductance generation factor (g_m/I_D) with respect to V_{GT} of InAs quantum well n-MOSFET with varying t_{ch} viz. 3 nm, 6 nm and 8 nm, respectively at V_{DS} = 0.25V for L_{ch}=14nm at T=300K.

Fig. 4.19 compares the voltage gain (A_V) of the InAs quantum well devices with different channel thicknesses viz. 3 nm, 6 nm and 8 nm, respectively at T=300 K at V_{DS} = 0.25V. This factor improves in device with t_{ch}= 3 nm compared to the other devices due to improvement in g_d despite partial compensation of g_m. Thus, peak gain of the device with t_{ch}=3 nm improves almost 1.53 times as compared to that with t_{ch}=8 nm.

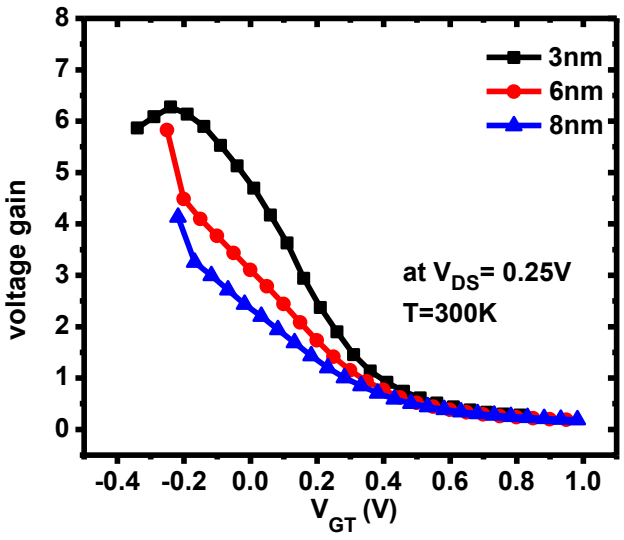


Fig. 4.19: Variation of voltage gain(A_V) with respect to V_{GT} of InAs quantum well n-MOSFET with varying t_{ch} viz. 3 nm, 6 nm and 8 nm, respectively at V_{DS} = 0.25V for L_{ch}=14nm at T=300K.

4.4.4 Impact of channel thickness on harmonic distortion analysis

The variation of HD_2 and HD_3 with respect to V_{GT} as shown in Fig. 4.20 reveals that both these factors tend to decrease with increasing value in channel thickness, thus showing improved linearity of the device. Both HD_2 and HD_3 vary inversely and directly with g_m and its derivative, respectively. From the analysis, the author has found out that at V_{GT} =V_{DS} = 0.25V ,the change of g_m with V_{GT} shows 43.07% decrement and the change of its derivative with V_{GT} shows about 9% increment in the device with t_{ch}=3 nm as compared to that with t_{ch}=8 nm. Thus, at V_{DS}= 0.25 V, the magnitude of the minimum value of HD_2 in the device having t_{ch}=3 nm increases by 5.71% as compared to that with t_{ch}=8 nm. Under the same biasing condition, the magnitudes of HD_3 (first minima, second minima) in the device having t_{ch}=3 nm increases by 0.54 % and 18.99 % , respectively as compared to that with t_{ch}=8 nm.

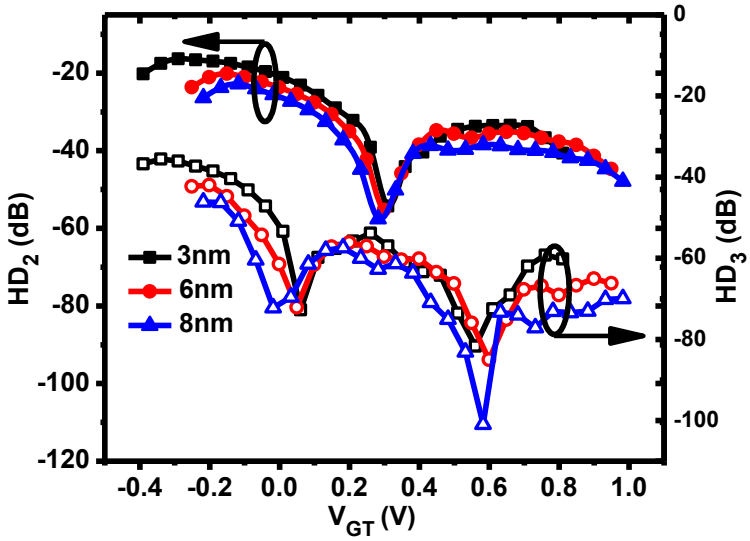


Fig. 4.20: Variation of HD_2 and HD_3 with respect to V_{GT} of InAs quantum well n-MOSFET with varying t_{ch} viz. 3 nm, 6 nm and 8 nm, respectively at V_{DS} = 0.25V for L_{ch}=14nm at T=300K.

Fig. 4.21 demonstrates the total harmonic distortion (THD) with V_{GT} with varying t_{ch} .Results show that THD decreases with increasing t_{ch} and thus improves the overall linearity of the device. Thus, at V_{DS}= 0.25 V, the magnitude of the minimum value of THD in the device having t_{ch}=3 nm increases by 6.99% as compared to that with t_{ch}=8 nm. In the same graph, the author has also plotted THD vs transconductance generation factor (TGF). This curve shows that beyond THD minimum, lower values of THD is obtained for thinner device. For higher TGF which means better DC to AC conversion efficiency, lowest THD is obtained for the device having t_{ch}=3 nm. At TGF of 5 V^{-1}, THD for the device with t_{ch} = 3 nm is showing at -34 dB which is 5 dB lower than 8 nm thick device at that TGF. This clearly indicated that the thinner device will have better DC to AC conversion efficiency with lower THD.

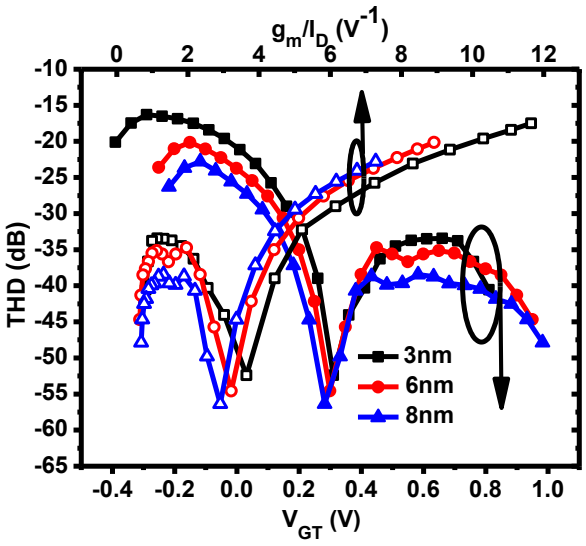


Fig. 4.21: Variation of THD with respect to V_{GT} and transconductance generation factor (TGF) of InAs quantum well n-MOSFET with varying t_{ch} viz. 3 nm, 6 nm and 8 nm, respectively at V_{DS} = 0.25V for L_{ch}=14nm at T=300K.

Fig. 4.22 shows the variation of THD with voltage gain. It is observed that 3 nm channel thick device is offering lowest distortion in the voltage gain range of 1.3 to 5.4.At voltage gain of 1.5, THD for the device with t_{ch} = 3 nm is -52 dB which is 17 dB lower than that of 8 nm thick device.

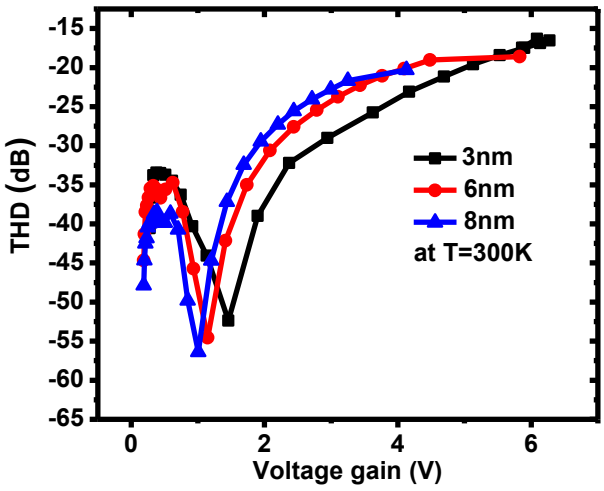


Fig. 4.22 : Variation of THD with respect to voltage gain of InAs quantum well n-MOSFET with varying t_{ch} viz. 3 nm, 6 nm and 8 nm, respectively at V_{DS} = 0.25V for L_{ch}=14nm at T=300K.

4.5 Comparative analysis of the proposed device with other reported devices

From the literature survey, the author has found out that there is less reported work on harmonic distortion analysis using III-V semiconductor based MOSFETs. In Table III, the author has made a comparative analysis of the proposed InAs based quantum well n-MOSFET structure with other reported Silicon-on insulator structures in terms of distortion parameters [4.14,5.17] derived using IFM technique. It can well be concluded that though the proposed device shows a rise in HD_2 parameter, it's HD_3 parameter has improved for which the THD parameter is showing better results. Also, the device is showing lowest value of THD at TGF of 5 V^{-1} signifying the fact that the proposed device will exhibit better DC to AC conversion with less distortion.

Table III: Comparative analysis of the proposed structure with other reported structures using IFM method for harmonic distortion analysis:

Type of Device with specifications	**HD_2 minimum (dB)**	**HD_3 1st minimum (dB)**	**THD minimum (dB)**	**THD at g_m/I_D = 5 V^{-1} (beyond THD minimum) (dB)**	**Ref**
FDSOI n-MOSFET L_{ch} = 250 nm v_a = 200 mV, V_{DS}=1.2 V	-62	-40	-55	-20	[4.14]
Vertically stacked SOI nanowire L_{ch} = 100 nm, t_{ch} =9 nm v_a = 50 mV, V_{DS}=0.75 V	-	-61	-26.5	-26	[4.17]
InAs quantum well n-MOSFET with raised source drain architecture L_{ch} = 14 nm, t_{ch} = 5 nm θ= 40^0, v_a = 50 mV V_{DS}=0.5 V (author's work)	**-54**	**-78**	**-51**	**-32**	[4.22]

4.6 Summary

The author has investigated and analyzed the analog and linearity performance of InAs based quantum well n-MOSFET having raised source/drain architecture with varying angle of grooving and channel thickness. Except transconductance, the author has found out that all other device parameters exhibit improvement in the thinner body and smaller groove angled device compared to the thicker body and wider groove angled one. However, analysis of the common source amplifier circuit reveals that distortions reduce and hence linearity improves in the circuit built with thicker body and higher groove-angled device compared to that with thinner body and lesser groove-angled device. Though the smallest angled and less thickened device ($\theta = 20^0$ and t_{ch} =3 nm) is showing improved performance in terms of voltage gain, output conductance and transconductance efficiency, the device shows compromised value of transconductance and high values of distortion minimum. Also, when the grooving angle is made 20^0, the distance between the source and drain (L_{SD}) increases to 406 nm resulting in a larger device impression. So, to keep a balance between analog and linearity performance, the author chooses the device with $\theta = 40^0$ and t_{ch} = 5 nm which gives voltage gain of 4.5 and HD_2 and THD minima of -54 dB and -51 dB, respectively. Also, at a high value of TGF of 5 V^{-1} and voltage gain of 3, the device shows THD values of -32dB and -25 dB, respectively, denoting the fact that the proposed device will execute better amplification and better DC to AC conversion with less distortion.

REFERENCES

[4.1] T.C Harman , H.L. Goering , and A.C Beer , " Electrical properties of n-type InAs," *Phys Rev*, vol. 104, no.6, pp1562–1564,1956. https://doi.org/10.1103/PhysRev.104.1562

[4.2] A.Lubow , S. Ismail-Beigi , and T.P Ma ,"Comparison of drive currents in metal-oxide-semiconductor field effect transistors made of Si, Ge, GaAs, InGaAs and InAs channels," *Applied Physics Letters* , vol. 96, no.12, pp.122105,2010. https://doi.org/10.1063/1.3367708

[4.3] K. Takei ,S. Chuang , H. Fang , R. Kapadia , C.H.Liu ,J. Nah , H.S Kim, E. Plis,S. Krishna , Y.L Chueh , and A. Javey , " Benchmarking the performance of ultrathin body InAs-on-insulator transistors as a function of body thickness," *Applied Physics Letters*, vol.99,no.10,pp.103507,2011. https://doi.org/10.1063/1.3636110.

[4.4] J. Nah , H. Fang ,C. Wang ,K. Takei ,M.H. Lee ,E. Plis , S. Krishna , and A. Javey , " III–V complementary metal-oxide-semiconductor electronics on silicon substrates.," *Nano Letters* , vol. 12, no. 7, pp. 3592–3595,2012. https://doi.org/10.1021/nl301254z.

[4.5] K. Takei ,R. Kapadia ,H. Fang , E. Plis , S. Krishna , and A.Javey, "High quality interfaces of InAs-on-insulator field-effect transistors with ZrO_2 gate dielectrics," *Applied Physics Letters*, vol.102,no. 15,pp.153513, 2013. https://doi.org/10.1063/1.4802779

[4.6] M. Yokoyama , H. Yokoyama , M. Takenaka,and S. Takagi,"III–V single structure CMOS by using ultrathin body InAs/GaSb-OI channels on Si," *Proceedings of VLSI Tech*, p 978,2014. http://dx.doi.org/10.1109/VLSIT.2014.6894350.

[4.7] T. Dutta ,S. Kumar ,P. Rastogi,A. Agarwal ,and Y.S. Chauhan , " Impact of channel thickness variation on bandstructure and source-to drain tunneling in ultra-thin body III–V MOSFETs," *J Electron Devices Soc*, vol.4, no.2, pp.66–71,2016. https://doi.org/10.1109/JEDS.2016.2522981

[4.8] J.A. del Alamo, "Nanometer-scale electronics with III-V compound semiconductors," *Nature*, vol.479, no.17, pp.317-323, 2011. https://doi.org/10.1038/nature10677

[4.9] S. Lee, C.-Y. Huang, D. Cohen-Elias, J.M. Law, V. Chobpattanna, S. Kramer, B.J. Thibeault, W. Mitchell, S. Stemmer, A.C. Gossard, and M. J. W. Rodwell, "High performance raised source/drain InAs/$In_{0.53}Ga_{0.47}As$ channel metal-oxide semiconductor field-effect-transistors with reduced leakage using a vertical spacer," *Appl. Phys. Lett*,vol.103, no.23,2013.pp.233503-1-4. https://doi.org/10.1109/VLSIT.2014.6894363.

[4.10] S. Lee, C.-Y. Huang, D.C. Elias, B.J. Thibeault, W. Mitchell, V. Chobpattana, S. Stemmer, A.C. Ossard, and M.J.W. Rodwell, "Highly scalable raised source/drain InAs quantum well MOSFETs exhibiting I_{ON} = 482μA/μm at I_{OFF}=100 nA/μm and V_{DD}=0.5 V," *IEEE Electron Device Lett*, vol.35, no.6, 2014, pp. 621-23. https://doi.org/ 10.1109/LED.2014.2317146.

[4.11] R. Salazar, A. Ortiz-Conde,and F.J. Garcia-Sanchez, "Harmonic distortion in MOSFETs calculated by successive integration of the transfer characteristics," 9th Int. Conf. on Solid-State and Integrated-Circuit Technology, 10440520, 2008. https://doi.org/10.1109/ICSICT.2008.4734556.

[4.12] R. Salazar, A. Ortiz-Conde, F.J Garcia-Sanchez, C.-S Ho, and J. J. Liou , "Evaluating MOSFET harmonic distortion by successive integration of the I–V characteristics," *Solid-State Electron.*, vol.,52, pp.1092–1098, 2008.

[4.13] P.G. Jespers,and A.B. Murmann ,"Calculation of MOSFET distortion using the transconductance-to-current ratio (g_m/I_D)," Proc. IEEE. Int. Symp. Circuits Syst. Lisbon, Portugal, pp. 529-532,2015. https://doi.org/10.1109/ISCAS.2015.7168687

[4.14] B. Parvais, A. Cerderia, D. Schreurs, and J.-P Raskin,"Harmonic Distortion Characterization of SOI MOSFETs," 11th GAAS Symposium, pp.357-360,2003.

[4.15] R.T. Doria, A. Cerdeira, J. Pierre, D.Flandre, and M.A.Pavanello, "Harmonic distortion analysis of double gate graded-channel MOSFETs operating in saturation," *Microelectronics Journal*, vol. 39, pp.1663–1670, 2008. https://doi.org/10.1016/j.mejo.2008.02.006

[4.16] R.T Doria, A. Cerdeira, J.A. Martino, E. Simoen, C. Claeys, and M.C. Pavanello, "Harmonic Distortion of Unstrained and Strained FinFETs Operating in Saturation," *IEEE Transactions On Electron Devices*, vol. 57,no.12, pp.3303-3311,2010. https://doi.org/ 10.1109/TED.2010.2079936

[4.17] C. A. B. de Carvalho, G. Mariniello, B. C. Paz, S. Barraud, M. Vinet, O. Faynot, and M. A. Pavanell, "Performance and Analysis of n-Type Vertically Stacked Nanowires Regarding Harmonic Distortion," *Journal of Integrated Circuits and Systems*, vol. 15, no 2, pp.1-5, 2020. https://doi.org/10.29292/jics.v15i2.202.

[4.18] M.A. Alemfin, and A.Cerdeira, "Determination of Non-Linear Harmonic Distortion in SPICE using the Integral Function Method," in PROC. 24th International

Conference On Microelectronics, Nis. Serbia, vol.2, 2004. https://doi.org/10.1109/ICMEL.2004.1314897

[4.19] M.A. Cerdeira, M. Aleman, M. Estrada, and D.Flandre, "Integral function method for determination of nonlinear harmonic distortion," *Solid-State Electron.*, vol. 48, pp. 2225–2234,2004. https://doi.org/10.1016/j.sse.2004.06.001.

[4.20] T. Dutta, K. Koley, S.K.Saha, and C.K. Sarkar, "Analysis of Harmonic Distortion in UDG-MOSFETs," *IEEE Trans. Electron Dev.*, vol. 61, no.4, pp.998-1005, 2014. https://doi.org/10.1109/TED.2014.2306971.

[4.21] S. Dasgupta, C. Mondal, and A. Biswas, "Role of grooving angle of 14-nm-InAs quantum well for improvement of analog/RF and linearity performance," *IET Circuits, Devices and Systems*, 2019. https://doi.org/10.1049/iet-cds.2019.0064.[Online].

[4.22] S.Dasgupta, C.Mondal and A.Biswas, " Reduction of Harmonic Distortion of 14-nm InAs quantum well n-MOSFET for high DC to AC conversion and high voltage gain," 4th IEEE Electron Devices Technology and Manufacturing (EDTM) Conference Proceedings of Technical Papers, Malayasia, pp. 28-31, April,2020.https://doi.org/ 10.1109/EDTM47692.2020.9118031.

[4.23] R. Das, A. Dasgupta, and A Kundu, "Reliability analysis through linearity and harmonic distortion of a dual material-gate asymmetric underlapped DGMOSFET," *Microelectronics Reliability*, vol. 92 pp.106–113, 2019. https://doi.org/10.1016/j.microrel.2018.11.002

CHAPTER-5

Enhancing Radiation Resilience in InAs Quantum Well n-MOSFETs through Optimized Groove Geometry and Channel Thickness: A Study of Single Event Transients under Varied Bias Conditions

In this chapter, the author has focused the research to study the single event transient effect of radiation on InAs quantum well N-MOSFETs with raised source-drain architecture featuring channel length of 14 nm and channel thickness varying from 4 nm to 10 nm in the presence of Neon, Krypton and Xenon ions. The angle of grooving (θ) of the device is varied ranging from 40° to 90° to find out an InAs MOSFET with highest radiation hardness.

5.1 Introduction

Lately, semiconductor-based devices find many applications in harsh radiation environments such as space, atomic research centers, and radiation physics laboratories. Degradation of the device performance due to radiation is a growing concern in the semiconductor industry. The study of radiation response has become an emerging field in semiconductor technology to find radiation-hard semiconductor materials and device structures. The need to explore the drain current pattern under the effect of radiation grows to build radiation-tolerant circuits that can be used in hostile environments.

Of the several methods that cover up this study of radiation, the category of single-event transient effect is being considered in this work. Single-event transient effect is the momentary transient disturbance created at the output of the device when one energetic ion strikes the device. This fast moving heavy energetic ion when traverses through the medium of the device, it interacts with the electrons of atoms of the material or medium and this interaction excites or ionizes the atoms, leading to an energy loss of the traveling ion. These two events are studied in terms of mean excitation energy and stopping power, respectively.

Some of the materials and the device structures that are widely examined to study radiation patterns include III-V nitride-based heterostructures, InAs/GaAs quantum dots (QDs), and GaAs/InGaAs quantum wells (QWs) [5.1-5.24].In fact the heavy ion testing of various structures is nowadays conducted in the presence of several high energy ions like Krypton, Argon, Neon, Xenon to study the single-event damages caused by these ions on the structures. In 2010, Dale Mc Morrow et al. measured drain charge-collection transients for InAlSb/InAs HEMT under irradiation by 3.1GeV and 5.9 GeV Xenon ions [5.6]. In the following year, Kuboyama studied single event damages caused by Neon (74 MeV), Argon (147 MeV), Krypton (315 MeV), and Xenon (443 MeV) in AlGaN/GaN HEMTs [5.10]. In 2015, Barth et al. performed single-event transient measurements on n-channel InAsSb quantum-well MOSFET using 9.3 MeV/amu Krypton ions [5.2] Later, in 2017, the same group carried on the radiation study on p-channel InGaSb quantum-well MOSFET using 10.0 MeV/amu Argon ions [5.3].Although there have been numerous reports on InAs MOSFETs, [5.25-5.34] less attentions have been paid to evaluate their performance in the presence of radiation [5.35-5.37].

In this chapter, the author has concentrated the radiation effects research on InAs quantum well N-MOSFET with raised source-drain architecture in the presence of Neon, Krypton and Xenon

ions using the concept of single event transient effects (SET). To study the impact of the angle of grooving (θ) on the radiation performance of quantum well MOSFET, the author has generated different device structures by keeping channel thickness t_{ch}= 5 nm using multiple values of θ = 40°, 60°, 70° and 90° [5.38] .The author has also studied this effect considering only Krypton ion on the channel thickness for which the author has considered varied channel thicknesses in the range of 4 nm to 10 nm, keeping θ constant [5.39].For both the cases, the author has selected the sensitive region as the channel length below the gate. Other sensitive regions are been neglected in this work because the channel length (L_{ch}) or the gate length (L_G) remains fixed at 14 nm throughout the simulation, but the distance between the source and the drain (L_{SD}) changes from 183 nm down to 14 nm as θ changes from 40° to 90°. So, to study and compare the effect of radiation on the devices with varying θ, as the gate length remains fixed for all the devices, the author has considered only that region as the sensitive region.

This chapter is organised as follows: In the section 5.2 the device structure is given followed by simulation set-up and model validation in section 5.3. The results are discussed in section 5.4. Section 5.5 has a comparative analysis of the proposed device with other reported devices. Finally, this chapter is summarized in section 5.6.

5.2 Device Description

Fig. 5.1 illustrates n-channel InAs quantum well MOSFET featuring vertical spacer and θ as the angle of grooving. The device dimensions and the material specifications remain same as previously discussed. Fig. 5.1 clearly denotes that the ion strike happens to be at the middle of the InAs channel and finally the ion emerges out of the device from the InP substrate after travelling through various layers of the device in the vertical downwards direction.

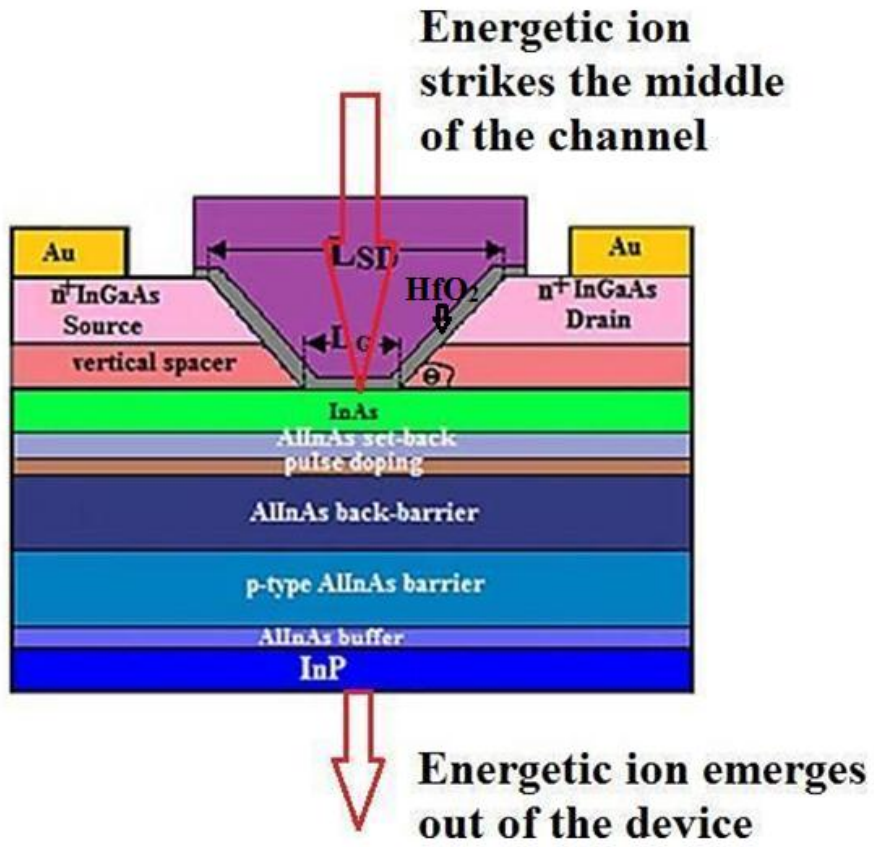


Fig.5.1: Cross-sectional view of InAs channel quantum well MOSFET with raised source/drain architecture. The gate length (L_G) or channel length (L_{ch}) beneath HfO_2 is 14 nm with L_{SD} as the spacing between the source and drain regions at the top of the device and θ as the angle of grooving.

5.3 Simulation set-up, model calibration and validation

The simulation set-up is kept same as that being discussed in the previous chapters. Thickness dependent models of bandgap, effective mass, and non-parabolocity factor are kept same as that previously said. Other models like mobility model, scattering model, tunneling model, recombination models, carrier statistics and transport model as well as methods of numerical implementation- all are used with the same parameter values as that explained in the previous chapter. With the proper inclusion all these models, the author has first calibrated the device and

the results of the calibration are then validated with the experimental results of [5.40] in the same way as done in the previous chapters.

To study the radiation effects, 9.3 MeV/amu of Neon (Ne), Krypton (Kr), and Xenon (Xe) ions are considered to be incident on the device, following [5.2]. The ion tracks are taken to be Gaussian both in time (T(t)) and space (R(r)), given by (5.1) and (5.2), respectively [5.41]

$$T(t) = \frac{2\exp\left(-\left(\frac{t-t_0}{t_c}\right)^2\right)}{t_c\sqrt{\pi}erfc\left(-\frac{t_0}{tc}\right)} \tag{5.1}$$

$$R(r) = exp\left(-\frac{r}{RADIUS}\right)^2 \tag{5.2}$$

The irradiation track has a Gaussian shape with a narrow radius of 5 nm, the width of 120 ps (t_c) and the time the radiation reaches its peak value time is considered as 600 ps (t_0) [5.2] To study the effect of the radiation across the devices, the author has considered the following calculations, following [5.5].

Stopping power in any medium is given by

$$-\frac{dE}{dx} = \frac{(5.08\times10^{-31}\times Z^2\times n)}{\beta^2}[F(\beta) - lnI_{eV}], \tag{5.3}$$

where I_{eV} is the mean excitation energy, n is the number of electrons per unit volume in the medium, Z is the atomic number of the incident ion and β is the velocity of the heavy particle ($= \sqrt{(\frac{2\times E}{M})}$), where E and M are energy and mass of incident ions, respectively) relative to velocity of light and

$$F(\beta) = ln\frac{1.02\times10^6\times\beta^2}{(1-\beta^2)} - \beta^2 \tag{5.4}$$

Mass stopping power also called linear energy transfer (LET) is calculated by

$$LET = -\frac{dE}{dx} \times \frac{1}{\rho}, \tag{5.5}$$

where ρ is the density of the medium.

Table I shows the calculated parameter specifications within different layers of InAs quantum well n-MOSFET for a fixed channel thickness of 5 nm. Moreover, Table II covers these calculated parameters within different layers of InAs quantum well n-MOSFET for varied channel thicknesses.

Table I: Calculated parameter specifications within different layers of InAs quantum well n-MOSFET for fixed channel thickness of 5 nm:

Incident Ions	**Material**	**Incident energy (MeV)**	**Mean excitation energy (eV)**	**LET ($MeV.cm^2/mg$)**
Neon	InAs	187.58	411.57	2.58
	$In_{0.52}Al_{0.48}As$	187.57	383.75	2.65
	InP	187.06	379.93	2.68
Krypton	InAs	771.9	411.57	33.45
	$In_{0.52}Al_{0.48}As$	771.8	383.75	33.75
	InP	765.29	379.93	37.42
Xenon	InAs	1227.6	411.57	75.52
	$In_{0.52}Al_{0.48}As$	1227.39	383.75	77.63
	InP	1212.42	379.93	80.87

Table II: Calculated parameter specifications within different layers of InAs quantum well n-MOSFET for varied channel thickness under influence of Krypton ion:

Channel thickness (t_{ch}) (nm)	Material	Incident Energy (MeV)	LET (MeV.cm^2/mg)
4	InAs	771.9	33.45
	$In_{0.52}Al_{0.48}As$	771.8	33.12
	InP	765.29	33.36
7	InAs	771.9	33.45
	$In_{0.52}Al_{0.48}As$	771.76	32.70
	InP	765.25	33.05
10	InAs	771.9	33.45
	$In_{0.52}Al_{0.48}As$	771.71	32.15
	InP	765.2	32.22

In the simulation, the entry point and exit point coordinates of the incident ion for each layer of InAs quantum well n-MOSFET are specified separately. Also, the theoretically calculated LET value for each layer for each radiating ion is converted to amount of generated charge for each layer using the conversion factor (X) for each layer, as given in Table III. [5.7] This conversion factor (X) is calculated as $X = \frac{q \times \rho}{E_{eh}}$, where E_{eh} is electron-hole pair creation energy, ρ is the density of the material and q is electronic charge. [5.2]

Table III: Energy to generated charge conversion factor within different layers of InAs quantum well n-MOSFET:

Layer	Conversion factor (X) to multiply LET values in (MeV.cm^2/mg) to obtain generated charge in (pC/µm)
InAs	0.05
InAlAs	0.01
InP	0.016

The radiation analysis is carried out for a time period of 0 to 2ns with a drain to source bias of 0.5V.

5.4 Results and Discussions

5.4.1 Effect of SET on the device performance for varied channel thickness under influence of Krypton ion when no control voltage is applied i.e., V_{GS} = 0.0 V

Fig. 5.2 shows the simulated drain current for the devices with varying channel thickness, viz. t_{ch} = 4 nm, 7 nm and 10 nm and L_{ch} =14 nm at V_{GS} =0.0V and V_{DS} = 0.5V under the effect of Krypton radiation. When the energised ion reaches its peak value at t=0.6ns, the device with t_{ch} = 10 nm shows maximum value of the radiation current and it is 59.48 % higher compared to that observed in the device with t_{ch} = 4 nm under identical bias conditions, e. g., V_{GS} = 0.0 V and V_{DS} = 0.5V. This increament of radiation current in the thickened device is due to the change of bndgap with channel thickness which decreases from 0.65 eV to 0.43 eV at T=300 K when t_{ch} changes from 4 nm to 10 nm, following [5.42].

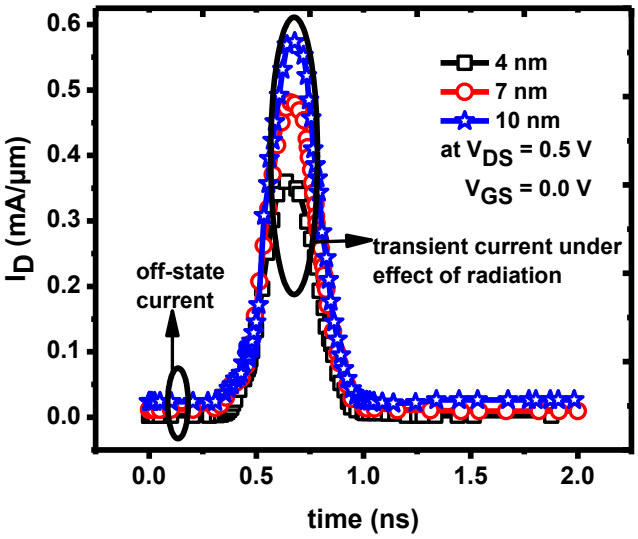


Fig. 5.2: Simulated transient current at V_{GS} = 0.0 V and V_{DS} = 0.5 V for InAs quantum well n-MOSFET with L_{ch} = 14 nm and t_{ch} varying as 4 nm, 7 nm and 10 nm.

Thus, the thickened device shows increased short channel effects (drain induced barrier lowering) due to decrement in bandgap . From the analysis, the author has found that at t=0.6ns, the lowering of source-to-channel barrier at t =0.6 ns are 11.3meV and 9.7 meV, respectively for the device with t_{ch} = 4 nm and 10 nm while these values are 28.2 meV and 27.4 meV, respectively at t=0 ns. Greater reduction of barrier causes more injection of carriers into the channel, which ultimately increases the drain current in the wider channel. Also, it is noted that the less thickened device is getting less affected due to radiation. It is found that in the time span of 0 ns and 0.6 ns, the reduction in the source-to-channel barrier is 4.5 % less in the less thickened device compared to the thicker one which results in 35 % less change in the drain current in the thinner device during that same time span. This makes the less thickened device to be more radiation tolerant.

The change of total collected charge, calculated by integrating drain current during the period of radiation, for V_{GS} = 0.0V and V_{DS} = 0.5V for different values of t_{ch} is shown in Fig. 5.3.

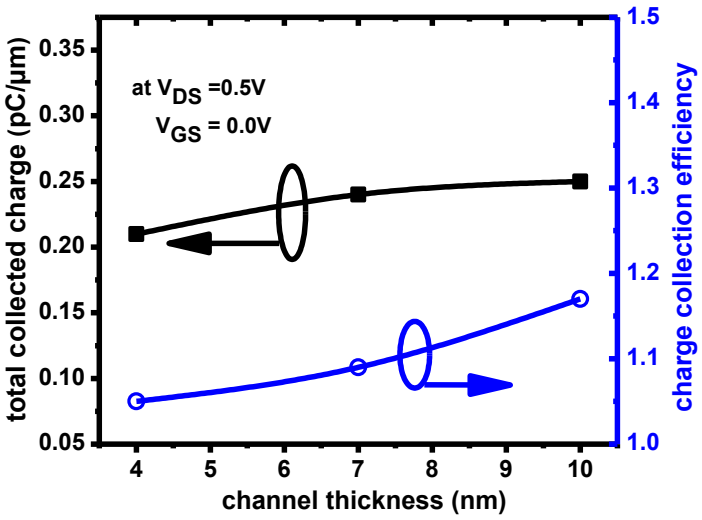


Fig. 5.3: Total collected charge for the total duration of radiation and charge collection efficiency at V_{GS} = 0.0 V and V_{DS} = 0.5 V for InAs quantum well n-MOSFET with L_{ch} = 14 nm and varying t_{ch} from 4 nm to 10 nm.

Availability of less number of carriers in the thinner channel decreases the amount of accumulated charge for which total collected charge is about 16 % less in the thinner channel compared to the thicker one at V_{GS} = 0.0 V and V_{DS} =0.5V.

The change of bandgap with channel thickness affects the electron-hole pair creation energy (E_{eh}), the value of which changes from 2.57 eV to 1.96 eV as t_{ch} increases from 4 nm to 10 nm following $E_{eh} = \frac{14}{5}E_g + 0.75$ [5.2]. Thus, deposited charge calculated using $Q_{dep} = \frac{LET.q.d.\rho}{E_{eh}}$ where d is the thickness of the material,[5.2] gets decreased by 13 % in t_{ch} = 4 nm device compared to t_{ch} = 10 nm device. The charge collection efficiency, considered as the ratio of the collected charge to that of the deposited charge within the devices, depicted across the secondary axis of Fig. 5.3, gets decreased by 10.25 % in the thinner device compared to the thicker one, concluding the fact that after radiation, the narrower channel device has the less capability of retention of charge.

The variation of full width half maximum (FWHM), rise time and pulse duration measured at 10 % of the peak value for different values of t_{ch} at V_{GS} = 0.0V and V_{DS} =0.5V are shown in Fig. 5.4[(a)-(b)]. It is observed that less thickened device is getting less affected due to radiation. At V_{GS} = 0.0V and V_{DS} =0.5V, t_{ch} = 4 nm device shows FWHM of 0.31 ns and pulse width of 0.54 ns which change to 0.34 ns and 0.58 ns, respectively for t_{ch} = 10 nm device. Also, the rise time in the thinner channel is 25 % less compared to the thicker one. For all these, the thinner channel device takes 7 % less time to fall back to steady state as shown in the secondary axis of Fig. 5.4(a).Thus, the narrower channel device displays a more steady behavior during hostile environmental conditions.

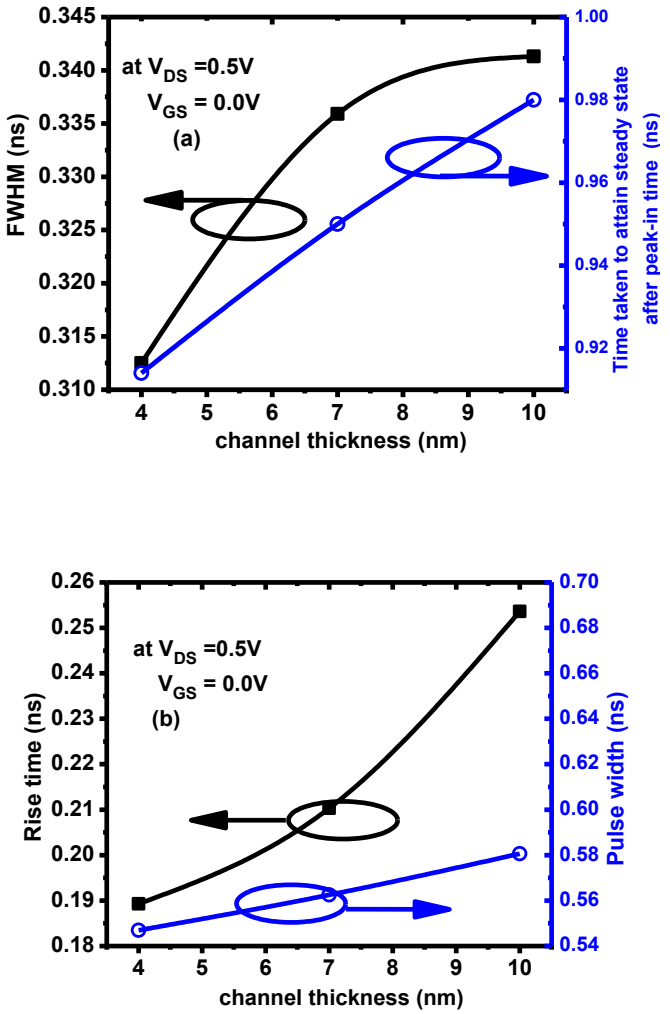


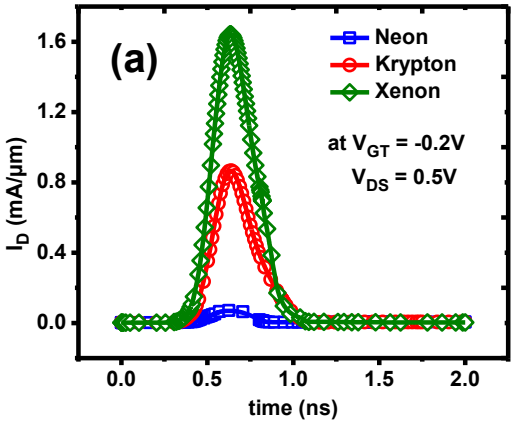
Fig. 5.4: (a): FWHM and time taken to attain the steady-state after peak-in time (b): Rise time and pulse width of radiation at V_{GS} = 0.0 V and V_{DS} = 0.5 V for InAs quantum well n-MOSFET with L_{ch} = 14 nm and varying t_{ch} from 4 nm to 10 nm.

5.4.2 Effect of SET on the device performance for varied angle of grooving under influence of Neon, Krypton and Xenon ions across varied bias conditions

To continue with the study on radiation effects, the author has further investigated the single event transient effect on the devices with varying groove angle under influence of Neon, Krypton and Xenon ions across varied bias conditions.

Fig. 5.5(a)-(b) demonstrate the simulated drain current for InAs quantum well N-MOSFET devices having channel thickness of 5 nm at gate length of 14 nm with the angle of grooving, θ = 40° at V_{GT} = -0.2V and 0.3V and V_{DS} = 0.5V for Neon, Krypton and Xenon ions. Fig. 5.5(c) shows the maximum change in the drain current within the time span of t=0 ns and t=0.6 ns under the influence of radiation for the devices with θ = 40°, 60°, 70°, and 90° at V_{DS} = 0.5V under various gate bias conditions.. The drain current profile shows a rise in the current to its peak value followed by a decay. From the characteristics, it is evident that the drain current attains the minimum value for the device with θ = 40° when the incident ion is Neon under all gate voltages. The atomic numbers for Neon, Krypton, and Xenon are 10, 36, and 54, respectively for which the energy transferred to the individual layers during irradiation with Neon is much less compared to Krypton and Xenon cases, as given in Table I following (5.3), (5.4), and (5.5).For this, drain current is minimum for all the devices when irradiated with Neon. Also, as θ changes from 40° to 90°, the distance between the source and the drain (L_{SD}) decreases from 183 nm to 14 nm as reported in the earlier findings. For this longer source-drain distance, the effect of the electric field on the channel with θ = 40° is less than the one with θ = 90°. This weak effect of electric field on smaller groove angled device causes less amount of DIBL in such a device. From Table IV, it is found that the effect of the electric field is least for the device with θ =40° when irradiated with Neon under all conditions. The changes in the peak values of electric field within the time span of t=0 ns and t=0.6 ns for the device with θ = 40° under the influence of Neon, Krypton, and Xenon ions at V_{GT} = -0.2 V and V_{DS} = 0.5V are less by 5.50 %, 7.8 % and 8.01 % respectively when irradiated with Neon, Krypton, and Xenon ions compared to the larger angled device. These percentages within the same time span are 5.06 %, 7.14 % and 7.28 % respectively at V_{GT} = 0.3 V and V_{DS} = 0.5V. As a result, the reduction in the source-channel

barrier within the same time span for the smaller angled device is less by 4.76 %, 6 % and 7 % respectively when irradiated with Neon, Krypton, and Xenon ions at V_{GT} = -0.2 V and V_{DS} = 0.5V compared to the larger angled device. These values within the same time span 2.63 %, 4.87 % and 6.8 % respectively at V_{GT} = 0.3 V and V_{DS} = 0.5V. A smaller lowering of the barrier leads to insufficient injection of carriers into the channel of the smaller angled device under all conditions. From Fig. 5.6 and Fig. 5.7, it is observed that the peak electron concentration within the time span of t=0 ns and t=0.6 ns at V_{GT} = -0.2 V and V_{DS} = 0.5V are 0.95 $\times 10^{18}/cm^3$, $1.03\times10^{18}/cm^3$ and $1.21\times10^{18}/cm^3$ for the device with $\theta = 40^{\circ}$ under the influence of Neon, Krypton and Xenon ions, respectively. Under the same conditions, the corresponding values increase to $1.01\times10^{18}/cm^3$, $1.19\times10^{18}/cm^3$ and $1.32\times10^{18}/cm^3$for the device with $\theta = 90^{\circ}$. These values are 1.05 $\times 10^{18}/cm^3$, $1.23\times10^{18}/cm^3$ and $1.35\times10^{18}/cm^3$ for the device with $\theta = 40^{\circ}$ and 1.12 $\times 10^{18}/cm^3$, $1.37\times10^{18}/cm^3$ and $1.4\times10^{18}/cm^3$ for the device with $\theta = 90^{\circ}$ under the influence of Neon, Krypton and Xenon ions, respectively within the same time span at V_{GT} = 0.3 V and V_{DS} = 0.5V.



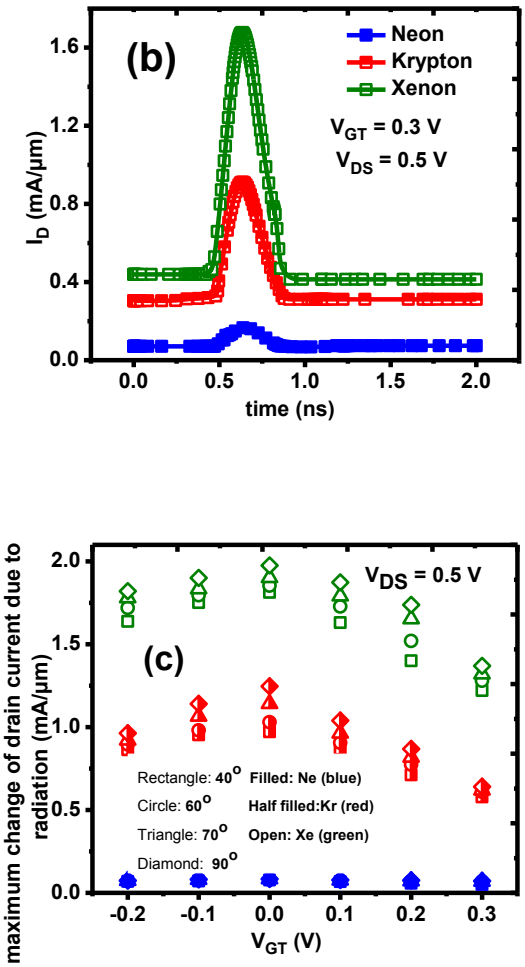


Fig. 5.5: Simulated drain current for θ = 40° at (a) V_{GT} = -0.2 V and (b) V_{GT} = 0.3 V (c) maximum change in the drain current due to radiation at V_{DS} = 0.5 V for InAs quantum well n-MOSFET with t_{ch} = 5 nm, L_G = 14 nm, and θ varying as 40°, 60°, 70° and 90° under the influence of Neon, Krypton and Xenon ions.

Thus, the weaker effect of electric field leads to smaller lowering of the barrier thereby injecting less amount of carrier which ultimately results in a decrement in the drain current for lower angled devices. Also, as the change in electric field is much less in the smaller angled device, the field exhibits better control on the drain current in the smaller groove angled and larger L_{SD} device, making it less prone to external effects compared to the larger angled and smaller L_{SD} device under all conditions. So, the change in the maximum drain current within t=0 ns and t=0.6 ns is always less in lesser angled larger L_{SD} device under all radiating ions, as in Fig. 5.5(c).

Table IV: Change in peak value of electric field and reduction in source-channel barrier lowering for InAs quantum well n-MOSFET with t_{ch} = 5 nm, L_G = 14 nm at V_{GT} = -0.2 V and 0.3V and V_{DS} =0.5 V with θ = 40° and 90° under the influence of Neon, Krypton and Xenon ions within the time span of t=0 ns and t=0.6 ns.

Angle of grooving (in degree)	40	40	40	40	40	40	90	90	90	90	90	90
V_{GT}(V)	-0.2	-0.2	-0.2	0.3	0.3	0.3	-0.2	-0.2	-0.2	0.3	0.3	0.3
Incident Ion	Ne	Kr	Xe	Ne	Kr	Xe	Ne	Kr	Xe	Ne	Kr	Xe
Change in peak value of electric field within the time span of t=0 ns and t=0.6 ns (× 10^5) (V/cm)	1.03	1.89	3.33	0.75	1.3	3.19	1.09	2.05	3.62	0.79	1.4	3.44
Reduction of source-channel barrier (eV)	0.4	0.47	0.53	0.37	0.39	0.41	0.42	0.5	0.57	0.38	0.41	0.44

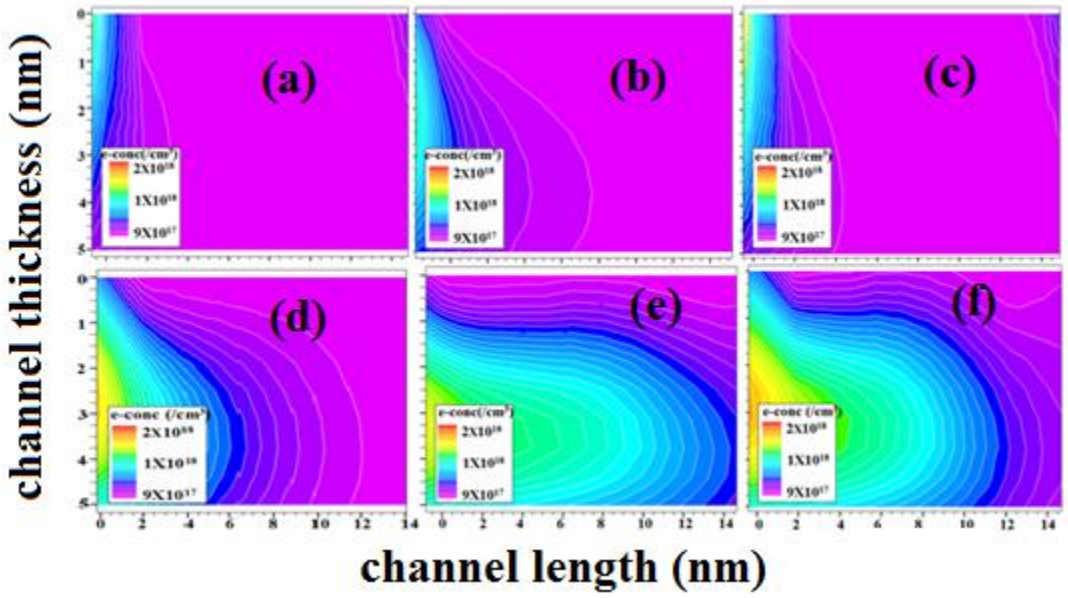


Fig. 5.6: 2-D electron concentration for (a) θ= 40° under effect of Ne (b) θ= 40° under effect of Kr (c) θ= 40° under effect of Xe (d) θ= 90° under effect of Ne (e) θ= 90° under effect of Kr (f) θ= 90° under effect of Xe at V_{GT} = -0.2 V and V_{DS} = 0.5 V within the time span of t=0 ns and 0.6 ns for InAs quantum well n-MOSFETs with t_{ch} = 5 nm, L_G = 14 nm.

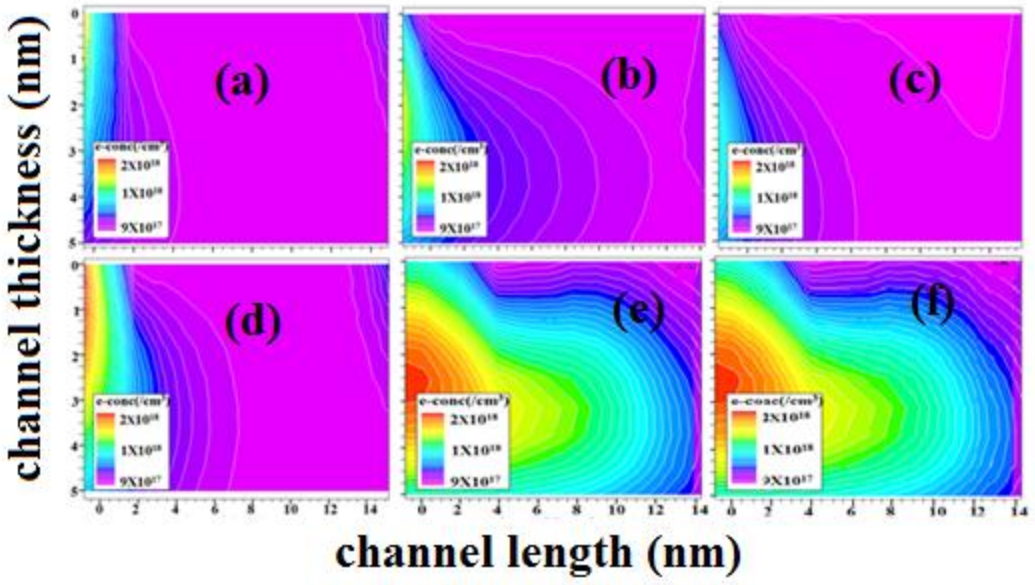


Fig. 5.7: 2-D electron concentration for (a) θ= 40° under effect of Ne (b) θ= 40° under effect of Kr (c) θ= 40° under effect of Xe (d) θ= 90° under effect of Ne (e) θ= 90° under effect of Kr (f) θ= 90° under effect of Xe at V_{GT} =0.3 V and V_{DS} = 0.5 V within the time span of t=0 ns and 0.6 ns for InAs quantum well n-MOSFETs with t_{ch} = 5 nm, L_G = 14 nm.

Also, it is observed that in all the devices, this change in the drain current shows increasing trend till the applied voltage reaches the threshold voltage.(i.e. V_{GT} =0.0 V). After the threshold voltage is crossed, once the devices start operation, the availability of empty density of states decreases and thus change of current also decreases. It is observed that the maximum change in the drain current within the time span of t=0 ns and t=0.6 ns at V_{GT} = -0.2 V and V_{DS} = 0.5V for the device with θ = 40° when irradiated with Neon, Krypton, and Xenon ions are 6.75 %, 10.28 % and 12.08 % respectively less compared to the device with θ = 90°. However, these percentages are 2.95 %, 9.52 % and 10.94 % respectively at V_{GT} = 0.3 V and V_{DS} = 0.5V.

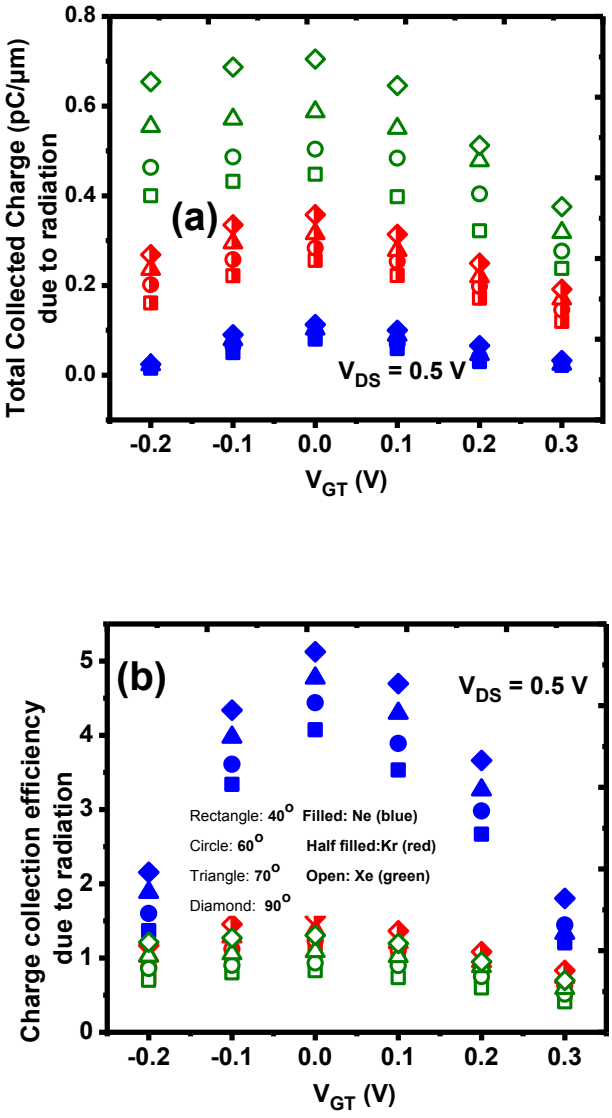


Fig. 5.8: (a) Total collected charge and (b) charge collection efficiency during the span of radiation with respect to V_{GT} at V_{DS} = 0.5 V for θ varying as 40°, 60°, 70° and 90°for InAs quantum well n-MOSFETs with t_{ch} = 5 nm, L_G = 14 nm under the influence of Neon, Krypton and Xenon ions .Filled symbols represent the influence of Neon, half-filled symbols represent the influence of Krypton, and open symbols represent the influence of Xenon. Rectangle, Circle, Triangle and diamond symbols are used to represent grooving angle of 40°, 60°, 70° and 90°, respectively.

The variation of total collected charge at different values of gate voltages and at V_{DS} =0.5V for multiple values of θ with different ion radiation is shown in Fig. 5.8(a). Among the radiating ions, as Neon ion transfers least energy to the medium, drain current is always minimum under Neon radiation and hence collected charge is also minimum. Again, the insignificant reduction of

the source channel barrier causes less influx of electrons from the source to the channel, which ultimately leads to the accumulation of fewer charges across the drain terminal for the narrow angled device, as illustrated in Fig. 5.8(a). Thus at V_{GT} = -0.2 V and V_{DS} =0.5V, the total collected charge after the span of radiation is less by 1.59 times, 1.67 times and 1.69 times respectively for $\theta = 40^{\circ}$ compared to the corresponding quantity with $\theta = 90^{\circ}$ when the devices are exposed to Neon, Krypton, and Xenon. This indicates the fact that after the span of radiation, a smaller amount of charge is retained in the narrower angled device. Fig. 5.8(b) shows charge collection efficiency, for different values of θ considering several ions of radiation at different gate bias for V_{DS} =0.5V. Deposited charge within the devices when exposed to Neon, Krypton and Xenon comes out to be 0.018 pC, 0.23 pC, and 0.54 pC respectively. Such variation is due to variation of energy transferred to the incident medium by the different radiating ions. Also, a smaller amount of source barrier lowering leads to lesser charge collection for narrower angled devices. Hence, the charge collection efficiency is less for narrower angled devices due to less adequate collection of charges. Also, as the deposited charge is minimum under the influence of Neon, the charge collection efficiency is always more for the devices when exposed to Neon. This collection efficiency thus gets reduced by 8.86 %, 12.3 %, and 12.71 % respectively in the device with $\theta = 40^{\circ}$ compared to the one with $\theta = 90^{\circ}$ under the influence of Neon, Krypton and Xenon ions at V_{GT} = -0.2 V and V_{DS} =0.5V. However, the variation percentages of collected charge are 2.85 %, 5.8 %, and 10.31 %, respectively less and of collection efficiency 6.37 %, 11.96 % and 10.30 % respectively less for smaller groove angled one compared to larger one at V_{GT} = 0.3 V. This indicates that after radiation, the confinement of charges within a lower angled device is less than that in the higher angled one which clearly suggests that the lower angled device is less prone to radiation both in absence and presence of control voltages.

Fig.5.9 demonstrates the variation of full width half maximum (FWHM) and the time required to settle down to steady state condition after peak-in time for different values of θ under the influence of different radiating ions under different gate bias for V_{DS} =0.5V. It is observed from the characteristics that FWHM shrinks as θ decreases, under all radiating ions. At V_{GT} = -0.2V and V_{DS} = 0.5V, the device with θ = 40° has FWHM of 0.285 ns, 0.355 ns and 0.44 ns, respectively under the influence of Neon, Krypton and Xenon ions. However, these values change to 0.33 ns, 0.42 ns, and 0.53 ns for FWHM for the device with θ = 90° under similar conditions. Again, for V_{GT} = 0.3 V, FWHM values are 0.24 ns, 0.27 ns and 0.28 ns for θ = 40° and 0.25 ns, 0.3 ns and 0.32 for θ = 90° under the influence of Neon, Krypton and Xenon ions, respectively. Also, the time periods taken by the 40° angled device to settle back to steady state condition after that radiation reaches the peak values at V_{GT} = -0.2V are 0.83 ns, 0.92 ns, and 1.01 ns respectively when exposed to Neon, Krypton, and Xenon ions. These values are 0.92 ns, 1.05 ns, and 1.18 ns respectively for 90° angled devices. Again, the device with θ = 40° takes settling time of 0.82 ns, 0.85 ns and 0.93 ns respectively, under irradiance of Neon, Krypton and Xenon ions at V_{GT} = 0.3 V. However, these values change to 0.9 ns, 0.94 ns and 1.03 ns respectively for the device with θ = 90° under exposure to Neon, Krypton and Xenon ions at V_{GT} = 0.3 V. Also, all the devices show narrowed pulse and also take less time to move back to steady state when exposed to ions transferring lesser energy to the medium. These findings suggest that the smaller angled device having a shorter transient current pulse is weakly sensitive to radiation which clearly indicates that degradation in the performance due to radiation will be less in such a device under all gate bias conditions.

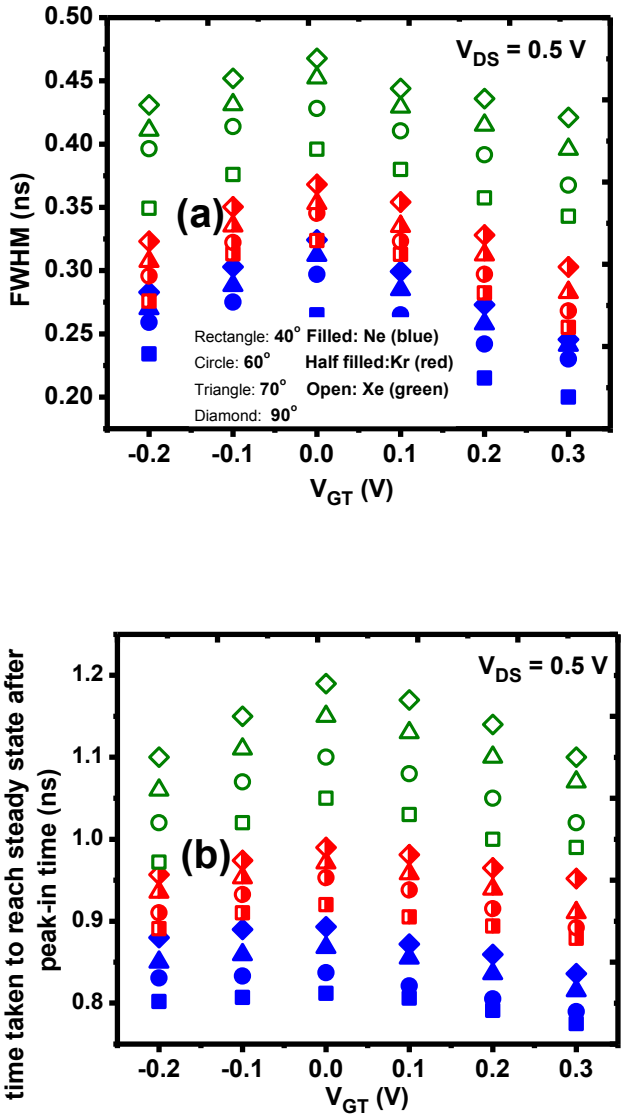


Fig. 5.9: (a) FWHM (b)Time taken to reach steady state after peak-in time with respect to V_{GT} at V_{DS} = 0.5 V for InAs quantum well n-MOSFET with t_{ch} = 5 nm, L_G = 14 nm. Filled symbols represent the influence of Neon, half-filled symbols represent the influence of Krypton, and open symbols represent the influence of Xenon. Rectangle, Circle, Triangle and diamond symbols are used to represent grooving angle of 40°, 60°, 70° and 90°, respectively.

5.5 Comparative analysis of the proposed device with other reported devices

In Table V, the author has provided a comparative analysis of the proposed device with other reported devices having comparable channel length [5.8, 5.23-5.24] in terms of charge collection efficiency due to radiation. From this table, it can be concluded that the proposed smaller groove angled and thinner channel device shows equivalent efficiency and thus can fairly withstand hostile environment.

Table V: Comparative analysis of the projected device with other reported MOSFET structures in terms of charge collection efficiency due to radiation:

Type of MOSFET with specifications	**Channel length (nm)**	**Incident ion**	**LET ($MeV.cm^2/mg$)**	**Charge collection efficiency**	**Ref**
InGaAs Quantum Well MOSFET L_{ch} =80 nm t_{ch}=8 nm V_{GS} = 0.0 V ,V_{DS} =0.5 V	80	Argon	9.28	0.44	[5.8]
SOI FINFET L_{ch} =14 nm t_{ch}=10 nm V_{DD}= 0.8V	14	-	5	1.33	[5.23]
Floating body PDSOI transistor L_{ch} =70 nm t_{ch}=11 nm V_{DD} =1V	70	Krypton	30	2	[5.24]
InAs Quantum Well MOSFET L_{ch} =14 nm t_{ch}=5 nm V_{GS} = 0V, V_{DS} =0.5 V θ = 40° (author's work)	**14**	**Neon, Krypton, Xenon**	**2.58 33.45 75.52**	**1.36 0.74 0.69**	[5.38]

5.6 Summary

Comparing all the radiation parameters of the devices in terms of angle of grooving and channel thickness, the device with θ = 40° and t_{ch} = 4 nm stands out as the better device during OFF conditions. However, from the previous study, the author has found out that the device with θ =

40° and t_{ch} = 5 nm to be the most improved one in device as well as circuit level performance. So, while making a comparison of the devices with t_{ch} = 4 nm with the one having t_{ch} = 5 nm, both having $\theta = 40^{\circ}$, it is found that though the less thickened channel device performs a little better than the thicker one under radiation during OFF condition, it's values of ON-current, transconductance and distortion minima are compromised with respect to the thicker one. It can be noted that the charge collection efficiency due to radiation during OFF condition is only higher by 1.9 % in the device with t_{ch} = 5 nm compared to the one with t_{ch} = 4 nm. With this little compromise, the author chooses to conclude that InAs channel quantum well n-MOSFET will show better results in terms of radiation resilience as well as device and circuit level performance by duly adjusting the angle of grooving at 40^{0} and maintaining a thin channel thickness of 5 nm.

REFERENCES

[5.1] V. Ramachandran, R. A. Reed, R. D. Schrimpf, D. McMorrow, J. Brad Boos, M. P. King, E. X. Zhang,G. Vizkelethy, X. Shen, and S. T. Pantelides, "Single-Event Transient Sensitivity of InAlSb/InAs/AlGaSb High Electron MobilityTransistors," *IEEE Transactions on Nuclear Science*,vol.59,pp.2691-2696,2012. https://doi.org/10.1109/TNS.2012.2223716

[5.2] M. Barth, H. Lieu, J. H. Warner, B. R. Bennett, J. B. Boos, D. McMorrow, N. Roche, P. Paillet, M. Gaillardin and S. Datta, "Single Event Measurement and Analysis of Antimony Based n-Channel Quantum-Well MOSFET With High- Dielectric," *IEEE Transactions on Nuclear Science*, vol.62, pp.2807-2814,2015..https://doi.org/10.1109/TNS.2015.2498905

[5.3] M. Barth, A. Kumar, J. H. Warner, B. R. Bennett, J. B. Boos, C. D. Cress, N.J.-H. Roche,M. Raine, M. Gaillardin, P. Paillet,D. McMorrow, K. Saraswat, and S. Datta, "Single-Event Measurement and Analysis of Antimony-Based p-Channel Quantum-Well MOSFETs with High-k Dielectric," *IEEE Transactions on Nuclear Science*, vol 64,pp.434-440,2017.https://doi.org/10.1109/TNS.2016.2637923

[5.4] V. Ferlet-Cavrois, P. Paillet, D. McMorrow, A. Torres, M. Gaillardin, J. S. Melinger, A. R. Knudson, A. B. Campbell, J. R. Schwank, G. Vizkelethy, M. R. Shaneyfelt, K. Hirose, O. Faynot, C. Jahan, and L. Tosti, "Direct Measurement of Transient Pulses Induced by Laser and Heavy Ion Irradiation in Deca-Nanometer Devices," *IEEE Transactions on Nuclear Science*,vol.52,pp.2104-2113,2005. https://doi.org/10.1109/TNS.2005.860682

[5.5] John Evan Turner, Atoms, Radiation, and Radiation Protection, third ed. WILEY-VCH Verlag GmbH & Co. KGaG, Germany.2007.

[5.6] D. McMorrow, J. Warner, S. DasGupta, V. Ramachandran, J. Brad Boos, R. Reed, R. Schrimpf, P. Paillet, V. Ferlet-Cavrois, J. Baggio, S.Buchner, F. El-Mamouni, M. Raine, and O. Duhame, "Novel Energy-Dependent Effects Revealed in GeV Heavy-Ion-Induced Transient Measurements of Antimony-Based III-V HEMTs, *" IEEE Transactions on Nuclear Science.* vol.57, pp.3358-3365,32010. https://doi.org/10.1109/TNS.2010.2086487

[5.7] T. R. Weatherford, W. T. Anderson, Jr., "Historical Perspective on Radiation Effects in III–V Devices," *IEEE Transactions on Nuclear Science*, vol.50, pp.704-710, 2003.https://doi.org/10.1109/TNS.2003.813124.

[5.8] K. Ni, "Single Event Transient And Total Ionizing Dose Effects On III-V

MOSFETs for SUB-10 nm Node CMOS," Ph.D. dissertation, Dept. Elect. Eng., Graduate School of Vanderbilt University, Nashville, Tennessee, 2016.

[5.9] A. Ionascut-Nedelcescu, C. Carlone , A. Houdayer , H.J. Von Bardeleben ,J.L. Cantin and S. Raymond, "Radiation hardness of gallium nitride," *IEEE Transactions on Nuclear Science*, vol.49,pp.2733-2738,2002. https://doi.org/10.1109/TNS.2002.8085363.

[5.10] S. Kuboyama, A. Maru, H. Shindou, N. Ikeda, T. Hirao, H. Abe ,and T. Tamura, "Single-Event Damages Caused by Heavy Ions Observed in AlGaN/GaN HEMTs," *IEEE Transactions on Nuclear Science*, vol. 58,pp.2734-2738,2011. https://doi.org/10.1109/TNS.2011.2171504

[5.11] V. Ramachandran, "Single-Event Mechanisms in InAlSb/InAs/AlGaSb High Electron Mobility Transistors," Ph.D. dissertation, Dept. Elect. Eng., Graduate School of Vanderbilt University, Nashville, Tennessee, 2013.

[5.12] G. Kaushal, S.S. Rathod, S. Maheswaram, S.K. Manhas, A.K. Saxena , and S. Dasgupta, "Radiation Effects in Si-NW GAA FET and CMOS Inverter: A TCAD Simulation Study, " *IEEE Trans. Electron Dev*, vol.59(2012)pp.1563-1566,2012.https://doi.org/10.1109/TED.2012.2187656

[5.13] K.H. Zaininger, and A.S. Waxman, "Radiation Resistance of Al_2O_3 MOS device," *IEEE Trans. Electron Dev*, vol. 16,1969.https://doi.org/10.1109/T-ED.1969.16753.

[5.14] A.Elwailly, J. Saltin, M. J. Gadlage and H. Y. Wong, "Radiation Hardness Study of L_G = 20 nm FinFET and Nanowire SRAM Through TCAD Simulation," *IEEE Trans. Electron Dev*, vol. 68 , pp.2289-2294, 2021. https://doi.org/10.1109/TED.2021.3067855.

[5.15] S.Yue , X. Zhang, Y. Zhao, L Liu, and H. Wang, "Modelling and simulation of

single-event effect in CMOS circuit," Journal of Semiconductors vol.36,2015. https://doi.org/10.1088/1674-4926/36/11/111002

[5.16] Y. Sun, R. Liu, Q. Huang, Z. Liu, T. Wang, Y. Shi, and X. Li, "Analysis of single-event effects in selected BOX-based FDSOI transistor and inverter," *Radiation Physics and Chemistry*, vol.186 ,2021.https://doi.org/10.1016/j.radphyschem.2021.109526

[5.17] M. Aneesh, S. Raghavendiran, P.Kr, and B. Boby, "An Analytical Model of Single-Event Transients in Double-Gate MOSFET for Circuit Simulation," *IEEE Transactions on Electron Devices*, vol.66, pp.3710-3717,2019. https://doi.org/10.1109/TED.2019.2926883.

[5.18] M. Zerarka, A. Patrick, B. Alain, M. Frederic, and D. Andre , "TCAD Simulation of the Single Event Effects in Normally-off GaN Transistors after Heavy Ion Radiation, " *IEEE Transactions on Nuclear Science,* vol. 64pp.2242-2249,2017. https://doi.org/ff10.1109/TNS.2017.2710629ff.

[5.19] A. Kerdpradist, A. Ruangphanit, W. Titiroongruang and R. Muanghlua, "The Effect of Gamma Irradiation on Threshold Voltage and Channel Mobility Degradation of NMOS," *International Electrical Engineering Congress (IEECON),* pp.1-4,2018.https:// doi: 10.1109/IEECON.2018.8712257.

[5.20] R. Harboe-Sorensen, "Test methods for single event upset/latch-up," *Radiation Physics and Chemistry*. vol.43, pp.165-174,1994.https://doi.org/10.1016/0969-806X(94)90209-7

[5.21] M. Aneesh, and B. Boby, "A physics-based analytical model for single-event transients in an InGaAs n-channel FinFET suitable for circuit simulations," *Journal of*

Computational Electronics, vol.22,pp.1-9,2022.https://doi.org/10.1007/s10825-022-01954-1

[5.22] C. Dimri, G.P. Nikhil, P.K. Mohanty , K.P. Pradhan , R. Agarwal , and S. Routray, "Investigating single event transients of advanced fin based devices for inclusion in ICs, " *Int. J. Electron. Commun. (AEÜ)* vol. 134153675,2021. https://doi.org/ 10.1016/j.aeue.2021.153675.

[5.23] B. Liu,C. Li, and M. Chen, "Investigation of Single Event Transient Induced by Process Variability in 14 nm High‐*k*/Metal Gate SOI FinFET Devices ,"*Silicon*. vol.15 pp.1317–1324,2023.https://doi.org/10.1007/s12633-022-02102-x

[5.24] D. McMorrow, V. Ferlet-Cavrois, P. Paillet, O. Duhamel, J. Baggio, J. Brad Boos, and J. S. Melinger, "Transient Response of Semiconductor Electronics to Ionizing Radiation. Recent Developments in Charge-Collection Measurement," *IEEE Transactions on Nuclear Science*, vol.54, pp.1010-1017,2007. https://doi.org/ 10.1109/TNS.2007.896345.

[5.25] Y. Zeng, S. Khandelwal, K..Shariar, Z. Wang, G. Lin, Q. Cheng, P. Cui, R. Opila, G. Balakrishnana, S. Addamane, P. Taheri, D. Kiriya, M. Hettick, and A. Javey, "InAs FinFETs Performance Enhancement by Superacid Surface Treatment, " *IEEE Transactions on Electron Devices*, vol. 66,pp.1856-1861,2019. https://doi.org/10.1109/TED.2019.2901281

[5.26] K. Sumita, K. Toprasertpong, M. Takenaka , and S. Takagi, "Proposal and Experimental Demonstration of Ultrathin-Body (111) InAs-On-Insulator nMOSFETs With L Valley Conduction," *IEEE Transactions on Electron Devices*, vol.68, pp.2003-2009,2021.https://doi.org/ 10.1109/TED.2021.3049455.

[5.27] P. Paramasivam, N. Gowthaman , V. M. Srivastava, “Design and Analysis of InP/InAs/AlGaAs Based Cylindrical Surrounding Double-Gate (CSDG) MOSFETs With La_2O_3 for 5-nm Technology,” *IEEE Access* vol.9 pp.159566-159576,2021.https://doi.org/10.1109/ACCESS.2021.3131094

[5.28] O. -P. Kilpi, J. Svensson, E. Lind, and L. -E. Wernersson, “Electrical Properties of Vertical InAs/InGaAsHeterostructure MOSFETs,” *JEDS* vol.7, pp.70 - 75,2019.https://doi.org/ 10.1109/JEDS.2018.2878659

[5.29] D.S. Yadav, D. Sharma, A. Kumar, D. Rathor, R. Agarwal, S. Tirkey,B.R. Raad, and V.Bajaj, “Performance investigation of hetero material(InAs/Si) based charge plasma TFET,” *Micro and Nano Lett*, vol.12,pp. 358-363,2017.https://doi.org/10.1049/mnl.2016.0688

[5.30] S.R. Mehrotra, M. Povolotskyi, D.C. Elias, T. Kubis, J.J.M. Law, M. J. W. Rodwell, and G. Klimeck, “Simulation Study of Thin-Body Ballistic n-MOSFETs Involving Transport in Mixed -L Valleys,” *IEEE Electron Dev. Lett*., vol.34,pp.1196-1198,2013. https://doi.org/ 10.1109/LED.2013.2273072

[5.31] I. Vurgaftman, J.R.Meyer, and L.R. Ram-Mohan, “Band parameters for III–V compound semiconductors and their alloys,” *J. Appl. Phys*, vol. 89,pp.5815-5875,2001. https://doi.org/10.1063/1.1368156.

[5.32] C.Rehnstedt, C. Thelander, C., L.E. Froberg, B.J. Ohlsson, L. Sameulson , and L.E. Wernersson, “Drive current and threshold voltage control in vertical InAs wrap-gate transistors,” *Electronics Lett.* vol. 44, pp.236-238,2008. https://doi.org/10.1049/el:20083188.

[5.33] A.C. Ford , J.C. Ho, T.Y. Chueh , Z. Fan, J. Guo, J. Bokor, and A. Javey,

"Diameter-Dependent Electron Mobility of InAs Nanowires," *Nano Lett*, vol.9 pp.360−365,2009. https://doi.org/10.1021/nl803154m

[5.34] G.Sujatha, N. Mohankumar,R. Poornachandran, R. Saravana, G.S. Mishra, V. Mahesh, and M. Arun kumar, "Noise Characterization of InAs Based Composite Channel DG-MOSHEMT with Different Gate Dielectrics," *Silicon* , vol.14pp.1925–1933,2022.https://doi.org/10.1007/s12633-021-00954-3

[5.35] F.F. Komarov, O.V. Milchanin, I.N. Parkhomenko, L.A. Vlasukova, N.S. Nechaev, V.A. Skuratov, and V.N. Yuvchenko, " Influence of the Irradiation with High-Energy Xe Ions on the Structure and Photoluminescence of Silicon and Silica with InAsNanoclusters," *Journal of Engineering Physics and Thermophysics,* vol.92, pp.508–515,2019. https://doi.org/10.1007/s10891-019-01958-y

[5.36] J. H. Warner, D. McMorrow, S. Buchner, and J.B. Boos, " Proton-Induced Transient Charge Collection in GaAs and InAlSb/InAs-Based FETs," *IEEE Transactions on NuclearScience.* vol.60, pp.2651-2659,2013. https://doi: 10.1109/TNS.2013.2261091.

[5.37] R. Wang, H. Guo, J. Tang, J. Liu, J. Liu, and L. Liu, "The Radiation Hardness of Quantum-Dot Embedded in High-Electron Mobility Transistor Force-Sensitive Structure," *IEEE Sensors Journal*, vol. 21,pp.22853-22857,2021.https:// doi: 10.1109/JSEN.2021.3107859.

[5.38] S. Dasgupta, C. Mondal and A.Biswas, "Radiation Resilience and Performance Analysis of InAs Quantum Well n-MOSFETs with Varied Groove Angles," communicated

[5.39] S. Dasgupta, C. Mondal and A.Biswas, "Impact of channel thickness on Single-Event Transient in InAs Quantum Well n-MOSFETs," in Proceedings of

Calcutta Conference (Calcon), pp.71-74,2022. ISBN: 978-1-6654-6241-9

[5.40] S. Lee, C.-Y. Huang, D.C. Elias, B.J. Thibeault, W. Mitchell, V. Chobpattana, S. Stemmer, A.C. Ossard, and M.J.W. Rodwell, "Highly scalable raised source/drain InAs quantum well MOSFETs exhibiting I_{ON} = 482μA/μm at I_{OFF}=100 nA/μm and VDD=0.5 V,"*IEEE Electron Device Lett*., vol.35,pp.621-23,2014. https://doi.org/ 10.1109/LED.2014.2317146.

[5.41] ATLAS users' manual: device simulation software' (Silvaco Int., Santa Clara, CA, USA, 2014), available at http://www.silvaco.com

[5.42] T. Dutta, S. Kumar, P. Rastogi, A. Agarwal, Y.S. Chauhan,Impact of channel thickness variation on bandstructure and source-to-drain tunneling in ultra-thin body III-V MOSFET, JEDS ,vol.4,pp.66-71,2016. https://doi.org/10.1109/JEDS.2016.2522981

Chapter-6

Conclusion

Investigations on InAs-on-insulator (InAsOI) devices suggest that InAsOI devices can become more effective for analog/RF circuit applications largely due to the enhanced electron mobility in InAs channel combined with better electrostatic integrity in thin-body architecture. All the device parameters except output conductance show improvement in InAsOI devices as compared to the corresponding parameters in Silicon-on–insulator (SOI) devices. But, on studying InAs based quantum well structure with raised source/drain architecture, it is found that the quantum well structure outperforms on-insulator structure in terms of subthreshold slope and peak value of transconductance by 1.09 times and 3.4 times respectively and also displays less distortions. This makes the quantum well structure to be more effective in the various fields of applications.

From the detailed study which includes physical analysis and also comparative survey of varied structures, the author would like to conclude to opt for InAs based quantum well n-MOSFET with raised source/drain architecture having channel thickness of 5 nm and angle of grooving of 40^0 as the optimised device to find applications in low power analog circuits. This proposed device exhibits delay of 60.5 ps, ON-OFF ratio of 345 with peak g_m of 3.8 mS/μm and peak voltage gain of 4.5.Also, this device shows better DC to AC conversion efficiency with lowest value of distortion compared to other devices. At the transconductance generation factor of 5 V^{-1}, this device shows distortion of -32 dB which is lowest among the other reported SOI structures.Moreover, this device also turns to be more radiation tolerant when subjected to harsh environment. The author has studied the radiation resilience of the said device by making Neon, Krypton and Xenon ions to be incident upon it. On comparing with other reported structures, it is

found that the proposed device exhibits lower charge collection efficiency which proves its ability to withstand hostile environment. Also, for the development of III-V CMOS technology, the author would like to opt for InGaSb based quantum well p-MOSFET with raised source/drain architecture having channel thickness of 5 nm and angle of grooving of 40^0 as the optimised device having OFF current of 0.39 µA/µm and peak voltage gain of 5.4. Also, to keep pace with the development of data science technology, the obtained simulated data of III-V MOSFETs can be used in the development of various predictive models.

Sunetra Dasgupta
9/11/23