THREE PHASE CONVERTER SYSTEMS FOR ELECTRICAL MACHINES WITH SERIES CONNECTED DC BUS

Thesis submitted by

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This is to certify that the thesis entitled "**Three Phase Converter Systems for Electrical Machines with Series Connected DC Bus**" submitted by **Sri Dipten Maiti**, who got his name registered on **27th September, 2016** for the award of Ph.D. (Engineering) degree of Jadavpur University is absolutely based upon his own work under the supervision of me, **Prof. Sujit K. Biswas**, Former Professor, Electrical Engineering Department, Jadavpur University and that neither his thesis nor any part of the thesis has been submitted for any degree/diploma or any other academic award anywhere before.

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ABSTRACT

With the advancement in electrical technology, the transmission voltage level is being increased gradually. Usually, the AC voltage generated by conventional generating system is stepped up for transmission and then stepped down for usage at different level. However, power electronic interfaces and renewable energy generation systems have brought a shift in this, although the fundamental idea remains same. The voltage level is still increased for transmission. However, for renewable energy systems which usually are interfaced by power electronic converter for maximum power extraction requires power electronic solution for this voltage stepping up. The solution should be compact, efficient and low cost. Similar is the case for stepping down of the voltage. Thus the power frequency transformer is being replaced by solid state transformers. Multilevel inverters are used for interfacing high DC bus voltage. This reduces the semiconductor breakdown voltage requirement also. The output AC of the inverter is controlled by modulation index of the inverter.

Problem arises when a low voltage AC motor is driven from a higher voltage DC bus. Multilevel inverter being almost a default choice can be utilized with a low modulation index. However, the resulting speed control can become coarse. Besides, the dv/dt may become high for the AC machine winding when the inverter frequency becomes higher. Thus DC to AC better matching inverter is essential.

An inverter topology in this direction is proposed and investigated in this work. The DC bus voltage is divided into several smaller parts by capacitive voltage divider, each with its own inverter feeding one phase of the open end winding AC machine. The scheme thus divides the total DC bus into 1/3 and thus results in better voltage matching between the DC and AC sides.

The voltage divider created by capacitors when are loaded can have a unbalance in the voltages. However, present work shows that reasonable balance in the voltage will be maintained inherently by the operation of the motor drive system.

There is chance of zero sequence current due to the open end winding motor and inverter connection. Thus suitable switching strategy should be employed to restrict this

current. This work also investigated in this direction. Using a zero sequence current loop the zero sequence current is kept nearly zero in this work.

Generation of a higher voltage from a low voltage renewable energy generation is a popular topic to the researchers. For wind energy generation, usually offshore ones, requires long cable for transmission, thus higher voltage is more preferred in this case.

Present work proposes a rectifier system for generating higher voltage from a lower voltage generator. The voltage that can be generated is higher than the convention three limb three-phase rectifier with similar voltage boost rating. The extra voltage gain achieved by series connection of the rectifier outputs.

Once again there would be voltage balancing and zero sequence current issues here. These issues are also investigated and mitigating steps are proposed.

Both topologies are simulated on MATLAB SIMULINK tool and then validated experimentally. The voltage balancing, zero sequence current issues are shown and mitigated in software platform as well as hardware implementation.

ACKNOWLEDGEMENT

As I am on the course of putting the final touch to the thesis, I would like to acknowledge the support and inputs from several people, without which, I would not have reached this far. It is difficult to name them all and thanking them would trivialize their support. Still, I must try this for the sake of my own self.

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I would like to thank ***Mr. Pravat Chandra*** for his support, suggestion, and assistance during the fabrication of the experimental set-up. I am thankful to all faculties and staff especially, *Dipankar Naskar, Jayanta Bhattacharya, and Indrajit Naskar* of the Machines and Drives Laboratory of the Electrical Engineering Department for their assistance.

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Last but not least, the moral support and sacrifice of my parents, my wife, parent-in-laws motivated me to work harder for the realization of the thesis. During the difficult time of the Covid-related lockdown and the helplessness due to the stagnancy of my research work, they all stood by me through thick and thin. My daughter sacrificed her time with her father. I feel indebted to her also.

September, 2023
Jadavpur University, Dipten Maiti
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Contents

List of Figures

List of Tables

List of Abbreviations

HVAC	High Voltage Alternating Current
HVDC	High Voltage Direct Current
SCR	Silicon Controlled Rectifier
THD	Total Harmonic Distortion
VSI	Voltage Source Inverter
VFD	Variable Frequency Drive
NPC	Neutral Point Clamp
EMI	Electromagnetic Interference
IM	Induction motor
PMSM	Permanent Magnet Synchronous Motor
FOC	Field Oriented Control
PWM	Pulse Width Modulation
SPWM	Sinusoidal Pulse Width Modulation
SVPWM	Space Vector PWM
GTO	Gate Turn Off Thysristor
OEIM	open end winding induction motor
RMS	Root Mean Square
OE-PMSG	Open end winding Permanent Magnet Synchronous Generator
PMSG	Permanent Magnet Synchronous Generator
MMC	Modular Multilevel Converter
ISOP	input-series-output-parallel
IPOS	input-parallel-output-series
IPOP	Input-parallel-output-parallel
ISOS	input-series-output-series
CSI	Current Source Inverters
SST	Solid State Transformer
DAB	Dual Active Bridge
ANPC	Active NPC
DF	Displacement Factor
df	distortion factor
DOL	Direct On Line
DAC	Digital to Analog Converter

Chapter 1

Review of Topologies and Switching Schemes

1.1. Introduction

Higher voltage level is popular for the transmission of bulk power [1]. Both High Voltage AC (HVAC) and High Voltage DC (HVDC) transmission systems are used depending upon the requirement, the voltage level of HVDC usually being higher than that of HVAC. Thus, on the generation side a lower voltage is stepped up by using different methods to a suitable higher voltage; on the consumer end the higher voltage is stepped down to a suitable lower voltage level. On the generation end this stepping up has become more important with the availability of lower voltage renewable energy sources. With the availability of high-speed semiconductor devices, the importance has shifted towards more compact, more efficient converters.

The type of AC to DC converter, called rectifier fundamentally consists of diode or Silicon Controlled Rectifier (SCR) bridges for a single phase system [2, 3]. The diode bridge rectifier is an uncontrolled one without any control over the rectified DC output voltage by the converter; while SCR based system has the capability of controlling the output DC voltage by controlling the firing angles of the SCRs. Both diode bridge based rectifier and SCR based rectifier draws non-sinusoidal current from the AC source, causing several detrimental issues on the power supply system as a whole [2, 3].

If the diode or SCRs are replaced by force-commutable semiconductor switches and the on-time period of the switches are pulse width modulated at a suitable frequency, current with low Total Harmonic Distortion (THD) can be drawn from the AC source by the converter. The single phase structure consisting of four switches distributed in two legs is as shown in fig. 1.1(a) is also called PWM rectifier. Operated from a single phase AC source this rectifier generates an output voltage greater than the peak of the applied AC voltage. For the operation of this rectifier, an inductor needs to be connected at the AC input. The three phase structure consisting of three

limbs each with two switches is shown in fig. 1.1(b). Here inductors need to be connected in each phase.

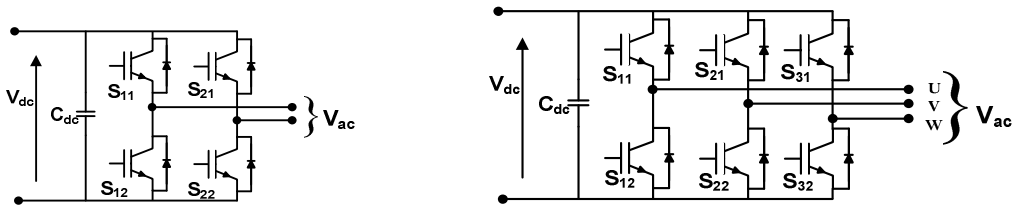

Fig. 1.1: (a) A single phase AC↔DC Converter (b) A Three phase AC↔DC Converter

A similar structure can be used for DC to AC conversion or inversion. The DC voltage at the input can be connected to the AC output through suitable switches. With proper switches turned on, the output voltage may be positive or negative. Thus generation of both polarity of the voltage is possible. If the output voltage is to be made free of higher harmonics, a low pass filter may be used. Thus, with a DC source, a suitable switch operation scheme, fig. 1.1(a) becomes a single phase Voltage Source Inverter (VSI) and fig. 1.1(b), a three phase three wire voltage source inverter. For three phase inverter or rectifier the three phase voltage and three phase currents remain 120° displaced from each other.

Two switches connected in series with the emitter of one switch connected to the collector of the other switch, is called a leg/limb of the converter and the common point, that is the connection of the emitter of the top switch and collector of the bottom switch is called the pole. Two legs as combined in fig.1.1(a) is called a full bridge or H-bridge configuration and thus one leg forming half a bridge is called a half-bridge. Three or four legs are there for a three phase converter. A single phase inverter can drive a single-phase AC motor while a three phase inverter can drive a three phase motor in Variable Frequency Drive (VFD) mode with control in both voltage as well as the fundamental frequency. Thus a smooth speed or precise position control is possible with AC motors also.

When the upper switch of leg-1, S_{11} and bottom switch of leg-2, S_{22} is turned on, the voltage across the AC side is $+V_{dc}$, when the upper switch of leg-2, S_{21} and bottom switch of leg-1, S_{12} are turned on, the voltage across the AC terminals or between the poles is $-V_{dc}$. When upper switches of both the limbs or lower switches of both the limbs are turned on voltage across the load is zero. It should be mentioned that once a switch is turned on in a leg, the other switch

must be turned off; otherwise, a short circuit across a voltage source may arise resulting in a catastrophe. Besides, because of the non-zero time required for turning on and off of a switch, some delay must be incorporated between the turn off of a switch of a leg and the turn on of a switch of the same leg. This time difference is called dead-time, when both switched of a leg remain turned off.

When one switch of a leg is tuned on the voltage appearing across the other switch is V_{dc}. Thus the switch must be capable of withstanding this voltage. If suitable switches cannot be found to withstand the voltage, a suitable number of switches can be connected in series with proper voltage balancing, to withstand the higher voltage.

Thus, the pole voltage can have values of $+V_{dc}$, 0 and $-V_{dc}$. When applied across a load, this will give rise to a rate of change of the voltage or dv/dt. Even in the absence of a conducting path for the pole voltage, this dv/dt may cause current in the associated equivalent capacitance. The dv/dt can be high if the magnitude of voltage change or the DC bus voltage is high or the switching frequency is high. The latter issue indirectly restricts the operating frequency of the switches. The dv/dt issue can be mitigated by using a multilevel converter as the most popular solution.

1.2. Converter structures for high voltage operation

High voltage withstand capability can be incorporated into the 2-level converter structures, those shown in fig. 1.1, by series connection of the switches. The series-connected switches require voltage balancing schemes. Besides, the dissimilar turn-on and turn-off time of the switches is to be taken care of. With a multilevel converter structure, these issues could be mitigated. Moreover, the multilevel schemes provide advantages in number of voltage levels generated on the AC side, thus reducing the harmonics in the AC voltage/current and in the size of the low pass AC filter required, along with other significant advantages.

The first multilevel inverter structure was proposed in a 1975 patent utilizing several cascaded H-bridges with their own DC sources, to generate a multi-stepped AC output voltage waveform [4]. Nabae et al proposed the first three level inverter structure, now called Neutral Point Clamped (NPC) multilevel inverter [5]. Diodes were used for connecting to the artificially formed DC bus midpoint, thus it is also called diode clamped multilevel inverter. Here two capacitor banks of similar values are used to form the mid-point of the DC source. Thus the

voltage across each capacitor bank is $V_{dc}/2$. Using diodes this midpoint is connected to suitable terminals of a four-switch leg as shown in fig 1.2(a). Normally the switches here are operated in a complementary manner, such that when S_{11} is on, S_{13} is held turned off and when S_{12} is on S_{14} is kept turned off and vice versa. Thus, by turning on S_{11} and S_{12} both, the pole voltage becomes $V_{dc}/2$, with S_{12} turned on pole voltage is 0, and with S_{11} and S_{12} both turned off pole voltage is $-V_{dc}/2$. Thus, the voltage change in achievable in each level is $V_{dc}/2$, which for the same dt gives rise to half dv/dt compared to a full bridge system. Even for the same output current, this reduces the switching loss also.

The blocking voltage requirement of the switches in this case is $V_{dc}/2$, half compared to a full bridge converter. Thus, switches with lower voltage ratings can be used for a DC bus with higher voltage. This also results in lower THD in the output voltage when a suitable high switching frequency is used. Besides, due to less dv/dt Electromagnetic Interference (EMI) problem reduces.

Depending on the requirement of total DC bus voltage and availability of switching devices the number of levels can be increased, using further division of the total DC bus voltage. Several converter structures emerged for proposing further development, say, to minimize the number of switches, to increase DC bus utilization, simplify the voltage balancing mechanism, so on.

Another popular modification of the NPC inverter structure shown in fig 1.2(b) is called the flying capacitor multilevel inverter [6] [7]. Several floating capacitors are connected as shown here. Compared to the NPC inverter this topology does not require the clamping diodes, thereby the loss in the diode can be reduced. Further, the redundant switching states can be used to maintain voltages across the flying capacitors C_A, C_B, C_C. In this structure shown, the flying capacitors remain charged at half the DC bus voltage and the capacitor voltage can be added or subtracted from the DC bus voltage creating a number of levels in the output AC voltage.

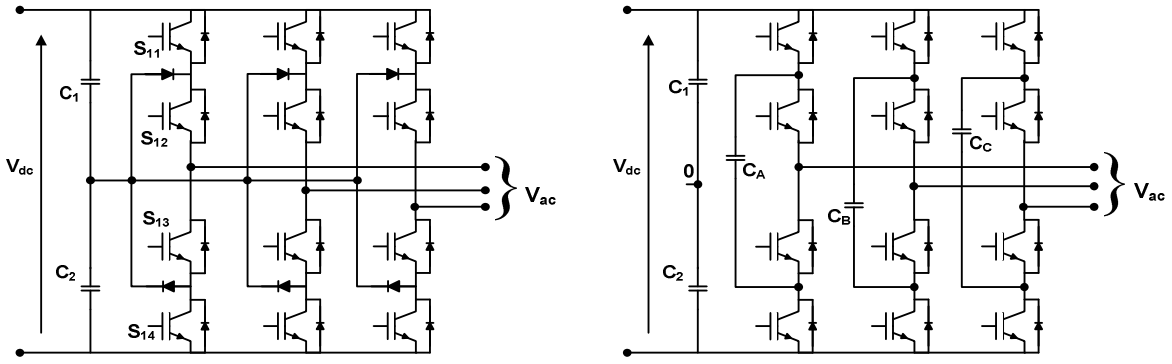

Fig. 1.2: (a) Neutral Point Clamped AC↔DC Converter (b) Flying Capacitor AC↔DC Converter

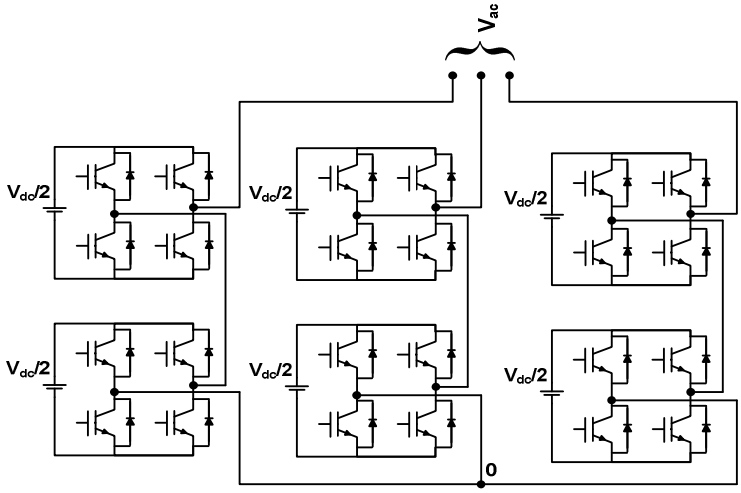

Fig. 1.3: H-bridge AC↔DC Converter

H-bridge multilevel inverter structure shown in fig. 1.3 uses cascaded H-bridge inverters to form a resultant multilevel inverter. Here each H-bridge has its own DC source, requiring several isolated DC sources [8]. Although the structure requires several switches and isolated DC sources, the structure is simple and does not require complex switching for capacitor voltage balancing as in the case of flying capacitor inverter or extra diodes as in NPC inverter.

The converter structures are popularly used for interfacing AC/DC machines. When used as an inverter to drive suitable AC machines, they are popularly used as VFD, resulting in speed control performance similar to DC motors. This drive scheme is used to drive three-phase Induction motor (IM) and Permanent Magnet Synchronous Motor (PMSM) to name a few, in Field Oriented Control (FOC) mode emulating the non-interfering control of the flux and armature current of a DC motor. Similarly, when used as a rectifier these converters can convert

AC voltage to suitable DC. The rectifier can be used to rectify as when as provide voltage gain when connected to the output of an AC generator.

1.3. Pulse Width Modulation (PWM) Schemes

The switches in any inverter structure are to be controlled in such a way, as to generate the required AC waveform out of the DC source. As the well known bulk power AC motors are mostly driven by sinusoidal AC waveforms for current or voltage, the inverters are usually used to generate sinusoidal AC waveforms. The PWM scheme used for modulating the turn-on time of any switch in a leg of the inverter is required to produce a fundamental AC waveform of a particular amplitude and frequency. With the advent of high speed power semiconductor switches and digital signal processors, the PWM can be performed at a much faster rate. In general, a PWM scheme for an inverter needs to fulfill non-exhaustive requirements such as, a good range of linear modulation, low harmonic content or THD, reduced lower harmonics, the minimum number of pole voltage transitions and simple implementation, etc [2, 3, 9].

For a single phase 2-level inverter, the most popular PWM scheme is called the Sinusoidal Pulse Width Modulation (SPWM) scheme. This is based on the comparison of a sine wave of required phase, frequency and amplitude with a triangular wave determining the switching frequency as shown in fig. 1.4. Here, one sinewave (say the blue one) is used for generating the switching pulses, the diagonal switches of a single phase H-bridge inverter are turned on and off simultaneously. This operation is called bipolar switching as the output voltage has both positive and negative voltage values in a switching cycle. When two sinewaves, one, the reference sinewave (say the blue one) and another, a of 180 deg phase shifted version (the red one) of the reference sinewave are used for PWM, the operation will be called unipolar SPWM as the inverter output voltage for a half cycle of a reference sinewave remain in the same polarity. The triangular pulse used for comparison is called the carrier waveform, which dictates the switching frequency. For unipolar SPWM the switching frequency harmonics has frequency double that of bipolar SPWM.

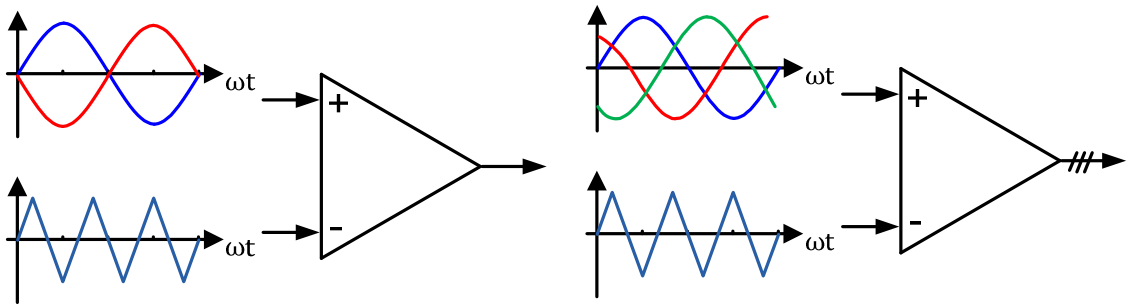

Fig. 1.4: (a) Carrier based Sinusoidal Pulse Width Modulation scheme for 1-phase converter (b) Carrier based Sinusoidal Pulse Width Modulation scheme for 3-phase converter

For a three phase inverter as the three legs of the inverter need to generate 120° phase shifted waveforms, three sinewave references of 120° phase apart are compared with the same carrier waveform to generate the SPWM switching pattern.

The modulation index for SPWM switching is defined as the ratio of the amplitude of the sinewave to the amplitude of the carrier wave, i.e.

$$m = \frac{V_{sine}}{V_{triangle}} \tag{1.1}$$

The amplitude of the output voltage for a two level inverter is given by

$$V_{out\_ac} = m \times V_{dc} \tag{1.2}$$

Thus, the modulation index determines the output amplitude.

Linear modulation range is for $0 \leq m \leq 1$; for $m > 1$ the operation is called overmodulation. Usually, overmodulation is avoided except in special cases as it results into the generation of lower harmonics, although the output voltage is higher. For multilevel inverters shifted carriers are used for SPWM or carrier based switching.

For three phase inverter Space Vector PWM (SVPWM) is more popular as it generates less THD with minimum switch transition in a switching cycle. The space vector is the extended idea of the rotating flux vector of a balanced three phase machine. When a three phase machine with its three windings placed 120° apart in space is supplied by currents 120° apart in time, a rotating magnetic field is created. Thus, a fictitious voltage vector can be imagined to have been

created when three such voltages are combined with 120° phase angle difference. A voltage space vector is defined as [9, 10, 11]:

$$\vec{v_s}(t) = v_a(t)e^{j0} + v_b(t)e^{j2\pi/3} + v_c(t)e^{j4\pi/3} \tag{1.3}$$

where, v_a, v_b, v_c are the instantaneous voltages applied to a, b, c phase windings. The windings should be mechanically apart in space by 120° electrical angle.

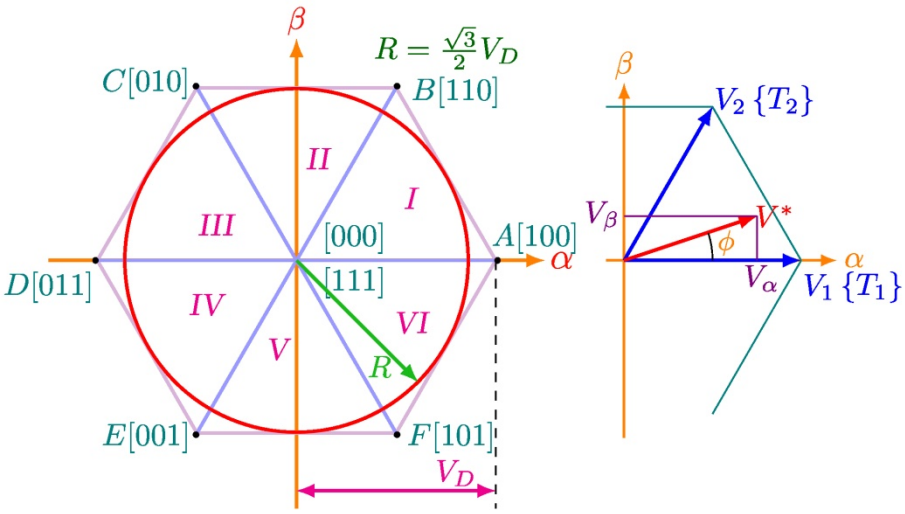

Fig. 1.5 (a) Space Vector PWM (SVPWM) for a two level 3-phase converter (b) Duty Ratio Calculation for SVPWM

As there is a limited number of switches in an inverter, namely six for a three phase inverter, the average voltage in a switching cycle is considered the output of the inverter. Thus, considering all possible switching combinations, i.e. 2^3 = 8 possible combination for six switches, eight possible voltage vectors can be generated when switches are fully on for a full cycle. The voltage vectors so generated, when put together with their magnitude and direction form a hexagon shown in fig. 1.5(a) with each vertex representing the of the vector in α-β voltage plane. Here, the part in the third bracket shows the switching states of the upper switches in each limb in order of UVW phases, with '1' representing an on switch while '0' representing an off switch. It should be mentioned that if the upper switch in a leg is on, the bottom switch of the same leg must remain off. The active vectors producing a non-zero voltage, represented by ABCDEF in the fig. 1.5(a) divides the hexagon into six smaller triangular regions, called sectors. The sectors are represented by sector numbers I to VI. The vector with switch states [000] and

[111] i.e. all bottom switches on or all top switches on do not produce any resultant voltage at the output. They are called null vectors and are thus shown at the origin of the space vector diagram. This figure also shows the limit of traversal of the voltage vector. In the linear modulation range, the tip of the voltage vector forms a uniform circle shown in fig 1.5(a). Thus any vector less than this value can be generated by the PWM of the switches where the modulation index is ≤1.

The on-time of a switch for SVPWM can be calculated using the voltage averaging principle as shown in fig. 1.5(b). Thus, a reference vector V* being applied for the whole switching duration is equivalent to V_1 and V_2 vectors being applied for T_1 and T_2 duration respectively. Thus, it can be written for α-β axis:

$$\begin{aligned} T_s V^* \cos\phi &= T_1 V_1 \cos(\theta_1) + T_2 V_2 \cos(\theta_2) \\ T_s V^* \sin\phi &= T_1 V_1 \sin(\theta_1) + T_2 V_2 \sin(\theta_2) \end{aligned} \tag{1.4}$$

Where, $|V_1| = |V_2| = V_{DC}$, θ_1 and θ_2 are the angle of V_1 and V_2 with α-axis respectively. In the case sector I, $\theta_1 = 0°$, $\theta_2 = 60°$. Thus, for sector-I :

$$\frac{T_1}{T_s} = \frac{V_\alpha}{V_{DC}} - \frac{1}{\sqrt{3}}\frac{V_\beta}{V_{DC}}; \frac{T_2}{T_s} = \frac{2}{\sqrt{3}}\frac{V_\beta}{V_{DC}} \tag{1.5}$$

where, $V_\alpha = V^* \cos\varphi$ and $V_\beta = V^* \sin\varphi$. In case the reference vector resides within the hexagon, $T_1 + T_2 \le T_s$.

Thus, for the rest of the duration i.e. $T_s - (T_1 + T_2)$, null or zero vectors will be applied with [000] and [111] being applied evenly such that there are a minimum number if switching in one switching cycle.

The switching pattern is arranged to apply the vectors in sequence, $V_z \rightarrow V_1 \rightarrow V_2 \rightarrow V_z \rightarrow V_2 \rightarrow V_2 \rightarrow V_z$ or reverse, according to the required direction of rotation with time $T_z/4 \rightarrow T_1/2 \rightarrow T_2/2 \rightarrow T_z/2 \rightarrow T_2/2 \rightarrow T_1/2 \rightarrow T_z/4$ respectively. The dwell time for other sectors can be calculated accordingly. Works have been done to relate carrier base PWM and SVPWM and thus, SVPWM can be generated even without going into the sector determination issues.

The per phase Root Mean Square (RMS) voltage generated by SVPWM switching is given by:

$$V_{rms-phase} = \frac{2}{3}R = \frac{2}{3}\frac{\sqrt{3}}{2\sqrt{2}}V_D = \frac{V_D}{\sqrt{6}} \approx 0.408\mathrm{V_D} \quad (1.6)$$

Here, R is the radius of the circle shown in fig 1.5(a), denoting the boundary of the linear modulation range.

In SPWM, the per-phase voltage that can be generated is given by:

$$V_{rms-phase} = \frac{1}{\sqrt{2}}\frac{V_D}{2} \approx 0.3535\mathrm{V_D} \quad (1.7)$$

Thus, for the same DC bus, the AC voltage generated can be around 15.5% higher.

For multilevel inverter as the number of switches increase, the number of vectors that can be generated by full on/off of the switches increases. For a three-level NPC inverter, as each leg can have three switching states, the total voltage vector that can be generated are $3^3 = 27$. Out of this total 18 are non-null vectors, rest are null vectors, as shown in fig 1.6. In the case of multilevel inverters, null vectors can be utilized for capacitor voltage balancing.

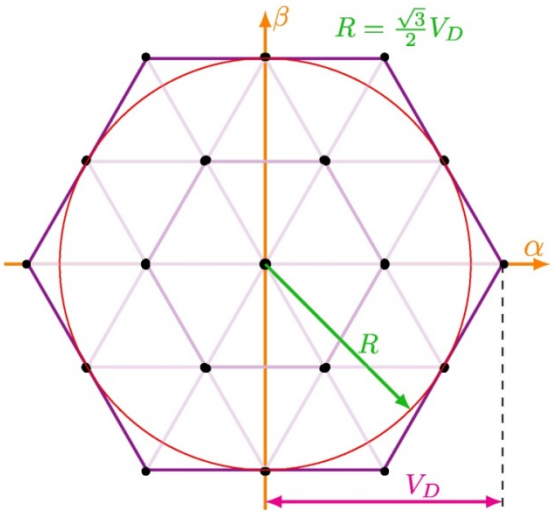

Fig. 1.6: Space Vector PWM (SVPWM) for a three-level 3-phase converter

1.4. Developments in Open-End Winding Machine

The idea that, an induction motor winding be opened and two sides of each winding be fed from separate inverters was shown to have various advantages. Stemmler et al. first proposed

the open-end winding motor drive configuration for enhancing the maximum power and speed of the Gate Turn Off Thysristor (GTO) based inverter system [12]. Both isolated and non-isolated DC bus systems were discussed. The non-isolated DC bus system employed zero sequence chokes to limit zero sequence current. Another early study on the performance characterization of open-end winding induction motor (OEIM) drive system was published by Corzine et al. [13]. The authors modified the DC bus voltages of the two inverters, to find that the structure can work as two, three, four-level inverters. The open-end inverter for an-open end winding AC machine is easier to construct using three phase inverter modules, compared to NPC inverters, which require clamping diode connections. The capacitor voltage balancing issue of the NPC or flying capacitor inverter was not present here.

Fig. 1.7 shows one such structure with two two-level inverters feeding an open-end winding AC machine from both sides. Although two-level inverters are used on both sides, the resultant voltage across the machine winding becomes equivalent to that supplied by a three-level inverter. Besides, for the same RMS voltage across the AC machine winding, the DC bus voltage required for the two inverter becomes half that of a single three level inverter. Another major advantage is the absence of neutral point fluctuation of the AC machine. Multilevel inverter structures as discussed earlier can be used in place of the two-level inverter, increasing the voltage levels across the AC machine windings.

If the two-level inverters feeding the open-end winding machine are fed by two isolated DC sources, as shown in fig. 1.7, the zero sequence current becomes zero inherently. The zero sequence current is defined as :

$$i_z(t) = \left[i_a(t) + i_b(t) + i_c(t) \right] \div 3 \qquad (1.8)$$

Where, i_a, i_b, i_c are the three phase currents.

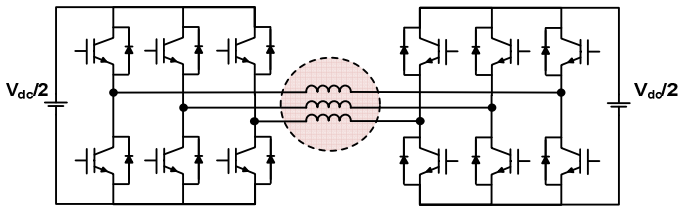

Fig. 1.7: Open end winding machine with AC↔DC Converter fed by two level converters with isolated DC buses

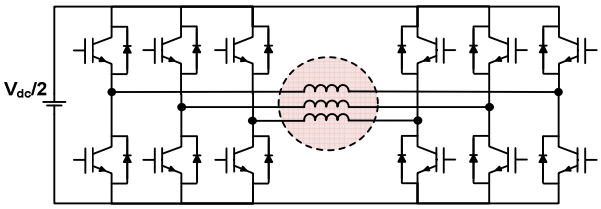

Fig. 1.8: Open end winding machine with AC↔DC Converter fed by two level converters with same DC bus

In the absence of the two isolated DC voltage sources, the DC bus of the two-level inverters can be connected, thereby both inverters being fed from the same DC source. All advantages of the open-end winding scheme would be present in this case, except the zero sequence current. In the case of the inverters fed from the same source, there exists a path for the zero sequence current [9-10]. As the zero current causes a stationary flux, the back emf or the induced voltage due to this flux is zero. Thus, in the presence of a zero sequence voltage, the zero sequence current is limited only by the zero sequence impedance of the AC machine. The zero sequence impedance of a machine is usually low, thus there is a chance of high zero sequence current due to a low zero sequence voltage. Besides this causes power loss and torque pulsation, hampering the life of the AC machine. Thus suitable switching scheme should be employed to restrict the zero sequence current in this scheme.

All these inverter topologies when looked at from the output to the input side become rectifiers due to the presence of bidirectional switches. Thus, the rectifiers would be able to generate and withstand higher DC bus voltage. Although, the topologies are similar and similar switch control methods can be employed, interesting developments on this topic happened in the name of multi-level converters [14].

For the structure shown in fig. 1.7, with open-end winding configuration and interfaced by two number two level converters with isolated DC buses, the SVPWM switching states are similar to a three level converter. This is because the structure in fig 1.7 also results in a three-level converter, although the constituent converters are two-level. Besides, the voltage magnitude of each bus for equivalent voltage on the AC side is half that in the three-level structure.

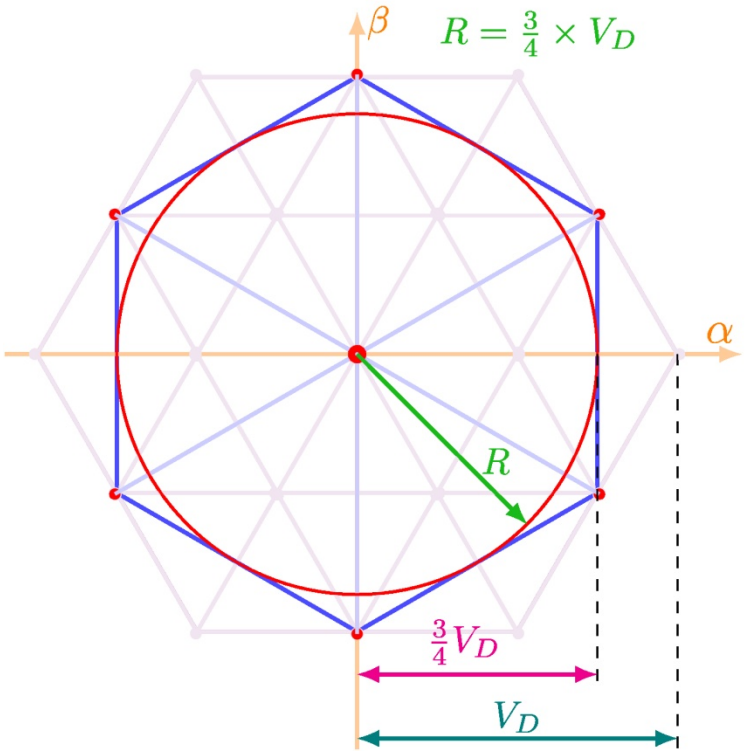

Fig. 1.9: Space Vector PWM (SVPWM) for a three-level 3-phase converter without any zero sequence voltage generating states

If the isolated voltage buses are connected, as in fig 1.8, the zero-sequence voltage generating states are to be removed from the applicable voltage space vectors to nullify zero sequence current. Thus, the space vector diagram results in the one shown in fig. 1.9. As shown in this diagram, the resultant voltage magnitude reduces, along with a number of achievable states. The red circle shows the boundary of linear modulation in this case.

In this case the per phase rms voltage is:

$$V_{rms-phase} = \frac{2}{3}R = \frac{2}{3}\frac{3}{4\sqrt{2}}V_D = \frac{V_D}{2\sqrt{2}} \approx 0.3535\mathrm{V_D} \tag{1.9}$$

which is the same as the voltage generated by SPWM switching scheme. Thus, for the structure shown in fig 1.8, SPWM switching can be performed to have similar voltage modulation, although SVPWM provides definitive minimum switching in a cycle.

Baranwal et al. proposed carrier based SVPWM switching scheme for zero common mode voltage [15]. The maximum voltage for a given DC bus voltage is that given by eq (1.9).

Carrier based SVPWM implementation does not require sector identification, thereby, reducing the processing time.

Open end winding Permanent Magnet Synchronous Generators (OE-PMSG) are studied for generating higher voltage. Each OE-PMSG feeds a diode bridge rectifier. The voltage of each such rectified winding voltage is boosted by boost converters the output of such boost converter is further converted to AC by single phase inverter. The outputs of the single phase inverters are connected in series to generate higher AC voltage [16]. This scheme thus connected multiple Permanent Magnet Synchronous Generators (PMSG) in series to generate higher AC voltage. Yuan et al. proposed a similar scheme, however using multiple segments of each winding [17]. The winding segments are isolated from each other. Thus authors proposed putting the boost output in series to step up the voltage further. Johnson et al. studied the issues when multiple generators are connected in series through rectifier circuits [18]. This study shows that the series connection this way may lead to a violation of operating limits both on the mechanical and electrical side.

Kshirsagar et al proposed operating and open end winding IM from a nine-level inverter [19]. The inverter structure consists of cascaded half bridge limbs as a leg of one side of the three phase inverter. The other side of the winding is fed by a similar inverter producing nine levels at the output voltage. The two sides are fed by four isolated DC sources, which is little difficult to achieve. However, there is no clamping diode as in the NPC inverter of capacitor as required in the flying capacitor inverter.

Different converter combinations can be used for feeding open-end winding machines from the two ends. PMSG system with two-level rectifier on one side and a diode rectifier on the other side has been proposed [20]. Modular Multilevel Converter (MMC) is also used for interfacing open end winding PMSG for wind energy conversion systems [21]. The modularity of MMC is a big advantage besides its suitability in high voltage application.

Kawabata et al. discuss inverter schemes for feeding open end windings machines including transformers for VAr compensators [22]. The authors studied various methods for generating the DC bus voltages for these inverters. As discussed earlier, common mode voltage and current become serious issues when open-end winding machine is fed by converters having linked DC bus. Somani et al. investigated the reasons behind the circulating current in open end

winding machine drive systems with common DC bus [23]. The circulating current is due to the common mode voltage generated in this structure. As the authors suggested, the common mode voltage even when nullified by switching strategy may come from non-linearity such as dead time, device on-time voltage drops, etc, which are inherent to the operation of the converters. The suggested methods to reduce this current are the use of common mode chokes, dead time compensation, etc. Vattuone et al. discuss the background reason for the common mode issues like shaft voltage, ground currents, and bearing currents and suggest the design procedure of a passive common mode filter to mitigate the issues [24].

Che et al investigated the operation of a six-phase induction motor from two three-phase inverters to feed the three sets of three-phase windings [25]. The DC buses of the two three-phase inverters are connected in series. The individual DC buses of the two three phase inverters are generated by using a capacitor voltage divider. The two three phase set of currents are converted to four decoupled AC components namely, α, β, x, y. The balance of the capacitor voltages is maintained by modifying the x, y components of the current.

One open-end winding PMSG is employed to feed two DC loads from its two ends through two three-phase converter structures. One end of the system drives a three-phase diode rectifier to feed a DC load, whereas on the other end, there is three-phase PWM rectifier charging or discharging a battery [26].

Sensorless control has been extended for open-end winding PMSG driven by a wind turbine. The fragile position sensors required for FOC of the PMSG can be done away with. The sensorless drive scheme for a three phase converter needs to be modified to apply in open end winding scheme [27].

Single-phase AC load can be fed from a three-phase open-end winding PMSG interfaced with three-phase converter structure. The converter involves no low-pass filter. The zero sequence current control and ripple on the output single-phase AC voltage are controlled in α-β-0 coordinate [28].

Thus, open-end winding schemes for interfacing AC machines are popular and relevant for the researchers due their advantages despite having higher number of switches compared to conventional converter structures.

1.5. Review of Series Parallel DC-DC Converters

The problem of interfacing high-voltage bus using lower voltage switches can be handled by multilevel inverters or series connection of suitable number of switches to withstand the bus voltage.

A parallel development went on to divide the bus voltage into several smaller voltage buses for smaller converters. The converter inputs are connected in series. Thus the total bus voltage is the sum of the voltages of the converter input buses. The voltage sharing of the converters needs to be taken care of. The initial development happened in terms of input-series-output-parallel (ISOP) DC-DC converters [29]. Capacitors are used to divide the total bus voltage into several sections. The capacitor voltages are measured and using suitable controller input current is regulated such that voltage balance can be ensured. ISOP inverter system has been reported with several h-bridges with their input bus connected in series, the AC side of the h-bridges feeding grid [30]. Thus, input currents of the h-bridges are controlled individually to maintain the input voltage sharing.

While an ISOP divides input DC bus into several smaller buses, input-parallel-output-series (IPOS) combines several smaller DC output in series to provide higher voltage DC [31]. Output-series converters are well-known in the field of DC-DC conversion. They have the advantage of controlling the input current individually to control the output voltage. Work on IPOS inverter control has been reported [32].

Input-parallel-output-parallel (IPOP) and input-series-output-series (ISOS) converter topologies are also studied. All these are static converters being DC-DC or AC-DC or vice-versa systems. However, no study has been reported involving electric machines, i.e. for electric drives. For electrical machines works have been reported with multiple segments of phase winding each with its converter. These converters are connected for higher voltage or current according to the requirements. Although these converters are utilized for DC-DC or DC-AC conversion systems, they are rarely used for AC motor interfacing. In the case of ISOP converters interfacing an AC machine input voltage balance has to be ensured along with output current sharing. Similarly, for IPOS converters interfacing with an AC machine, input current sharing has to be ensured simultaneously with output voltage balancing. In both cases, the

second balancing requirement limits the performance of the first sharing requirement. Thus, there is some scope for investigation.

1.6. Other Developments related to AC machines interfaced to higher voltage

AC motors driven by Current Source Inverters (CSI) are popular due to their inherent controlled current capability, eliminating the chance of over-current, which is a risk in a VSI [33-34]. When an AC motor is driven by CSI, the driving inverters can be made 1-phase, connected in series on the DC side, such that the total voltage applied is divided across the component inverter [31-32]. The constant current drawn from the DC bus by each 1-phase CSI can be either bypassed or permitted through the respective stator phase windings of the 3-phase motor to control the motor. This utilized the reliability of a CSI in terms of inherent short circuit/over-current protection while adding the scope of independent switching of the inverter devices with reduced voltage ratings of the semiconductor switches.

Ruseler et al. proposed several h-bridge inverters connected in series on the DC bus side [35]. The AC output of the inverters drives winding segments of a three-phase transformer winding. Thus the AC voltage outputs can be connected in series or parallel depending on the requirement. The secondary of the transformer is driving a three-phase RLC load simulating an induction motor. As the windings can be segmented to have equal impedance and as the current through the segments are same, the voltage balance of the DC bus capacitors is ensured. AC machine interfaced to higher DC bus voltage is thus, still an area of development. New devices are coming up to cope with this requirement. Some solutions with the existing technology may be considered for further research.

1.7. Research related to the generation of higher DC voltage from AC generator

The generation of higher DC voltage has been an area of interest for a long time. This has important audiences in wind generation systems along with many other fields.

In the case of bulk wind energy conversion system, offshore wind generation system is more popular due to the availability of offshore wind resources with higher and steadier wind speed and reduced environmental issues [36, 37]. As space required for offshore wind power systems on the land is negligible, it is beneficial in terms of space savings for human settlement, or other land utilization. Due to the requirement that large power be transmitted over a long distance to the onshore substations, the natural choice is to increase the voltage level of transmission to make the system efficient and economical. The available literature related to this purpose can be broadly classified into HVAC and HVDC transmission with the latter being more popular. In both cases, either the high voltage can be produced by each individual source themselves and then the sources may be connected in parallel for increased power or the sources can be connected in series to produce further higher voltage level [38-39].

Power frequency transformers or autotransformers may be used to provide the required voltage boost, but they are not the preferred choice in off-shore applications due to higher cost, weight and floor space requirement [39]. Solid State Transformer (SST) operating at high frequency with high voltage SiC devices or different multilevel converters reduces the overall size [21, 40].

For smaller generators with lower voltage ratings, mainly the PMSG, the higher DC voltage suitable for transmission can be generated by rectifying the AC voltage and then using a DC-DC voltage boost stage [11, 39, 41] that processes the full power produced by the generators. For achieving higher DC voltage, the outputs of several such DC-DC voltage boost converters powered by individual PMSG can be connected in series [37]. This scheme is well established in the literature as this does not require a DC substation onshore although a voltage balancing scheme is necessary between the DC sources to maintain the DC bus voltage for transmission. However, the rectifier input power factor can be very poor due to the non-sinusoidal input current, preventing extraction of the maximum active power from the generator. To improve the power factor, a front-end PWM converter can be employed, also making the output DC voltage to be higher than the highest peak voltage, helping to increase the DC bus voltage. A significant boost through the PWM converter increases the blocking voltage requirement of the converter switches, often making it difficult for economical commercial implementation. To reduce the blocking voltage of switches, various multilevel DC-DC converter sub-modules may be used [36, 37, 38, 42]. This may be series connected Dual Active Bridge (DAB) converters, which

reduces the voltage rating of each DAB converter [40]. Cascaded H-bridge (CHB) or MMC are also employed due to modular design and lower filter size requirement [21, 43]. Other multilevel voltage source converters namely NPC, Active NPC (ANPC), T-type converters, etc., are also used with multiple segments of generator windings to create high-voltage DC buses using lower voltage devices [36, 21, 42, 43, 44, 45].

Various schemes for the design of wind parks have been suggested by Holtsmark et al. [46]. One option is to rectify the AC outputs of the generators and connect the DC buses of the generator to have a HVDC voltage suitable for transmission to the on-shore substation, where it will connect to the AC grid through the inverter. AC parallel windfarm design is suggested utilizing a transformer for interconnecting several wind generators. The stepped-up AC voltage at the secondary of the transformer is rectified to transmit to the on-shore substation.

The AC outputs of the wind generators can be converted to high DC voltage suitable for transmission using various schemes discussed by Meyer et al [47]. Gjerde et al. proposed converting the AC voltage of several stator winding segments to higher DC voltage and then connecting them in series for higher DC voltage generation [48].

Doubly-fed induction generator is popular in wind generation applications. Soares et al. suggested connecting them directly to form a DC microgrid [49]. Both stator side and rotor side converters are connected to the same DC bus of the microgrid. Besides for higher power operation a diode-bridge rectifier for the stator windings is also suggested.

Beik et al. suggest a new generator configuration with a rotor having both wound-field and permanent magnet [50]. The designed 9-phase generator has an exciter on the rotor also. The output voltage is the phasor summation of the voltage generated by the wound field and permanent magnet.

Zeng et al. proposed the utilization of three-phase PWM rectifiers on the two ends of the open end winding PMSG [51]. The DC bus of the two rectifier systems is further boosted by a DC-DC converter with high-frequency isolation. The outputs of the isolated DC-DC converters are connected in series to generate high voltage. Compared to earlier systems of line frequency transformers to combine the AC voltages for HVAC, this system can produce HVDC voltage directly both by boosting, stepping up and series connection of the voltage sources.

A complete scheme for connecting an open end winding PMSG to the power grid through NPC inverters fed by an HVDC link has been proposed by Vattuone et al [52]. The PMSG voltage is rectified by three-phase diode rectifier on both ends, which is then stepped up by individual conventional boost converters. The outputs of the boost converters are connected in parallel. Simulation results are presented to substantiate the proposal.

Guo et al. suggested using the MMC for converting the AC power of the wind energy system to DC and then several such DC sources can be connected in series to generate HVDC suitable for transmission using submarine DC cable to the onshore substation [42].

Thus, research on the direct connection of offshore wind generators to the power system is still an active subject of interest. Both HVAC and HVDC are popular for power delivery by long-distance cable from offshore generators to onshore substations, with HVDC gaining an edge in recent times.

1.8. Scope and Organization of the thesis

This thesis investigates suitable converter topology, control, and the related issues for interfacing an AC machine of lower voltage rating to a higher voltage DC bus. The study as a whole is based on the idea of dividing the higher voltage DC bus into smaller ratings and then individually interfacing the AC machine windings in open-end configuration through suitable converters.

Chapter 2 deals with the mathematical modeling of AC machines in this thesis namely induction machines and permanent magnet synchronous machines. The mathematical models usually considering a star-connected stator, are well discussed in the available literature. However, when the stator windings are opened for open-end winding connection, there is a path for zero sequence current, which is to be considered by the mathematical model.

Chapter 3 proposes an inverter structure suitable for interfacing a lower voltage three-phase induction motor to a higher voltage DC bus. The total DC bus is subdivided into smaller DC buses by capacitive voltage dividers, each feeding a single-phase inverter module. The single-phase inverters feed the stator windings of the induction motor. It is shown that the capacitor voltages remain balanced inherently.

Motoring operation also calls for a regenerative mode of operation. This has been dealt with in chapter 4. Instead of limiting to the regenerative operation only, this chapter deals with the issues in operating a lower voltage AC generator to generate a much higher voltage DC bus. Due to the presence of a low impedance path of zero sequence current without a back-emf, suitable generators for this operation are those, which generate sinusoidal voltage. Thus, PMSG is a good choice for this discussion. The PMSG stator winding is connected in an open-end winding configuration, each feeding a single-phase PWM rectifier, generating much higher DC bus voltage from a lower stator winding voltage rating. The operation, control, and voltage balancing issues have been discussed in this chapter.

Finally, chapter 5 considers the scope for future work, to improve upon the configurations discussed in earlier chapters.

Overall, the thesis attempts to study the proposition of dividing a higher voltage DC bus into smaller DC buses, those interfacing phases of an open-end winding AC machine through an AC↔DC converter. The proposed configurations including the AC machines are simulated using MATLAB SIMULINK. These are also verified experimentally. The machine parameters used for simulation and experimental studies are provided at the end of chapters 3 and 4.

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Chapter 2

Machine modeling for Simulation Study

2.1. Introduction

The mathematical models of the electrical machines under study are to be developed for software simulation of these machines with the interfacing converters. 3-ph open winding Induction motor and an open winding PMSG are used for two studies in this work. Their mathematical models are discussed in this chapter. Here the standard two-axis models are augmented by the zero sequence network of these machines.

2.2. Induction Machine model

The 3-phase voltage applied across the induction motor stator winding is first converted from dependent three-axis quantity to independent 2-axis namely α, β and zero sequence quantity by Clarke Transformation given by:

$$\begin{bmatrix} v_\alpha \\ v_\beta \\ v_0 \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & \sqrt{3}/2 \\ 1/2 & 1/2 & 1/2 \end{bmatrix}\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{2.1}$$

Here, v_a, v_b, v_c are the voltage across the three windings of the IM. The transformed voltage on α, β are orthogonal to each other, but they are sinusoidally varying similar to v_a, v_b, v_c.

These sinusoidally varying quantities are again transformed into steady d-q, zero axis by Prak's Transformation using:

$$\begin{bmatrix} v_{sd} \\ v_{sq} \\ v_{0s} \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta & 0 \\ -\sin\theta & \cos\theta & 0 \\ 0 & 0 & 1 \end{bmatrix}\begin{bmatrix} v_\alpha \\ v_\beta \\ v_0 \end{bmatrix} \tag{2.2}$$

Here, $\theta = \omega_s t$ is the angle of the flux vector with respect to axis of the A-phase winding. The calculation of θ is different for depending on the selection of the flux vector. In case of IM, there are three flux vectors to work with. Depending upon the requirement any one of them can be selected. Rotor flux axis is the most popular reference frame. Thus, for a rotor flux oriented model the rotor flux vector is considered to be along the angle θ and no component of the rotor flux exits in other directions. ω_s is the speed of rotation of the selected flux vector, i.e. rotor flux in this case. This is also the synchronous speed of the IM. The generalized d, q, zero equivalent circuit of the induction machine can be represented as in fig 2.1.

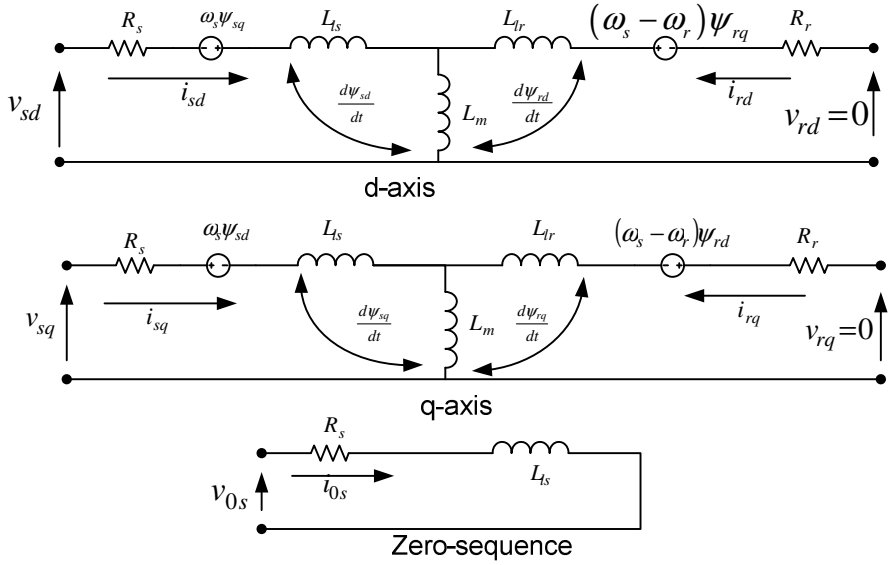

Fig. 2.1: equivalent circuit of the induction machine in d, q, zero axis

The rotor flux oriented mathematical model can be derived from the generalized equivalent circuit of the IM with $\psi_r = \psi_{rd}$ and $\psi_{rq} = 0$. The induction motor is modeled using the following equations in the rotor-field oriented reference frame in this study [9, 10, 11].

$$v_{sd} = R_s i_{sd} + \frac{L_m^2 R_r}{L_r^2} i_{sd} + \sigma L_s \frac{di_{sd}}{dt} - \frac{L_m R_r}{L_r^2} \psi_{rd} - \sigma L_s \omega_s i_{sq} \tag{2.3}$$

$$v_{sq} = R_s i_{sq} + \sigma L_s \frac{di_{sq}}{dt} + \omega_s \frac{L_m}{L_r} \psi_{rd} + \sigma L_s \omega_s i_{sd} \tag{2.4}$$

$$\psi_{rd} = L_m i_{mr} \text{ and } \frac{L_r}{R_r}\frac{di_{mr}}{dt} + i_{mr} = i_{sd} \tag{2.5}$$

Here, R_s = stator winding resistance per phase, L_s = stator self inductance per phase, L_m = magnetizing inductance per phase, L_r = rotor self inductance, R_r = rotor resistance per phase, v_{sd} = stator voltage in d-axis, v_{sq} = stator voltage in q-axis, i_{sd} = stator current in d-axis, i_{sq} = stator current in q-axis, i_{mr} = rotor magnetizing current. Ψ_{rd} = rotor flux linkage in d-axis and $\sigma = 1 - L_m^2 \big/ L_s L_r$.

The rotor flux being considered to be aligned along the d-axis of the rotor, rotor flux linkage in the q-axis becomes zero and total flux linkage is along the d-axis of the rotor.

It is well established that for a symmetrical rotor structure, zero sequence current does not produce any back emf or resultant torque. However, this produces a torque pulsation, which is detrimental for the life of shaft. For a given zero sequence voltage the zero sequence current generated can be calculated using the following equation:

$$v_{os} = R_s i_{os} + L_0 \frac{d}{dt}\left(i_{os}\right) \tag{2.6}$$

The developed electromagnetic torque in the rotor filed oriented scheme can be calculated as:

$$T_e = \frac{2}{3}\frac{P}{2}\frac{L_m}{L_r}\psi_{rd} i_{sq} \tag{2.7}$$

Where, P = number of poles of the induction motor

The mechanical speed of the rotor can be calculated as

$$J\frac{d\omega_r}{dt} = T_e - T_l - B\omega_r \tag{2.8}$$

Where, J = moment of inertia of the motor drive system, T_l = load torque, B = coefficient of friction.

The stator phase currents can be calculated from d-q currents using Inverse Park's Transformation first and then Inverse Clarke's Transformation as given below.

$$\begin{bmatrix} i_\alpha \\ i_\beta \\ i_0 \end{bmatrix} = \begin{bmatrix} \cos\theta & -\sin\theta & 0 \\ \sin\theta & \cos\theta & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_{sd} \\ i_{sq} \\ i_{0s} \end{bmatrix} \tag{2.9}$$

and

$$\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & 0 & 1 \\ -1/2 & \sqrt{3}/2 & 1 \\ -1/2 & -\sqrt{3}/2 & 1 \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \\ i_0 \end{bmatrix} \tag{2.10}$$

2.3. Permanent Magnet Synchronous Generator model

The PMSG is usually modeled in the synchronously rotating reference frame which is also the rotor field oriented reference frame in case of a PMSG [9, 10, 11, 53].

$$v_{sd} = R_s i_{sd} + L_d \frac{d}{dt}\left(i_{sd}\right) - \omega_e L_q i_{sq} \tag{2.11}$$

$$v_{sq} = r_s i_{sq} + L_q \frac{d}{dt}\left(i_{sq}\right) + \omega_e \left(L_d i_{sd} + \lambda_{1r}\right) \tag{2.12}$$

$$v_{os} = r_s i_{os} + L_0 \frac{d}{dt}\left(i_{os}\right) + 3\omega_e \lambda_{3r} \sin\left(3\theta_r\right) \tag{2.13}$$

where, v_{sd}, v_{sq}, v_{os} are the d-axis, q-axis and zero axis voltage components respectively. They are obtained from the voltages applied across the stator winding by Clarke and Park's Transformations as in equations (3.1) and (3.2). In case of PMSG the angle for Park's Transformation and $\theta_r = \omega_e t$ is the electrical angle subtended by the rotor with respect to stator A-phase wingding axis. Thus information about the position of the rotor axis is essential. The corresponding components of currents are i_{ds}, i_{qs}, i_{0s} respectively. R_s is the stator winding resistance and L_0 is the zero sequence inductance while L_d, L_q are d and q-axis self inductance. ω_e is the electrical synchronous speed and λ_{1r}, λ_{3r} are the fundamental and 3rd harmonic component of the rotor flux linkage. There can be other harmonic flux linkages also, depending on the construction of the machine. This generally happens for the Interior PMSGs (IPMSG). The equivalent circuit of the PMSG is shown in fig 2.2.

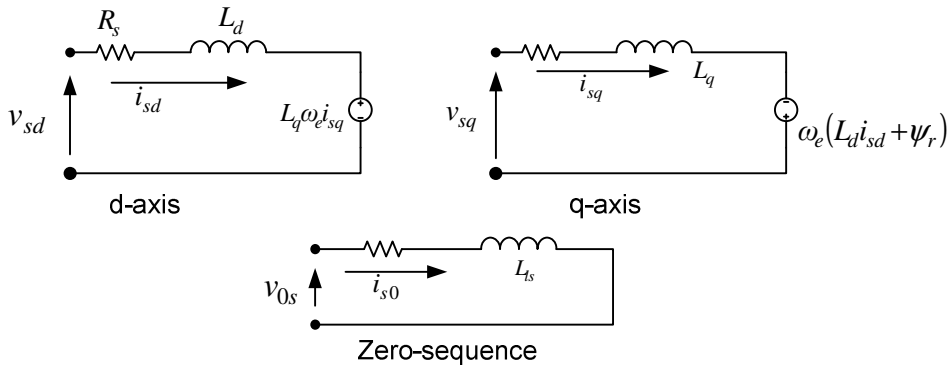

Fig. 2.2: Mathematical equivalent circuit of the PMSG in d, q, zero axis

The electromagnetic torque produced, can be calculated as:

$$T_e = \frac{2}{3}\frac{P}{2}\left[\psi_{1r} i_{sq} + \left(L_d - L_q\right) i_{sd} i_{sq}\right] \tag{2.14}$$

The mechanical speed of the rotor can be calculated as using equation (2.8).

The stator phase current can be found using inverse Park and Clarke Transform in order using equation (2.9) and (2.10).

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Chapter 3

Operation of a Lower Voltage Induction Motor from Higher Voltage DC Bus

3.1. Introduction

Electric drive technology advanced in diverse applications due to the progress of low-cost digital controller technology with high-speed processing capability [9, 11, 54-56]. According to the consumption of bulk electrical power, the most popular AC drive topologies consist of squirrel cage induction motors driven from PWM VSI, fed from a suitable voltage source DC bus.

Induction motor drive usually requires a matching DC bus voltage. The DC bus voltage must be greater than a minimum value, that can be calculated using eq. (1.9), and theoretically, there is no limit to the maximum DC bus voltage. The inverter uses proper the modulation index to achieve the required AC voltage across the motor windings. In practice, however, if the DC bus voltage becomes much higher, the range of modulation index becomes very low. Thus as the speed control requires a change in modulation index along with the change in frequency, the resolution of the speed control reduces. Thus a crudely matching DC bus voltage is required for the induction motor drive system.

Further, for higher DC buses, the high magnitude voltage pulses, when switched at a high switching frequency, create high dv/dt, rapidly deteriorating the insulation of the motor [57]. The inverter semiconductor devices also have to withstand the high DC bus voltages, resulting in higher costs and higher losses. To mitigate this issue, multilevel inverters can be used which divides the high voltage into multiple voltage levels. However, the restricted range of the modulation index still remains a problem.

Part of the contents of this chapter has been published in the paper entitled “Three-Phase Open-End Induction Motor Drive Interfaced to Higher Voltage DC Bus,” by D. Maiti and S. K. Biswas, in IEEE Transactions on Industrial Electronics, vol. 71, no. 2, pp. 1277-1285, Feb. 2024, doi: 10.1109/TIE.2023.3262874.

The use of an intermediate stage of DC-DC conversion is another solution to match the voltage. Such a DC-DC converter will have a somewhat higher power rating than that of the inverter considering the efficiency involved, and have higher voltage & higher current-rated semiconductor devices, all increasing the cost, size, and weight of the entire system while reducing the efficiency[58].

If the input is derived from an AC voltage source it is possible to use a transformer to implement voltage matching. This also has the disadvantages of higher cost, more space and weight with lower efficiency. As discussed, earlier, a front-end PWM rectifier can be employed instead of a thyristor-controlled rectifier to achieve better Displacement Factor (DF) and distortion factor (df). However, the output DC voltage in this case has to be higher than the highest peak voltage. Such a situation may just aggravate the problem by increasing the DC bus voltage further.

The work presented here proposes to drive each phase of the 3-phase Open-End (Winding) Induction Motor (OEIM) by one 1-phase PWM VSI with the input DC bus of these three inverters connected in series across the available DC bus voltage. Thus, the total available DC bus voltage is split into three equal smaller voltage levels with individual lower voltage-rated single-phase PWM inverters driving each isolated winding. Thus, an IM of a lower voltage rating can be connected to the available higher DC voltage bus through a modification of the inverter topology and the use of open-end winding, without the need for transformers or DC-DC converters. It is shown that the individual DC bus voltage levels remain reasonably balanced in the normal operation of the machine.

3.2. Proposed Scheme

The proposed series connected 3-phase OEIM drive scheme is presented in fig. 3.1. The individual phase windings of the IM, which are electrically isolated from each other, are connected separately to 1-phase H-bridge VSI each. The input DC buses of these inverters with their DC bus capacitors are connected in series to form the total input DC bus of the complete inverter, which may be connected to the higher voltage DC supply. Each 1-phase inverter operates with a 180º phase shift between its two limbs to create the highest possible fundamental output voltage. However, it maintains a 120º phase shift between its output fundamental voltage

and that of its adjacent VSI through a coordinated PWM control to create a balanced 3-phase voltage supply to the OEIM windings. Thus, the proposed scheme creates a 3-phase open-end winding induction motor drive interfaced with a higher DC voltage bus than what would have been required as a normal 3-phase motor in a star or delta connection.

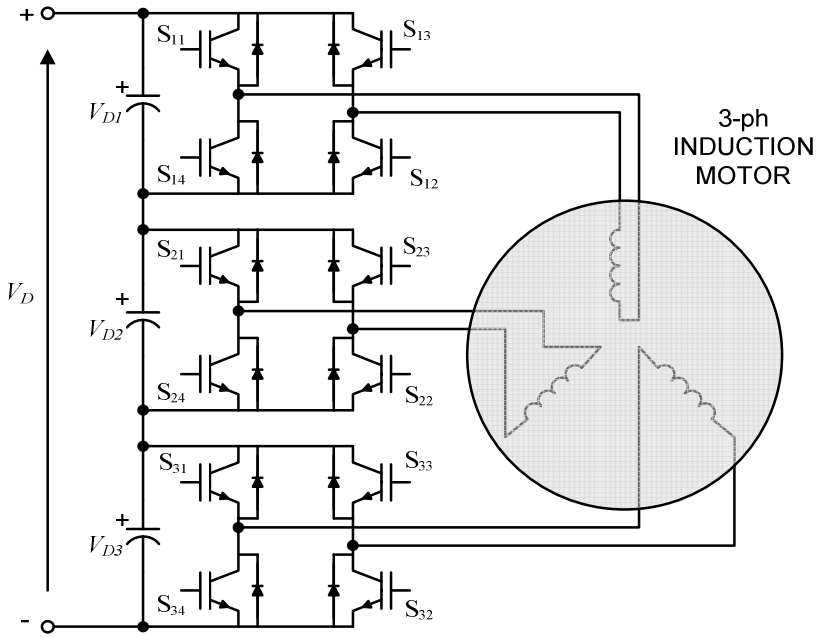

Fig. 3.1: Proposed Scheme for driving a low voltage motor from higher voltage DC bus

This scheme permits better resolution of speed control of an IM of a given winding voltage rating from a DC voltage of higher value, over the full linear range of modulation index of PWM, than permissible by a direct 3-phase inverter due to restriction of produced voltage by limiting modulation index. Conversely, it permits the operation of an induction motor of a lower voltage rating than what would be necessary through a normal 3-phase inverter from the given DC bus voltage.

The total input DC bus is split into three equal smaller voltage DC buses using series connected DC bus capacitors. Thus, the actual capacitors on the DC bus are of lower voltage rating than the input DC bus voltage (ideally ⅓ of the total input DC bus voltage). Since each of the three inverters is connected across each capacitor, the switching devices (like IGBTs) in each inverter are also of lower voltage rating than the input DC supply. Since the capacitors on the DC bus are connected in series, there is concern about their voltage balance, but this topology is shown to automatically maintain reasonable balance once the motor is in running condition.

The inherent type of the winding connection of the IM has two options to match the given high DC bus voltage: star or delta connection, before being converted to OEIM. If the motor is normally delta connected but now operated in open-end mode, the current to be supplied by each 1-phase inverter is only the phase current of the motor, which is $1/\sqrt{3}$ times the original line current while the total DC bus voltage required is the highest. Thus, the current rating of the switches becomes lower than what is needed in a normal 3-phase VSI. However, if the motor was normally star connected, each 1-phase inverter current same as the original line current of the motor while the total DC bus voltage required is the lowest.

3.3. Output Voltage for the Proposed Topology

The individual 1-phase VSI, switching with 180º phase shift between its two limbs has low impedance path for zero sequence current flow through the motor winding, leading to increased losses. Therefore, precaution must be taken, such that the PWM scheme used does not generate any significant zero sequence voltage [59-63]. As discussed earlier this can be achieved by using those states of the Space Vector that guarantee the absence of zero sequence voltage.

Subsequent analysis shows this converter maintains the reasonable balance of the component DC buses in the running condition. Thus, for the three-phase structure shown in fig. 3.1, the DC bus voltages, V_{d1}, V_{d2}, V_{d3} become equal to each other. Thus, the analysis for the output voltage can be done following the analysis in fig. 1.9. With an input voltage of V_{D_inv} for each 1-phase inverter using Sinusoidal PWM, the maximum per phase rms fundamental voltage applied across one winding of OEIM is:

$$V_{rms-ph} = (V_{D\_inv}) / (\sqrt{2}) = (V_D) / (3\sqrt{2}) \tag{3.1}$$

Moreover, as the output AC voltage is the same for both SPWM or SVPWM without zero states, either a Sinusoidal PWM or Space Vector PWM with the removal of states that cause zero sequence voltage can be used to obtain the same result.

As an example, with a 1700V supply DC bus, the maximum rms fundamental output line voltage that can be ideally created by a 3-phase VSI with Sinusoidal PWM is given by:

$$V_{rms\text{-}line\text{-}line} = (1700\sqrt{3}) \div (2\sqrt{2}) = 1041.1\text{V} \tag{3.2}$$

With the same input DC bus, the maximum rms fundamental output winding voltage that can be ideally created by the proposed scheme using 1-phase VSI with Sinusoidal PWM is:

$$V_{rms-ph} = (1700) \div (3\sqrt{2}) = 400.7\text{V} \qquad (3.3)$$

This shows that a normal 400V 3-phase induction motor (assumed original delta connection converted to open-end connection as in fig. 3.1) can be driven from a 1.7kV DC bus through the proposed inverter drive scheme. In the case of a normal star-connected induction motor being converted to similar open-end connection, a standard 690V 3-phase motor can be similarly driven from the same 1.7kV DC bus. Further, a 1kV DC input bus can be used to drive a 400V star connected IM converted to a similar open-end connection.

It is possible to create a lower fundamental voltage than the value given by eq. (1.9) by limiting the range of modulation index in the proposed scheme, but at the sacrifice of limited resolution of speed control. However, such a technique may be useful for matching the motor to the inverter output when the rated winding voltage is somewhat smaller than the voltage predicted through eq. (1.9).

A comparison between the proposed inverter and a conventional 3-phase 3-limb inverter is presented in Table II in terms of the number of devices along with their voltage & current ratings. It will be observed that even though the proposed scheme uses a higher number of devices, the device ratings are smaller, hence the overall cost (depending on specific voltage & current rating) will not be very large.

TABLE 3.1

Comparison of Proposed Inverter with 3-phase 3-limb Inverter

Type of Inverter	Devices	Device Voltage	Device Current
3-phase, 3-limb	6 nos	High (same as input)	Same as the motor line current
Proposed	12 nos	Low (about 1/3 of input)	Same as Motor phase current (57.7% of line for Delta motor)

3.4. Capacitor Voltage Balancing

Although the series connected DC bus capacitors for inverter input sections should be identical, practical tolerance in values makes them unequal. Moreover, their characteristics may

differ with aging. Thus, there is a chance of voltage unbalance across the series connected capacitors, resulting in each 1-phase inverter being supplied by different voltages, which will need to be taken care of to prevent unbalanced supply voltage to the motor. It should be noted that under an unequal capacitor combination, the capacitor with the lowest value will have the maximum voltage.

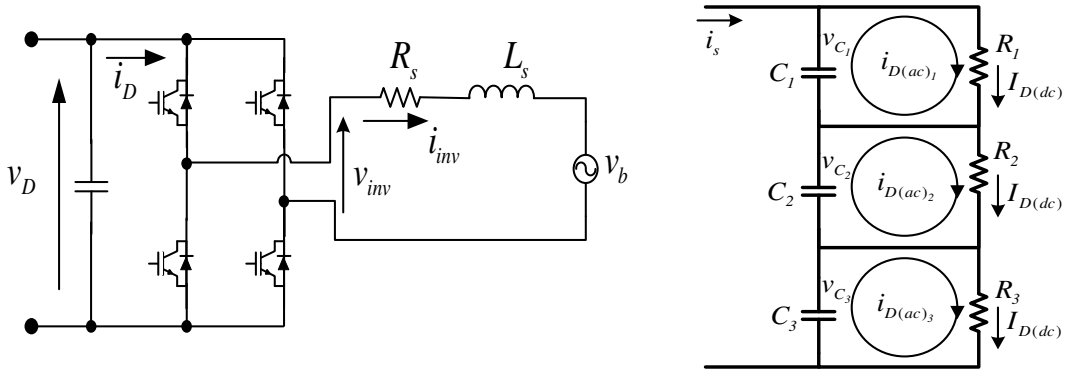

Fig. 3.2 : (a) Per phase inverter circuit configuration with per phase motor winging as load (b) Per phase equivalent circuit from the DC source

The steady-state equivalent circuit of one of the three 1-phase inverters with motor winding load is shown in Fig. 3.2(a). Taking only the fundamental component of inverter output, with its angular frequency as ω and θ as the angle between the inverter fundamental voltage and current:

$$v_{inv}(t) = \sqrt{2} V_m \sin(\omega t) \tag{3.4}$$

$$i_{inv}(t) = \sqrt{2} I_m \sin(\omega t - \theta) \tag{3.5}$$

Thus, instantaneous fundamental power sent to load is:

$$p_{inv}(t) = 0.5 V_m I_m \cos\theta - 0.5 V_m I_m \cos(2\omega t - \theta) \tag{3.6}$$

The first part is a constant component while the second is sinusoidal time-varying at twice the fundamental frequency. Assuming very low voltage ripples on the DC bus, its voltage can be approximately represented by a constant magnitude V_D.

Thus the total instantaneous DC bus current i_D flow out from the DC bus voltage V_D can be split into two components, one constant and the other oscillating [64]:

$$I_{D(dc)} = \frac{V_m I_m}{2V_D} cos\,\theta \tag{3.7}$$

$$i_{D(ac)}(t) = -\frac{V_m I_m}{2V_D} cos\left(2\omega t - \theta\right) \tag{3.8}$$

Since the capacitor voltage is assumed to be steady, the DC component $i_{D(dc)}$ cannot flow through it and hence will flow only through the equivalent load resistor and the input DC source. On the other hand, the alternating component $i_{D(ac)}$ will flow through the equivalent load resistance and the capacitor. This AC component of the current flowing through the capacitor creates a voltage ripple, expressed as:

$$v_{Cr} = \frac{1}{C} i_{D(ac)} dt = \frac{V_m I_m}{4\omega C V_D} sin\left(2\omega t - \theta\right) \tag{3.9}$$

Thus, the magnitude of the DC bus voltage ripple created by the inverter load depends on the capacitance value and the DC voltage across the capacitor at a given constant power flow from the inverter.

If three such 1-phase inverters are connected in series through their DC bus with the inverter outputs creating a balanced 3-phase fundamental voltage supply for a balanced 3-phase machine as proposed, the individual $i_{D(ac)}$ components will be phase displaced by 120º along with the corresponding capacitor ripple voltages. Fig. 3.2(b) shows the equivalent circuit with resistors R_1, R_2 & R_3 representing the phase load.

Under steady state, since the DC component of individual currents cannot flow through the capacitors, they must all be equal in magnitude to $i_{D(dc)}$ and be equal to the DC component of the source current.

$$I_{D(dc)} = I_{D(dc)_1} = I_{D(dc)_2} = I_{D(dc)_3} \tag{3.10}$$

Thus, the steady voltage distribution across the individual capacitors will now dominantly depend on the individual equivalent load resistors R_1, R_2 & R_3 and less on the values of C_1, C_2 &

C_3. Since the reflected load is from a balanced 3-phase induction motor, the dominant active power per phase due to load can be expressed approximately by:

$$P_{ph} = I_r^2 (r_2' / s) \tag{3.11}$$

Where I_r is the rotor current, r_2' is the rotor resistance, both referred to the stator while *s* is the per-unit slip. Since each winding of the motor is of balanced construction, fed by a reasonably balanced 3-phase voltage source, operating with the same flux and slip, the power drawn by individual phases shall be very close to each other. This implies that with the same DC component of inverter input current, the reflected resistances R_1, R_2 & R_3 shall be quite close to each other.

Hence, even if the DC bus capacitors are somewhat different in value, with a reasonable amount of power drawn by the load, the capacitor voltages shall tend to maintain an automatic balance without any runaway. At the same time, since the same modulation index is used in each inverter, once the capacitor voltages become very close to each other under steady state, the situation ensures a balanced fundamental voltage supply across each winding, ensuring the convergence of each reflected resistances to be quite close to each other.

Before the motor is started, the reflected resistances R_1, R_2 & R_3 will be very large and possibly somewhat different, thus less effective towards maintaining voltage balance on the series connected capacitors C_1, C_2 & C_3. Hence, the capacitor voltages may differ, with the smallest capacitor having the largest voltage. However, after starting of the motor, the balancing situation will improve as the motor is loaded further and the value of reflected resistances becomes lower and closer to each other. This is possible because each capacitor forms a parallel RC circuit (using the reflected load resistance), which will permit local charging or discharging of the capacitor, converging towards a set of series-connected capacitors with balanced voltage.

If the three capacitors are equal, then ripple voltages across each will sum up to a total of zero across the total DC bus, due to the 120º phase difference between individual ripple voltages.

$$\sum v_{Cr} = v_{Cr_1} + v_{Cr_2} + v_{Cr_3} = 0 \tag{3.12}$$

Consider the current from the source to be is, current through capacitor C_1 be i_{C1}, its voltage be v_{C1}, and current through R_1 be i_o. Current through capacitor C_1 can be given as:

$$i_{C_1} = i_s - i_o = C_1 \frac{dv_{C_1}}{dt} = i_s - \frac{v_{C_1}}{R_1} \tag{3.13}$$

Solving, the voltage across the capacitor at any instant of time is given by:

$$v_{C_1}(t) = i_s R_1 (1 - e^{-\frac{t}{C_1 R_1}}) \tag{3.14}$$

Thus, the steady-state voltage across the capacitor C_1 will be equal to R_1 and the same across all capacitors in the series. Moreover, in the case of unequal capacitors, the time for voltage balance depends on the time constant C_1R_1, and not on the voltage difference. Thus, if the loads are balanced, then the capacitor voltages remain balanced and the PWM scheme for the same DC voltage can be applied here.

Despite this auto-balancing feature, passive or active balancing is suggested to be used [65], to prevent the chance of major voltage unbalance before starting of the motor and during transients. Although this may result in short-time power loss, any attempt to balance by sending the extra power from the capacitor to the motor will also result in the same power loss due to the unbalanced condition at that time.

3.5. Zero Sequence Current Suppression

In the proposed scheme, the motor back-emf opposes the inverter applied voltage per phase, thereby restricting the current. However, as there is no back-emf for the zero sequence, such current is only limited by the low magnitude winding resistance and the leakage reactance, permitting such current to become very high. Hence, this may become a limiting factor. To restrict the zero sequence currents, SVPWM states generating zero sequence voltage should be excluded, thereby resulting in the Space Vector Diagram shown in Fig. 1.9. However, due to dead time of the switching and other practical factors like unequal voltage drops in phases, harmonics in back emf, etc., nonlinearity creeps in.

Thus, SPWM with a zero sequence current loop may be applied to keep the zero sequence current within the limit [66-69]. Along with the *d-q* components of current, zero

sequence current can be calculated with the information of all the phase instantaneous currents, which is readily available.

The zero sequence current is compared with a reference, which in this case is zero, to nullify this component of current. A suitable controller is used to generate the correction from this comparison. The correction factor is added to all three phases for the generation of the pulse width for switching, as shown in Fig. 3.3.

In the proposed scheme, an FOC algorithm with zero sequence current control loop was implemented for the control of the induction motor through the inverter and experimentally verified to be effective.

Even in the case of V/f control of the inverter, a zero sequence current control loop should be employed. This can be done using a non-intrusive Hall Effect current sensor taking into account current through all three phases.

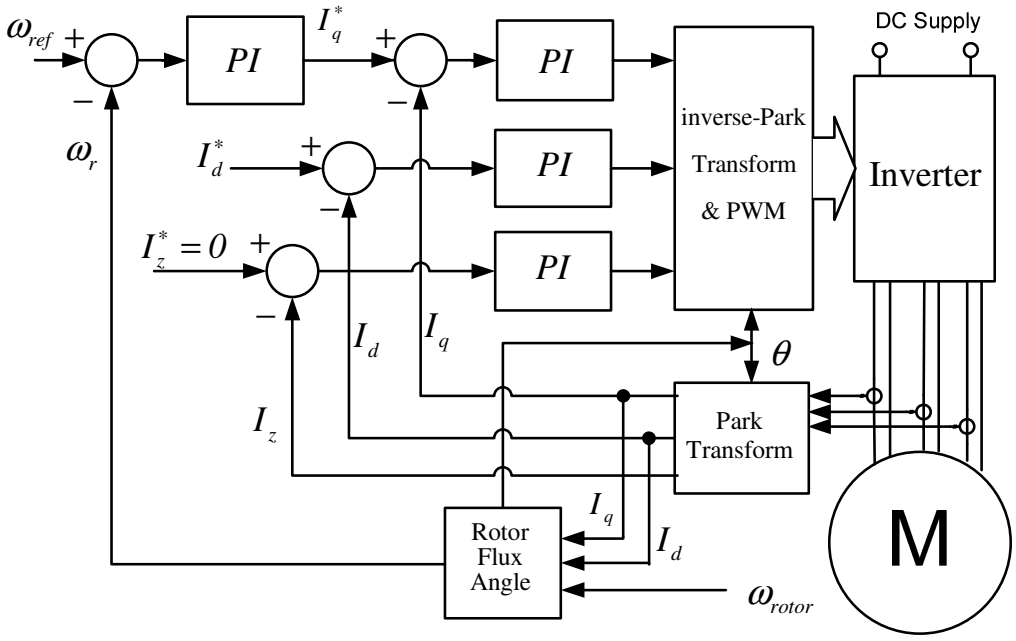

Fig. 3.3: Field-oriented control scheme for the proposed inverter

3.6. Control Circuit

The Indirect FOC algorithm was used for the proposed OEIM drive with a zero sequence current control loop as depicted in fig. 3.3.

Speed feedback was used for speed control of the motor. ω_{ref} is the speed reference, which is compared with the actual speed ω_r and the error is processed in a speed controller which is of PI type. The output of this speed controller I_q^* corresponds to the reference current equivalent to the torque reference. The actual instantaneous values for the three phase currents are sensed and converted to their *d-q* equivalents I_d & I_q in the rotor field reference frame using Park Transformation. The actual value of I_q is compared with the reference I_q^* and the error is processed through a PI controller to make the actual value follow the reference. I_d^* corresponds to the reference current equivalent for rotor flux reference (maintained constant for constant rotor flux operation). The actual value I_d is compared with the reference and the error is processed through a PI controller to make the actual value follow the reference. In addition, I_z^* is the zero sequence current reference for this scheme, which should be kept zero.

From eq. (2.5) the steady state value of the magnetizing current $i_{mr} = i_{sd}$. Thus, the reference current I_d^*should be equal to the amplitude of the magnetizing current of the induction motor, scaled properly by the Clarke Transformation. The magnetizing current is found from the no-load test of the induction motor.

The actual value of zero sequence current I_z is computed and compared with the set value of zero. A PI controller is used to control the zero sequence current.

The speed sensed by a quadrature encoder is used as feedback and to obtain information about the position of the rotor flux axis. The angular speed of the rotor flux ω_{mr} is required to find the position of the rotor flux, which can be obtained by:

$$\omega_{mr} = \omega_r + \left[(L_r / R_r)(i_q / i_d) \right] \tag{3.15}$$

where, ω_r is the rotor speed, L_r, R_r are the rotor inductance and resistance respectively. i_q and i_d are the instantaneous *q* and *d* axis currents computed from the actual motor currents. Integrating ω_{mr} provides the position of the rotor flux vector and the angle required for Park and Inverse Park Transformation.

The commanded *d-q* axis voltages are processed through Inverse Park Transformation to obtain the stator voltage values which are used for SPWM or SVPWM control of the inverter switches. SPWM switching is employed incorporating the voltage command from the zero sequence current control loop along with the required *d-q* voltages.

3.7. Simulation Results

The proposed drive scheme is simulated using MATLAB/ Simulink. The induction motor used for simulation as well as experiment was of 220V rated phase voltage, 50Hz, 4-pole, 1hp. The DC bus voltage was considered to be 1kV for simulation. Thus, in steady state, the average voltage across each capacitor should be 333.3V and per phase maximum voltage of the induction motor can be:

$$V_{rms-phase} = (1000) \div (3\sqrt{2}) \approx 236 \qquad (3.16)$$

At first, the three bus capacitors are considered to have a worst-case ±20% difference in their values, ie., 1.2pu, 1.0pu & 0.8pu capacitance values. Under this condition, fig. 3.4 shows the individual DC bus voltages as the motor starts up. It can be seen that under hypothetical direct-on-line starting of the motor sourced from the inverter, the individual DC bus voltages although being different due to different capacitor values, become balanced automatically. However, as expected with DOL starting, the initial current in the motor phases is high.

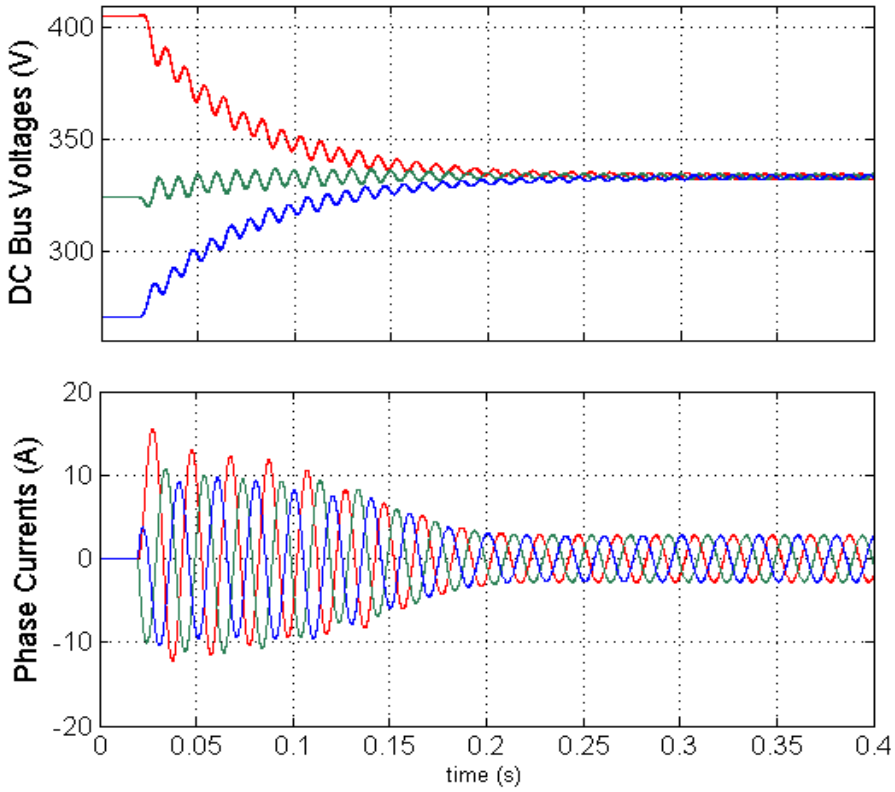

Fig. 3.4: Capacitor voltage (upper trace) and stator current per phase for DOL starting of the induction motor for the proposed scheme

In the case of FOC, individual DC bus voltage at the starting is expected to be balanced for best performance. Although, the voltages become balanced naturally, similar to the earlier cases, the flux and torque controller may try to delay the process by limiting the changes in motor current. This may cause unbalance in case of speed reversal, where, the motor has to stop at a certain point to change the direction of rotation and at that point of time there is no power exchange and no back emf. However, once the motor reaches steady state, there is little chance of capacitor voltage unbalance as long the back emf or power handling of each phase remains balanced. With the intentional use of different values of DC bus capacitors, fig. 3.5 shows the DC bus voltage variation with a change in motor speed under constant load torque. With either the same or different capacitor values, the average DC voltages across them remain balanced with a double-frequency voltage oscillation depending on the load, for speed and corresponding power variation.

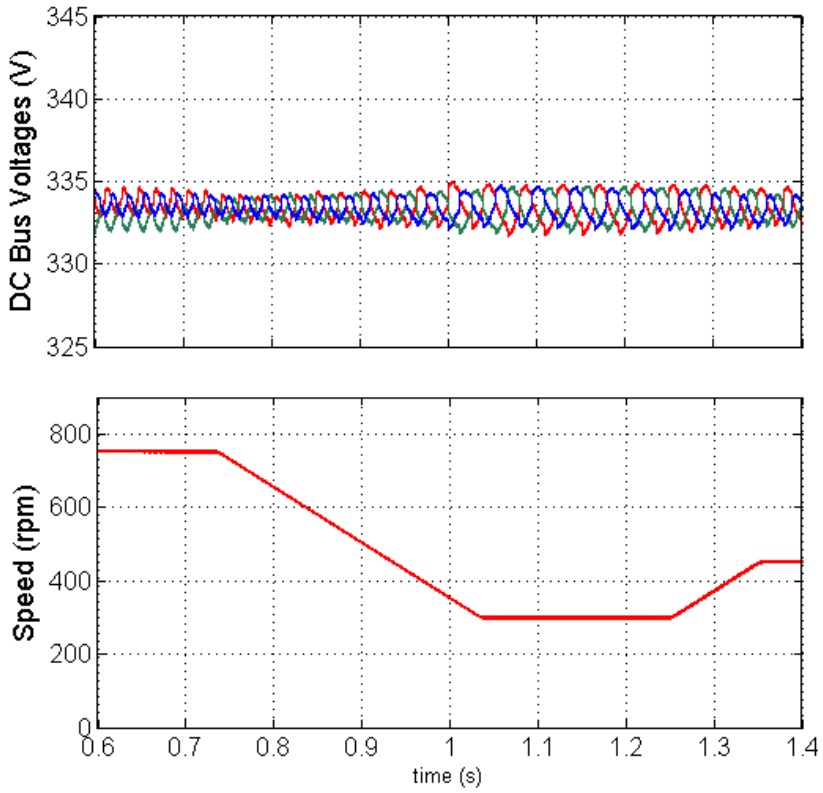

Fig. 3.5: Capacitor voltage variation with respect to the change in speed of the induction motor

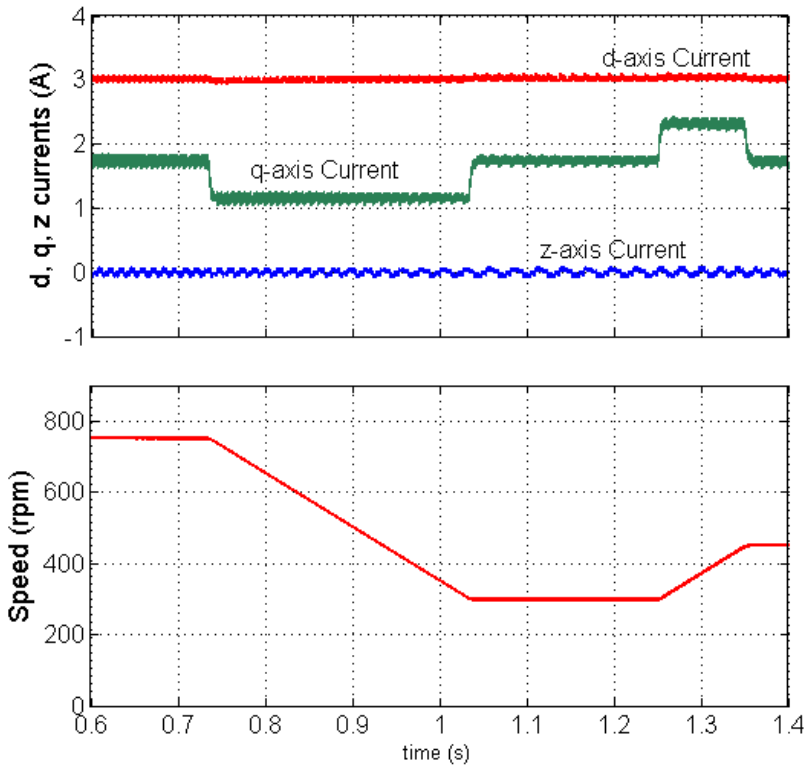

Fig. 3.6: d, q, zero axis current variation with respect to the change in speed of the induction motor

Fig. 3.6 shows the simulation result for flux, torque, and zero components of stator current against speed variation with constant torque load under FOC operation of the induction motor driven by the inverter. Here also, the capacitance values are considered different. However, as the motor was still in running condition, the individual DC bus voltages are balanced and for the PWM they were considered to be the same magnitude. Even for the unbalanced condition, for example at starting, the FOC operation can be started, by allowing little speed oscillation depending on the limit of voltage unbalance.

Fig. 3.7(a) shows the simulation result when there is no zero sequence current control loop. It can be seen that in the absence of the said loop, the zero sequence current becomes high in case of any unbalance or nonlinearity due to the inherent low impedance path for the zero sequence current. Upon implementing a zero sequence current control loop as shown in fig. 3.3, this current can be limited as depicted in Fig. 3.7(b).

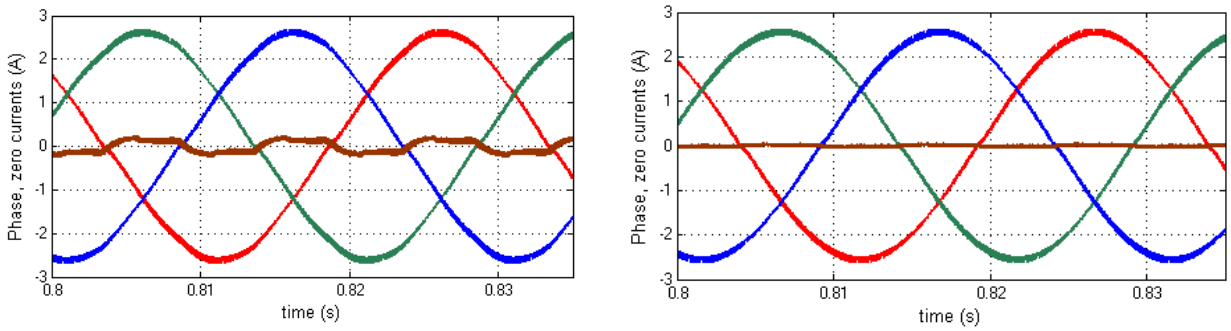

Fig 3.7 : Simulated three phase current waveform (a) without and (b) with zero sequence current control

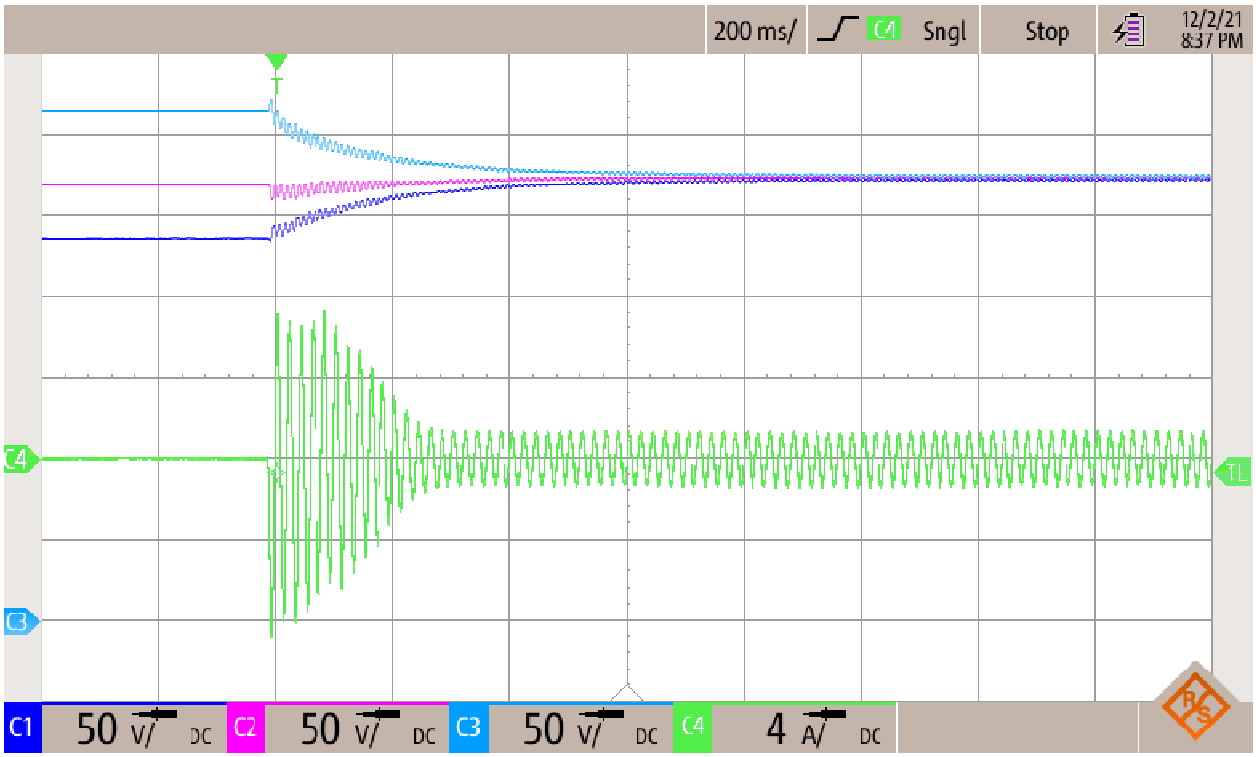

Fig 3.8 : capacitor voltage (channel 1, channel 2, channel 3) and one phase current of the induction motor for DOL starting with unequal capacitor per phase

3.8. Experimental Results

A prototype inverter was fabricated in the laboratory to experimentally validate the performance of the proposed scheme through the application of FOC. For the experiment, the capacitance values were made to intentionally differ by around ±20% from one another. It can be seen in fig. 3.8, that while the voltages of the three unequal capacitors are unbalanced at start, they become well-balanced once the motor is started (in DOL mode) and there is no variation even when there is a change in speed. Thus the natural balancing remains in force.

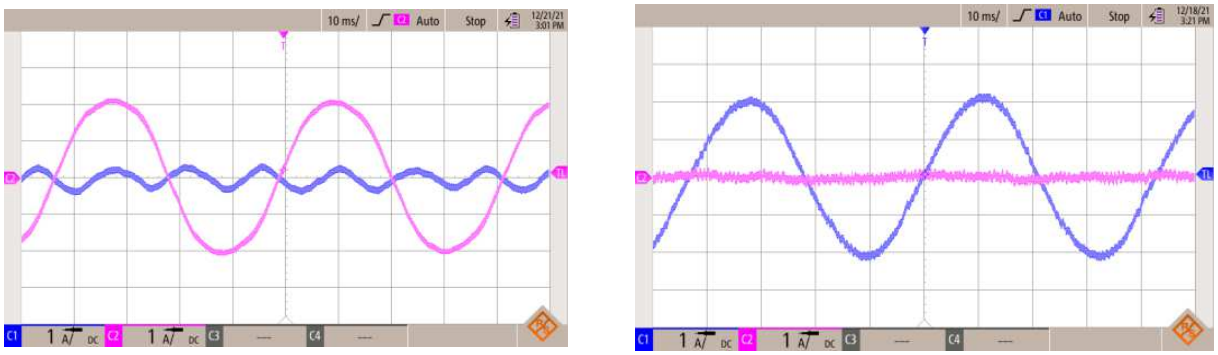

Fig 3.9 : Experimental phase current waveform (a) without and (b) with zero sequence current control

SPWM and SVPWM control without using zero common mode voltage switching state was initially applied. However, due to different nonlinearities introduced, including dead time, significant zero sequence current flows through the motor windings. One phase current of the open windings and zero-sequence current are presented in fig. 3.9(a) as discussed.

Fig. 3.9(b) shows a similar oscillogram for zero sequence current control implemented with SPWM switching. It can be observed that the scheme has effectively controlled the flow of zero sequence current through the motor windings. Fig. 3.10 shows the 3-phase currents for the motor under FOC with SPWM with zero sequence current control loop. It can be observed that the currents are balanced, predicting a balanced power transfer and balanced back emf for each phase.

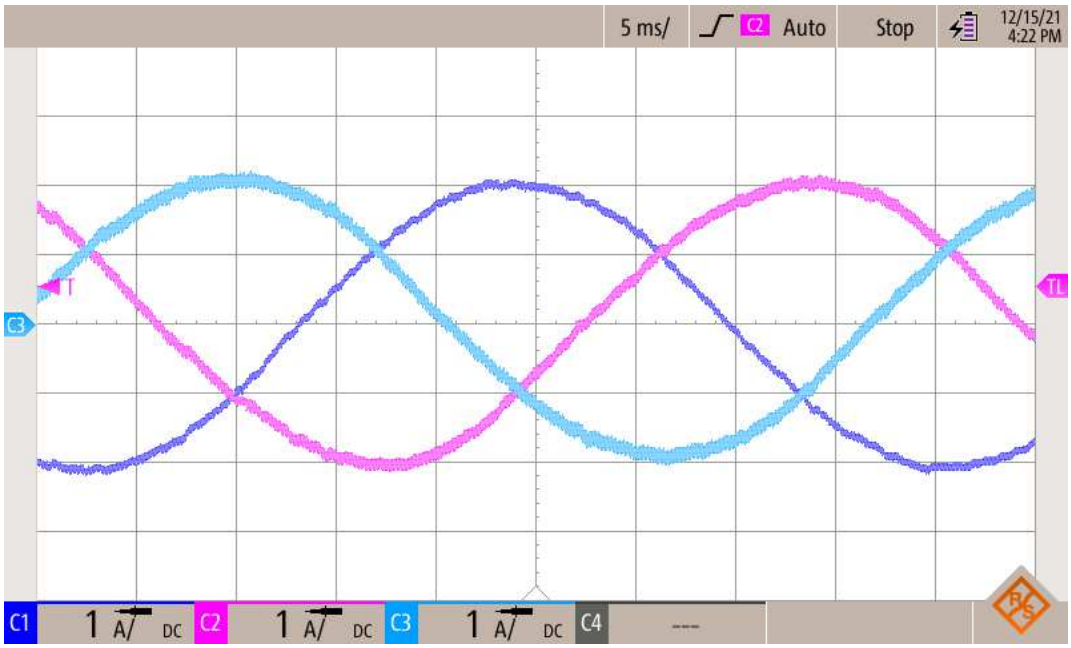

Fig 3.10: Experimental three phase current waveform with zero sequence current control

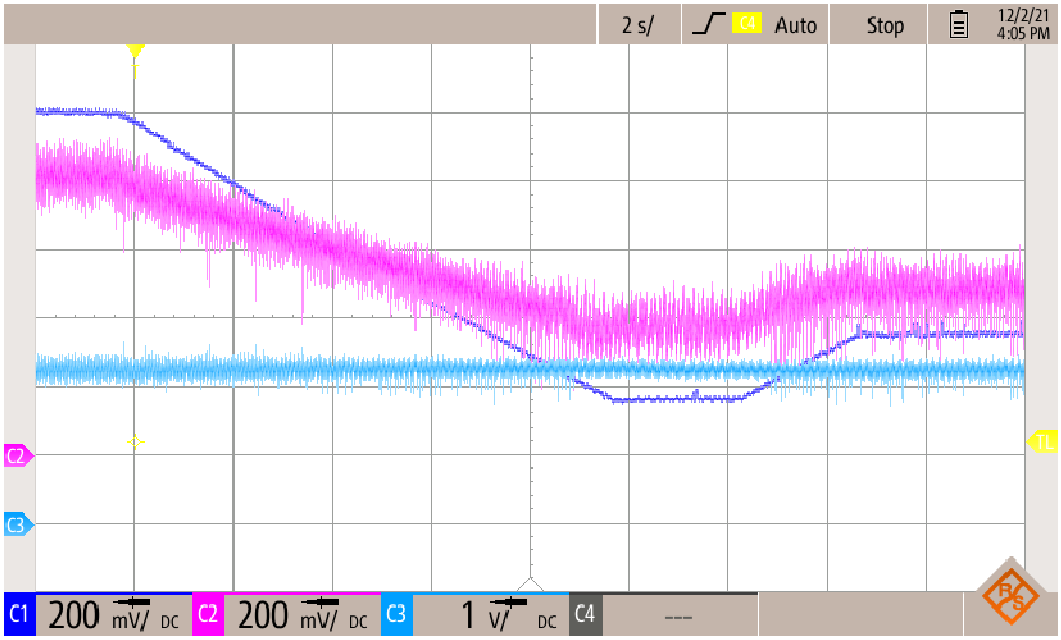

Fig 3.11: FOC operation of the induction motor; channel 1: speed, channel 2: q-axis current, channel 3: d-axis current

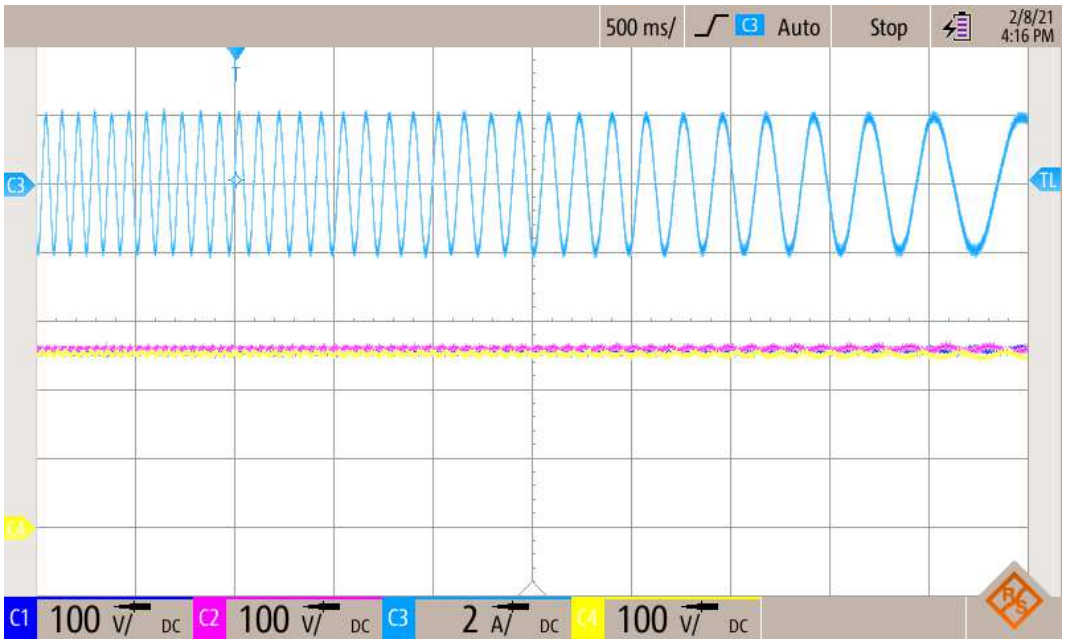

Fig 3.12: FOC operation of the induction motor; channel 1: one phase current, channel 2, channel 3, channel 4: capacitor voltage for a speed variation

Fig. 3.11 shows the transient performance for indirect rotor flux oriented FOC with SPWM. The speed is reduced from 750rpm to 300rpm and then increased to 450rpm. A separately excited DC generator connected to a resistance bank was used as a variable mechanical load to the induction motor. As can be observed, the flux component of the current remains undisturbed, and there is a smooth variation in the torque component of the current with speed variation. As the method of testing does not yield a true constant torque load, the q-axis current behavior is a bit different from that in the simulation result. Fig. 3.12 shows the variation in phase current frequency when the speed of the motor changes.

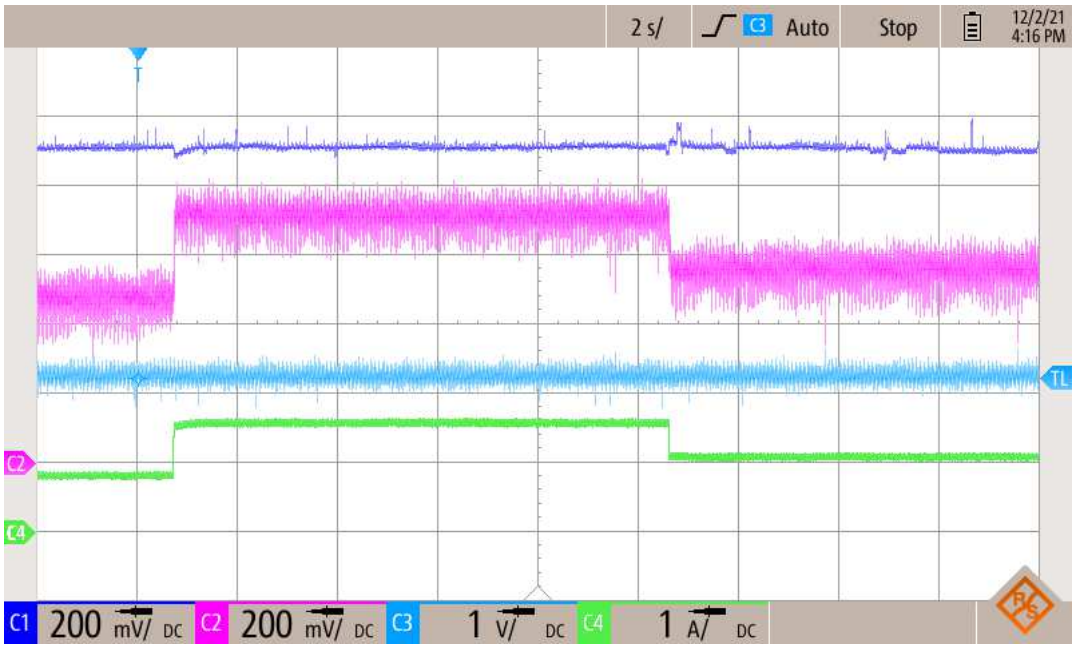

Fig 3.13: FOC operation of the induction motor; channel 1: speed, channel 2: q-axis current, channel 3: d-axis current, channel 4: change in load current.

Fig. 3.13 depicts the response to a momentary load throw on and its removal on the motor operation. The induction motor is operated at constant speed and loaded through a DC generator with adjustable load. The load of the generator is momentarily changed to study the load regulation of the induction motor drive. The behavior of computed current components I_d & I_q (from DAC) to the load change shows expected performance. However, a momentary slight drop in speed is noticed.

The experimental setup in the laboratory is presented in fig. 3.14, with the inverter setup using dual IGBT modules shown in fig. 3.14(a). Fig. 3.14(b) shows the open end motor coupled with a DC generator for loading and an encoder for speed feedback.

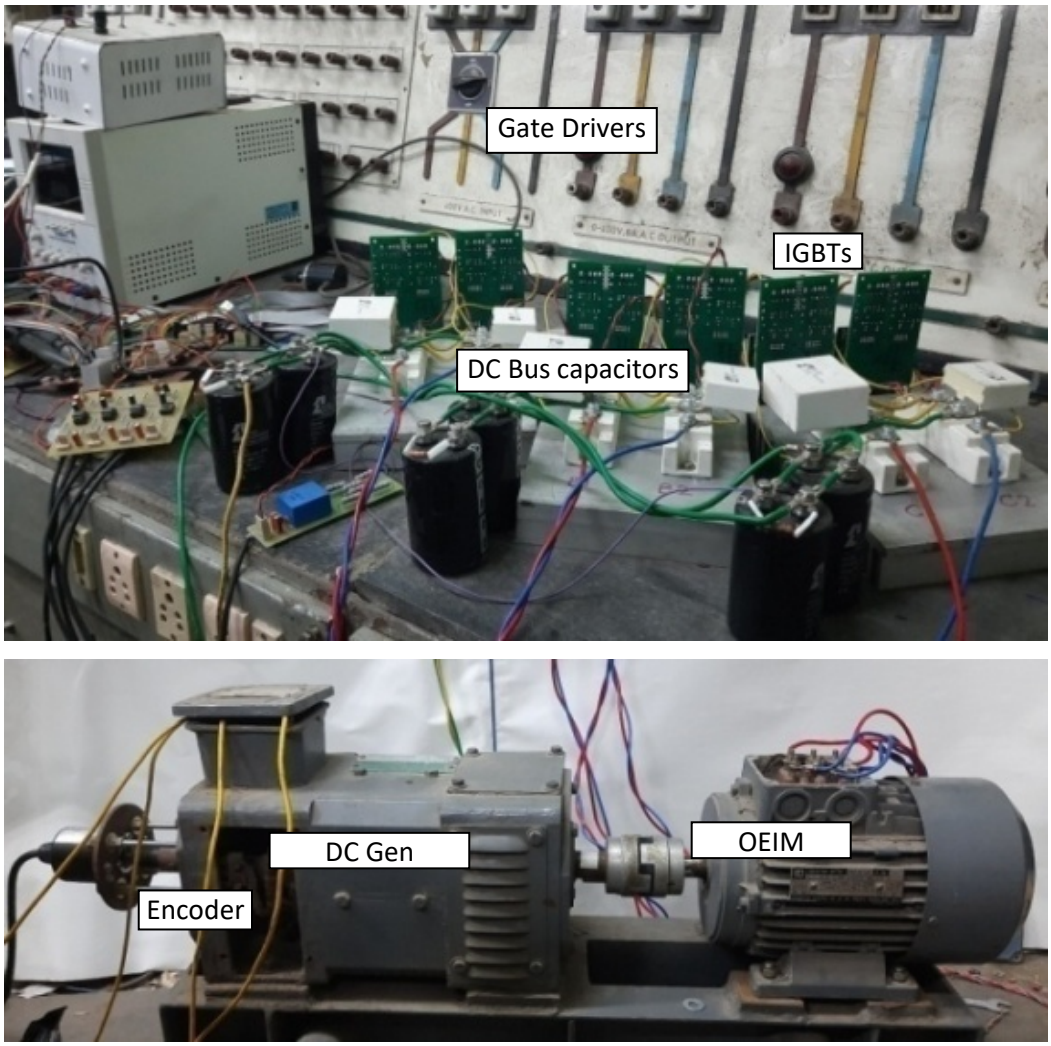

Fig 3.14: Experimental setup.

3.9. Conclusion

A scheme is proposed for the operation and wide range speed control of a 3-phase induction motor from a higher voltage DC bus than what would have been normally required. The proposed scheme uses the Open End Winding technique for the induction motor drive with one 1-phase inverter supplying each isolated winding. The input DC bus of each of the three 1-phase inverters is connected in series to the higher voltage input DC bus. However, if the input DC voltage is made lower than three times that required by each constituent inverter, the motor applied voltage will be lower, reducing torque capability. Contrary to existing alternatives, this scheme utilizes low voltage rating switches and capacitors, impresses less stress on motor insulation, and permits operation over a wide range of modulation index. In the case of an originally delta connected motor, the inverter switch current rating is also lower. There is also no

need for full power rated step-down DC-DC converter or transformer (in case of AC input) which would have incurred extra power loss, space, and weight. Due to practical situation if the DC bus capacitors are not of same value, the three DC bus voltages may not be initially perfectly balanced, but they become naturally balanced under normal operation, Inherent voltage balancing of the capacitors means it does not require any extra switching state in the control. However, a control over the zero sequence current flow through each phase winding is required. Analysis, simulation and experimental results are used to depict the performance of the proposed scheme.

Parameters of the Induction Motor:

Rating: 1hp, 3-phase, 4-pole, 220V, 3.8A, 50Hz, 1390rpm.

Stator referred parameters at 50Hz: Stator Resistance, R_s = 9.4Ω, Stator Leakage Inductance, L_{ls} = 0.0338H, Rotor Resistance, R_r = 10.8Ω, Rotor Leakage Inductance, L_{lr} = 0.0389H, Magnetizing Inductance, L_m = 0.4724H,

Parameters of the inverter:

Simulation: Total DC bus voltage = 1kV, Inverter switching frequency = 10kHz.

Experiment: Total DC bus voltage = 800V (highest possible in the laboratory), Inverter switching frequency = 10kHz.

DC bus capacitor per phase = 470μF, 2 in parallel.

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Chapter 4

Generation of Higher DC Voltage from Lower Voltage AC Generator

4.1. Introduction

As discussed earlier, the issues in generating higher DC voltage suitable for transmission are still open. This is especially true for wind power generation, where offshore wind farms are in vogue.

The most popular types of generators employed for wind energy conversion are induction or synchronous generators. They are used in different configurations both in terms of their windings and interfacing power electronic converters. PMSG is gaining more popularity nowadays, due to their low maintenance, lower losses and higher power density [70].

The voltage boost by modulation index or PWM of the switches has a certain practical limit, which should be augmented by other voltage boost methods to achieve higher voltage gain. To generate higher voltage any type of voltage gain anywhere adds to the overall voltage gain, be it in the windings, be it in converter configuration, and be it a transformer with required ratio. If the generator is designed for normal operation in delta connection, its windings can be rearranged in a star connection to be able to deliver a $\sqrt{3}$ times higher voltage. However, for obtaining a DC output, the rectifier components will be rated at high voltages if operated by a simple PWM rectifier.

The work in this chapter proposes a scheme for using a PMSG of a lower voltage rating than that required for the medium voltage DC voltage transmission by using open-end winding, without employing transformers or DC-DC converters in between. Hence, extra weight, floor space requirement, and extra power loss are avoided. This work proposes to utilize individual 1-

The paper entitled "Series Connected Open-End Winding Generator for Higher Voltage DC Supply," in IEEE Transactions on Industrial Electronics," by D. Maiti and S. K. Biswas, accepted for publication in IEEE Transactions on Industrial Electronics (doi: 10.1109/TIE.2023.3288207), is based on the content of this chapter.

phase H-bridge PWM converters for rectifying the AC power generated by each of the three isolated phase windings of PMSG. Each component PWM converter boosts the phase AC voltage to a higher DC bus voltage and these three DC buses are added together in series to obtain further higher total DC bus. Thus, each 1-phase PWM converter requires a blocking voltage of only about ⅓ of the total DC bus voltage.

4.2. Proposed Scheme:

The proposed open-end winding 3-phase Permanent Magnet Synchronous Generator based AC to DC converter system is presented in fig. 4.1. Each of the individual windings of the generator, isolated from each other internally, is connected to a 1-phase PWM rectifier with a capacitor at the DC side. The DC buses of three rectifiers for the three phases are then connected in series with additive polarity. Thus the scheme permits the operation of a synchronous generator of a given voltage rating to generate a DC voltage of higher value than can be normally done by a 3-phase rectifier from the same generator. Conversely, to create a required DC bus voltage, a synchronous generator of a lower voltage rating can be used.

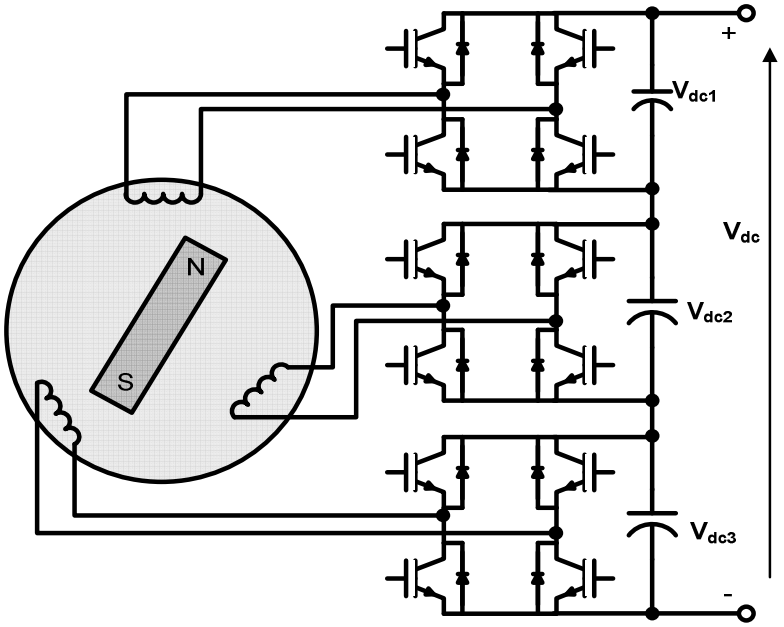


Fig. 4.1: Proposed scheme for open end winding PM synchronous generator for medium voltage dc supply

The total DC bus voltage is generated by using the series connection of the three DC side capacitors that form smaller individual DC buses. Thus, each capacitor on the DC bus can be of

lower voltage rating than the total output DC bus requirement (ideally ⅓ of the total output DC bus voltage). Since the three rectifiers are connected to each phase rated up to the phase voltage, the switching devices (like IGBTs) in the rectifier system are also of lower voltage rating compared to that for the total output voltage of a single 3-phase rectifier. Since the capacitors on the DC side are connected in series and energy is fed to them from the AC side, there is a concern about the capacitor voltage balance, but this topology is shown to automatically maintain reasonable balance when the generator winding voltages have built up.

The inherent type of winding connection of the generator before being converted to OE-PMSG has two options to match the given high DC bus voltage: star of delta connection. If the generator is normally delta connected but now operated in open end mode, the maximum AC current drawn by each 1-phase rectifier is only the maximum phase current of the generator, which is $1/\sqrt{3}$ times the original line current while the total DC bus voltage built up is the highest. Thus, the current rating of the switches becomes lower than what is needed in a normal 3-phase VSI. However, if the generator was normally star connected, each 1-phase rectifier draws the maximum AC current the same as the maximum original line current of the generator while the total DC bus voltage created (for a given boost) is the lowest. However, the voltage rating of the switches is less than that needed in a normal 3-phase rectifier.

Since each rectifier is a 1-phase H-bridge operating with 180° phase shift between its two limbs, the line voltages will contain harmonics. Hence, a suitable PWM switching strategy should be employed to reduce the harmonic currents, mainly zero sequence currents.

For PWM rectifier mode of operation, the minimum DC bus voltage should be:

$$V_{dc} > V_{rms-phase} \times 3\sqrt{2} \times boost\_factor \tag{4.1}$$

For a standard 3-limb 3-phase PWM rectifier with a similar boost factor, DC voltage achievable is given by [11]:

$$V_{dc} > V_{rms-phase} \times \sqrt{3} \times \sqrt{2} \times boost\_factor \tag{4.2}$$

The DC bus voltage achieved using an open-end PMSG and dual inverter (operating as a PWM rectifier) scheme is [59]:

$$V_{dc} > V_{rms-phase} \times \sqrt{2} \times boost\_factor \tag{4.3}$$

Thus higher DC voltage can be achieved by using the proposed scheme from the same generator.

Similar to the case of motor operation as the SVPWM scheme without zero states does not produce any zero sequence voltage, this scheme would not be able to mitigate any zero sequence voltage appearing from some other source in the rectifier/inverter. If all SVPWM states were used as shown in fig. 1.6, the converter produces zero sequence voltage that can be used to mitigate the unwanted zero sequence voltages from other sources. However, in this case, since the generation of fundamental and zero sequence are related to each other, such a scheme to control the zero sequence components would affect the fundamental also. Thus, it would be appropriate if the fundamental and zero sequence are controlled separately. This can be achieved by using Sine PWM with added an zero sequence current control loop.

4.3. Capacitor Voltage Balancing

Each 1-phase rectifier comprises of 1-phase PWM converter operating in boost mode, thus storing energy in the generator winding inductance and then delivering that to the output capacitor and the load. Additional inductors, if required, may be added externally in series with each winding. Thus, in case of any unbalance in the energy fed to the DC side capacitors, the voltages across the capacitors become unbalanced. This can happen even if the capacitance values are equal. In the case of a practical situation of unequal actual capacitor values (due to tolerances), the occurrence of voltage unbalance is natural. This not only can create problems for the life of the capacitor, but may also generate zero sequence current, and higher torque ripple. Thus capacitor voltage balancing is necessary.

The capacitor voltages can be made to be equal forcefully by modifying the modulation index of the feeding rectifiers separately. However, this will cause an unbalance in the phase currents, thereby producing zero sequence current. This will also introduce oscillation in flux and torque component of current in the case of FOC. Since this causes torque pulsation for the synchronous machine it should be avoided. If it was a case of separate AC-DC converters with DC buses connected in series, the per-phase control was a good candidate. However, in this case, the three phases are not independent but are interrelated for producing the total instantaneous counter torque.

Thus passive or active balancing remains the only option. Suitable resistances of proper

value and wattage should be connected across the capacitors to balance the voltage by absorbing the extra energy delivered to the capacitors. This will help in slow balancing, thus slow dynamics of the rectifier. This may be sufficient for a slow speed change of the generator, when designed properly. However, during load variation which is a power drawing mechanism, the unbalance would be nullified much faster just with parallel resistances. In case of the need for fast transient and fast balance, choppers with damping resistance should be put across individual capacitors and the chopper switches should be controlled accordingly to reduce the voltage differences between individual DC buses.

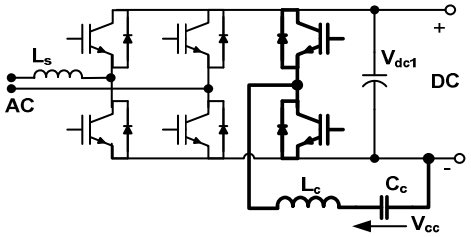


Fig. 4.2: DC bus double frequency ripple reduction scheme.

Single phase rectifier output voltage will have double frequency ripple voltage, which usually is mitigated by increasing the DC bus capacitor size, increasing the size of the overall converter, and hampering the life of the converter due to the limited life of bulk electrolytic capacitors. If the ripple voltage is not reduced, this may increase the current harmonics in the rectifier input. Thus, a suitable scheme should be employed to reduce the voltage ripple as well as the bulk capacitor usage. One such scheme is shown in fig. 4.2 [71], using a buck-boost type converter with its own energy storage capacitor and an inductor. The ripple voltage of the rectifier DC bus can be reduced by utilizing the energy stored in capacitor C_c. As estimated by the authors, there can be a reduction of DC bus capacitor size by a margin of around 12.

4.4. Performance Evaluation by Simulation

The active rectifier system was simulated using MATLAB. A dynamic model of PMSG was developed in the synchronous reference frame to incorporate the zero sequence computation circuit following the modeling procure described in chapter 2.

The PMSG under experimentation has an emf constant of 0.01476 V/rpm, a parameter

also used for the simulation. In the simulation, different values of the DC bus voltage were generated to study the behavior of the generating system. The values of the individual DC bus capacitance were made to differ by around 10% from one another in this study.

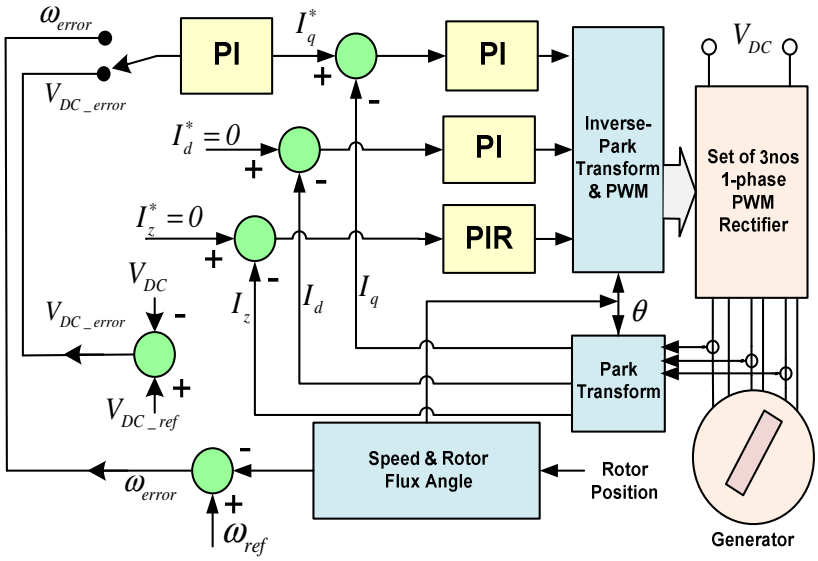


Fig. 4.3: FOC Control loop structure with a zero sequence current control loop

The converter was simulated both for MPPT operation of the PMSG and for load-supporting mode i.e., maintaining a regulated DC bus with variable load. In both cases, rotor FOC of the PMSG was performed, keeping the d-axis injected current to zero. The structure for both the FOC operations is shown in fig. 4.3 with respective feedback quantities. A zero sequence current control loop is added to the controller, to limit the zero sequence current [53, 72].

The built-in MATLAB model of a variable speed wind turbine was used for the simulation of the wind power MPPT operation involving the PMSG. The mechanical power available from a variable speed wind turbine is [73-75]:

$$P_{turbine} = 0.5\rho A C_p(\lambda,\beta) v^3 \qquad (4.4)$$

where, ρ is the air density, A is the area swept by the rotor blades of the turbine, v is the wind speed, C_p is the coefficient of the power conversion, which again is a non-linear function of tip speed ratio λ and pitch angle β. Power conversion becomes maximum, when C_p is maximum.

The tip speed ratio is expressed by:

$$\lambda = (\omega_m R') / v \tag{4.5}$$

where, ω_m and R' are the rotor angular velocity and radius respectively. It should be noted that the PMSG, if directly coupled to the turbine, will also have the same angular velocity.

For fixed pitch turbine operation, C_p is maximum when λ is at the optimum. Thus optimum angular velocity is given by:

$$\omega_{m-opt} = (v\lambda_{opt}) / R' \tag{4.6}$$

Eq. (4.6) is used to set the speed reference for the PMSG so that maximum power can be extracted.

In fig. 4.3, I_z^* is the zero sequence current reference, which should be kept zero. A PIR controller is used to restrict the zero sequence current with transfer function as [53]:

$$G_{PIR}(s) = K_p + \frac{K_i}{s} + \sum_{h=3,9,15..} \frac{K_{rh}\omega_{ch}s}{s^2 + 2\omega_{ch}s + (h\omega_o)^2} \tag{4.7}$$

where, K_p, K_i, are the proportional and integral gains, K_{rh} is the zero sequence current regulator gain for h harmonic, $h_{\omega o}$ is the resonant frequency of h-harmonic and ω_{ch} is the cutoff frequency. To incorporate the command from the zero sequence current control loop, SPWM switching was used.

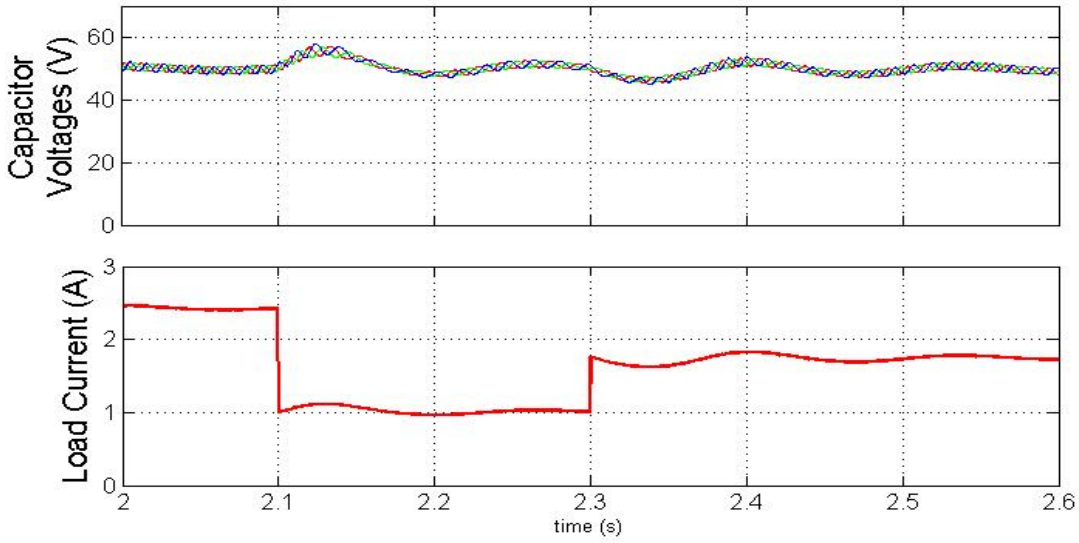


Fig 4.4: Capacitor voltage variation with change in load current, with a constant voltage operation of the PMSG in the proposed scheme

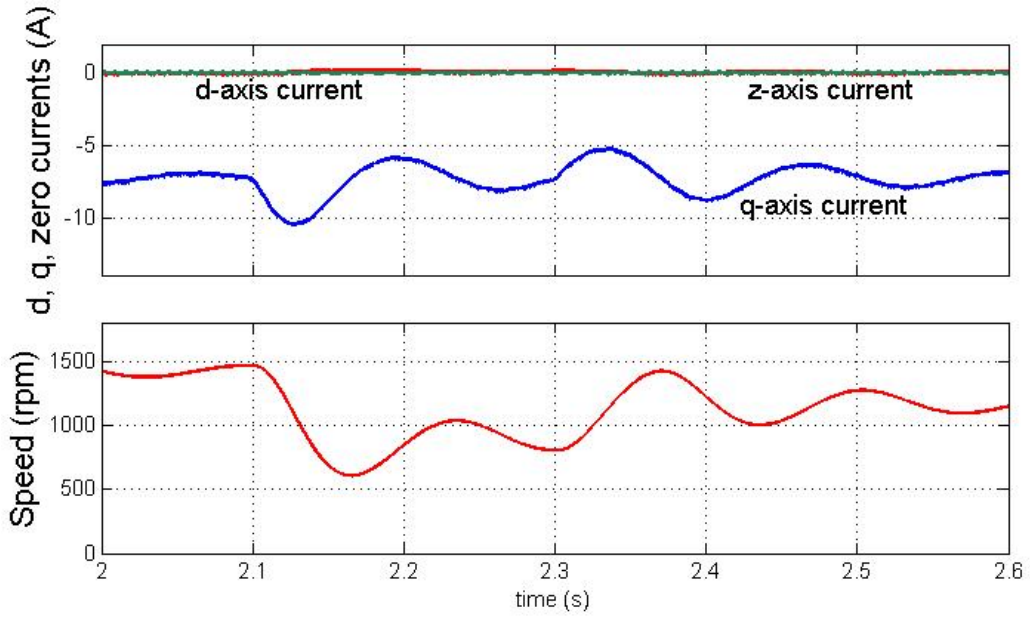


Fig 4.5: d, q, zero axis current for constant voltage operation of the PMSG

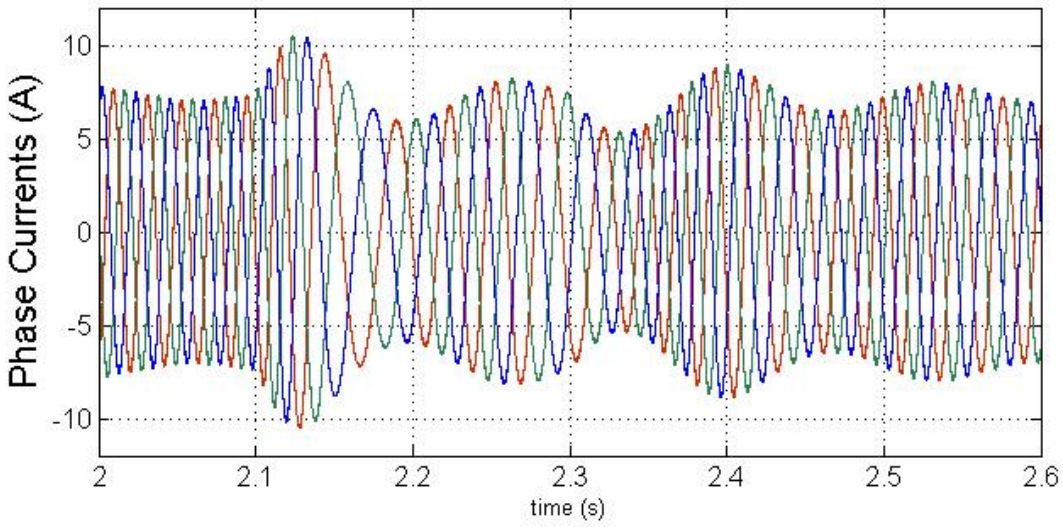


Fig 4.6: Three phase currents of the PMSG in constant voltage mode of operation

Fig. 4.4 shows the simulated voltage across the DC bus capacitors with respect to the variation in load current during load supporting mode of operation. It can be seen that even with a step change in load the three voltages remain balanced with only passive balancing although the capacitance values were different. Fig. 4.5 shows the *d*-, *q*-, zero axis current for the load change shown in fig.4.4. As discussed earlier, the *d*- and zero axis currents are maintained to be

zero. In this case, only the *q*-axis current changes with the change in the load, which changes the opposing torque, produced by the PMSG, thereby the speed. Fig. 4.6 presents the phase currents of PMSG for load supporting mode with load variation. In fig. 4.4 due to boost converter dynamics, the output voltage oscillates with a change in load, resulting in the oscillation in the *q*-axis current of the generator, hence also in its phase current.

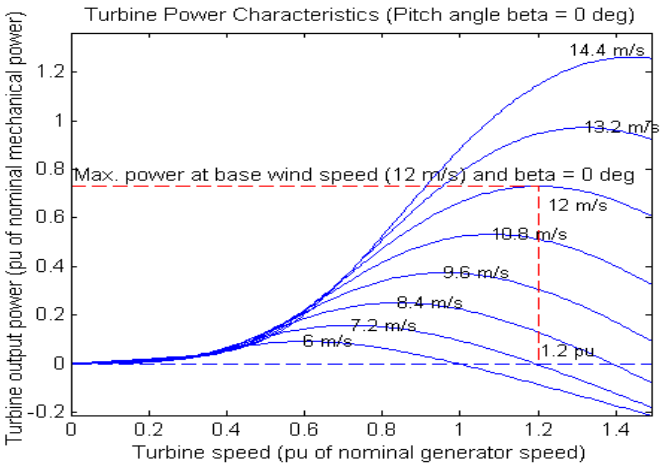


Fig. 4.7: Power-speed characteristics of wind turbine used for simulation.

The wind turbine power-speed characteristics for different wind velocities are shown in fig. 4.7, which are generated from MATLAB Simulink Wind-turbine block for a constant pitch angle of zero. Fig. 4.8 depicts the MPPT operation of the PMSG-wind turbine system driven by the turbine with characteristics shown in fig. 4.7. The speed waveform shows the reference speed dictated by the MPPT calculation system taking into account the wind speed to extract maximum power. The trace shows that PMSG follows the reference speed and increased speed increases the power generation. The emf trace shows the per phase induced emf of PMSG at different speeds.

The *d*, *q*, *z* current trace in fig. 4.8 shows the *d*-, *q*- & *z*-axis currents for the MPPT operation. For the FOC operation, the *d*-axis current is maintained at zero value as can be verified from simulation. The *q*-axis current is dictated by the speed controller and for higher speed the *q*-axis current is higher. The *z*-axis current is also maintained at zero through the use of a *z*-axis current controller to avoid zero sequence current.

The next trace in fig. 4.8 shows the power factor at the PSMG stator terminal and thus at

the rectifier input. As the current increases, the power factor at the terminal reduces due to the per-phase lagging impedance. The capacitor voltages and the load current are shown in the last two traces of fig. 4.8. It can be seen that the capacitor voltages remain balanced even with the change in speed although the capacitance values differ.

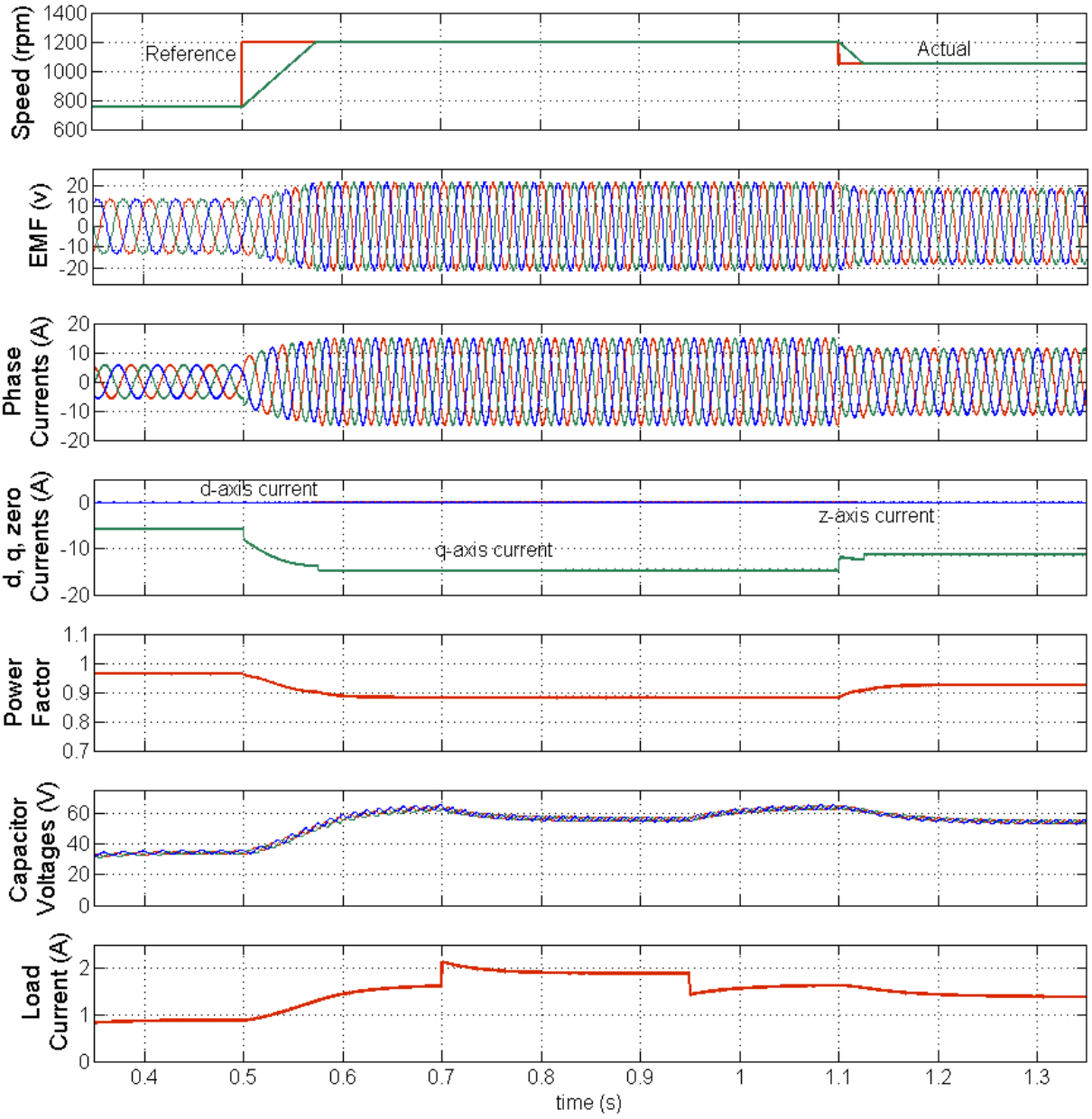
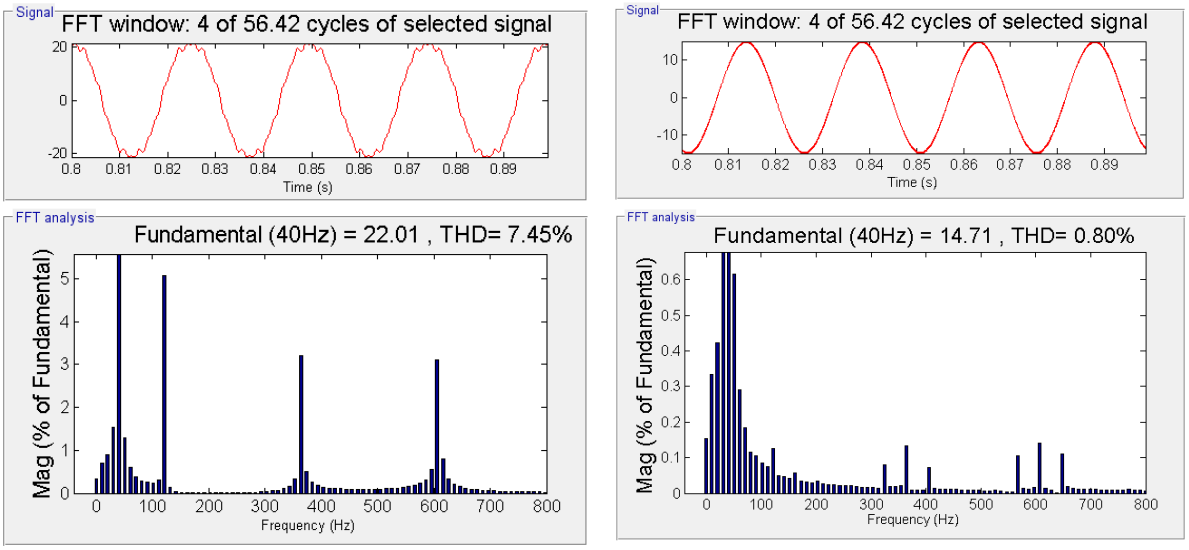


Fig 4.8: MPPT operation of the PMSG driven by a wind turbine

A load change during MPPT operation is shown in fig. 4.8. As can be seen, there is a

change in load at 0.7s and again at 0.95s. It can be seen that no change in speed, induced emf or phase currents occur. Only the capacitor voltage and thereby the total DC bus voltage changes, keeping the total power delivery unchanged. Thus, in the case of a grid connected converter connected to this DC bus, it is the role of the former to maintain the DC bus by drawing the proper level of power.



(a) (b)

Fig. 4.9. (a) Induced emf from the simulation study and its FFT; (b) Simulated phase current and its FFT

The FFT of the induced emf is shown in fig. 4.9(a) having THD=7.45% while Fig. 4.9(b) shows the FFT plot of one phase current of the PMSG having THD=0.8%.

4.5. Experimental Performance Evaluation

A prototype inverter was fabricated in the laboratory for experimentation and validating the performance of the proposed scheme. For this, the values of the capacitance were made to differ by around 10% from one another.

Experimentation was done using an available PMSG of 1hp (rating as the motor) with the specification given at the end of the chapter, with each of its star connected winding opened and connected to separate 1-phase PWM rectifiers. The total DC bus voltage was controlled at 150V

in voltage regulation mode supporting the load. The PMSG was driven by a 200V, 1hp DC motor.

A Texas instruments TMS320F28377S board was used for the FOC control. The speed was measured and the position of the PMSG was sensed by a 10 bit absolute encoder.

The DC bus capacitors were damped by 150kΩ resistances. The individual capacitor voltages were fed back to the microcontroller for over-voltage protection but only the total bus voltage was used for voltage control. Both DC bus voltage control and speed control operation (suitable for MPPT) were carried out. Unipolar Sinusiodal PWM switching was used for the control of the rectifiers. A zero sequence control loop was used to control the zero sequence current as in eq. (4.7).

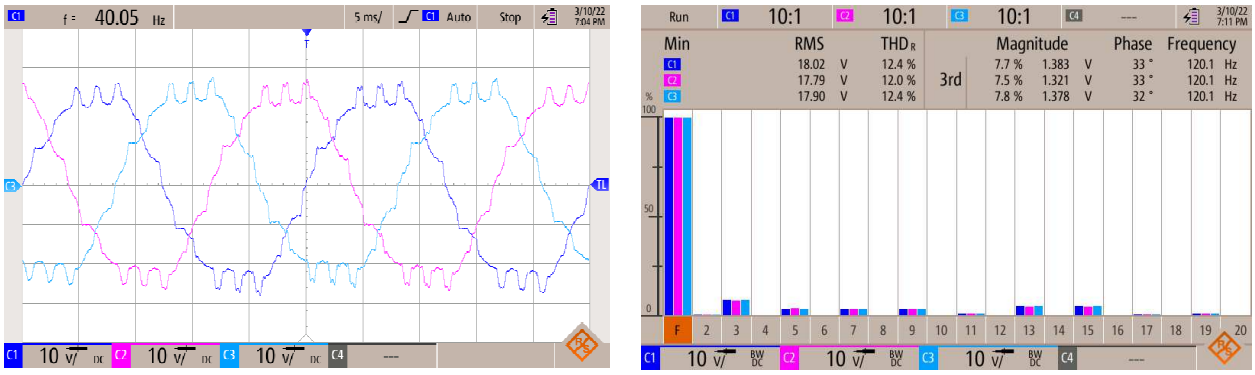


Fig 4.10: Three phase emfs of the PMSG used for experimentation, FFT of the induced emfs

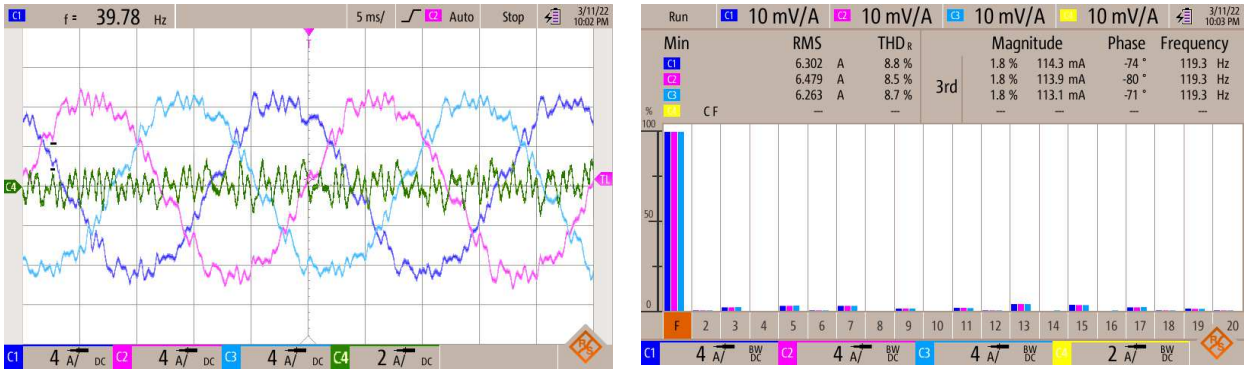


Fig 4.11: Three phase currents of the PMSG with their FFT

Fig. 4.10(a) shows the no-load induced emf per phase of the PMSG and its FFT in fig. 4.10(b). A significant amount of harmonics are found to be actually present. The flux density distribution in the PMSG is influenced by factors like winding distribution, type of magnetization, arrangement of magnets, shape of magnets, and tooth saturation and these may result in harmonic fluxes, which create harmonics in induced emf [53]. Fig. 4.11(a) shows the per-phase currents and the zero sequence currents for the FOC operation of the PMSG with the proposed converter. It is to be noted that the zero sequence current is measured by passing the three phase wires through the same current probe, thus the theoretical current is ⅓ of the measured value. Fig. 4.11(b) shows the FFT plot of the phase currents. The zero sequence current can be seen to be restricted by the zero sequence loop, without which the THD may go beyond 60%.

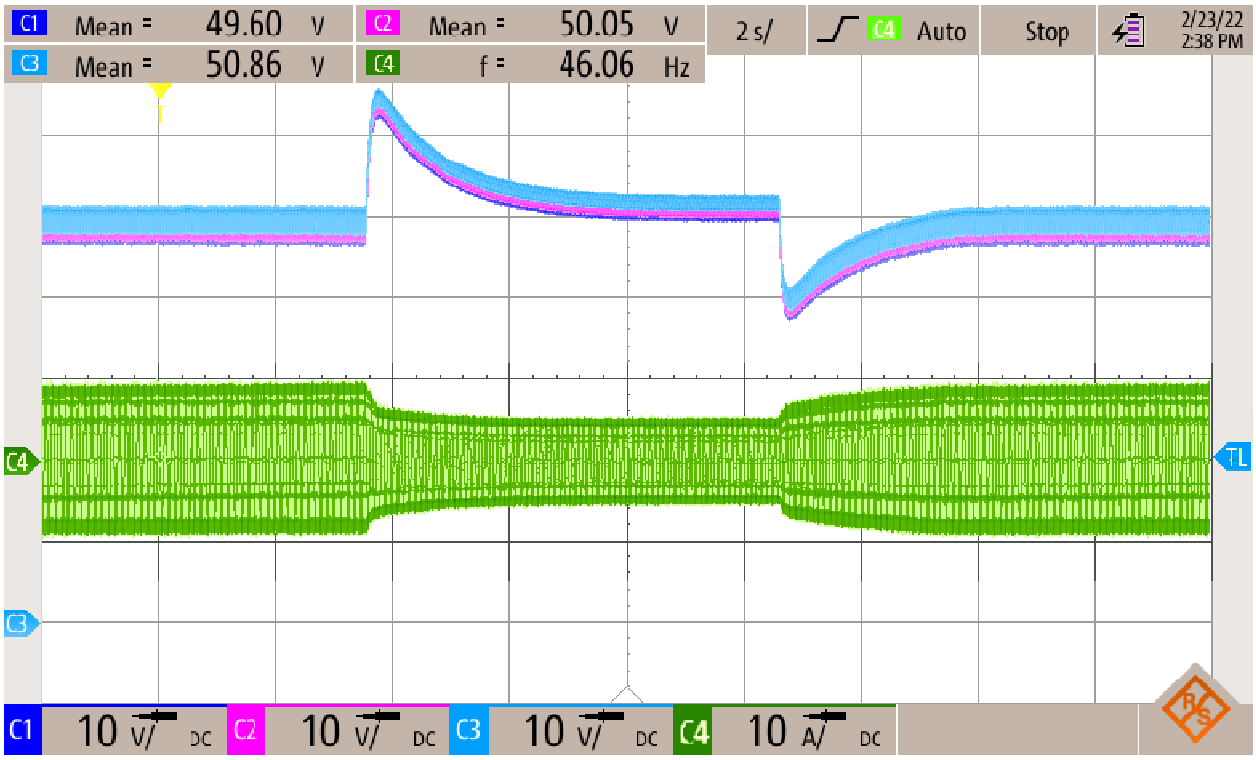


Fig 4.12: Capacitor voltage and one phase current for constant voltage mode operation

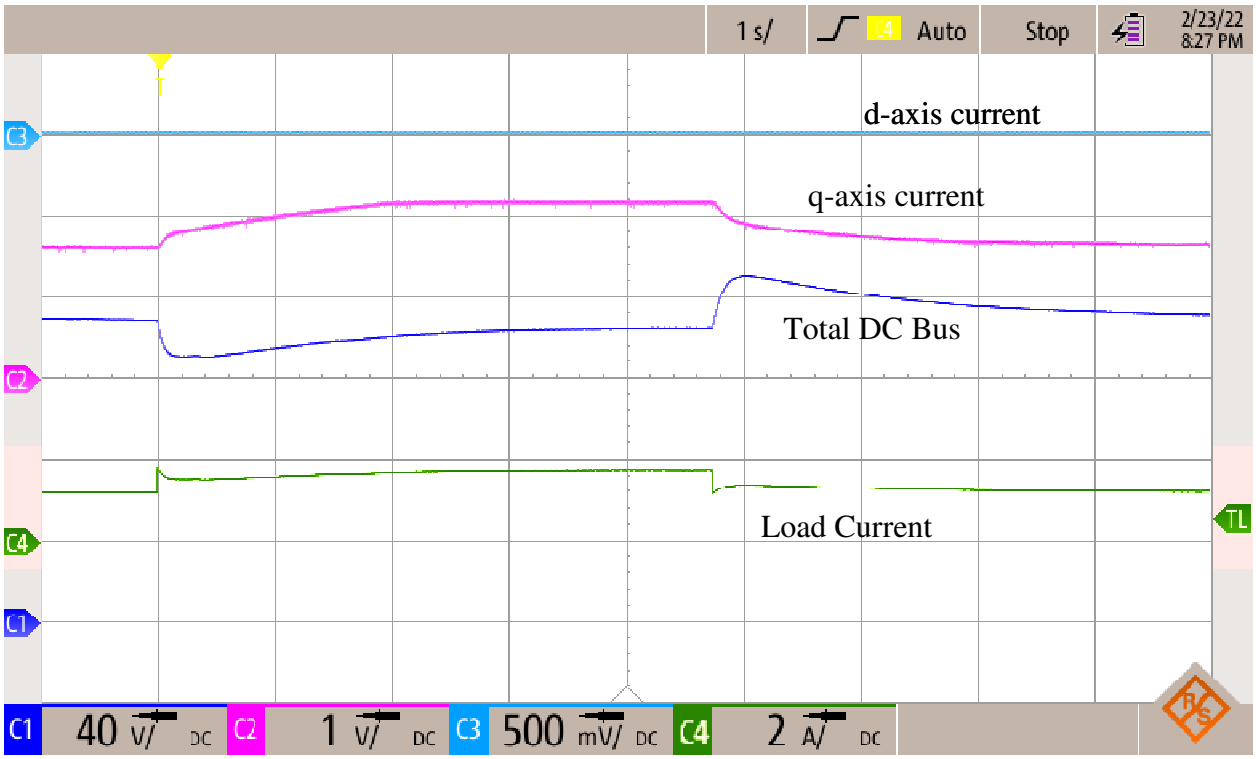


Fig 4.13: d, q, zero axis currents for a load change in constant voltage mode operation. Channel 1: total DC bus voltage, channel 2: q-axis current, channel 3: d-axis current channel 4: change in load current.

Fig. 4.12 shows the experimental results for DC bus voltage regulation operation, which may be required for isolated DC source operation for load supporting. The figure shows the variation in individual capacitor voltages and change in the phase current for change in the load. The load current is increased and then reduced to show the run-time voltage balancing of the capacitors. The capacitor voltages remain balanced at one-third of the total DC bus voltage value. Double harmonic ripple on the capacitor voltages can be seen with respect to the average voltage. Fig. 4.13 shows the total DC bus voltage, d-, q- axis currents with the variation in load current shown in the same figure. Although the capacitor voltages have some voltage ripple on them as seen in fig. 4.12, since they are 120° phase shifted from one another, the total DC bus voltage is almost ripple free. Under a steady state, the DC bus remains constant irrespective of the load current. However, the response of the converter is a bit sluggish due to the presence of mechanical inertia as well as the boost mode operation of the converter, which has a right-half plane zero. This dynamics also shows that despite the difference in capacitor values, the DC

voltages across them do not have significant deviation. It was observed that a slow dynamics balances the capacitor voltages naturally. However, a fast change in the voltage may cause voltage differences. Fast balancing of the significantly different voltages requires extra balancing resistances which can be turned on and off depending upon the requirement. However, in voltage mode control, due to overall control, the capacitor voltages remain reasonably balanced.

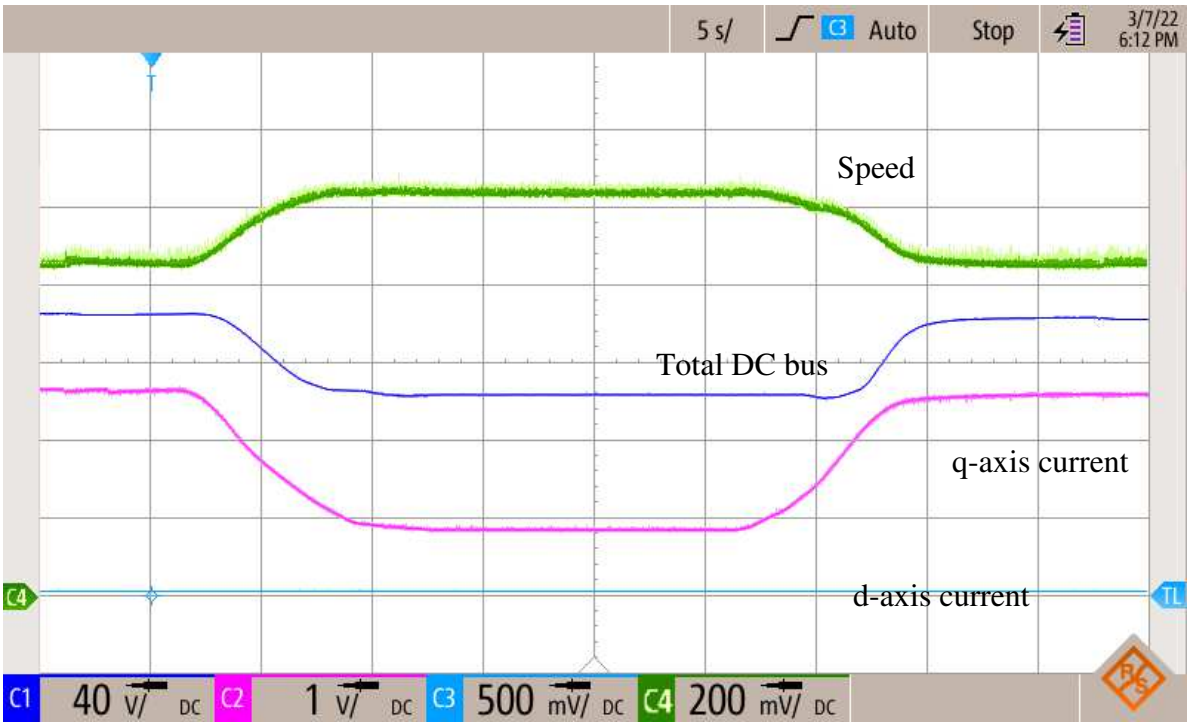


Fig 4.14: Speed control mode, speed variation from 900 rpm to 1050rpm and back: Ch. 1: Total DC bus voltage (40V/div); Ch. 2: q-axis current from DAC (1V/div); Ch. 3: d-axis current from DAC (0.5V/div); Ch. 4: Speed change from 900 rpm to 1050 rpm and back;

Fig. 4.14 shows the speed control operation of the PMSG by changing the speed reference. The speed was ramped from 900rpm to 1050rpm then reduced to 900rpm again. As the PMSG is driven by a separately excited DC motor, in order to increase the speed of the motor, PMSG produced counter torque should be reduced. Thus there is a reduction in *q*-axis current as the speed increases and this also reduces the output voltage of the converter. Moreover, as the possible variation in speed by torque variation is small for a separately excited DC motor the speed control limit in this case is small when the DC motor is supplied by a constant voltage. The *d*-axis current in both fig. 4.13 & 4.14 remains zero as dictated by FOC current control.

Fig. 4.15 presents the experimental setup used in the laboratory for this experiment. The top part shows the rectifier structure and the bottom part shows the PMSG coupled to w DC motor and the encoder.

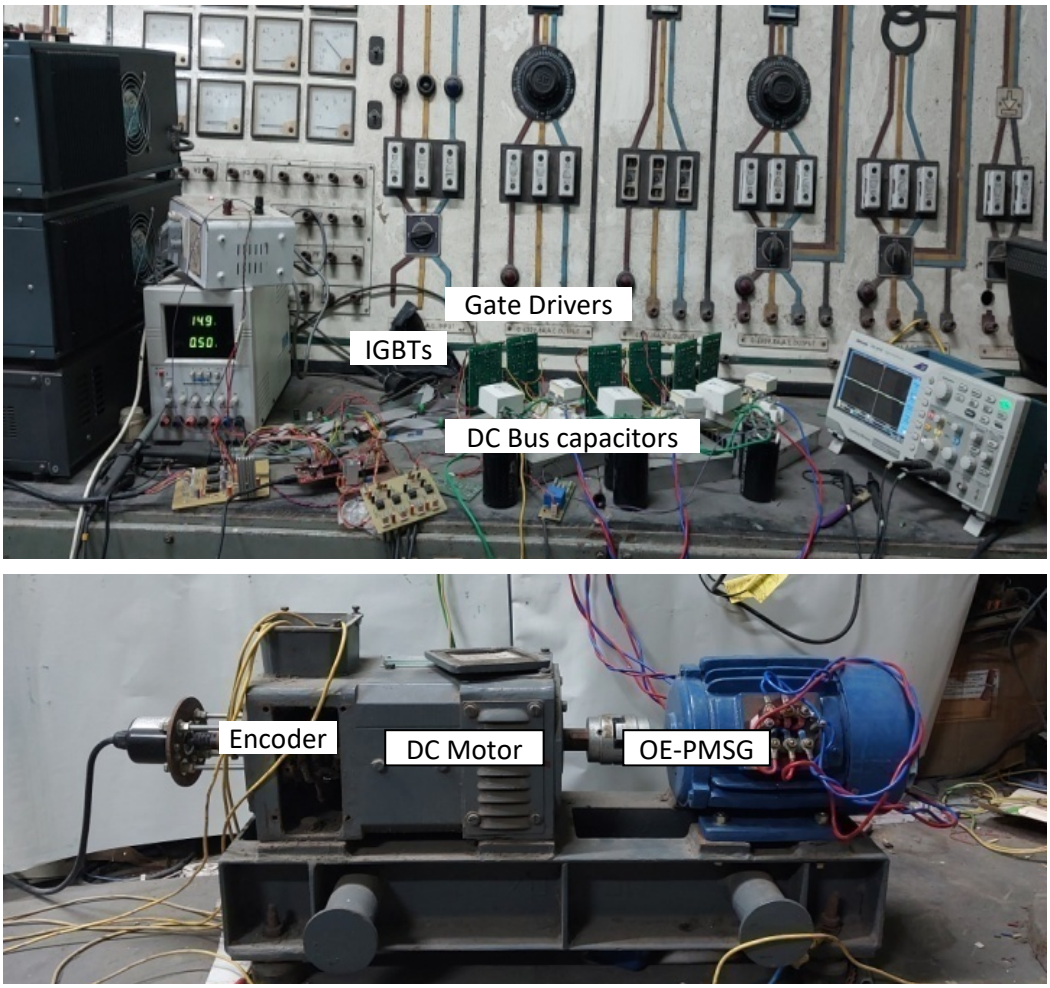


Fig. 4.15. Experimental setup.

4.6. Conclusion

A new scheme is proposed for the generation of medium to high DC voltage from a lower voltage rated 3-phase generator, suited for off-shore wind application. There is no need for full power rated step-up DC-DC converter or transformer which would have incurred extra power loss, space and weight. The scheme uses the Open End Winding technique for a PM generator with one 1-phase PWM rectifier connected to each isolated winding. The output DC bus of each of the three 1-phase rectifiers is connected in series to form the higher voltage outgoing DC bus. Contrary to existing 3-phase alternatives, this scheme utilizes low voltage rating switches and

capacitors and permits operation over a wide range of modulation index to create a higher total DC voltage bus from the same machine. In the case of an originally delta connected generator, the rectifier switch current rating is also lower. Compared to conventional schemes with same DC bus voltage, the generator to be used in the proposed scheme will be of lesser size and weight due to lower insulation requirement following a lower voltage rating. However, a control over the zero sequence current flow through each phase winding is required that has been incorporated. The performance of the proposed scheme has been demonstrated in both constant voltage mode and speed control mode (for MPPT operation).

System Parameters used for simulation and experiment:

PMSG specification:

Phase voltage: 24V, Phase current: 10A,

Stator winding resistance: 0.9 Ω,

X_d : 2.8mH; X_q : 3.6mH; X_0 : 0.5mH

Other specifications:

DC bus capacitance per phase: 470μF, 450V; 4 in parallel.

Converter switching frequency : 10kHz

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Chapter 5

Conclusion and Future Scope

5.1. Overview and Conclusion

The investigation in the present work is on topologies, one as an inverter and another as a rectifier. These two also involved different machines namely an induction motor and a permanent magnet synchronous generator.

The first scheme involving an inverter circuit driving an induction motor is suitable for operating from high voltage DC voltage, where the induction motor rated voltage may be lower. The induction motor is an OEIM, with each phase winding driven by an individual single-phase inverter. The open-end winding can be created by opening the star/delta connection of the three phase machines. Thus, it requires no special winding scheme. The DC bus of the inverters are connected in series. Thus for a three phase motor the DC bus voltage for individual inverter is one-third the total applied DC bus voltage. The inverter scheme has advantages compared to the existing scheme namely:

- The scheme is suitable for smooth wider speed variation with a better match for DC to AC voltage.
- Low voltage rating switches and capacitors can be used
- The voltage stress on the motor winding in case of the inverter scheme is lower
- The DC bus capacitor voltages become and remain balanced during normal operation of the inverter due to the inherent voltage balancing

However, due to the presence of a low impedance zero sequence current path in the inverter structure, zero sequence current needs to be limited by a dedicated loop for this current.

The other scheme is for the generation of higher DC bus voltage compared to the existing scheme, from a lower voltage AC generator. Similar to the earlier case of the motor drive, here, the AC generator namely PMSG winding terminals are opened. Each phase winding of the

generator is then connected to single-phase PWM rectifier. The DC buses of the rectifiers are connected in series.

Thus for high-voltage generation, this scheme does not require a full-power DC-DC converter for voltage boosting. Besides, the winding inductance in most cases would be the sufficient for required voltage boost for PWM rectifier operation. This scheme has all the advantages along with the issue of zero sequence current, like the motor drive case of the first scheme. Here, the generator voltage stress being lower the insulation requirement may be lower, thus, the generator size may be lower compared to that required by the conventional scheme of three phase three limb rectifier fed by an AC generator.

In both cases, the performances of the schemes have been validated by simulation as well as experiment.

5.2. Scope for Future Work

The present work on the inverter is on an induction motor drive capable of operating from a higher voltage DC bus. A better match for the DC to AC voltage can be achieved by the converter compared to existing schemes. However, there is a certain limit to this match beyond which the voltage match becomes worse. Thus, work is to be done for a generalized scheme. In the present scenario, further higher DC bus voltage increase in the number of phases of the motor is one option, but the motor would then be specifically designed for this operation. Motor phase winding can be segmented and isolated. Although that does not require a complete new design of the motor, an already fabricated motor requires large modification. In the inverter structure for higher voltage operation multilevel inverter structure can be employed.

Voltage balancing at the starting of the motor may be an issue. Although the inherent balancing mechanism balances the voltage once the motor starts, the initial negative and zero sequence current can be mitigated if a voltage balancing process is applied before the motor starts.

The fault tolerance of the structure can be investigated. With capacitors connected in series and the number of semiconductor modules employed, the chances of fault in bulk capacitors or semiconductor devices increase. Thus, if some fault-tolerant mechanism is found, that would be beneficial for the inverter scheme.

On the rectifier scheme, capacitor voltage balancing needs more study. Although passive balancing keeps the voltages acceptably balanced, there is still a natural tendency for voltage unbalance. Thus a closed loop scheme is required to be established for maintaining capacitor voltage balance.

The controllers for the rectifiers should be designed and tuned properly for the required dynamic behavior. The harmonic mitigation method applied for the rectifier scheme requires further investigation. As can be seen from the experimental results of the rectifier, the THD of the phase currents of the generator is still on the higher side. The literature on similar open-end winding generator-based PWM rectifier has much lower THD reported with the conventional schemes. Thus, there may be some issues with the process of harmonic mitigation, which needs to be taken care of.

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