A NEW NON-ISOLATED DC-DC CONVERTER FOR HIGH VOLTAGE BOOST RATIO

Thesis submitted by

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"Statement of Originality"

I, **Sri Koustuv Sarkar** registered on **19th September, 2016** do hereby declare that this thesis entitled **"A New Non-Isolated DC-DC Converter for High Voltage Boost Ratio"** contains literature survey and original research work done by the undersigned candidate as part of Doctoral studies.

All information in this thesis have been obtained and presented in accordance with existing academic rules and ethical conduct. I declare that, as required by these rules and conduct, I have fully cited and referred all materials and results that are not original to this work.

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Date: 14-09-2023

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CERTIFICATE FROM THE SUPERVISOR

This is to certify that the thesis entitled "**A New Non-Isolated DC-DC Converter for High Voltage Boost Ratio**" submitted by Sri **Koustuv Sarkar**, who got his name registered on **19th September, 2016** for the award of Ph.D. (Engineering) degree of Jadavpur University is absolutely based upon his own work under the supervision of **Prof. Sujit K. Biswas**, Former Professor, Electrical Engineering Department, Jadavpur University and that neither his thesis nor any part of the thesis has been submitted for any degree/diploma or any other academic award anywhere before.

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Prof. Sujit K. Biswas
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Dedicated to

Maa Bhabatarini

&

my Mother

ABSTRACT

The topology of a floating output, voltage boost, non-isolated interleaved buck-boost DC-DC converter is proposed. Without utilization of transformers or coupled inductors, voltages are added symmetrically on both sides of the input DC bus in series, through two 180° phase shifted buck-boost sub-converters operating from each side of the input DC rails. This results in reduction of input current and output voltage ripples. Therefore, semiconductor and passive component ratings are also reduced compared to classical DC-DC boost converters. There is no subtraction of the total input voltage from the output voltages of the sub-converters. Since fraction of the load power flows in directly from the input, each sub-converter does not process the entire output power. This results in minimizing the current & voltage ratings of the semiconductor devices resulting in improving the overall system efficiency. Due to the symmetrical addition of voltages on both sides of the incoming DC bus, the converter that has been proposed can be used to create multiple DC voltage levels for multilevel inverters.

In the linear modulation range, the maximum fundamental voltage that can be generated across the motor terminal is less than the input AC voltage fed to the diode bridge rectifier. Further, supply voltage can dip by about 10%, either momentary or long term, which is common. Thus, it is essential to boost the DC bus voltage to maintain the rated AC voltage at the motor terminal despite the mentioned practical limitations.

A modified topology for efficiently boosting the DC bus voltage in a transformer-less 5-level Neutral Point Clamped (NPC), Voltage Source Inverter (VSI) based Open End Induction Motor (OEIM) drive is shown as the application of the proposed DC-DC boost converter. Out of the four separate voltage levels, the two middle levels are obtained by dividing the input DC voltage using a capacitor voltage divider. The top and bottom voltage levels are obtained from the sub-converters of the proposed DC-DC converter whose generated voltages are kept just sufficient to cater to the boost need, resulting in low additional power loss in the process of boosting the voltage.

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List of Abbreviation

Renewable Energy Source	RES
Government of India	GoI
Photovoltaic	PV
Ministry of New and Renewable Energy	MNRE
Maximum Power Point Tracking	MPPT
Maximum Power Point	MPP
Metal Oxide Semiconductor Field Effect Transistor	MOSFET
Tapped Inductor Boost Converter	TIBC
Electromagnetic Interference	EMI
Classical/Conventional Boost Converter	CBC
Quadratic Boost Converter	QBC
Quadratic Following Boost Converter	QFBC
Buck-Boost Flyback Integrated Converter	BBFIC
Floating Interleaved Boost DC-DC Converter	FIBC
Interleaved Double Dual Boost converter	IDDB
Insulated Gate Bipolar Transistor	IGBT
Continuous Conduction Mode	CCM
Discontinuous Conduction Mode	DCM
Pulse Width Modulation	PWM
Proportional Integral	PI
Printed Circuit Board	PCB
Multi-Input Multi-Output	MIMO
Safety Factor	SF
Voltage Safety Factor	VSF
Peak Inverse Voltage	PIV
Ultra Fast Recovery	UFR
Electric Vehicle	EV
Neutral Point Clamped	NPC
Voltage Source Inverter	VSI
Induction Motor	IM
Hybrid Electric Vehicle	HEV
Total Harmonic Distortion	THD
Phase Disposition-Pulse Width Modulation	PD-PWM
Medium Voltage	MV
Cascade H-Bridge	CHB
Flying Capacitor	FC
Medium Voltage High Power	MVHP
Variable Speed Drive	VSD
Open End Induction Motor	OEIM
Space Vector Pulse Width Modulation	SV-PWM

Chapter 1

Introduction and Literature Survey

1.1 Brief Background and Present Statistics of Renewable Energy Sources (RES)

Electricity is the most acknowledged and the most crucial requirement for human being to survive. The evolution and the enlargement of the country in every sphere is largely dependent on the overall consumption of electrical energy. From the recent statistics it has been reported that India has become the third largest producer of electricity in the world. The consumption of electricity in India is also placed third in the global spectrum. The national electric grid in India has an installed capacity of 416 GW reported till 31st March 2023 [1]. The World Bank research claims that during the period 2010 and 2016 India has come up with electricity to power the houses of 30 million people each year. Although it will be a challenge to extend it to 15% of 1.25 billion of the Indian population which is still under poor infrastructure and has no proper access to electricity. However, India has done extremely well in extending access to electricity to 85% of its huge population and it has set an all-inclusive target for access to electricity for all at the end of 2030 [2][3]. India has a surfeit power generation capability but has a disadvantage that it does not have requisite infrastructure to distribute it. To deal with this issue, the Government of India (GoI) has floated a program named "Power for All" in 2016. The electricity sector in India is hugely governed by fossil fuels, particularly coal. In the fiscal year 2021-22 coal mass-produced about three-quarters of the country's electricity [1]. Although in due course of time the fossil fuel reserve will get drained out and as a result the price is growing at an exponential rate. Due to the above mentioned issues it is extremely important to shift focus to Renewable Energy Sources (RES).

RES often introduced as a clean form of energy. It usually descends from natural sources or processes that are constantly refilled. There are several kinds of RES [4]:

- Solar Energy
- Wind Energy
- Hydroelectric Power
- Biomass Energy
- Geothermal Energy

- Tidal & Wave Energy

In 2015, the government made its objective clear by aiming at a target which comprise of 175 GW energy from renewable by 2022. The intent is to process cheaper and a wider form of energy alternative. The renewable energy industry made a positive impression by belligerently spiking up the magnitude by an annual increment rate of 17.5% during the period 2014 and 2019 and strengthening the allocation of renewables in India's total energy mix from 6% to 10%. Present day scenario states that the installed capacity of the RES is of the order of 83 GW. There is a further program where 31 GW is under process and an additional 35 GW which is placed under tender. India has emerged as one of the top contenders for clean energy manufacturers in the global map. In due course of time looking at the advancement, the revised aim is installing 225 GW energy purely from renewable sources by 2022 and to reach a target of 40% clean energy by 2030. [5]

From all these energy sources Solar Photovoltaic (PV) has emerged as one of the most distinguished non-conventional energy sources. It is thriving in the recent era due to the reasons which follow as (a) it is accessible in abundance (b) inexhaustibility (c) cleaner and quieter operation (d) there is trimming in the price of the solar PV modules (e) research initiatives have been carried out due to the reduction in cost and increased efficiency of the power electronic converters required for the expulsion of the solar power and (f) government is encouraging and has been granting money to help the sector grow [6-8].

The annual report on National Solar Mission (2022-23) published by Ministry of New and Renewable Energy (MNRE) GoI states that as on 31.12.2022 a 63.3 GW of solar energy has been installed which includes installation in ground-mounted, rooftop and from off-grid systems. Additionally, a capacity of around 51.13 GW is in the stage of implementation and 31.4 GW is under tendering stage. It is expected that the solar power projects of capacity around 15 GW will be commissioned during the Financial Year (FY) 2022-23 [9].

1.2 Stand Alone System Based on Solar PV for Rural Deployment

There is still a large gap in infrastructure in rural areas in the sector of electricity as extension of grid is not economically feasible. This leads to a hindrance in the overall growth of the country. So, to deal with this issue the main target is the formation of RES based stand alone /off-grid systems in the rural areas. Solar PV system has been considered as the most favourable component for the following reasons (a) it is perfect for small-scale and isolated

applications, (b) placing of PV panels is not at all an issue in the rural areas, (c) India receives high level of solar insolation and (d) PV panels does not require constant maintenance. The load for such stand alone systems is single phase household appliances in the range of 250-500VA.

1.3 Vital Issues Regarding Designing a Stand Alone Scheme Based on Solar Photovoltaic

The basic block diagram of a typical solar PV based stand alone system along with the voltage levels are shown in the Fig.1.1. In the figure P_{PV} is the power from PV source, P_B denotes the battery power and P_L is the demand load power. The power output of a solar PV is sporadic in nature so it is necessary for a storage element which will balance the power between the PV modules and the demand from the load side [6]-[8]. The above mentioned storage element is mainly a battery bank. There is also requirement of a power electronic converter in a stand alone scheme to interface amongst PV panel, battery and the AC side load. It generally interfaces one DC-AC converter and two or more DC-DC converters. Here the DC-AC converter is of prime importance as the solar PV and the storage elements are in DC form whereas the load requires AC power.

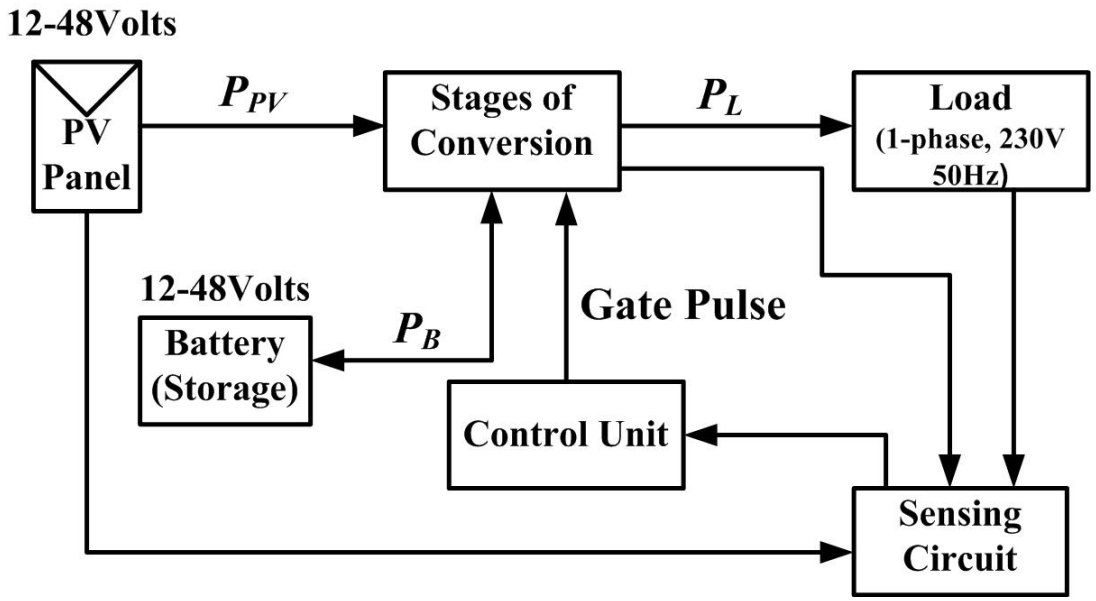


Figure 1.1: Schematic for a basic stand alone system

The function of DC-DC converter is to draw maximum power from the PV panel and to protect the battery from getting overcharged or discharged. There is another purpose of DC-

DC converter which is to realize high boosting capability.

1.3.1 Requirement of DC-DC converter

The standard voltage level for the AC appliances used in household services is 230V. This results in maintaining the voltage at the input of the DC-AC inverter around 360-400V, if a conventional full bridge inverter is taken into consideration for DC-AC conversion. Here the high boost voltage can be achieved by selecting PV panel and battery of higher voltages. Stepping up the PV panel voltage and that of the battery makes the design and installation complicated. There is also an issue regarding the personnel and equipment safety [10]. Taking into point that ramping up the PV voltage requires a sizeable amount of PV modules to be connected in series. This condition will lead to depletion in power because different modules connected in series will experience varying operating conditions. The voltage level of the battery can also be incremented by connecting several batteries in series. However, the employment of large number of battery bank will increase the cost as well as the size of the system. So, to keep the reliability of the system on the higher side the PV panel and the battery bank are kept in the range of 12-48V. This leads to high voltage requirement which can be fulfilled by intermediate power electronic converters. High gain can also be accomplished by the help of low frequency step-up transformer at the AC side of the inverter. But this will lead to increase in weight, cost and volume of the system. In order to reach high voltage or achieve high gain (in the order of 8-15) intermediate high gain DC-DC converters are essential which interface between the PV panel, the battery and the DC link of the inverter.

Integrating the above mentioned issues and concluding that the major opposition in designing and implementing a PV based stand alone system and operating it with a battery as a storage element are as follows:

1. Maximum amount of power that can be extricated from the PV panel at variable operating conditions (insolation level, temperature and loading conditions)
2. Allocation of bidirectional power flow for the battery.
3. Conversion of DC-AC.
4. Supplying with requisite amount of voltage gain as the voltage level(s) of PV panel and the batteries are usually clamped to a certain low value for domestic applications.
5. A competent control strategy which steers it through different operating modes which a typical stand alone system encounters.

Hence from the above points it can be identified that ramping up the voltage gain is

essential. The incremented gain can accomplish a voltage level suitable to be fed to the DC link of the standard inverter circuit. The voltage level should also be stable. While inverters are specifically utilised to convert DC to AC, inverter will be unable to produce the required boost. Hence, either power frequency transformer is prerequisite at the AC side of the inverter or a non-isolated DC-DC converter at the DC input of the inverter. The scheme employing transformer has advantages in providing electrical isolation, averting DC current flowing into the grid, resulting in increased safety. However, the incorporation of a low frequency transformer increases the overall weight and volume of the system and decreases the reliability of the overall system. Therefore, non-isolated DC-DC converter topologies are favored in spiking up the voltage levels.

1.4 Stand Alone Configuration Engaging DC-DC Converter for High Gain

Several stand alone schemes have been reported in the literature where a non-isolated DC-DC converter has provided the prerequisite boost voltage that is necessary.

One of the schemes is a four stage configuration shown in Fig. 1.2. The diagram shows a four stage configuration where three DC-DC converters are used. Out of the three converters one of them i.e. DC-DC converter ‘A’ is employed in Maximum Power Point Tracking (MPPT), second bidirectional converter depicted as DC-DC converter ‘B’ is used in charging and discharging of battery and the final one step-up DC-DC converter ‘C’ is used solely for voltage boosting purpose [11]. When a PV panel collects solar radiation it produces power. The current versus voltage can be obtained by plotting it graphically (I-V curve) and the point is identified in the graph where it produces maximum power. This particular point is isolated as the maximum power output of the PV panel.

It is important to set a tracking system because it will increase the power output of the solar panel and will lead to maximize its efficiency [12],[13]. MPPT engages a DC-DC converter which interfaces the PV module and transfers the maximum power to load. Several established algorithm already reported in literature is used to vary the duty cycle of the DC-DC converter to change the load impedance and emulate it with the Maximum Power Point (MPP) of the source to transfer maximum power [14],[15].

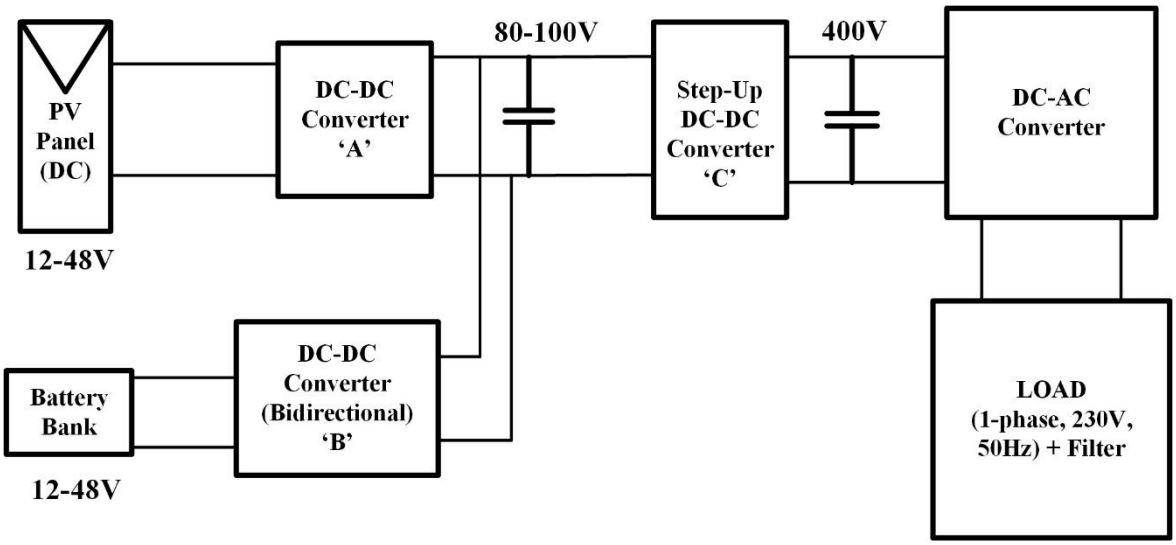


Figure 1.2: Rudimentary four-stage framework

Although the configuration shown is suitable for a stand alone system, but there are some shortcomings of the scheme. The greater number of conversion stages will invariably diminish the reliability and efficiency of the overall system as the number of component count increases. There is depletion in battery charging efficiency as there are two converters present in the battery charging path. The DC-DC converter 'A' used for MPPT control remains inactive when the PV power is low. So, keeping a check on the above mentioned issues a three stage configuration is shown in Fig. 1.3 where a single DC-DC converter is present between the PV panel and the battery charging path as a result increasing the battery efficiency [16].

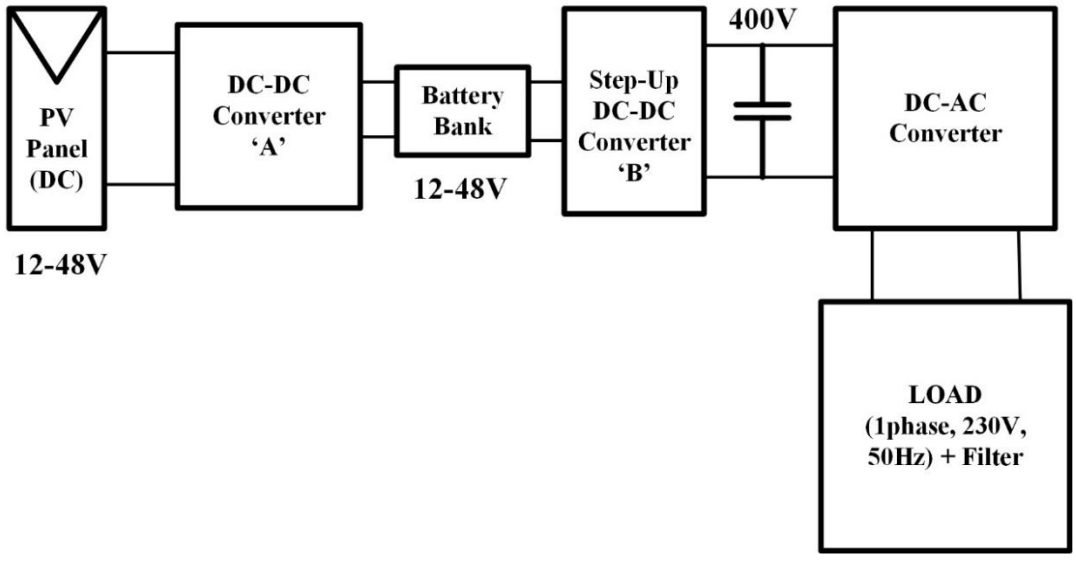


Figure 1.3: Three stage framework with battery bank incorporated in cascade

Here the DC-DC converter has to be designed carefully as the converter single handedly is responsible for the voltage gain, if the battery bank voltage is not high. So, from the above schematic it can be decided that intermediate converter with high step-up characteristics is very essential in the stand alone structure. Therefore, in the thesis the high step-up DC-DC converter will be taken up as the main form of study and analysis. Starting from analysis, literature survey, limitations of some of the boost converters will be discussed in the following sections.

1.5 High Gain DC-DC converter

So initially starting with different types of DC-DC converters given below, the preliminary study is formed.

Some of the basic non-isolated DC-DC converters are as follows:

- Step-down (buck) converter
- Step-up (boost) converter
- Step-down/step-up converter (buck-boost)
- $Cu'k$ converter

Out of these four non-isolated converters the main objective is to ramp up the voltage. So, step-up converter or Classical Boost Converter (CBC) is the most fundamental and essential topology in the family of boosts converters (non-isolated).

1.5.1 Classical Boost Converter (CBC)

Fig. 1.4 shows the topology of a step-up converter/CBC. The main property of the converter as the name suggests is to obtain a higher voltage level than what is fed to the input of the converter. There are several applications to this converter but few of the highlights are that it is used in regulated DC supplies and DC motor regenerative braking [17].

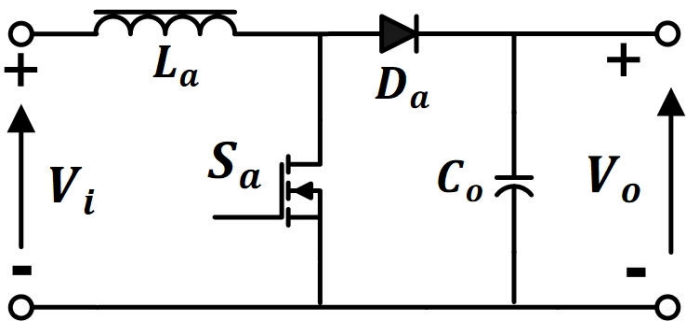


Figure 1.4: Schematic of a Classical Boost Converter

A. Operating Principle

When Switch S_a turned ON

At this instant the diode D_a becomes reverse biased. The load current is supplied by the output capacitor C_o. The input V_i feeds energy to the inductor L_a. The inductor stores energy and the current through the inductor increases.

When Switch turned S_a OFF

During this interval the polarity of the voltage across the inductor L_a reverses. This condition along with the input voltage forward biases the diode D_a. The current along the inductor diminishes and transfers the energy to the capacitor C_o and the output load.

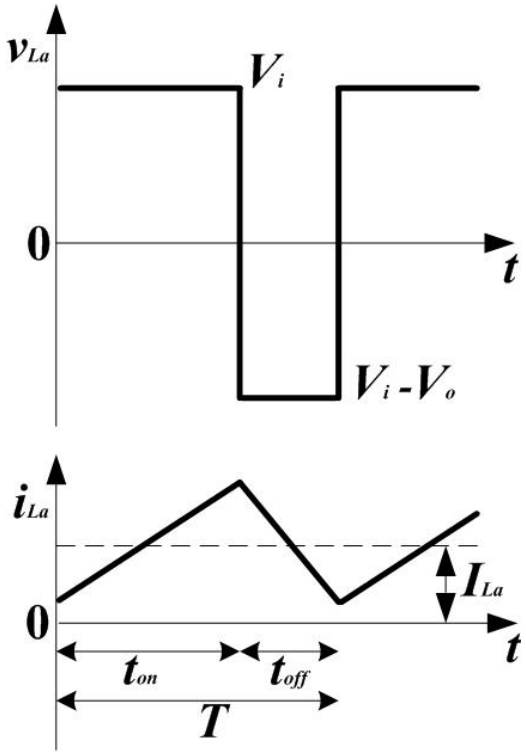


Figure 1.5: Inductor voltage and current waveform during Continuous Conduction Mode for CBC

From the Fig. 1.5, during steady state the time integral taken for the inductor voltage over one time period will be zero.

Therefore $V_i t_{on} + (V_i - V_o) t_{off} = 0$ (1.1)

From equation number (1.1)

The voltage gain of CBC is given as: $\frac{V_o}{V_i} = \frac{1}{1-D}$ (1.2)

Where, V_O is the total output voltage.

V_i is the input voltage fed to the converter.

D is the duty ratio of the converter.

I_{La} is the average inductor current

Duty Ratio= $D = \frac{V_o}{V_i} = \frac{t_{on}}{t_{on} + t_{off}}$ (1.3)

Here, t_{on} is the time during which the switch remains ON.

t_{off} is the time during which the switch remains OFF.

And $T = t_{on} + t_{off}$ (1.4)

T is the total time period.

The boost converter can achieve the target voltage level but it has several limitations. The drawbacks are:

1. High duty cycle is mandatory for high voltage applications.
2. Instability of closed loop control at high Duty Ratio due to sharp rise in voltage gain.
3. Reduced Efficiency.
4. Reverse recovery problem of the diode used in the boost circuit.
5. Voltage stress across the switch is high. So switches with higher $R_{DS(on)}$ is required.
6. Higher level of conduction losses due to high $R_{DS(on)}$ of the switch.

The $R_{DS(on)}$ described in point 5 and 6 indicates the drain to source on resistance. It is the drain to source resistance of the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) switch (considering MOSFET is used in Boost hardware topology). $R_{DS(on)}$ is directly proportional to the square of the voltage blocking capability. As discussed in point number 5 rise in $R_{DS(on)}$ increases the conduction losses (I^2R loss) which implies the decrease in overall efficiency of the converter[18],[19].

To illustrate the point 1 in the above mentioned drawback section. A curve is plotted with Voltage Gain versus Duty Cycle for CBC. The Fig. 1.6 shows the plot, where it has been vividly seen that with increase in the boost voltage there is a significant jump in the duty ratio. A point is marked on the plot which signifies the claim that for a gain of 10 the duty

ratio has risen sharply to 0.9 which is very close to unity. Extreme duty cycle operation for obtaining the voltage gain is the originator of several difficulties. It brings into the picture the parasitic element associated with the passive components which can degrade the gain value at high duty cycle. The current and the voltage stress across the semiconductor elements also rises to significant level leading to diminishing the overall efficiency of the converter [20],[21]. Taking an example to understand the role of parasitic element better, if the internal resistance of the coil is considered it is observed that with duty ratio approaching towards unity the gain value degrades significantly. Although the parasitic element does not play a significant role when the duty ratio is at around 0.5, this proves as the duty cycle reaches a high value the parasitic elements of the passive components pose a threat to the efficiency of the converter [24].

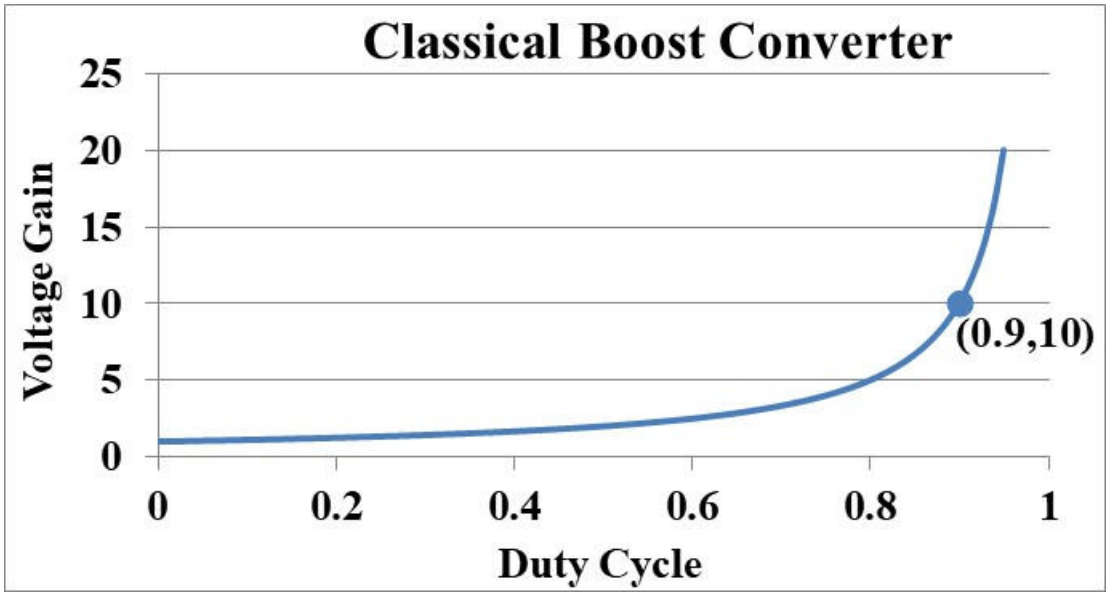


Figure 1.6: Voltage versus Duty Cycle of a CBC

There are several boost topologies apart from CBC which is very well articulated in various research studies. From several boost topologies one of the most highly researched boost topology is the Tapped Inductor Boost topology. Here in the next section the circuit will be studied and explained with various literature references.

1.5.2 Tapped Inductor Boost Converter (TIBC)

The Fig. 1.7 shows the topology of TIBC. It is very favorable topology where the inductor of the boost converter is tapped like an autotransformer either at the switch or at the diode.

Tapping the inductor has the convenience that the converter duty cycle at the operating

point can be rearranged to achieve a distinctive value at which the device utilization will get enhanced. The tapped versions are categorized mainly into two types [22]:

- Switch tapped- Here the switch is linked to the point where the inductor is tapped and not to one of the extreme points of the inductor.
- Diode tapped- Similarly here the diode is linked to the tapped point of the inductor and not to any of its end.

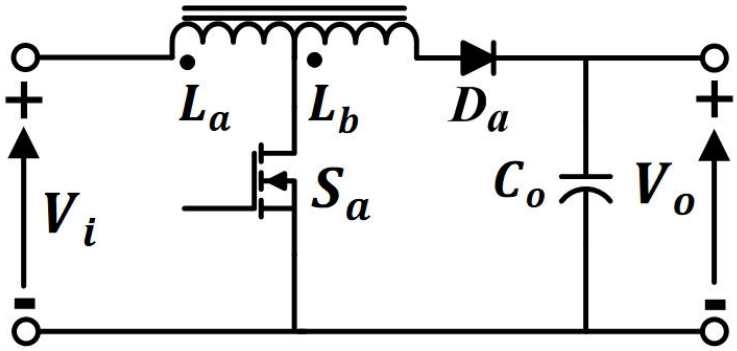


Figure 1.7: Schematic of a Tapped Inductor Boost converter

Through TIBC a boost capability can be obtained without extreme duty cycle requirement and lower amount of stress on the semiconductor devices. The boosting in this topology is of a higher level as the inductance involved during discharging has an inflated value because it is considered as equivalent. It can be observed in the converter working principle. The operating principle of the TIBC is explained below [23].

A. Operating Principle

When Switch S_a turned ON

In the duration of conduction of switch S_a, the diode D_a becomes reverse biased due to the reverse polarity of voltage across the inductor L_b. The input feeds the inductor L_a and the energy is stored in it and there is an increase of current through the inductor.

When Switch S_a turned OFF

At the instant of turn OFF of the switch, the diode D_a starts to conduct and the energy which was stored in the inductor L_a now starts to discharge through both the inductors L_a and L_b.

The voltage gain of TIBC is given as: $\frac{V_o}{V_i} = \frac{1+\left(\frac{N_2}{N_1}\right)D}{1-D} = \frac{1+ND}{1-D}$ (1.5)

Where, N_2 is the number of turns in the inductor L_2.

N_1 is the number of turns in the inductor L_1.

D is the duty ratio of the converter.

TIBC can achieve the high boost but it has some limitations which are discussed below:

1. Leakage inductance will be present as in practical inductors there will considerable amount non-ideal coupling. This non-ideal flux coupling between the two coils gives rise to high voltage spikes across the semiconductor devices leading to considerable amount of losses.
2. The peak to peak ripple for the input current is higher compared to a conventional boost converter.

Extensive research has been conducted in this domain to deal with the shortcomings of TIBC. Various techniques have been employed to combat this above mentioned issues and it is very distinctively articulated in various research papers.

In [24] a single switch topology is proposed where two taped inductors are employed along with diodes and capacitor to attain the boosting capability. The topology is rearranged further in such a way such that it retains the same boosting capacity but the stress across the semiconductor devices is reduced. The high voltage spike due to non-ideal flux coupling also gets diminished to lower level. At around 0.5 duty cycle it is able to deliver high gain and in addition the current stress across the switch reduces which enables it to improve its efficiency.

The steady state performance of TIBC is analyzed. Comparison has been done between a TIBC and CBC on same output parameters such as output voltage and output current [25]. It has been noted theoretically that taking into account the parasitic parameters generated from the various components in the circuit, TIBC has a higher gain value than CBC when operating under same duty ratio. Thus, the efficiency of TIBC tends to be higher than CBC operating under similar parameters. Experimental results also confirmed the theoretical claim that TIBC offers better voltage gain and efficiency under equivalent parameter selection.

Here a topology is proposed that cascades a traditional boost converter and connects a TIBC in series for maximum voltage boosting capability. In order to increment the boost

voltage, the duty ratio and the turns ratio is simultaneously used. This increases the boost capability to manifold compared to a traditional converter [26].

A boost converter along with a tapped inductor has been introduced to negate the input current ripple. A capacitor and inductor aids in reducing the input current ripple in the circuit, without increasing the Electromagnetic Interference (EMI) and degrading the reverse recovery problem of the diode. The tapped inductor can be easily registered by attaching an extra tap in the main inductor of the Classical/Conventional Boost Converter (CBC) [27]. The weight and volume of the converter remains lower compared to the CBC with an input LC filter, as the inductor and the capacitor does not handle the total power. A soft switched tapped boost converter is proposed [28]. Here the soft switching has a wide operating range and function under a wide duty ratio and varied load conditions. The voltage stress across the active switch is below the load voltage and the current stress is also below permissible limit. The topology can be utilised in power factor correction circuits due its wide operating range.

As TIBC is one of the many boost topologies, there are several other non-isolated converter topologies that produce the boost voltage which is required without much complication. Another boost topology which can provide a considerable amount of gain without much duty cycle requirement is the Quadratic Boost Converter (QBC) which is discussed in the following section with its benefits and voltage gain.

1.5.3 Quadratic Boost Converter (QBC)

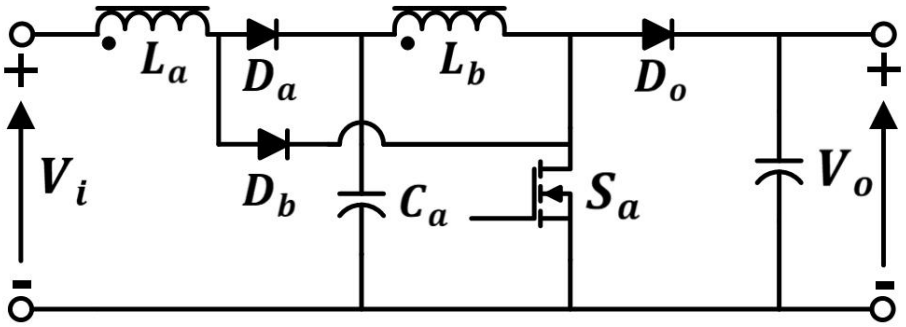


Figure.1.8: Schematic of a Quadratic Boost Converter

Fig. 1.8 shows the QBC topology. In QBC the voltage conversion ratio is related to the duty ratio in a quadratic way. This leads to a very high voltage conversion ratio which is desirable. QBC is arranged in such a way such that two CBC converters are connected in

cascade providing the high gain which amounts to high conversion ratio and efficiency. The QBC is basically a single switch topology which provides an advantage compared to cascading two boost converters. Here as QBC is a single switch topology as the other switch is replaced by a diode the driver circuit requirement also vanishes which in turn enhances the efficiency and diminishes the complexity of the total system [29],[30].

A. Operating Principle

When Switch S_a turned ON

The diode D_a gets reverse biased due to the opposite polarity of the inductor L_a. The input V_i provides energy to the inductor L_a. As the diode D_b is forward biased the inductor current flows through the diode D_b to the switch. The capacitor C_a discharges to the inductor L_b so the energy is stored in L_b. The capacitor C_o discharges to the load and the diode D_o is reverse biased.

When Switch S_a turned OFF

The diode D_o is forward biased due the polarity change in the inductor L_b. The energy which was stored in L_b discharges to the output. Diode D_b gets reverse biased and the inductor current ramps down and flows through the capacitor C_a and L_b. The inductor current of the inductor L_b flows to the output via the forward biased diode D_o.

The voltage gain of QBC is given as: $$\frac{V_o}{V_i} = \frac{1}{(1-D)^2} \qquad (1.6)$$

Here D is the duty ratio of the converter.

The equation number (1.6) shows that the voltage ratio is dependent on the square of the duty cycle. This leads to a very high step-up gain for the converter. However, the major hindrance in QBC is that the voltage and the current stress across the switching device are quite high.

In [31] a topology is proposed which is built on the idea of QBC. Here the conversion ratio is ramped up by integrating coupled inductor and switched capacitor technique. A clamped capacitor is inserted in the switch path to clip the voltage across it. The efficiency of the converter increases as the leakage energy of the coupled inductor could be revitalized.

High voltage can also be acquired by integrating a voltage multiplier with the standard

QBC [32]. The major limitation of QBC is the voltage stress is very high across the switching devices. The stress across the semiconductor device can be restricted to a permissible level by employing this topology.

QBC has the ability to ramp up the voltage gain but the conversion ratio becomes sensitive at high duty ratio. This brings forward controlling factors which deteriorate at higher duty ratio range. So, a Quadratic Following Boost Converter (QFBC) is proposed [33]. The circuit comprises of three capacitors and diodes, two switches and two inductors. A duty ratio increase will give rise to the voltage gain, maintaining a balance in the high duty ratio range but with less sensitivity. The voltage gain of the converter is given as:

$$\frac{V_o}{V_i} = \frac{1 - D + D^2}{(1 - D)^2} \tag{1.7}$$

Here D is the duty ratio of the converter.

The gain equation number (1.7) for QFBC differs with gain equation number (1.6) for QBC in the numerator part which brings in the extra gain for the converter.

A quadratic boost converter is proposed with a voltage gain that is quite high and possesses reduced voltage stress at the semiconductor devices [34]. Here an additional coupled inductor is integrated to the circuit to increase the gain. Clamp circuit has been included to nullify the effect of leakage inductance as there is presence of coupled inductors. Similarly, a quadratic converter in combination with coupled inductor topology is discussed [35]. Higher voltage gain can be obtained along with reduction in the voltage stress. Quadratic buck-boost converters are proposed with wide range of conversion ratios [36]-[38]. The converter topology [36] possesses low input current and quadratic gain characteristics. The gain of the converter can be further expanded with the help of diode capacitor multiplier cell circuitry. The inductor size also diminishes with the reduction in input current ripple, which serves as a merit to this topology. In [37] the topology can operate as a quadratic boost as well as quadratic buck converter. The wide range of conversion ratio allows the converter to have a broader application range (battery charging, UPS etc). Wide conversion spectrum can be achieved without operating the converter at extreme high or low duty cycle. If the converter had to operate under extreme duty cycle then there would be various issues which are specifically discussed in section 1.5.1.

Voltage lifting technique can also be applied to step-up the output voltage. There are various research works on the voltage lifting technique. This topology has been broadly discussed in the next section.

1.5.4 Voltage Lift Techniques

Voltage lift techniques are widely accepted and extensively used in electrical circuits to provide the vital boost requirement. As earlier it was discussed in section 1.5.1 that the presence of parasitic elements vigorously affects the efficiency of the converter at higher duty ratios. Various research work claims that voltage-lift techniques productively elevate the efficiency of the circuit. The positive output Luo converters works as a step-up DC-DC converter derived from the prototype employing voltage-lift technique. The topology produces higher conversion ratio that in turn results in escalating the efficiency [39]. The elementary circuit is shown in the Fig. 1.9.

A. Operating Principle

When Switch S_a turned ON

At this instant the inductor L_a stores energy which gets supplied from the input V_i. Inductor L_b absorbs energy from both the input and the capacitor C_a. Both the inductor currents increase.

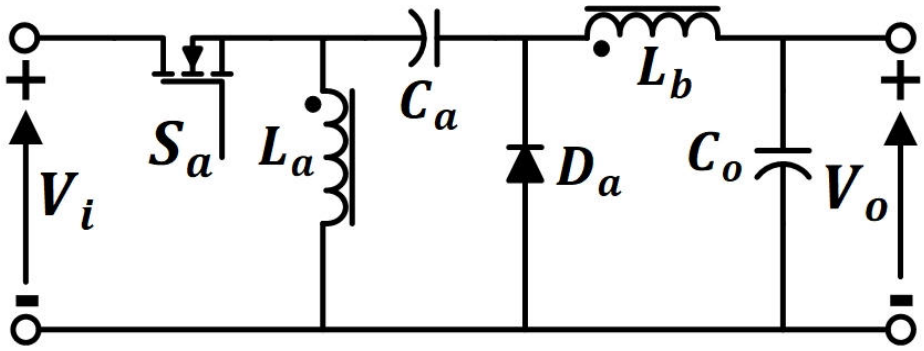


Figure 1.9: Elementary circuit of a Positive output Luo converter

When Switch S_a turned OFF

The inductor current from L_a flows through the freewheeling diode D_a to charge the capacitor C_a. L_a transports its energy which is stored to the capacitor C_a. The current from the inductor L_b also flows through C_o, D_a and load. So, both the inductor currents start to reduce.

The voltage gain of the elementary circuit is given as: $\frac{V_o}{V_i} = \frac{2}{1-D}$ (1.8)

Here in equation number (1.8) D is the duty ratio of the converter.

There are several other positive output Luo converters which are derived from the elementary circuit shown in the Fig. 1.9. Some of them are the self-lift, re-lift and the multiple lift circuits.

In the self-lift topology a diode and a capacitor which are added to the original circuit for voltage lifting function. The task of the capacitor is to raise the capacitor voltage by source voltage. The Re-lift circuit is acquired from the self-lift circuit. Here an inductor, diode, switch and a capacitor is added into the circuit. The capacitors in the topology raise the capacitor voltage to twice the source voltage [39].

The voltage gain of the re-lift circuit is given as: $\frac{V_o}{V_i} = \frac{4}{1-D}$ (1.9)

Addition of inductors, capacitors and diodes to the re-lift circuit, multiple lift circuit can be achieved. By multiple lift circuit it means the capacitors can be made to function to increase the voltage at the capacitor to be three times or four times the source voltage.

The voltage gain of a triple-lift circuit is given as: $\frac{V_o}{V_i} = \frac{3}{1-D}$ (1.10)

And the voltage gain of a quadruple -lift circuit is given as: $\frac{V_o}{V_i} = \frac{4}{1-D}$ (1.11)

In [40] a super-lift boost topology is discussed where a high voltage transfer gain is acquired. The converter topology is discussed in various steps such as the rudimentary circuit along with the re-lift and the triple-lift circuit. From the circuit derivation it is seen the voltage gain increases as the stages change from elementary to the triple-lift level in geometric-progression.

A voltage lift technique by employing the $Cu'k$ converter is proposed [41]. As seen in the earlier voltage lift schemes this circuit is also classified into self-lift, re-lift and multiple lift circuits. The proposed topology greatly enhances the output voltage gain. The converter also is able to repress the effects of parasitic framework and refrains from taking a very steep value of duty ratio. High efficiency and lesser amount of ripple are observed in the elementary circuits.

However, to increase the voltage boost level additional number of diodes and capacitor are added to the elementary circuit. This aids in increasing the voltage boost but the circuit becomes complex. So, several other boost topologies reported in literature are examined thoroughly that provide a higher boost ratio.

A high step up DC-DC converter had been proposed [42], where the high gain is achieved

by dual coupled-inductors. Here a parallel connection of the structure is made at the input which aids in reducing the input current ripple. Filter capacitor of smaller value is required at the input. Higher gain can be achieved by the input parallel and series output structure along with the dual coupled inductors. Soft switching minimizes losses in the switches and diodes. An active clamp effectively minimizes the voltage spike of the main switches and the energy in the leakage inductor is also recycled with the help of a passive snubber. Two switches are employed in establishing the active clamp.

A soft switched coupled inductor based scheme [43] had been introduced to acquire a high voltage gain. The converter topology accomplishes high gain requirements together with minimizing the voltage stress on semiconductor devices. A clamp circuit is formed with an auxiliary switch and capacitor employed lowers the impact of voltage spike in the semiconductor switches due to the leakage inductance. A voltage doubler circuit is incorporated that enhances the ability of the converter scheme to obtain an enhanced voltage gain in a convenient and easier way.

A coupled-inductor SEPIC DC-DC converter presented [44] achieves an elevated voltage gain in an effective and energy efficient way. The semiconductor count to accomplish the required voltage gain is also reduced. The voltage stress across the semiconductor components is also alleviated. However due to the use of coupled-inductors there will be presence of leakage inductance which compromises the efficiency at various loading conditions which have not been dealt with.

A Buck-Boost Flyback Integrated Converter (BBFIC) had been presented [45]. The topology consists of a single active switch which has the credit of coherent power structure and control design. In the topology mentioned the energy stored in the coupled-inductors is used in the flyback mode to charge capacitors connected in series in order to accomplish a high output gain. As opposed to the earlier topologies discussed in [42-43] where more than one switch is used. The energy stored in the leakage inductor is reprocessed without an active clamp or snubber circuit. It helps in attaining higher conversion efficiency and the topology becomes simple.

In [46] a quadratic buck-boost converter is suggested, where lower number of semiconductor component is employed to achieve the large amount of voltage gain. However, there in this converter topology there is a high input current ripple which is a major drawback and the issue is also not addressed and probable solution is not provided.

Another non-isolated high step up/step down bidirectional converter is presented [47], where a dual active half bridge DC transformer is integrated to a non-isolated buck-boost

bidirectional converter to accomplish a high voltage boost. However, the scheme uses cascaded converters processing full power along with a transformer, leading to sacrifice in efficiency.

Increase in voltage gain can be attained by Floating Interleaved Boost DC-DC Converter (FIBC) [48]. It has two interleaved boost modules linked together to have parallel input and series output formation. As discussed in [42] this scheme also accomplishes low input current ripple as the input is connected in parallel and low output voltage ripple due series output framework. The high step up voltage gain is also accomplished due to the connection of the (boost) modules in series at the output. The floating output double boost converter reported in [49] also has similar characteristics and it accomplishes high output voltage gain.

The Interleaved Double Dual Boost Converter (IDDB) [50] is a similar topology which also can achieve high voltage gain. It employs multiple phase shifted FIBC structures to have parallel input formation. The procedure of interleaving contributes in improving the input ripple current by lowering its amplitude.

Many more IDDB schemes catering different applications have been discussed in the literature [51]-[56]. Like in [53] an idea has been explored where an CBC employed in hybrid electric vehicle for boosting purposes can be replaced by IDDB. In [54] the control design and modeling of IDDB is executed such that it can be applied to fuel-cell application. The IDDB topology focuses on high boost purposes along with diminishing the quantity of ripple simultaneously in the input current and the output voltage [55].

However, these converters [48]-[56] have an output voltage which is the sum of the two individual converters but with the input voltage being subtracted. Hence, all the converters process more power than what is actually required by the load.

The converter having two interleaved boost structure is shown in the Fig. 1.10 for further mathematical analysis in the following section.

1.5.5 Interleaved Boost DC-DC Converter

In the Fig. 1.10 an interleaved boost DC-DC converter is shown. There are two boost converters which are interleaved. Interleaving signifies judicious connection of several switching devices for which the conversion frequency is similar but the switching instants are consecutively phase apart for equal fraction of the total switching instant. Interleaving reduces the ripple amplitude and increases the ripple frequency [57]-[61]. It is beneficial as it diminishes the filtration requirement and as a consequence increases the efficiency of the total system.

The positive bus converter consists of switch S_a, inductor L_a, diode D_a and the capacitor C_a. The output voltage of the converter is V_a. The negative bus converter consists of switch S_b, inductor L_b, diode D_b and the capacitor C_b. The voltage output for the converter is V_b.

The two boost modules are interconnected in parallel at the input and there is a gate pulse given to the gate of the switches which are phase shifted. The high gain is obtained due to series connection at the output and the voltage ripple at the output also diminishes to a significant level. The boost modules operate at identical duty ratio. So, it is presumed that the output voltages V_a and V_b of the respective converters are same.

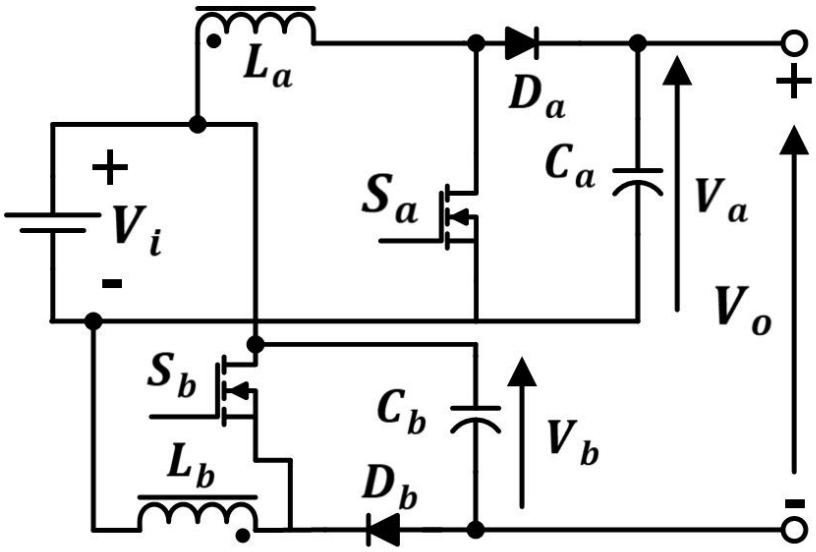


Figure 1.10: Schematic of interleaved boost DC-DC converter

From the Fig. 1.10 the output voltage can be expressed as: $V_o = V_a - V_i + V_b$ (1.12)

If it is assumed that $V_a = V_b = V_c$ (say) (1.13)

Hence, the total output voltage of the converter is given as: $V_o = 2V_c - V_i$ (1.14)

The Fig. 1.11 shows an interleaved boost DC-DC converter where modification is done in accordance with equation number (1.13).

Hence, from the output voltage equation (1.12) & (1.14) it can be seen that the input voltage V_i gets subtracted from the sum of the individual converter voltages as earlier stated in section 1.5.4. This leads to the fact that all the converters process more amount of power through each boost modules than what is actually required by the load.

From the equation number (1.12) the overall voltage gain of the IDDB converter can be further mathematically obtained as:

$$V_o = \frac{V_i}{1-D} - V_i + \frac{V_i}{1-D}$$
$$V_o = \frac{V_i - V_i + V_i D + V_i}{1-D} \tag{1.15}$$

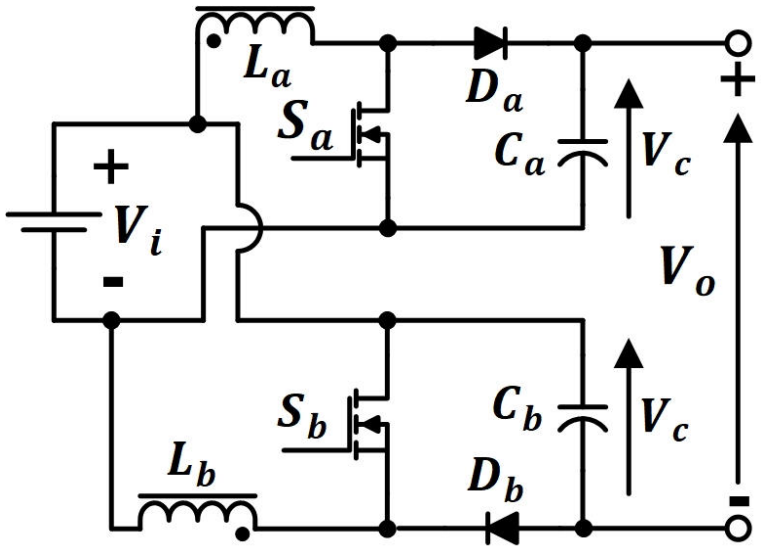


Figure 1.11: Modified diagram of interleaved boost DC-DC converter

From equation number (1.15) the voltage gain of interleaved boost DC-DC converter is:

$$\frac{V_o}{V_i} = \frac{1+D}{1-D} \tag{1.16}$$

This leads to the prime objective of thesis problem formulation. The focus will be to come up with a new topology which will deal with the existing issues regarding various boost/high voltage conversion topologies pointed out in literature survey which are already used extensively in various research areas.

1.6 Objective of the Thesis Formulation

So, the objective of the thesis is to build a boost topology that can contribute in the following aspects:

- High step-up voltage gain characteristics.
- Attaining a reasonably high efficiency.
- Building a non-isolated topology (benefits discussed in section 1.3.1)

- The structure should be economically viable.
- The system should be lower in size and weight.
- The input current and the output voltage ripple content should be at a low value.

In this thesis, a unique topology of a voltage boost non-isolated DC-DC converter will be designed, analyzed and presented. In the proposed topology the voltages are added symmetrically on both sides of the input DC bus in series, using two interleaved buck-boost DC-DC converters operating from each side of the input DC rails. This results in reduction of input current and output voltage ripples while the individual semiconductor and passive component ratings are also reduced. The proposed topology is analyzed and investigated in details.

1.7 Organization of the Remainder Thesis

The research work implemented and executed through this thesis which is arranged in six chapters. Introduction part consists of a background study and present statistics involving RES. The solar PV system deployment in rural areas and its drawbacks while employing it in stand alone structure is explained. The requirement of high gain DC-DC converters in existing stand alone framework has also been brought forward. Relevant literature survey on high gain DC-DC converter topologies is presented and elaborately discussed throughout **Chapter 1**. From there the prime objective of research work, thesis formulation and problem designing has been conceptualized and further processed through experimental and mathematical analysis in the chapters to follow.

Chapter 2 leads to the thesis problem designing and analysis. Here a new buck-boost derived non-isolated floating output topology is presented. The operating principle is explained with voltage expression for various passive components and semiconductor devices. The voltage gain of the topology is analyzed and expressed in this section. The conduction states of the converter (both in Continuous Conduction Mode & Discontinuous Conduction Mode) are presented in schematic form and each mode of conduction is explained minutely using mathematical expression. The entire control structure is also depicted properly and discussed in detail.

In **Chapter 3** comprises of the small-signal modeling of the complete topology. Then the parameter selection is implemented for the performance evaluation of the proposed converter. The section consists of the Bode plot of the entire system. The simulation results of the obtained current waveforms for semiconductor components as well as passive

components are also shown. Input and output waveforms for both current and voltage are depicted. To validate the concept experimentally the laboratory prototype results are compared with the simulated results which show the acceptability of the proposed system.

Chapter 4 mainly deals with the comparison of the proposed topology with high voltage conversion ratio converters already explained in the literature survey section. Various voltage, current, voltage gain and ripple components are compared with the presented converter. The comparison is carried out for different duty cycles and the results are presented in tabular form. The effectual nature of the presented converter over the existing high gain topologies are explained in a rational manner. Efficiency curves at different loading conditions are also plotted graphically to show the advantages of the proposed topology. The cascade extension of the proposed converter is also shown. Here the advantages of the cascade form are explained through mathematical analysis as well as with simulated results which proves its higher gain capability.

Chapter 5 deals with the application of the proposed DC-DC converter topology. An energy efficient 5-level Neutral Point Clamped (NPC) inverter based boost inverter topology for transformer-less medium voltage high power Open End Induction Motor (OEIM) drive is proposed. In the proposed scheme, two partly rated DC-DC sub-converters of the Proposed DC-DC converter which generate only the required boost fraction of the voltage are connected to either end of the DC bus. The input DC is divided into two equal parts using a capacitor voltage divider circuit. These four effective voltage sources in cascade serve as the four DC bus for the two five level NPC VSI of the OEIM drive. A substantial amount of power directly flows to the inverter through the capacitor voltage divider circuit and hence the size as well as power loss of the proposed DC-DC converter scheme is much smaller. The voltage generated from the DC-DC sub-converters is lower than the voltage in the capacitor voltage divider circuit, creating unequal step heights in the pole voltage of the 5-level NPC VSI. These unequal steps in the pole voltage of the two VSI of open end drive restrict the use of existing control technique for operating an OEIM drive from a single DC source. A carrier based PWM technique is proposed to restrict the circulating current caused by CMV even when the voltage steps are unequal.

Chapter 6 presents the conclusion and future scope of the thesis work.

Chapter 2

A New Interleaved Boost DC-DC Converter

2.1 Introduction

DC-DC boost converters that are non-isolated in nature dominate the present power electronic sphere due to their implementation and utilization in several wide areas. DC-DC converters particularly those which can augment the available DC voltage to higher level can be employed in applications where overall system is powered by batteries [62]-[64]. Various Renewable Energy Sources (RES) are already discussed in the section 1.1. From the list if solar Photovoltaic (PV) cells are considered, the output of such a PV cell has a very low output DC voltage. Therefore, if step-up DC-DC converter is utilized to hoist the output voltage, the system becomes congruent for inverters (DC-AC) for powering several household appliances [65]-[67]. Higher DC voltage may also be obtained when there is a series connection of several PV cells [68], [69] or with a higher number of series connected storage cells/batteries. Although such an arrangement will lead to diverse types of complications in power yield [70], [71] and also increases the overall size of the system.

In Power Electronics there has been a steady rise in DC-DC converter topologies which are capable of ramping up the DC output voltage. Extensive research study has been conducted in the field of non-isolated boost DC-DC converters acting as an interface between the battery and the DC link of the inverter. The voltage gain proficiency of various topologies were closely monitored in section 1.5 where their working principle was explained and mathematical analysis were done to validate the entire working mechanism. From the study of various single as well as multiple switch topology the issues which crop up during analysis leads to the idea of this particular thesis problem formulation.

In this thesis, a non-isolated voltage boost converter with a floating output topology has been conceptualized. It consists of two buck-boost DC-DC converter structured in an interleaved fashion. The two buck-boost DC-DC modules are positioned in a manner such that there is addition of individual converter output voltages to either side of the input DC bus without the use of transformer or coupled-inductors. The proposed non-isolated DC-DC converter is analyzed schematically and mathematical analysis has been carried in detail in the sections to follow.

2.2 Proposed Converter

In Fig. 2.1 depicts the schematic presentation of the proposed converter system. The topology comprises of two interleaved buck-boost DC-DC converters. The topology consists of switches named S_a & S_b (MOSFET or Insulated Gate Bipolar Transistor (IGBT)), which operates at 180° phase shift along with their associated inductance, diode and capacitor. In the proposed topology, there is addition of each individual converter output voltage to the positive side of the input DC bus or to the negative side of the input DC bus respectively. Therefore, the total output DC voltage can be obtained as the series sum of individual converter output voltages with the input DC bus voltage V_i of the converter. This phenomenon is capable of generating an effective voltage boost at the output, over the input DC voltage. The positive bus converter constitutes of switch S_a, inductor L_a, diode D_a and capacitor C_a, which will establish the voltage V_a at its output which adds up to the input voltage V_i. The negative bus converter consists of switch S_b, inductor L_b, diode D_b and capacitor C_b, creating a negative voltage V_b at its output which is also added to the input voltage V_i.

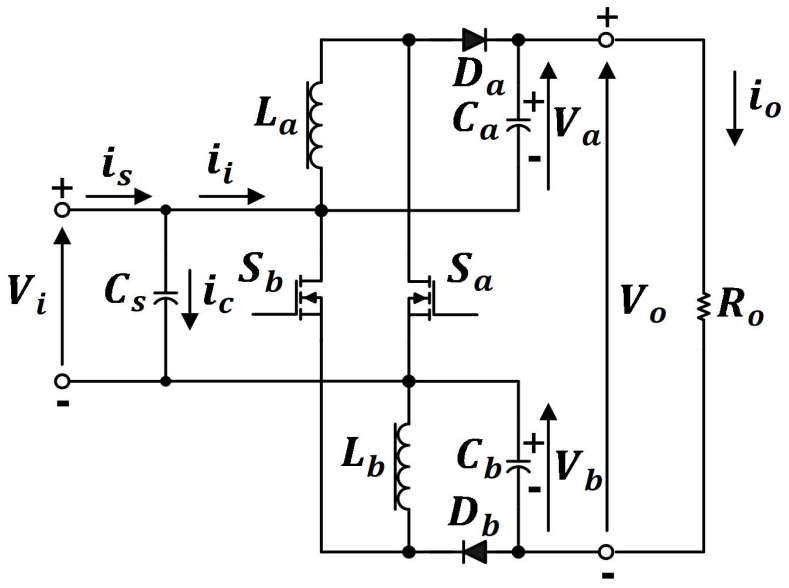


Figure 2.1: Proposed boost DC-DC converter

Thus the total output voltage across the load resistance R_O can be expressed as:

$$V_o = V_i + V_a + V_b \tag{2.1}$$

While a significant amount of power may be directly administered from the input source

to the load end. This result in individual converter providing only a part of the total output voltage and hence it is involved in carrying a fraction of the total power to load, which depends on the amount of voltage boost required. The instantaneous value of the total input current drawn by the converter is represented as i_I. The ripple content in the source current can be brought down significantly with the employment of a filter capacitor C_S (shown in fig. 2.1) placed across the DC source.

The two buck-boost sub-converters are arranged in an interleaved manner which results in input current ripple to have a diminished value [72]. The individual converters are connected in parallel at the input side with a phase shift of 180° in the switching function. The load current which is almost steady is also in integration with the system, is extracted directly in parallel from the input. Thus, the total input current is never zero at any instant, during the operation of the duty cycle in Continuous Conduction Mode (CCM). The input current ripple for each converter will greatly diminish at 50% duty cycle operation. The input current ripple is minimized as the input current pulse of one individual converter starts with the input current pulse of other converter ending at that particular instant. In Fig. 2.2 the schematic is presented which further validates the theory discussed above. Here an illustrative example is taken and simulated at the specified 50% duty cycle to show that there is input ripple current minimization due to the summation of each individual converter input current and that of the load which is flowing directly from the input.

Simultaneously, the output voltage ripple minimization for the converter can also be analyzed in an analytical way and proved schematically in a simulation platform. As the output voltages of the individual converters are interleaved in series with a 180° phase shift and as expressed in equation number (2.1) that the total output voltage comprises of the summation of each converter output voltage and the input voltage. Thus, taking an illustrative example for 50% duty cycle, the result shown in Fig. 2.3 depicts clearly and vividly that the total per unit voltage ripple at the output side is alleviated as stated above. The fig. 2.3 clearly establishes the fact that the voltage ripple minimization can be obtained mainly for two main factors namely, the interleaving of the voltage ripples at the output and due to the addition with the steady input side voltage.

Due to the fact that the converter structure is interleaved, each individual converter is assigned to employ the same switching frequency & duty ratio D. If it is assumed that each inductor current functions in CCM, the output voltage of each converter being equal, the

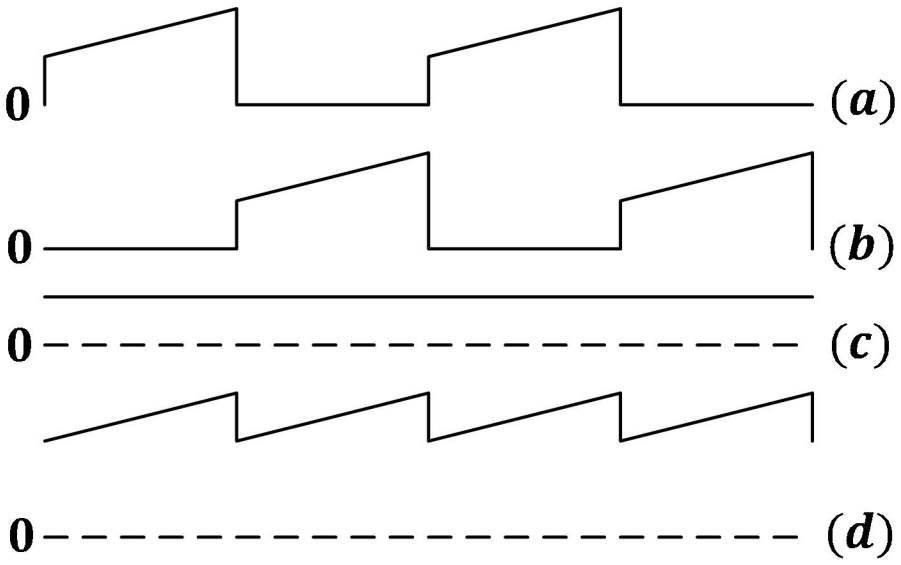


Figure 2.2: Components of instantaneous input current of proposed boost DC-DC converter (a) input current of converter ‘a’ (b) input current of converter ‘b’ (c) load current component (d) total input current

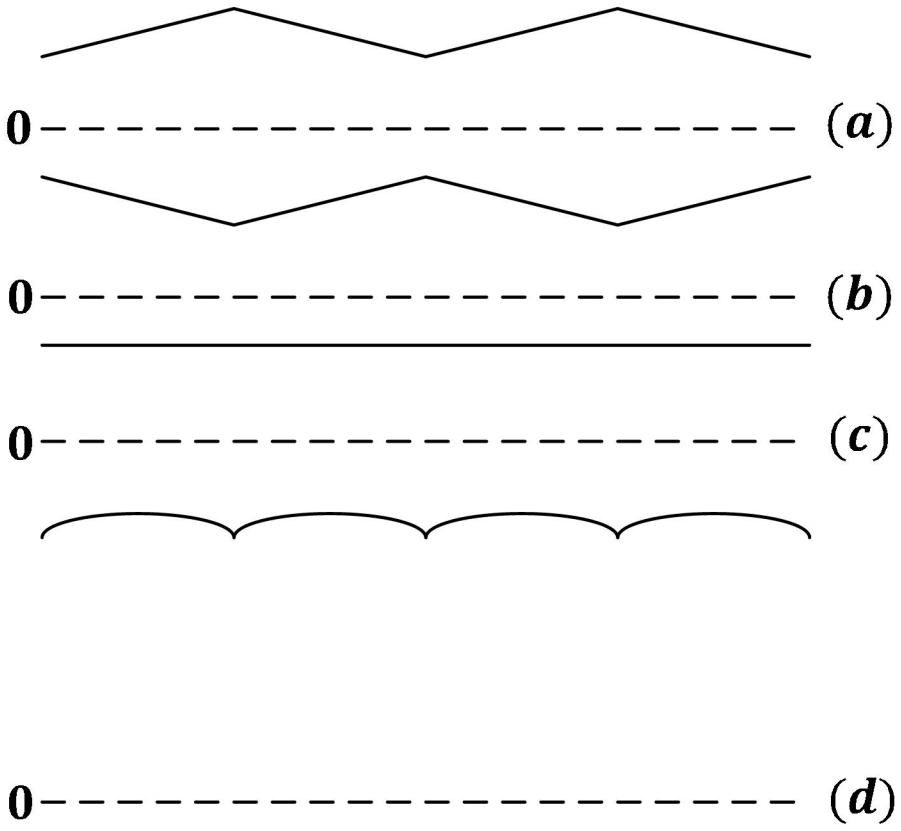


Figure 2.3: Components of instantaneous output voltage of proposed boost DC-DC converter (a) output voltage of converter ‘a’ (b) output voltage of converter ‘b’ (c) input voltage (d) total output voltage

individual converter output voltage can be derived from the Fig. 2.4 and the equation number (2.2).

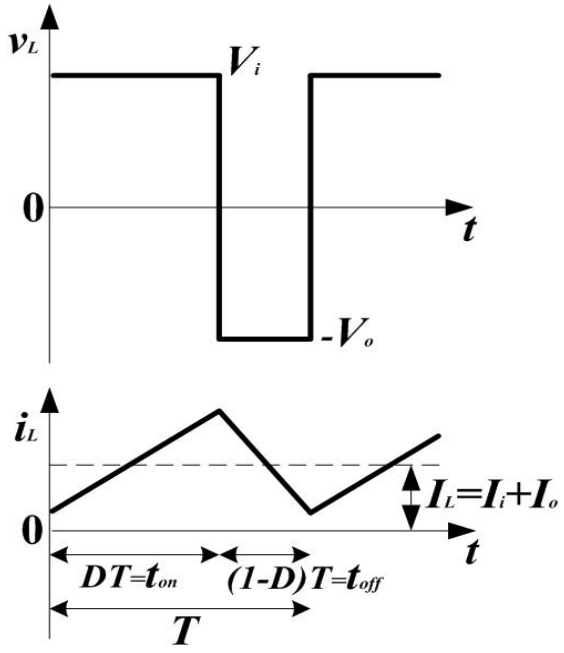


Figure 2.4: Inductor voltage and current waveform during CCM for individual converter (proposed converter)

Therefore, the inductor voltage integral through a time period to zero results in the derived voltage gain of the individual converter.

$$V_i DT + (-V_o)(1 - DT) = 0$$

$$\frac{V_o}{V_i} = \frac{D}{1 - D} \tag{2.2}$$

Here, V_i is the input voltage fed to the converter

V_O is the output voltage of the converter.

D is the Duty Ratio.

T is the total time period.

I_i is the input current of the converter & I_O is the output current of the converter.

I_L is the average Inductor current.

As the output voltages of each converter are the same it can further be simplified and represented by a common value of V_X as:

$$V_x = V_a = V_b = \frac{V_i D}{(1 - D)} \tag{2.3}$$

where, V_a & V_b are output voltages of individual converter.

Therefore, the voltage gain of the total proposed system can be expressed with the help of equation numbers (2.1) and (2.3) as:

$$V_o = \frac{V_i D}{(1-D)} + V_i + \frac{V_i D}{(1-D)}$$

$$\frac{V_o}{V_i} = \frac{(1 + D)}{(1 - D)} \tag{2.4}$$

The equation number (2.4) is the voltage gain of the complete system. Further to compare with the conventional boost topology the overall voltage gain of the proposed converter topology is depicted as a function of duty ratio in Fig. 2.5. From the figure it is clearly visible that in comparison with the conventional boost topology, the proposed DC-DC boost converter topology provides a given voltage gain with a lower value of duty ratio of its switches. Conversely, it can be also stated that the proposed DC-DC boost converter topology has a higher voltage gain for a given duty ratio.

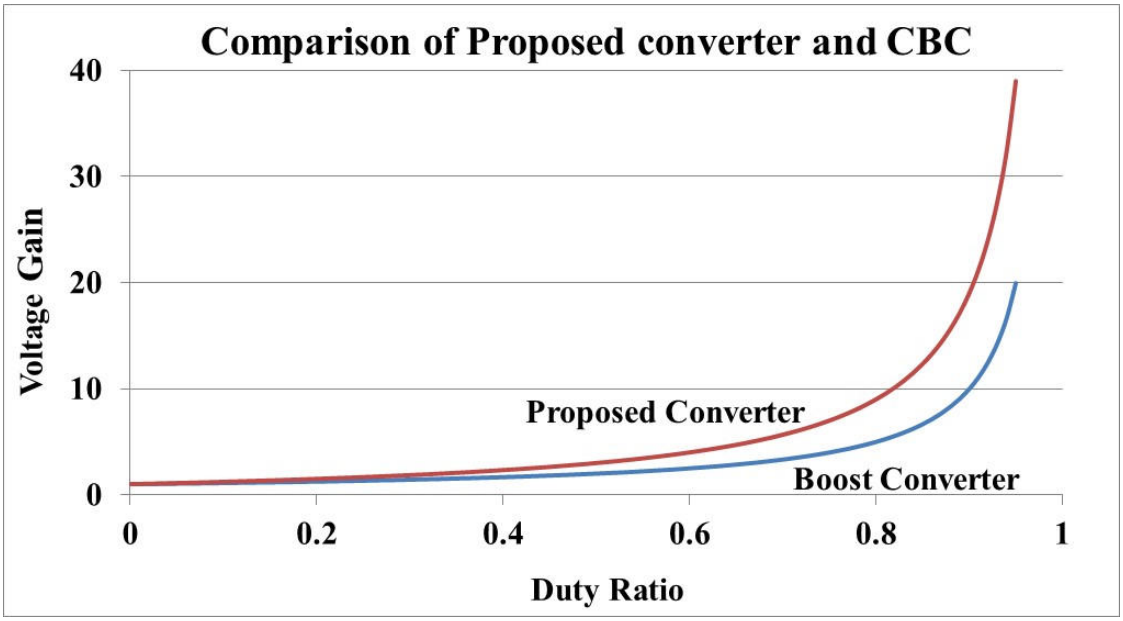


Figure 2.5: Voltage gain of proposed converter and CBC versus duty ratio

The minimum output voltage obtained from equation number (2.4) is equal to the input voltage at a specific duty ratio i.e. D=0, same statement is also applicable in the case of CBC (see equation number (1.2)). The output voltage in both the above cases at this limiting condition will be unregulated. Hence, the performance of proposed DC-DC boost converter can be analytically compared with CBC.

Considering a working instant of the presented converter where the voltage boost and the output power is given. Then as stated earlier that the individual sub-converters of the proposed DC-DC converter handles only a fraction of the total output power, therefore it can be asserted that each constituent/elemental component has much lesser voltage rating as well as current ratings than in a CBC.

Ideally, each semiconductor device (switch and diode) of the converter, are assigned to block a voltage of V_{block} instead of the total output voltage V_o. The voltage V_{block} can be expressed as:

$$V_{block} = V_i + V_x = \frac{V_i}{(1 - D)} \tag{2.5}$$

This, when infused with equation number (2.4) results in

$$V_{block} = \frac{V_o}{(1 + D)} \tag{2.6}$$

From equation number (2.6), it can be clearly noticed that the semiconductor device blocking voltages are determined by the magnitude of total voltage boost required. Therefore, it will be invariably much less than the magnitude of the total output voltage, unlike for a CBC where the semiconductor device has to block a higher voltage magnitude.

Since each converter handles lower-level of output voltage and power than the total output voltage, switching losses in the semiconductor device (switches and diodes) attain a diminished value than in the CBC/SBC. The capacitors of each converter are connected in series at the output side with the input DC voltage to generate the total output voltage across them as V_{cap}, which can be expressed by:

$$V_{cap} = V_x = \frac{V_i D}{(1 - D)} = \frac{V_o D}{(1 + D)} \tag{2.7}$$

From (2.7) it can be seen that the rating of the capacitor voltage are dependent on the amount of total boost required. Hence, the individual converter capacitor voltage rating has a lower value than full output voltage, each being less than 50% of the total output voltage.

Individual converter inductor rating is less than what would be needed for single switch boost converter, due to handling a fraction of power.

2.3 Conduction States of the Proposed Converter

There are primarily two conduction states i.e. Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM). The conduction states indicate whether the current in the inductor reaches zero during each switching cycle. In CCM the current in the inductor does not touch the zero point over the entire time period. Whereas in DCM the inductor current reaches zero and stays there over the switching period [73],[74].

The CCM of the proposed converter is discussed in the next section in detail with schematic diagram and in depth analysis for each CCM conduction state.

2.3.1 Continuous Conduction Mode (CCM)

In this section the constituent converter operates in CCM where it is stated above that the inductor current never reaches zero over the switching period. Analysis of the CCM is carried for the proposed topology.

Here the input voltage is designated as V_i, the output voltage as V_o and the load current i_o. The input voltage, output voltage is assumed to be steady without any presence of ripple and the load current is assumed to be continuous. Each of the constituent/elemental switches functions on its own with identical frequency value and Duty ratio D. It is necessary to mention the color codes for working states of semiconductor devices (ON state) as well as color codes to represent the current passing through the passive components in the conducting states of the proposed converter. Here the ON state of the upper switch S_a is identified by the color blue while that of lower switch S_b is associated with the color pink. The inductor current for inductor L_a is represented with blue whereas the inductor current for inductor L_b is pink. The current passing through both the capacitors C_a and C_b is designated with the color green. The load current i_o flowing through the proposed boost DC-DC converter is represented with the color red.

State I is depicted in Fig. 2.6, where switch S_b has just turned OFF and switch S_a has been turned ON. The diode D_b is turned ON with the energy being transferred from the inductor L_b, with $i_{Lb}>i_o$.

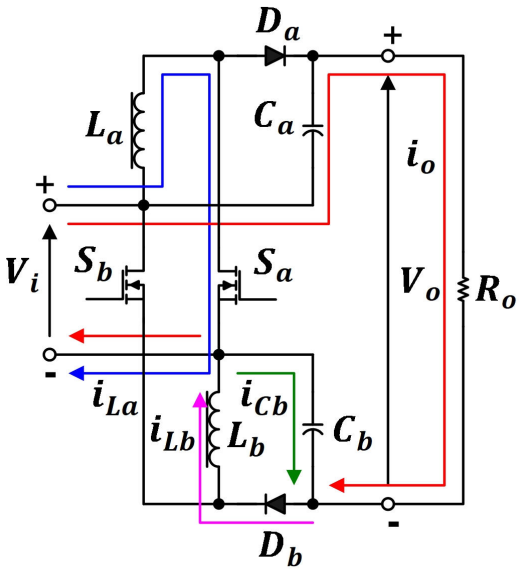
The current i_{La} which builds up through the inductor L_a is expressed now as:

$$V_i = L_a \frac{di_{La}}{dt} \tag{2.8}$$

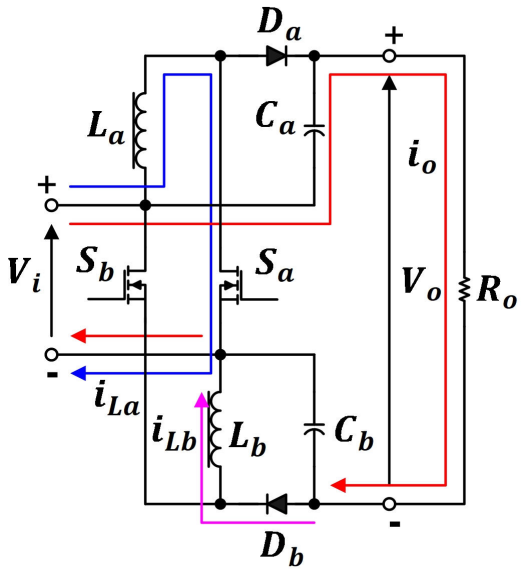
During this state, the load current i_o will flow directly from the source. Hence, the total input current to the converter at this time instant is the sum of the current through the inductor L_a and the load current can be expressed as:

$$i_i = i_{La} + i_o \tag{2.9}$$

The flow of steady load current causes capacitor C_a to be discharging at constant current. As the switch S_b has just turned OFF, its inductor current through L_b continues through its diode D_b. Since the inductor current is higher in magnitude than the load current i_o ($i_{Lb}>i_o$), a part of it charges capacitor C_b while the remaining current is fed to the load.



State I [$i_{Lb}>i_o$]
Figure 2.6



State II [$i_{Lb}=i_o$]
Figure 2.7

In State II is the situation where the switch S_a is still ON and the current in the inductor becomes equal to the load current ($i_{Lb}=i_o$). Here the inductor current has stopped charging the capacitor C_b as it is equal to the load current. The upper capacitor C_a is still discharging at constant current. The conduction state is shown in Fig. 2.7.

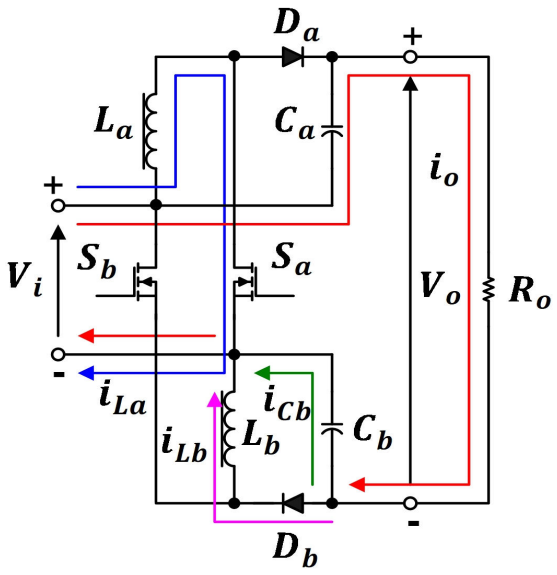
The current i_{Lb} through inductor L_b is now given as:

$$V_b = L_b \frac{di_{Lb}}{dt} \tag{2.10}$$

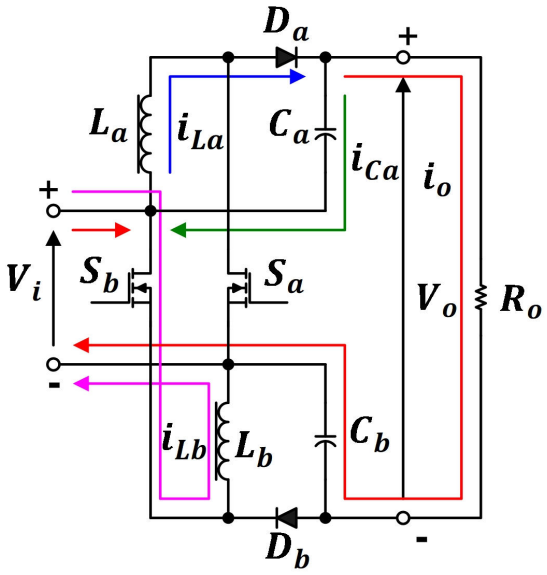
The current i_{Cb} through capacitor C_b is now given as:

$$i_{Cb} = i_{Lb} - i_o \quad (2.11)$$

During the energy transfer from the inductor the energy in the inductor L_b reduces. As the instantaneous value of its current i_{Lb} becomes lower than load current i_o ($i_{Lb}<i_o$) the capacitor C_b starts discharging at that instant which is shown in the Fig. 2.8. This specific instant where the switch S_a is ON while the diode D_b is ON and both the capacitors C_a and C_b are discharging depicts the condition to be State III.



State III [$i_{Lb}<i_o$]
Figure 2.8



State IV [$i_{La}>i_o$]
Figure 2.9

In state IV where the switch S_b gets turned ON while the switch S_a is OFF. Energy gets transferred from the inductor L_a, with $i_{La}>i_o$. As the inductor current is higher than the load current the capacitor C_a gets charged by the inductor current and rest is fed to the load.

The current i_{Lb} building up through the inductor L_b is given by the equation number (2.8)

The total input current to the converter at this instant is expressed as:

$$i_i = i_{Lb} + i_o \quad (2.12)$$

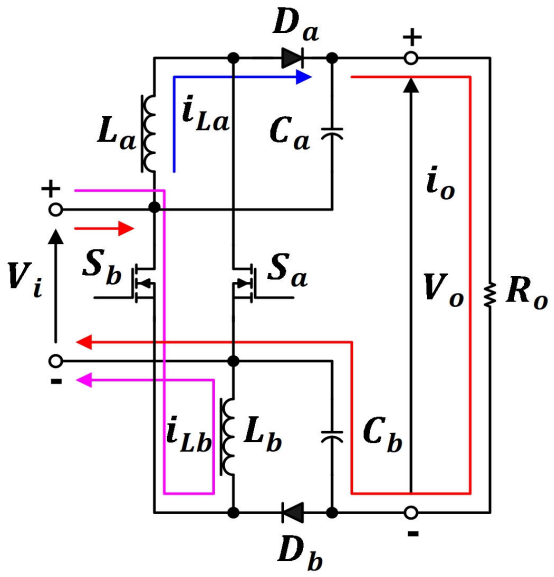
The state IV is clearly depicted in the Fig. 2.9.

State V clearly depicts the modulation state where the lower switch S_b is ON and the inductor current i_{La} is equal to the load current i_o. Therefore, the inductor current does not charge the capacitor C_a and the lower capacitor C_b is still discharging. The Fig. 2.10 shows

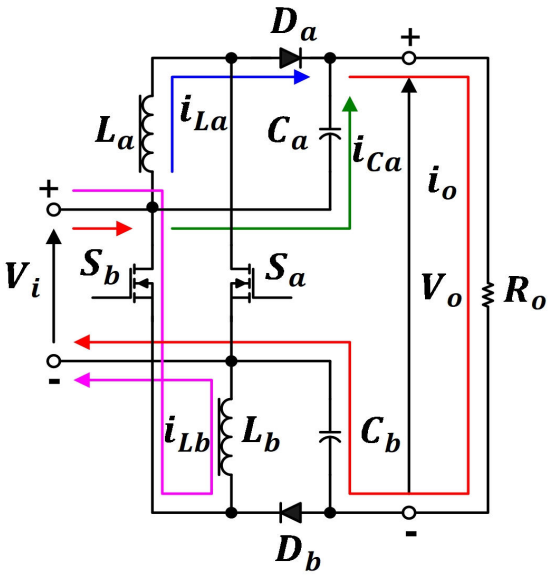
the modulation state.

State VI is a condition where the inductor current falls below the load current ($i_{La}<i_o$) with the diode D_a ON and both the capacitors C_a and C_b are discharging. The operation of the state is similar to the State III.

The Fig. 2.11 schematically shows the state where the inductor current i_{La} is lower than the load current i_o.



State V [$i_{La}=i_o$]
Figure 2.10



State VI [$i_{La}<i_o$]
Figure 2.11

State VII shown in Fig. 2.12 discusses the state where both the switches S_a and S_b are OFF. The diode D_a and D_b is ON and there is overlap of current flow in both the inductors L_a and L_b. The state shows that the capacitor C_a is charging while the capacitor C_b is still discharging.

The input current in this interval can be expressed as:

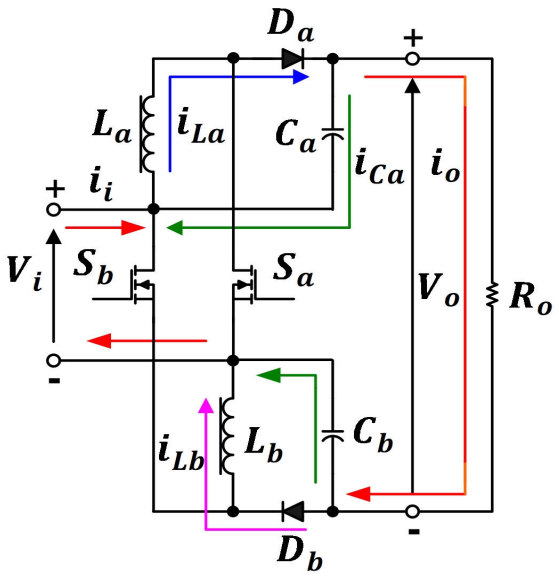
$$i_i = i_o \tag{2.13}$$

In Fig. 2.13 State VIII is shown where both the switches (S_a and S_b) are OFF and there is a overlap of current flow in both the inductors (L_a and L_b). But in this state the capacitor C_b is charging while the capacitor C_a is discharging. It is reversed condition of State VII.

The input current is expressed similar to the equation number (2.13).

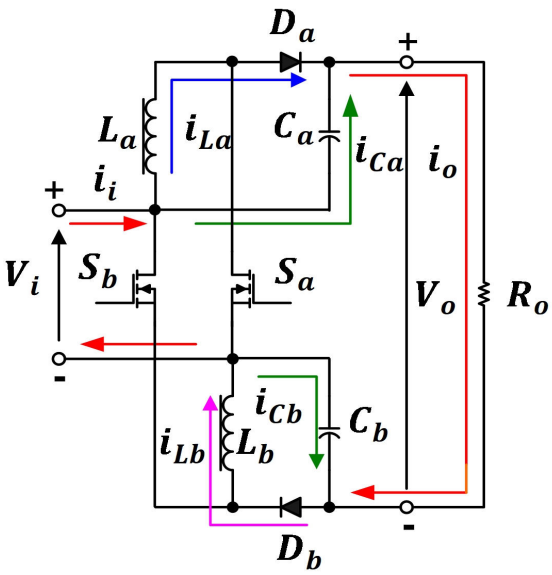
In Fig. 2.14 the State IX is shown where there is an overlap of ON states of the switches

S_a and S_b. Both the diodes D_a and D_b are in the OFF state. The capacitors C_a and C_b are discharging at a constant load current. The current through each inductor current is governed by the equation numbers (2.8) and (2.10).



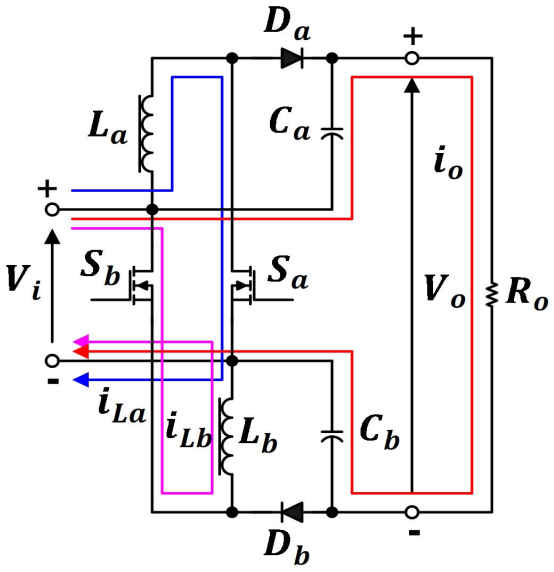
State VII [$i_{La}>i_o$][$i_{Lb}<i_o$]

Figure 2.12



State VIII [$i_{La}<i_o$][$i_{Lb}>i_o$]

Figure 2.13



State IX

Figure 2.14

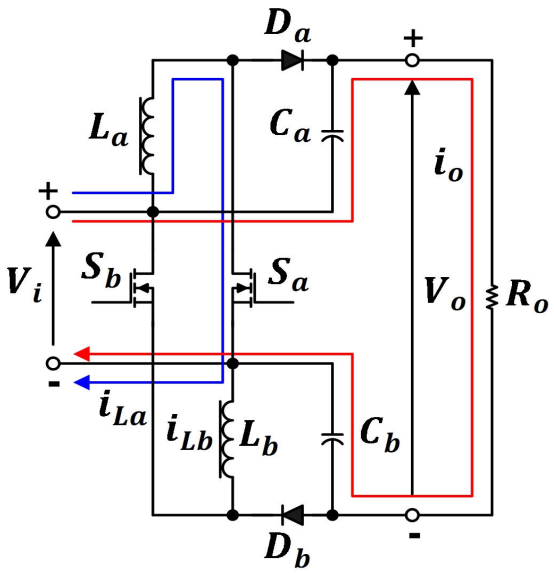
The total input current at this time interval is expressed as:

$$i_i = i_{La} + i_o + i_{Lb} \tag{2.14}$$

2.3.2 Discontinuous Conduction Mode (DCM)

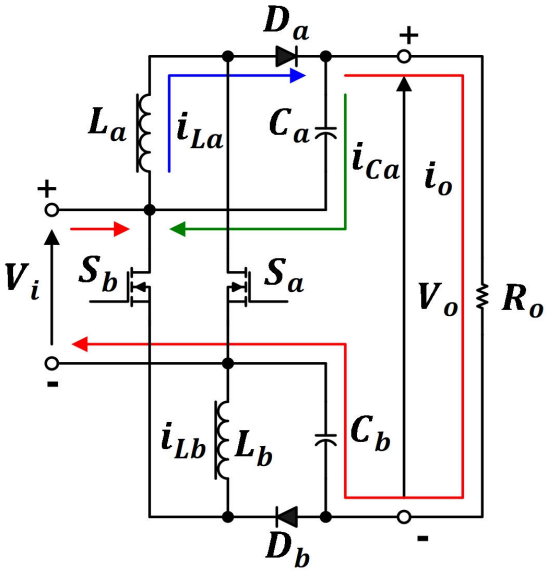
In this section the operation of the proposed converter in DCM is discussed in detail. The DCM conduction mode is a condition where the inductor current reaches zero over the switching period. Analysis of the DCM is carried for the presented topology in the following section. The color codes for the conduction of the semiconductor device and the current through the passive components are similar to that of CCM.

State I in the DCM mode shown in the Fig. 2.15 has the switch S_a ON. Both the diodes D_a and D_b are OFF and the capacitors C_a and C_b are in the discharging state. The current building up through the inductor L_a can be given by the equation number (2.8). Assuming steady input and output voltages, the load current i_o directly flows from the source. Thus, the total input current now will be the sum of the current through the inductor L_a and the load current i_o and can be expressed as equation number (2.9).



State I

Figure 2.15



State II [i_{La}>i_o]

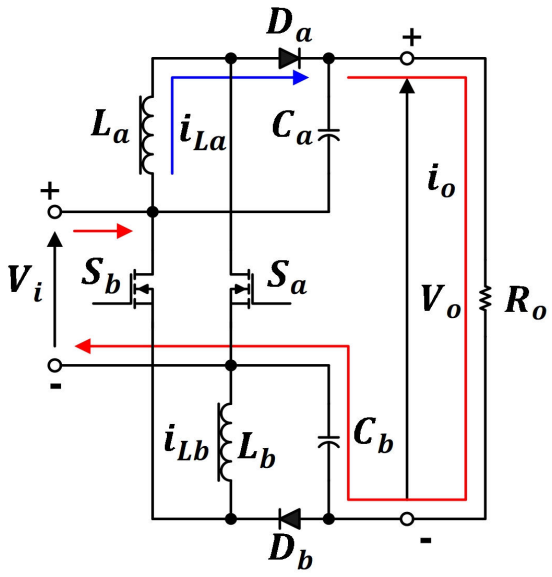
Figure 2.16

In State II presented in the Fig. 2.16 both the switches S_a and S_b are turned OFF and the diode D_a is ON. A part of the inductor current flowing through L_a is charging the capacitor C_a while the balance current is fed directly to the load. The capacitor C_b is discharging during this duration. The current i_{La} through the inductor L_a can be given by the equation

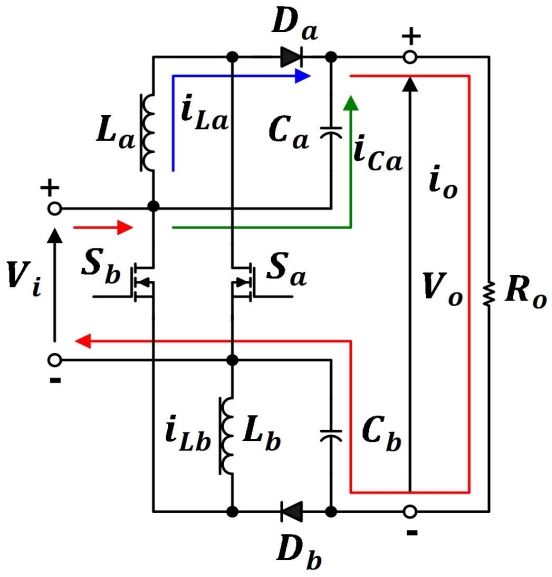
number (2.8) and the input current is same as the load current and can be expressed as equation number (2.13).

State III shown in Fig. 2.17 has the upper diode D_a in the forward biased condition. The lower capacitor C_b is discharging in this state. In this particular state the inductor current i_{La} is equal to the load current i_o and therefore it is not charging the upper capacitor C_a.

In Fig. 2.18 the State IV of DCM of the proposed converter is discussed. Here the during the energy transfer from the inductor current falls and becomes $i_{La}<i_o$. Here both the switches S_a and S_b are OFF. The current flowing through the inductor L_a flows directly to the load via the diode D_a. The discharging current from the capacitor C_a makes up for the remaining load current required. In this state both the capacitor current (C_a and C_b) are in the discharging mode. The input current can be expressed by the equation number (2.13).



State III [$i_{La}=i_o$]
Figure 2.17

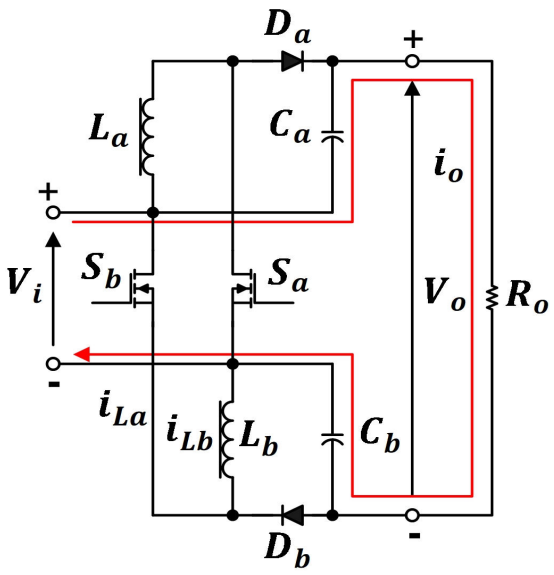


State IV [$i_{La}<i_o$]
Figure 2.18

State V has both the switches S_a and S_b in OFF mode. The diodes D_a and D_b are also OFF and both the capacitors C_a and C_b are discharging at a constant current which is equal to the load current i_o. The input current for this state can be again represented by the equation number (2.13). The Fig. 2.19 shows the State V schematically.

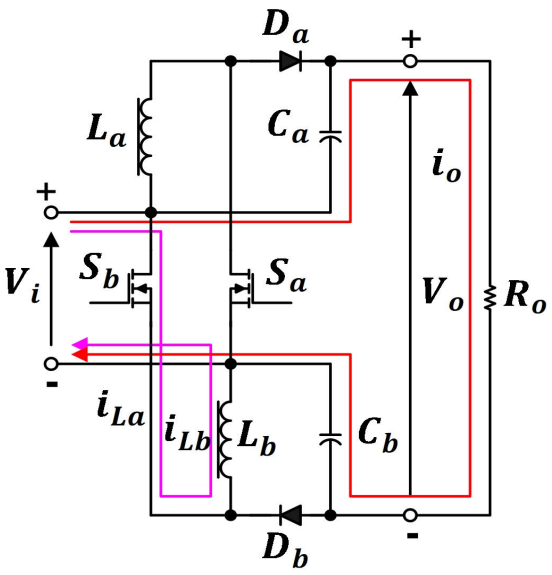
State VI in the DCM mode shown in the Fig. 2.20 has the switch S_b ON. Both the diodes D_a and D_b are OFF and the capacitors C_a and C_b are in the discharging state. The current

building up through the inductor L_b is similar to the equation number (2.10). Assuming steady input and output voltages, the load current i_o directly flows from the source. Thus, the total input current now will be the sum of the current through the inductor L_b and the load current i_o and can be expressed as equation number (2.12).



State V

Figure 2.19

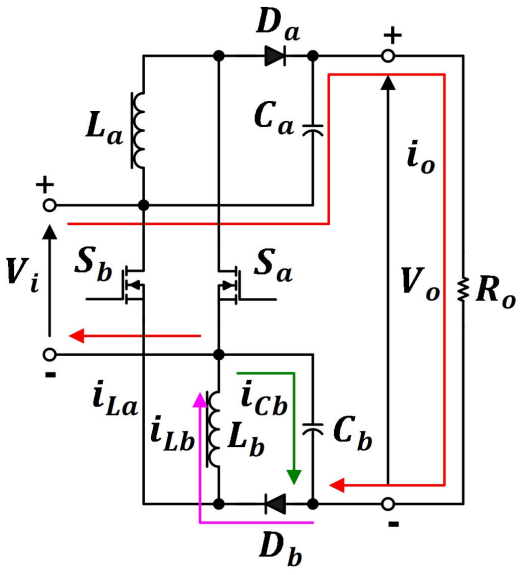


State VI

Figure 2.20

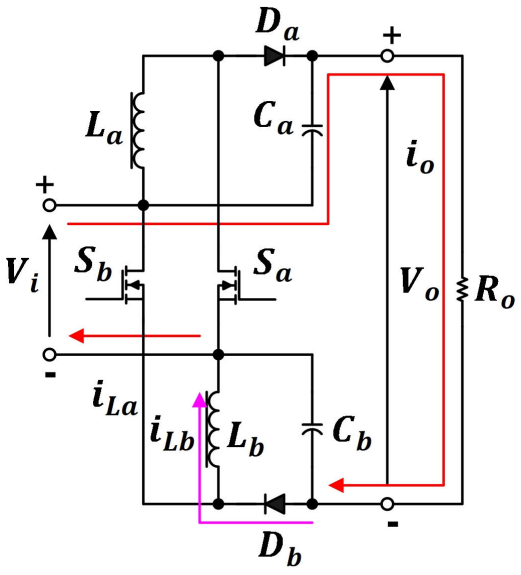
State VII shows the state where both the switches S_a and S_b are OFF. The lower diode D_b is forward biased and part of the inductor current i_{Lb} is charging the capacitor C_b while the remaining current is fed directly to the load. The capacitor C_a is discharging during this interval. The current i_{Lb} through the through the inductor L_b is given by the equation number (2.10). The current through inductor L_b is greater than the load current i_o therefore it can be expressed by the equation number (2.13). The Fig. 2.21 shows the state in detail.

State VIII shown in Fig. 2.22 has the lower diode D_b in the forward biased condition. The upper capacitor C_a is discharging at this interval. In this particular state the inductor current i_{Lb} is equal to the load current i_o and therefore it is not charging the lower capacitor C_b.



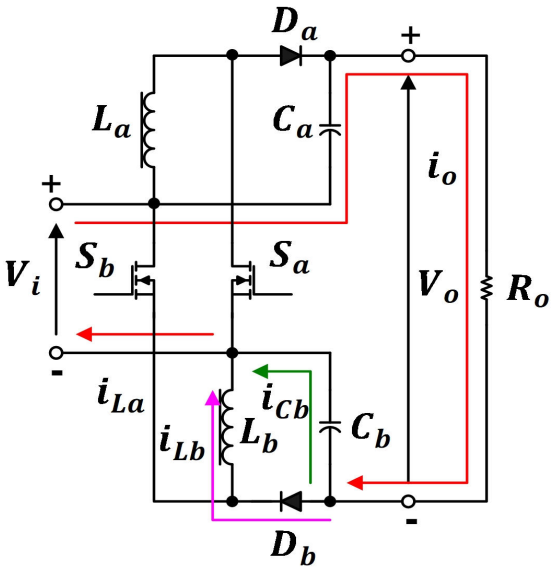
State VII [$i_{Lb}>i_o$]

Figure 2.21



State VIII [$i_{Lb}=i_o$]

Figure 2.22



State IX [$i_{Lb}<i_o$]

Figure 2.23

State IX shows that during energy transfer from the inductor presented in Fig. 2.23, the inductor current i_{Lb} falls below the load current i_o. The switches S_a and S_b are OFF and the current through the inductor L_b flows through the forward biased diode D_b. Both the capacitors C_a and C_b are in the discharging state. The input current can again be described by the equation number (2.13).

2.4 Control Design of the Proposed Converter

2.4.1 Introduction

The output voltage of typical DC-DC converter should be within the specified range of a preset parameter in spite of variations in the input voltage, load current and changes in values of various elements in the converter within the tolerance limit. Typically, the DC-DC power supply specification is set such that the output voltage should remain within the 1% of the 5V supply system whenever it faces a step variation in the load current. The output voltage for a switching converter will therefore be the function of the input voltage, duty ratio, load current and the various converter element values. Thus, to maintain the output voltage at a specified value the duty ratio of the converter has to be changed to support the output voltage [17]. So conventionally a negative feedback is used to automatically regulate the duty ratio, which is the variable that can be altered to generate the desired results at the output side of the converter.

The output voltage can be measured with the help of a sensor (voltage divider) and then a comparison can be done with the reference input voltage. The difference obtained from the reference signal and the actual output voltage is the error signal. This error signal is primarily passed through a controller having a transfer function. Finally, the output of the controller is fed to comparator where the control voltage is compared with the fixed frequency sawtooth waveform. The output produces the necessary switch control signal which is fed to the gate driver circuit and then to the gate of the converter's switching device [73], [74]. The block diagram of a feedback based scheme used for Pulse Width Modulation (PWM) technique is shown in the Fig. 2.24.

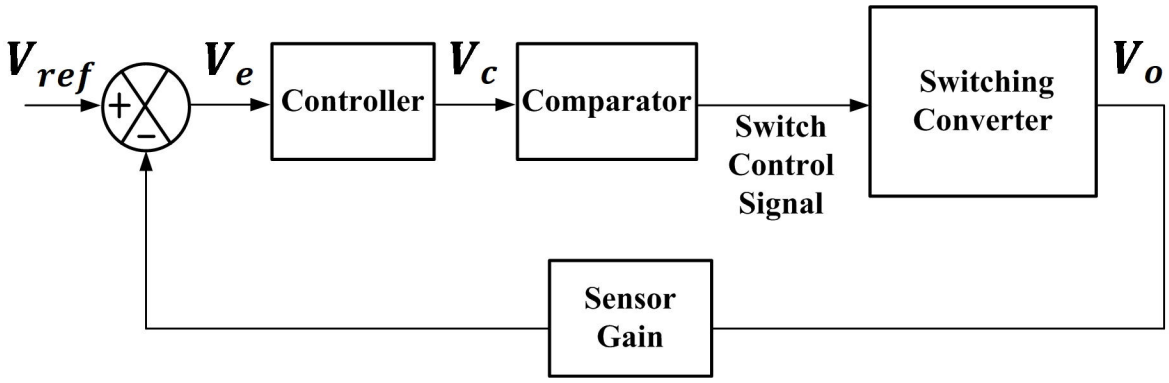


Figure 2.24: Block diagram of a feedback system generally used in PWM operation

In the Fig. 2.24 V_{ref} is the reference input voltage, V_e is the error signal obtained from comparison between the reference input voltage and the actual output voltage, V_c is the control voltage which is the input to the comparator and V_o is the actual output voltage.

However, a feedback system can be a cause for a stable open loop system to display oscillations, overshoot and ringing. Therefore, the loop gain phase margin should be optimum to make the feedback system stable. The steady state error is also a grave concern so to arrest it generally a Proportional Integral (PI) controller is used as an error amplifier [75], [76]. To elaborate on the basic nature of the PI controller the schematic is shown in Fig. 2.25 and further explained.

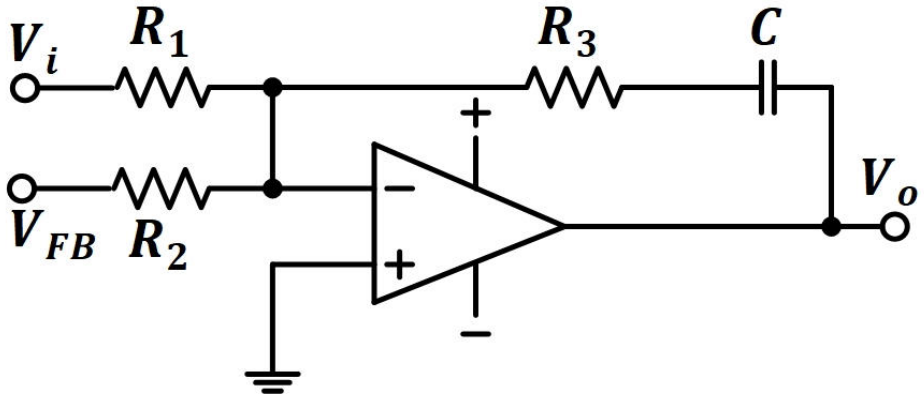


Figure 2.25: Standard PI controller

From the Fig. 2.25 it can be expressed:

$$(0 - V_o) = i_3 R_3 + \frac{1}{C}\int i_3 dt \tag{2.15}$$

$$i_3 = i_1 + i_2$$

Where, $i_1 = \dfrac{V_i - 0}{R_1}$ (2.16)

$$i_2 = \frac{V_{FB} - 0}{R_2}$$

If, $R_1 = R_2 = R$ (say) (2.17)

$$-V_o = \frac{R_3}{R}(V_i + V_{FB}) + \frac{1}{RC}\int (V_i + V_{FB})dt \tag{2.18}$$

If, V_{FB} is negative, then

$$-V_o = \frac{R_3}{R}(V_i - V_{FB}) + \frac{1}{RC}\int (V_i - V_{FB})dt$$
$$-V_o = K_p\varepsilon + K_i\int \varepsilon dt \tag{2.19}$$

Here V_i is the reference input voltage, V_{FB} is the feedback voltage, V_o is the actual output voltage, C is the capacitance and R_1, R_2, R_3 are the resistances.

Usually, the reference is positive and the feedback is negative. Therefore, the reference is at V_i and the feedback is at V_{FB}.

2.4.2 PWM Control Methods for Voltage-Fed DC-DC Converter

There are various methods discussed in literature for the PWM block realization. Conventionally a ramp generator is employed where a constant frequency and constant amplitude sawtooth waveform is generated [77], [78]. The ramp generator is an R-C network where the resistor is used to charge the capacitor and the capacitor is discharged when the desired voltage level is achieved. The error signal obtained after compensation is made to compare with the ramp signal. A high output is provided when the ramp signal is higher than the error signal. An S-R latch is set which resets itself in each clock pulse. The voltage divider of the output is so designed that the reference voltage becomes equal to the output voltage when the required voltage level is reached. If for some reason the output goes to a higher value the error will set itself low hence reducing the duty ratio and the output follows. This can be the explanation for DC-DC converters having a single switch but when considering the case of two switches at the same leg and the simultaneous conduction of both the switches are not allowed for e.g. Push-Pull converter. Here a latch is used which toggles with every clock pulse. The latch output toggles with every clock pulse and remain in that particular mode unless there is arrival of next pulse.

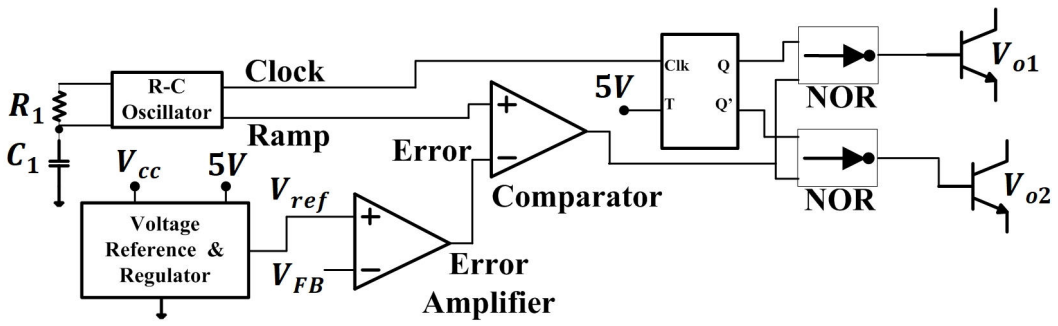


Figure 2.26: Schematic for PWM controller having two switches on the same leg

Therefore, at any given instant only a single latch output provides a high. It is possible to achieve dead short with this method but the dead time requirement which is the time interval between one switch going OFF and another ON is very hard to achieve with this circuit analogy. The schematic of the controller circuit for two switches on the same leg is shown in Fig. 2.26

2.5 PWM Control Using PWM IC UC3525A

The issues relating to the PWM control methods are broadly discussed in the section 2.4.2. Therefore, it is of prime importance to address these drawbacks and strive for a better PWM IC which has a versatile regulating capability and are familiar in the designing arena as well as which is available in power electronic market.

One of the very well known PWM IC is the UC3525A. It provides superior performance and reduces the use of external hardware circuitry for designing switching power supplies. The PWM IC generates the ramp and the pulse output. The comparator is set high when the ramp exceeds the output of the error amplifier. The NOR gates at the output whenever it sets low then the transistors are turned off. The oscillator output has the function to toggle the flip-flop enabling one of the gates to respond to the comparator. This will allow push-pull operation. The transistor selected is on and is turned off as soon as ramp exceeds the error signal. At the end of each cycle the gates are forced to set low by the oscillator pulse thus enabling the dead time for the transistors when both being on at the same time.
The block diagram of UC3525A is shown [79] in the Fig. 2.27.

The oscillator frequency is primarily being set with the help of R_T (Pin 6) and C_T (Pin 5). The push-pull output frequency is one –half of the oscillator frequency which is done by the flip-flop. The internal discharge transistor is in control of the discharge time at the end of each ramp. This makes sure that there is a stop time between the output pulses and the transistors are not set on at the same instant. Connection of a resistance between C_T (Pin 5) and discharge (Pin 7) will provide a wide spectrum of dead time adjustment.

The oscillator frequency (approximate) can be expressed as:

$$f_{OSC} = \frac{1}{C_T(0.7R_T + 3R_D)} \tag{2.20}$$

Here R_D is the dead time constant

The error amplifier output is the difference obtained between the reference input (Pin 2)

and the feedback pin (Pin 1). The instant when the output increases there will be decrease in the error voltage. The ramp signal will reach the error voltage and subsequently the transistor is turned off. This will persist until the instant when the output voltage will again be equal to the reference voltage.

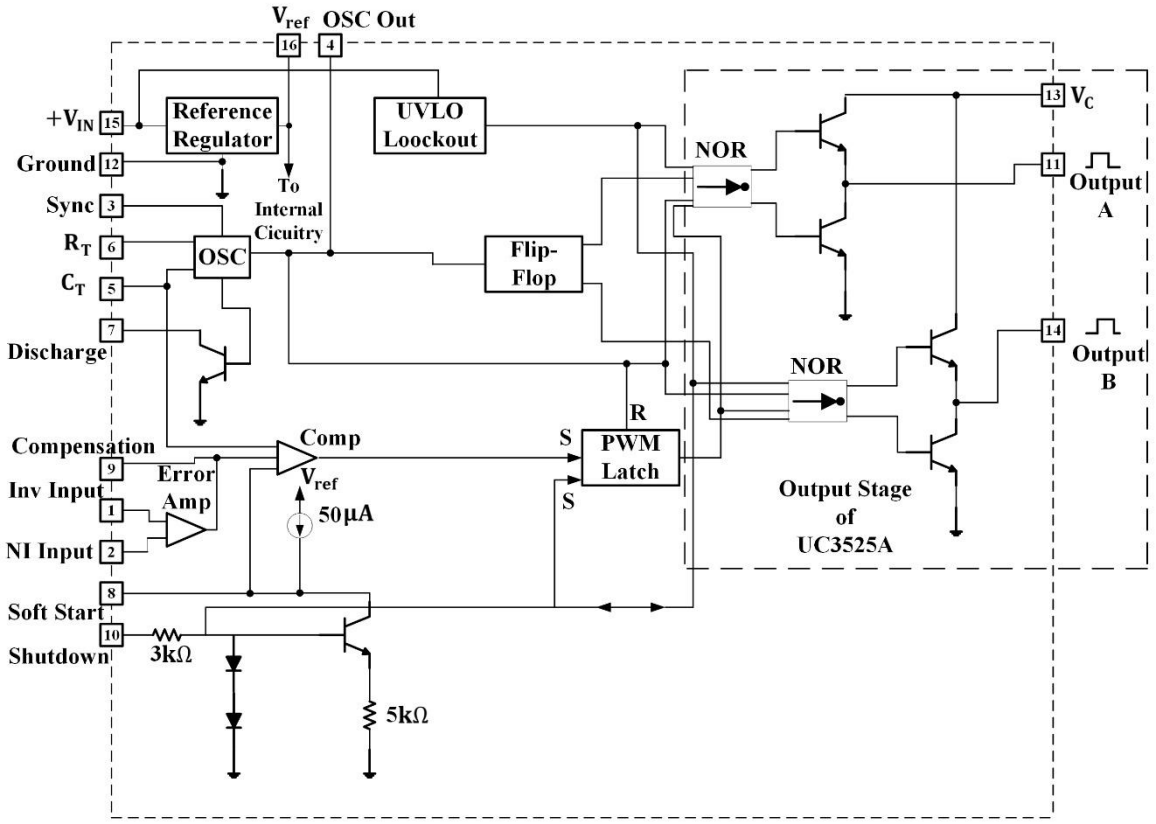


Figure 2.27: Block diagram of PWM IC UC3525A

Frequency compensation (closed loop stability) is achieved by connecting *R* and *C* between the compensation pin (Pin 9) and Inverting pin (Pin 1). The benefit of under voltage lockout is it disables the regulator unless its input crosses the threshold value of 8 volts. The oscillator sync pin (Pin3) aids to lock frequencies for several IC's. The sync input in the oscillator permits numerous units to be synchronized to an external clock. The output stage comprises of totem-pole designs capable of fast solid switching.

The PWM IC has a soft start circuit incorporated which requires an external capacitor. Whenever the input power is applied the IC recuperate from the state of shutdown and the soft start mechanism is getting charged from the 50 μA current source which assist the voltage to rise gradually. The soft/gradual rise in the output voltage will be successful in arresting the start up current surges. The shutdown pin (Pin 10) manages both the soft start

and the output stages. It provides instantaneous shutdown through the PWM latch with the help of pulsed shutdown.

In this circuitry the feedback can be connected to Pin 1 and reference to Pin 2. The compensating R-C network is connected between Pin 9 and Pin 1. The clock frequency (PWM operation) is determined and the oscillator frequency is set by mathematically choosing the values of R_T, C_T and R_D. This setup can be used to drive two switches.

2.6 PWM Control for the Proposed Converter

In the sections 2.4.2 and 2.5 discussions on PWM control primarily were focused on general voltage fed converter topologies where DCM of operation was executed. But for the proposed scheme and its conduction states broadly explained and classified in the section 2.3.1operates in CCM as well, the PWM control medium will somewhat be different from the discussed techniques available in literature.

In this proposed scheme there is overlapping of the pulses i.e. two semiconductor switches maybe switched ON at the same instant of time as shown in the section 2.3.1 State IX, Fig. 2.14. Going by the layout of UC3525A it is not possible for the IC to achieve such a phenomenon all by itself. Hence two UC3525A IC's are used which will be synchronized accordingly with the external clock and providing the desired pulses with more than 50% duty cycle and overlapped ON period of two switches. The external clock is set up using another UC3525A IC. Therefore, a block diagram is shown in Fig. 2.28 which projects the switching control scheme (providing the gate pulses) for the proposed converter.

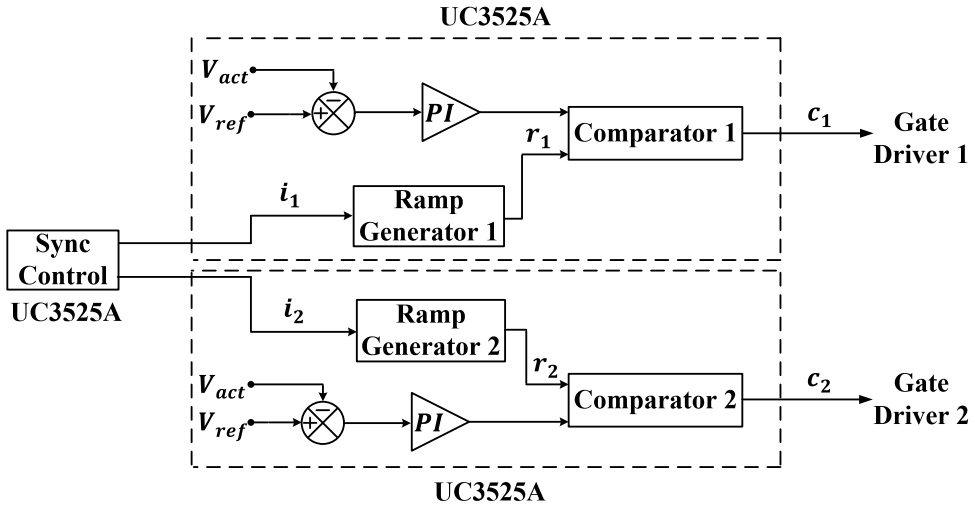


Figure 2.28: Basic block diagram for PWM control of the proposed converter

In the Fig. 2.28 V_{ref} is the input reference voltage to the error amplifier, V_{act} is the actual voltage. The markings i_1 and i_2 signify the input signal to the ramp generator 1 and ramp generator 2 respectively. The output signal from the ramp generators are marked as r_1 and r_2 respectively. The signals c_1 and c_2 are obtained after comparing the ramp signals with the $V_{control}$ (output of the Error amplifier). The input to the gate driver 1 and gate driver 2 is denoted as c_1 and c_2 respectively which is the signal generated after comparison with repetitive signal and the control voltage. All the signals will be addressed with the aid of waveform analysis in Fig. 2.29 categorically.

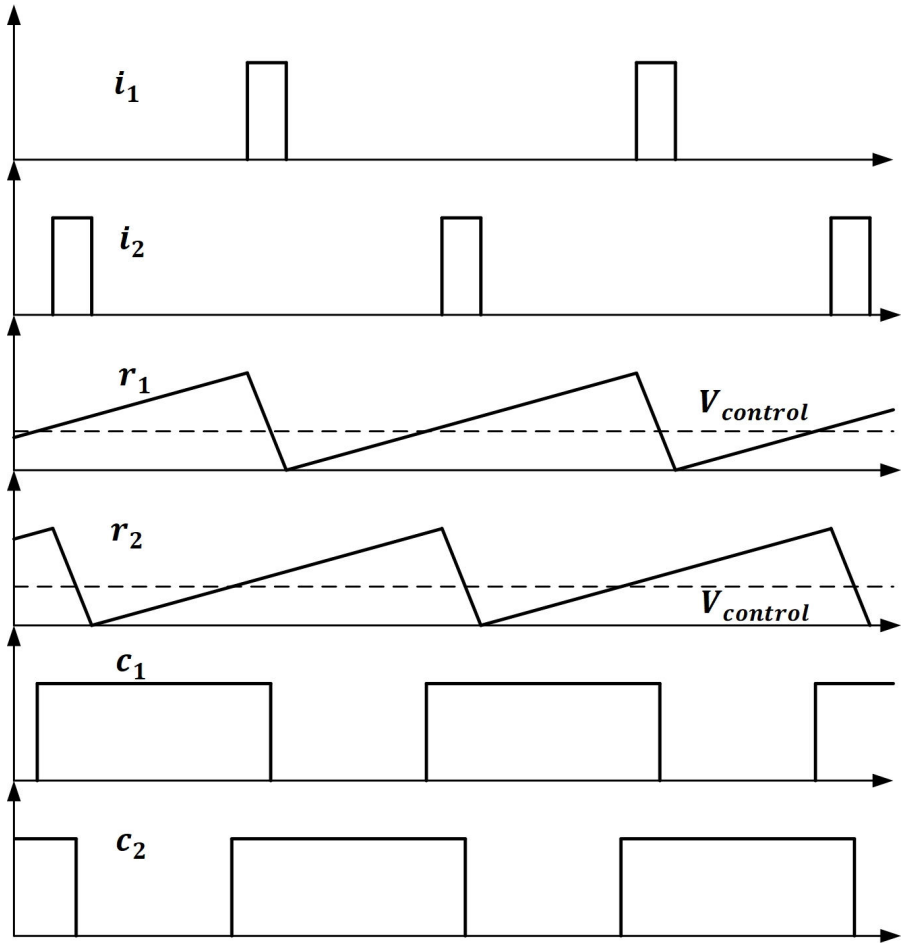


Figure 2.29: Waveforms at various designated points in Fig. 2.28

In the Fig. 2.29 the concept of using UC3525A as an external clock is explained schematically. The UC3525A provides two pulses which are being fed to the two sync outputs. The pulses are of 180^{o} phase shifted and of the specified switching frequency. The

two slave UC3525A PWM IC's can perform both ramp generation as well as a comparator. Whenever a common error voltage is produced by the external error amplifier the two IC's are designated to function as unity gain buffer, so that they follow the common error voltage. Therefore, it is necessary to build an external error amplifier and compensation circuitry instead of the existing error amplifier and compensation facility available on board.

2.6.1 UC3525A Synchronization through Sync Pin

In the proposed control scheme, the PWM IC's are synchronized with the assistance of sync pin (Pin 3). The sync pin performs the function of flooring the rising ramp of the sawtooth waveform. Hence in order to lock with the oscillator with the sync pin the rising ramp waveform should be floored by the sync pin and not by the internal circuitry of oscillator which happens in normal operation of UC3525A. This technique will be successful in intercepting the unequal periods in the ramp generator output. Therefore, it is imperative to have the frequency of the oscillator (f_{osc}) to be less than the frequency of the sync pin (f_{sync}). It can be stated through analysis that the value of f_{osc} should be around 10% less or more than 90% of f_{sync} value for optimal operation to take place. However, it should be taken to note that the oscillator frequency (f_{osc}) should not be too less otherwise the ramp will be forced to reach zero at a premature level. There may be issues regarding the amplitude of the oscillator output. The error amplifier output must have a scaled value to be within the limit of the maximum synchronized amplitude level of the ramp.

The synchronized ramp amplitude can be expressed as:

$$V_{ramp,amp_{sync}} = V_{ramp,amp_{orig}} \text{ x } \frac{f_{osc}}{f_{sync}} \tag{2.21}$$

Where, $V_{ramp,amp_{sync}}$ is the ramp amplitude of the oscillator after synchronization.

$V_{ramp,amp_{orig}}$ is the original ramp amplitude of the oscillator.

2.7 Control Loop for Voltage

The output voltage is sensed with the help of a voltage divider circuit. The voltage divider resistances R_{11}, R_{21}, R_{12}, R_{22}, R_{13} and R_{23} are chosen appropriately according to the voltage sensed i.e. v_{21}, v_{22} and v_{23}. The voltage kv_{21}, kv_{22} and kv_{23} are different voltage levels at designated points in the Fig. 2.30 from ground generated by the proposed converter. The term 'k' is a constant as the voltages depend on the change in the output voltage levels. The voltages V_1, V_2 and V_3 are the output side voltages of the proposed converter. Capacitance C_1, C_2, C_3, C_4 and C_5 are the capacitance values added to reduce the noise/distortion in the signals. The diodes D_1, D_2, D_3 and D_4 are employed in the circuit as protection/safety diodes. Their function is to block the reverse voltage and current flowing in the circuitry. It primarily focuses on arresting the reverse flow of current which is capable of damaging the total unit [80]. In the circuit a differential amplifier is used viz. TL084, whose basic function is to amplify the voltage between two input voltage signals. Here the difference in voltage in the inverting (Pin 2) and the non-inverting terminal (Pin 3) is amplified and an amplified output (Pin 1) is received [81]. The resistances R_{31}, R_{32}, R_{33} and R_{34} are used in the connection to differential amplifier circuit. The voltage feedback circuit is connected to the control circuit with the help of resistances R_{43} and R_{36}. In the circuit the voltage v_{13} which is obtained from the voltage divider circuit is directly fed via resistance R_{43} to PI_1 i.e. the frequency compensation circuit connecting the Pin 9 (Compensation) and Pin 1(Inverting) of one of the PWM IC UC3525A. Similarly, the voltages v_{11} and v_{12} are passed through the differential amplifier and the output of TL084 is fed via resistance R_{36} to PI_2 i.e. frequency compensation circuit of another UC3525A.

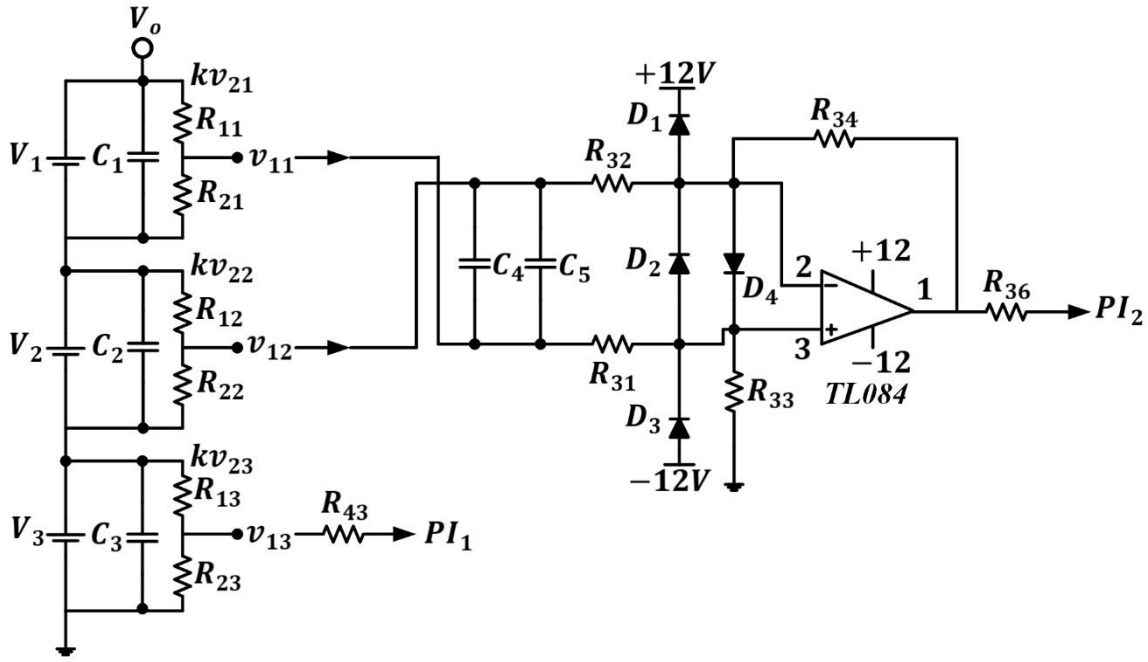


Figure 2.30: Schematic of the hardware voltage feedback loop

2.8 Hardware Design of the Entire Control Circuit

The entire control circuit schematic has been extensively presented in the Fig. 2.31. The concept has been built on a Printed Circuit Board (PCB) prototype for the hardware designing of the control circuit for the proposed DC-DC converter. Here the resistance, potentiometer, capacitance, diodes and all other passive components have been labeled as per the PCB prototype. Presentation of the entire control circuit in schematic form helps in justifying the idea which have been extensively proposed and waveforms shown in the sections 2.6 and 2.7.

The photograph of the control circuit PCB is presented in Appendix A.

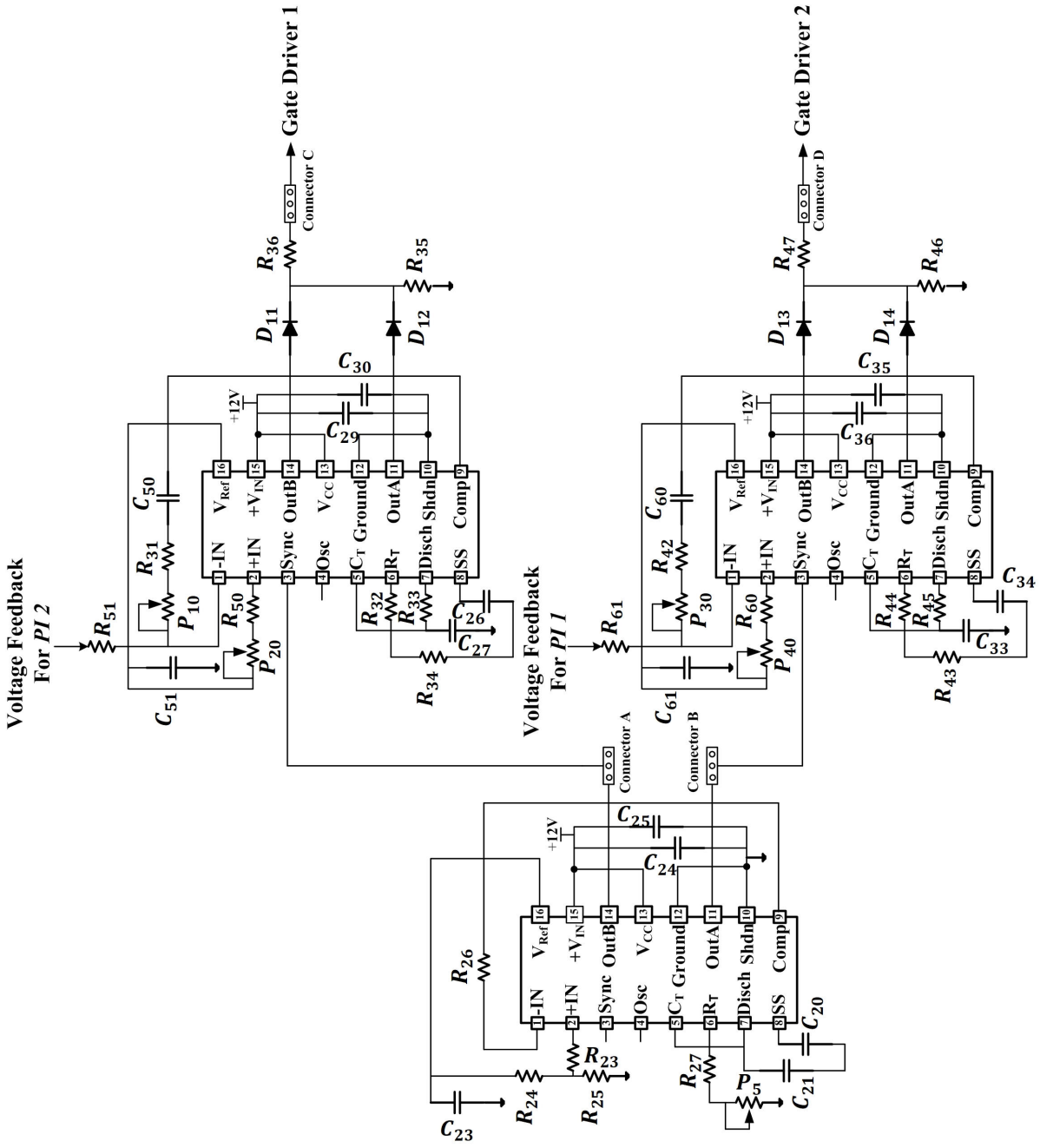


Figure 2.31: Schematic diagram of the total control circuit

2.9 Conclusion

A non-isolated floating output boost DC-DC converter is proposed. The structure comprises of two interleaved buck-boost sub-converters. The highlights of the proposed converter is (a) the output of each sub-converter adds up to the positive and negative side of the input DC bus rail, (b) the volume and size of the entire system as well as losses due to leakage inductance is alleviated, (c) interleaved switching function diminishes the input

current ripple and the output voltage ripple and (d) the sub-converters are not accountable of handling the total power thus reducing the ratings of the semiconductor devices. In depth discussion of the conduction states (CCM and DCM) of the proposed converter is schematically presented and mathematically analyzed.

The Fig. 2.32 represents the proposed control scheme for the converter. The actual input DC voltage (V_i) is subtracted from the set output reference voltage (V_o^*) and the difference is divided by 2 to create the two equal references (V_a^* and V_b^*) for the two individual converters. The two added components of output DC voltage from each converter (V_a, V_b) are compared with their reference voltages and each error is processed in separate Proportional Integral-Controller (PI-Controller) to obtain the reference for the corresponding ramp generator waveforms shifted 180° in phase so that individual converter switching duty cycle can be set. Both the switches S_a & S_b (see Fig. 2.1) simultaneously determine the total output voltage, thus V_a^* and V_b^* are set to be the same for balanced power flow through each converter. This takes care of misalliance in switches or inductance values such that even if individual converter outputs differ slightly, the total output voltage will be regulated against load variations at D>0. The resulting pulses are then fed to the individual power switches through isolated gate drivers.

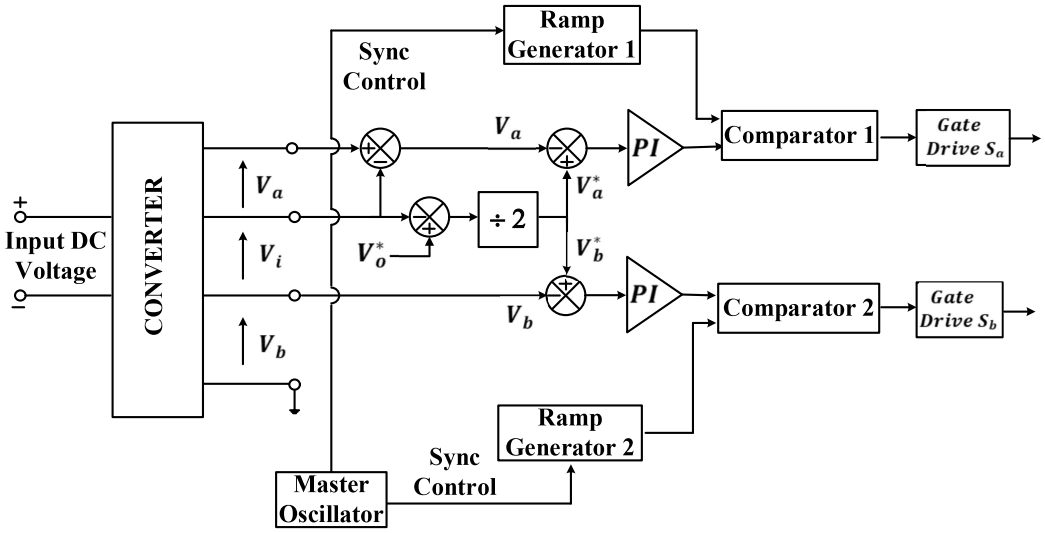


Figure 2.32: Block diagram of the control scheme

The efficacy of the proposed converter will be ascertained further in the following chapter where small signal modeling and the Bode plot will be derived and presented. Then the parameter selection for extensive hardware prototype and results from the setup will be shown to further validate the practicality and the acceptability of the proposed converter system.

Chapter 3

State Space Modeling and Results from Hardware Prototype

3.1 State Space Model

3.1.1 Introduction

In the conventional approach carried out in control systems via transfer function and the graphical approach viz. root locus, Bode plot and Nyquist plot the relation between the input and output is in the form of transfer function. Here, it is taken into consideration that the initial condition is zero i.e. the system is assumed to be at rest at the initial condition. However, if the multi-input and multi-output systems are considered then these systems are not at rest at the initial condition. Therefore, it can be stated that the transfer function based analysis will be inefficient and not convenient for multi-input multi-output (MIMO) based control systems.

State space method for analysis is a suitable approach to get over the drawbacks of the transfer function method. In the state space method the equations in the MIMO system can be organized in the matrix form which enables its simplified solution. Some the basic terms regarding the state space analysis are as follows [82],[83]:

1. State Variables: It can be stated as the smallest set of variables which assists in determining the state of a dynamic system.
2. State: It is depicted as the smallest set of variables such that the knowledge at initial condition i.e. $t=t_O$ along with all the inputs is able to determine the behavior of the system at any time $t>t_O$.
3. State Vector: Assuming that n state variables is necessary to ascertain the complete behavior of the system that is given, then n state variables are contemplated as n components of a vector $x(t)$. The vector is stated to be a state vector.
4. State Space: The n dimensional state variables are elements of the n dimensional space (having $x_1, x_2....x_n$ axis), which can be stated as state space.

In the following section the prime objective is to obtain the small signal transfer function

$\frac{\tilde{v}_o(s)}{\tilde{d}(s)}$, for the proposed converter in the CCM. Here, $\tilde{v}_o$ and $\tilde{d}$ represent small perturbations in the output voltage and duty ratio of the switch around the steady-state DC operating values V_O and D.

The proposed converter for which the small signal transfer function is to be obtained is considered to operate in CCM. Therefore, the various cases for the conduction states of the switch are discussed and the current and voltage equations are developed.

3.2 State Space Modelling for the Proposed Converter

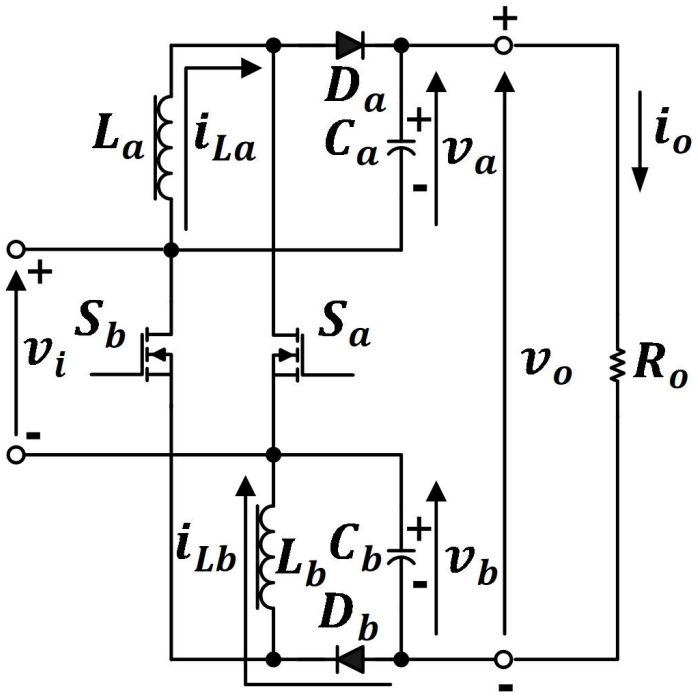


Figure 3.1: Schematic for State Space Modeling

Here v_i is the input voltage, v_o is the total output voltage, v_a is the output for converter 'a' and v_b is the output for converter 'b'. The lower case letters are variable which is explained later in the section in equation number (3.20). L_a and L_b are inductance for converter 'a' and 'b' respectively. As the value of capacitance for both the sub-converters of the proposed DC-DC converter are same it is expressed as:

$$C_a = C_b = C \text{ (say)} \tag{3.1}$$

A. Case I

When the switch S_a is ON

$$v_i - L_a \frac{di_{La}}{dt} = 0$$
$$\overline{i}_{La} = \frac{v_i}{L_a} \tag{3.2}$$

$$C\frac{dv_a}{dt} = -\frac{v_a}{R_o}$$
$$\overline{v}_a = -\frac{v_a}{R_o C} \tag{3.3}$$

B. Case II

When the switch S_b is ON

$$v_i - L_b \frac{di_{Lb}}{dt} = 0$$
$$\overline{i}_{Lb} = \frac{v_i}{L_b} \tag{3.4}$$

$$-C\frac{dv_b}{dt} = \frac{v_b}{R_o}$$
$$\overline{v}_b = -\frac{v_b}{R_o C} \tag{3.5}$$

C. Case III

When the switch S_a is OFF

$$-L_a \frac{di_{La}}{dt} - v_a = 0$$
$$\overline{i}_{La} = -\frac{v_a}{L_a} \tag{3.6}$$

$$-i_{La} + C\frac{dv_a}{dt} + \frac{v_a}{R_o} = 0$$
$$\overline{v}_a = \frac{i_{La}}{C} - \frac{v_a}{R_o C} \tag{3.7}$$

D. Case IV

When the switch S_b is OFF

$$-L_b\frac{di_{Lb}}{dt} - v_b = 0$$
$$\overline{i}_{Lb} = -\frac{v_b}{L_b} \tag{3.8}$$

$$i_{Lb} - C\frac{dv_b}{dt} - \frac{v_b}{R_o} = 0$$
$$\overline{v}_b = -\frac{v_b}{R_o C} + \frac{i_{Lb}}{C} \tag{3.9}$$

The Fig. 3.2 shows schematically the conduction states of the switches S_a and S_b over a switching period. During each state of the circuit, the circuit (linear) is illustrated by state variable vector 'x' comprising of inductor current and capacitor voltage. The lowercase letter depicts a variable, which contains steady state DC value and a small AC perturbation [17].

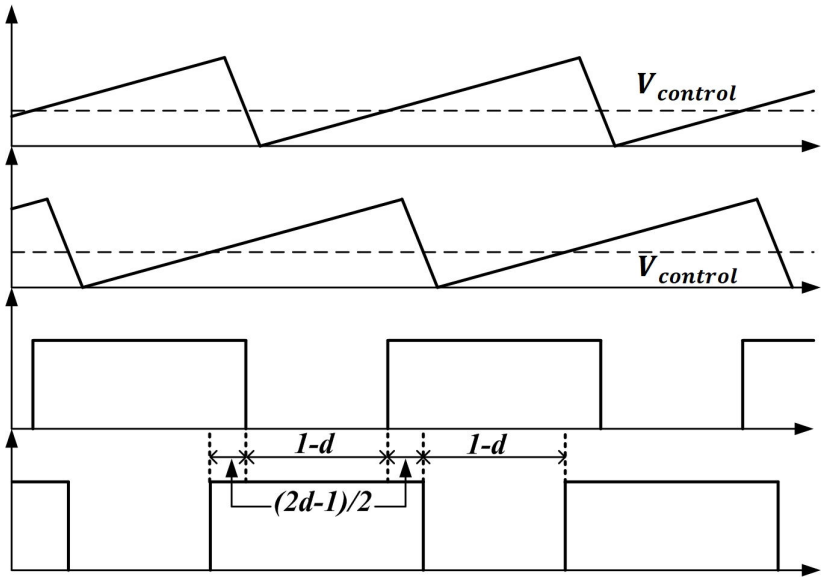


Figure 3.2: Conduction states of the switches over a switching period

So, the equations can be expressed as:

$$\dot{\mathrm{x}} = \mathrm{A}_1\mathrm{x} + \mathrm{B}_1 v_i \quad \text{during} \quad \frac{2d-1}{2} \tag{3.10}$$

$$\dot{\mathrm{x}} = \mathrm{A}_2\mathrm{x} + \mathrm{B}_2 v_i \quad \text{during} \quad 1-d \tag{3.11}$$

$$\dot{\mathrm{x}} = \mathrm{A}_3\mathrm{x} + \mathrm{B}_3 v_i \quad \text{during} \quad \frac{2d-1}{2} \tag{3.12}$$

$$\dot{\mathrm{x}} = \mathrm{A}_4\mathrm{x} + \mathrm{B}_4 v_i \quad \text{during} \quad 1-d \tag{3.13}$$

Where, A_1, A_2, A_3 and A_4 represent state matrices and B_1, B_2, B_3 and B_4 are vectors.

The output v_o of the converters is represented in terms of their state variables as:

$$v_o = \mathrm{C}_1\mathrm{x} + \mathrm{P}_1 v_i \quad \text{during} \quad \frac{2d-1}{2} \tag{3.14}$$

$$v_o = \mathrm{C}_2\mathrm{x} + \mathrm{P}_2 v_i \quad \text{during} \quad 1-d \tag{3.15}$$

$$v_o = \mathrm{C}_3\mathrm{x} + \mathrm{P}_3 v_i \quad \text{during} \quad \frac{2d-1}{2} \tag{3.16}$$

$$v_o = \mathrm{C}_4\mathrm{x} + \mathrm{P}_4 v_i \quad \text{during} \quad 1-d \tag{3.17}$$

Where, C_1, C_2, C_3 and C_4 are transposed vectors.

The representation of the average description of the converter over a switching period can be done with the equations of the various states to be time weighted and averaged, which results in the following equations:

$$\begin{aligned}\dot{\mathrm{x}} = {} & [\mathrm{A}_1\frac{(2d-1)}{2} + \mathrm{A}_2(1-d) + \mathrm{A}_3\frac{(2d-1)}{2} + \mathrm{A}_4(1-d)]\mathrm{x} \\ & + [\mathrm{B}_1\frac{(2d-1)}{2} + \mathrm{B}_2(1-d) + \mathrm{B}_3\frac{(2d-1)}{2} + \mathrm{B}_4(1-d)]v_i\end{aligned} \tag{3.18}$$

and

$$\begin{aligned}v_o = {} & [\mathrm{C}_1\frac{(2d-1)}{2} + \mathrm{C}_2(1-d) + \mathrm{C}_3\frac{(2d-1)}{2} + \mathrm{C}_4(1-d)]\mathrm{x} \\ & + [\mathrm{P}_1\frac{(2d-1)}{2} + \mathrm{P}_2(1-d) + \mathrm{P}_3\frac{(2d-1)}{2} + \mathrm{P}_4(1-d)]v_i\end{aligned} \tag{3.19}$$

$$x=X+\tilde{x}$$

$$v_o = V_o + \tilde{v}_o$$

Where, $$d = D + \tilde{d} \qquad (3.20)$$

$$v_i = V_i$$

Using the equation number (3.20) in equation number (3.18) the equation can be given as:

$$\begin{aligned}\dot{\tilde{x}}=&[A_1 D - \frac{A_1}{2} + A_2 - A_2 D + A_3 D - \frac{A_3}{2} + A_4 - A_4 D]X \\ &+[B_1 D - \frac{B_1}{2} + B_2 - B_2 D + B_3 D - \frac{B_3}{2} + B_4 - B_4 D]V_i \\ &+[A_1 D - \frac{A_1}{2} + A_2 - A_2 D + A_3 D - \frac{A_3}{2} + A_4 - A_4 D]\tilde{x} \\ &+[A_1 X - A_2 X + A_3 X - A_4 X + B_1 V_i - B_2 V_i + B_3 V_i - B_4 V_i]\tilde{d}\end{aligned} \qquad (3.21)$$

The steady state equation obtained from equation number (3.21) by fixing the perturbation and derivative terms to zero. Hence, the steady state equation is expressed as:

$$AX + BV_i = 0 \qquad (3.22)$$

Therefore, the equation number (3.21) can be expressed as:

$$\begin{aligned}\dot{\tilde{x}}=&[A_1 D - \frac{A_1}{2} + A_2 - A_2 D + A_3 D - \frac{A_3}{2} + A_4 - A_4 D]\tilde{x} \\ &+[A_1 X - A_2 X + A_3 X - A_4 X + B_1 V_i - B_2 V_i + B_3 V_i - B_4 V_i]\tilde{d}\end{aligned} \qquad (3.23)$$

Similarly using equation number (3.20) in equation number (3.19) the equation obtained:

$$\begin{aligned}V_o+\tilde{v}_o=&[C_1 D - \frac{C_1}{2} + C_2 - C_2 D + C_3 D - \frac{C_3}{2} + C_4 - C_4 D]X \\ &+[P_1 D - \frac{P_1}{2} + P_2 - P_2 D + P_3 D - \frac{P_3}{2} + P_4 - P_4 D]V_i \\ &+[C_1 D - \frac{C_1}{2} + C_2 - C_2 D + C_3 D - \frac{C_3}{2} + C_4 - C_4 D]\tilde{x} \\ &+[C_1 X - C_2 X + C_3 X - C_4 X + P_1 V_i - P_2 V_i + P_3 V_i - P_4]\tilde{d}\end{aligned} \qquad (3.24)$$

Therefore, from equation number (3.24) the next set of equations can be obtained as:

$$\begin{aligned}\tilde{v}_o=&[C_1 D - \frac{C_1}{2} + C_2 - C_2 D + C_3 D - \frac{C_3}{2} + C_4 - C_4 D]\tilde{x} \\ &+[C_1 X - C_2 X + C_3 X - C_4 X + P_1 V_i - P_2 V_i + P_3 V_i - P_4 V_i]\tilde{d}\end{aligned} \qquad (3.25)$$

The equation number (3.23) and (3.25) comprises of AC perturbations. Using Laplace transformation the expression for transfer function can be obtained as:

$$T_{p(s)}=\frac{\tilde{v}_o(s)}{\tilde{d}(s)}=\mathrm{C[SI-A]^{-1}B+E} \tag{3.26}$$

Where, I is the unity matrix.

From the equation numbers (3.2) to (3.9) the state matrices and vectors can be represented as:

$$\begin{bmatrix} \dot{i}_{La} \\ \dot{v}_a \\ \dot{i}_{Lb} \\ \dot{v}_b \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & -\frac{1}{R_oC} & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{R_oC} \end{bmatrix} \begin{bmatrix} i_{La} \\ v_a \\ i_{Lb} \\ v_b \end{bmatrix} + \begin{bmatrix} \frac{1}{L_a} \\ 0 \\ \frac{1}{L_b} \\ 0 \end{bmatrix} v_i \tag{3.27}$$

A_1 B_1

$$\begin{bmatrix} \dot{i}_{La} \\ \dot{v}_a \\ \dot{i}_{Lb} \\ \dot{v}_b \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & -\frac{1}{R_oC} & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{L_b} \\ 0 & 0 & \frac{1}{C} & -\frac{1}{R_oC} \end{bmatrix} \begin{bmatrix} i_{La} \\ v_a \\ i_{Lb} \\ v_b \end{bmatrix} + \begin{bmatrix} \frac{1}{L_a} \\ 0 \\ 0 \\ 0 \end{bmatrix} v_i \tag{3.28}$$

A_2 B_2

$$\begin{bmatrix} \dot{i}_{La} \\ \dot{v}_a \\ \dot{i}_{Lb} \\ \dot{v}_b \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & -\frac{1}{R_oC} & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{R_oC} \end{bmatrix} \begin{bmatrix} i_{La} \\ v_a \\ i_{Lb} \\ v_b \end{bmatrix} + \begin{bmatrix} \frac{1}{L_a} \\ 0 \\ \frac{1}{L_b} \\ 0 \end{bmatrix} v_i \tag{3.29}$$

A_3 B_3

$$\begin{bmatrix} \dot{i}_{La} \\ \dot{v}_a \\ \dot{i}_{Lb} \\ \dot{v}_b \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L_a} & 0 & 0 \\ \frac{1}{C} & -\frac{1}{R_o C} & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{R_o C} \end{bmatrix} \begin{bmatrix} i_{La} \\ v_a \\ i_{Lb} \\ v_b \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ \frac{1}{L_b} \\ 0 \end{bmatrix} v_i \qquad (3.30)$$

A4 B4

Therefore, from equation number (3.23) it can be obtained:

$$[\mathrm{A}] = \begin{bmatrix} 0 & \frac{D-1}{L_a} & 0 & 0 \\ \frac{1-D}{C} & -\frac{1}{R_o C} & 0 & 0 \\ 0 & 0 & 0 & \frac{D-1}{L_b} \\ 0 & 0 & \frac{1-D}{C} & -\frac{1}{R_o C} \end{bmatrix} \text{ and } \qquad [B] = \begin{bmatrix} \frac{v_i + v_a}{L_a} \\ -\frac{i_{La}}{C} \\ \frac{v_i + v_b}{L_b} \\ -\frac{i_{Lb}}{C} \end{bmatrix} \qquad (3.31)$$

Similarly, from equation number (3.25) it can be obtained:

$$[C] = [0 \quad 1 \quad 0 \quad 1] \text{ and } \qquad [E] = [0] \qquad (3.32)$$

Therefore, substituting the values from equation numbers (3.31) and (3.32) into (3.26) the expression for transfer function can be obtained as:

$$T_{p(s)} = \frac{\tilde{v}_o(s)}{\tilde{d}(s)} = \frac{\left[s^2 + \frac{s}{R_o C} - \frac{(1-D)(D-1)}{L_b C}\right]\left[\frac{v_i + v_a(1-D)}{L_a C} - \frac{i_{La}}{C}s\right] + \left[s^2 + \frac{s}{R_o C} - \frac{(1-D)(D-1)}{L_a C}\right]\left[\frac{v_i + v_b(1-D)}{L_b C} - \frac{i_{Lb}}{C}s\right]}{\left[s^2 + \frac{s}{R_o C} + \frac{(1-D)(1-D)}{L_b C}\right]\left[s^2 + \frac{s}{R_o C} + \frac{(1-D)(1-D)}{L_a C}\right]} \qquad (3.33)$$

In the equation number (3.33) $v_i + v_a = \frac{v_o}{1+D}$ can be expressed.

Therefore, further simplifying the equation number (3.33) it can be expressed as:

$$T_{p(s)} = \frac{\tilde{v}_o(s)}{\tilde{d}(s)} = \frac{\left[\frac{V_o(1-D)}{L_aC(1+D)} - \frac{I_{La}}{C}s\right]}{\left[s^2 + \frac{s}{R_oC} + \frac{(1-D)(1-D)}{L_aC}\right]} + \frac{\left[\frac{V_o(1-D)}{L_bC(1+D)} - \frac{I_{Lb}}{C}s\right]}{\left[s^2 + \frac{s}{R_oC} + \frac{(1-D)(1-D)}{L_bC}\right]} \quad (3.34)$$

In equation number (3.34) I_{La} and I_{Lb} are the steady state average values of the inductor L_a and L_b respectively. V_o is the steady state average value for the total output voltage.

Hence the small signal transfer function for the proposed converter is deduced successfully and presented clearly in the equation number (3.34).

Now, various parameters for the proposed DC-DC boost converter need to be ascertained. The following sections will aid in determining the values for the passive components as well as governing the correct value for the semiconductor components which is necessary for building the hardware prototype of the converter.

3.3 Inductor Design

3.3.1 Introduction

Power level inductors are one of the crucial passive components in the circuit system. In the field of power electronics there is a huge upsurge in high frequency DC-DC boost converters with increased efficacy and reliability. Therefore, the inductors are of prime importance as it aids in filtering aspects, used as an energy storage element and as an instantaneous high impedance to arrest over current surge to name a few. There is a substantial amount of literature present in the sphere which assists in inductor designing [84],[85]. Magnetic circuits in practical are provided with air gap. When the flux lines crosses the air gap it tends to follow curved path and not the shortest path across the gap. This effect is known as fringing which increases the effective area of the air gap from the area of the core which can be vividly seen in Fig. 3.2. The term A_{ag} represents area of flux (effective) in the air gap, A_{gm} is the core area (mechanical), l_{ml} depicts the mean magnetic path length traversing the magnetic material, l_{ag} is the total air gap length of the inductor and N represents number of turns present. The presence of fringing factor usually

complicates the design process. The process followed in the following section accurately accomplishes the design without considering fringing factor as a vital determining factor.

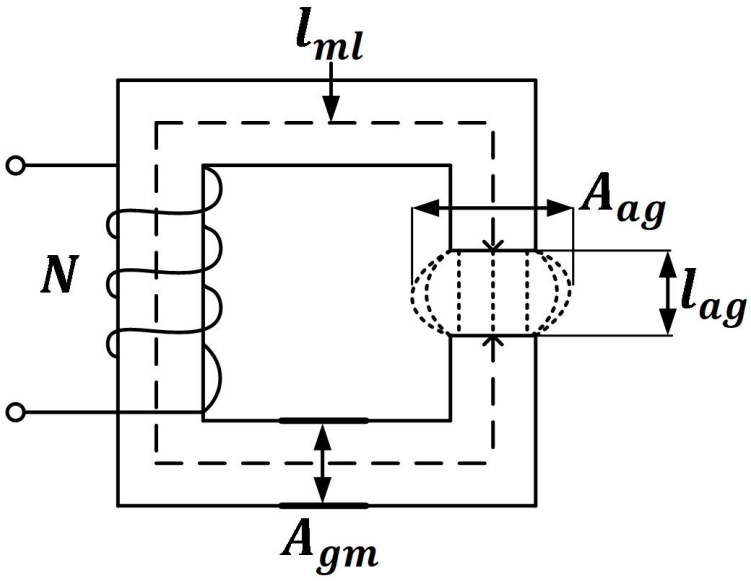


Figure 3.3: Diagram for inductor magnetic circuit

3.3.2 Inductor Value Determination

Primarily the input voltage, output voltage and the output power have been assumed which is necessary in deriving the approximate value of the power level inductor.

For the overall system level (proposed converter):

Assume: V_O= 690V, V_i= 110V, P_O= 1500W.

Therefore, from the above parameter values the output current can be ascertained as:

$$I_o = \frac{P_o}{V_o} = \frac{1500}{690} = 2.174\text{A} \tag{3.35}$$

$$I_o' = 2.174\text{A} \tag{3.36}$$

Where, I_o' indicates the output current for each converter level.

$$V_o' = \frac{V_o - V_i}{2} = \frac{690 - 110}{2} = 290\text{V} \tag{3.37}$$

Where, V_o' indicates output voltage for individual converter level

$$P_o' = V_o' \text{x} I_o' = 290\text{x}2.174 = 630.5\text{W} \tag{3.38}$$

Where, P_o' indicates output power for each sub-converter

The switching frequency is assumed to be $f_{sw} = 50\text{kHz}$.

$$I_i' = \frac{P_o'}{\eta V_i} = \frac{630.5}{0.8\text{x}110} = 7.16\text{A} \tag{3.39}$$

Where, I_i' indicates input current for individual sub-converter

The duty ratio of the converter can be expressed as:

$$D = \frac{V_o'}{V_o' + V_i} = \frac{290}{290 + 110} = 0.725 \tag{3.40}$$

The average inductor voltage for each sub-converter can be expressed as:

$$I_{L(avg)} = I_i' + I_o' = 7.16 + 2.174 = 9.334\text{A} \tag{3.41}$$

Assuming the ripple inductor current is 20% of $I_{L(avg)}$, hence it is expressed as:

$$\Delta I_L = 20\% I_{L(avg)} = 1.87\text{A} \tag{3.42}$$

Finally the value of the inductor can be determined as:

$$L = \frac{V_i D}{\Delta I_L f_{sw}} = \frac{110\text{x}0.725}{1.87\text{x}(50\text{x}10^3)} = 0.853\text{mH} \approx 0.85\text{mH} \tag{3.43}$$

The peak value of the current in the converter can be expressed as:

$$I_{pk} = I_{L(avg)} + \frac{\Delta I_L}{2} = 9.33 + \frac{1.87}{2} = 10.27\text{A} \tag{3.44}$$

Finally, the rms current is given as:

$$I_{rms} = I_{L(avg)} \approx 9.33\text{A} \tag{3.45}$$

3.3.3 Design Process of the Inductor

The section 3.3.2 determines the value for inductance which is vital for the designing purpose of the power level inductor. Therefore further proceeding, the step wise calculation for the inductor is shown.

The values of various which are given:

$L = 0.85\text{mH}$, $I_{L(avg)} = I_{dc} = 9.33\text{A}$, $\Delta I_L = 1.87\text{A}_{pk\text{-}pk}$, $I_{pk} = 10.27\text{A}$ and $I_{rms} = 9.33\text{A}$.

Assume: $B_{pk} = 0.27\text{T}$, $J_c = 300\text{A/cm}^2$, $K_{wi} = 0.35$ and $K_{st} = 1$ [86].

Where, B_{pk} is the peak flux density in the core, J_c is the current density, K_{wi} is the window utilization factor and K_{st} is the stacking factor.

The Area product of the solid core can be expressed as:

$$A_{ap} = \frac{LI_{pk}I_{rms}}{K_{wi}B_{pk}J_c} = \frac{0.85\text{x}10^{-3}\text{x}10.27\text{x}9.33\text{x}10^{4}}{0.35\text{x}0.27\text{x}300} = 28.73\text{cm}^4 \quad (3.46)$$

Selecting the ferrite core EE-65-27, one pair from manufacturer's data [87] having:

The effective core area which is same as the mechanical core area $A_{ec} = 5.48\text{cm}^2$, the required window area to accommodate the winding $A_{wi} = 5.372\text{cm}^2$ and the area product obtained from the datasheet $A_{ap} = 29.44\text{cm}^4$.

The number of turns which is necessary is given by:

$$N = \frac{LI_{pk}}{B_{pk}A_{ec}} = \frac{0.85\text{x}10^{-3}\text{x}10.27\text{x}10^{4}}{0.27\text{x}5.48} = 59 \quad (3.47)$$

Therefore, $N = 59$ turns are required.

The current density is chosen to be $J_c = 300A/\text{cm}^4$ as stated earlier. The conductor cross sectional area is expressed as:

$$a_{ca} = \frac{I_{rms}}{J_c} = \frac{9.33}{300} = 3.11\text{mm}^2 \quad (3.48)$$

Irms is the rms current through the inductor.

To reduce the skin effect loss the expression is given as:

$$d_{\max} < \frac{145.3}{\sqrt{f_{sw}}} = \frac{145.3}{\sqrt{50\text{x}10^{3}}} = 0.649\text{mm} \quad (3.49)$$

i.e. 23SWG from the manufacturer's datasheet and $a_c = 0.2919\text{mm}^2$

$$\text{Hence the number of conductors} = \frac{3.11}{0.2919} = 10.65 \approx 10 \quad (3.50)$$

For proper fitting of the winding, 23SWG is necessary with 10 conductors in parallel i.e.

$$a_{ca} = 0.2919\text{x}10 = 2.919\text{mm}^2 \quad (3.51)$$

Again, the fitting needs to be checked properly

$$A_{wi} = \frac{a_{ca}N}{K_{wi}} = \frac{2.919\text{x}59}{0.35\text{x}100} = 4.92\text{cm}^2 \quad (3.52)$$

This fitting will perfectly fit into the available window area (manufacturer's datasheet) of 5.372cm^2.

Thus, the actual current density that is obtained:

$$J_c = \frac{I_{rms}}{a_{ca}} = \frac{9.33}{2.919} = 3.19\text{A/mm}^2 \text{ or } 319\text{A/cm}^2 \quad (3.53)$$

3.3.4 Calculation of Air Gap of the Inductor

The calculation of the air gap required for the inductor designed can be accomplished using approximation method.

The inductance with the present configuration can be expressed as [86]:

$$L = \frac{N\phi_{pk}}{I_{pk}} = \frac{N^2 I_{pk}\mu_o F_f A_{ec}}{l_{ag} I_{pk}} = \frac{N^2 \mu_o F_f A_{ec}}{l_{ag}} \quad (3.54)$$

Where, ϕ_{pk} is the peak flux in the magnetic circuit.

μ_o is the permeability of free space (defined value $= 4\pi\text{x}10^{-7}\text{H/m}$)

F_f is the fringing factor.

l_{ag} is the total length of the air gap.

Therefore, $\frac{l_{ag}}{F_f} = \frac{0.4\pi N^2 A_{ec}\text{x}10^{-8}}{L} = \frac{0.4\pi\text{x}59^2\text{x}5.48\text{x}10^{-8}}{0.85\text{x}10^{-3}} = 0.282$ (3.55)

Assuming the initial value of $F_f = 1.2$ then $l_{ag} = 0.338\text{cm}$

The fringing factor formula [88] [89] given as:

$$F_f = 1 + \frac{l_{ag}}{\sqrt{A_{ec}}}\ln\left(\frac{2H_{wi}}{l_{ag}}\right) \quad (3.56)$$

Where, A_{ec} is the effective area of the core.

H_{wi} is the effective height of the window or the limb.

$$F = 1 + \frac{0.338}{\sqrt{5.48}}\ln\left(\frac{2\text{x}4.44}{0.338}\right) = 1.472 \quad (3.57)$$

Therefore, if $l_{ag} = 0.4151\text{cm}$ then from equation number (3.56) $F_f = 1.543$

for $l_{ag} = 0.4352\text{cm}$ then $F_f = 1.560$

for $l_{ag} = 0.4401\text{cm}$ then $F_f = 1.564$

for $l_{ag} = 0.4412\text{cm}$ then $F_f = 1.565$

for $l_{ag} = 0.4415\text{cm}$ then $F_f = 1.566$

$$\text{for } l_{ag} = 0.4416\text{cm} \text{ then } F_f = 1.566$$

$$\text{for } l_{ag} = 0.4416\text{cm} \text{ then } F_f = 1.566 \tag{3.58}$$

Since the values become reasonably stable the final values are as obtained from equation number (3.58).

Hence, for $l_{ag} = 0.4416\text{cm}$ the length of the sole air gap can be expressed as:

$$l_{sa} = \frac{l_{ag}}{2} = \frac{0.4416}{2} = 0.2208\text{cm}=2.21\text{mm} \tag{3.59}$$

In the Fig. 3.4 the dimension of the ferrite core (EE-65-27) is clearly specified which is obtained from the datasheet [90].

As approximate calculation is carried out for the fabrication process of the inductor, it is necessary to adjust the final value for air gap until the required inductance obtained in equation number (3.43) is correctly obtained. The required number of turns is adjusted and fitted into the bobbin for the core. The EE ferrite core halves are duly fitted onto the bobbin leaving the required air gap. The inductance is measured during this fabrication process and final adjustment in the air gap is done.

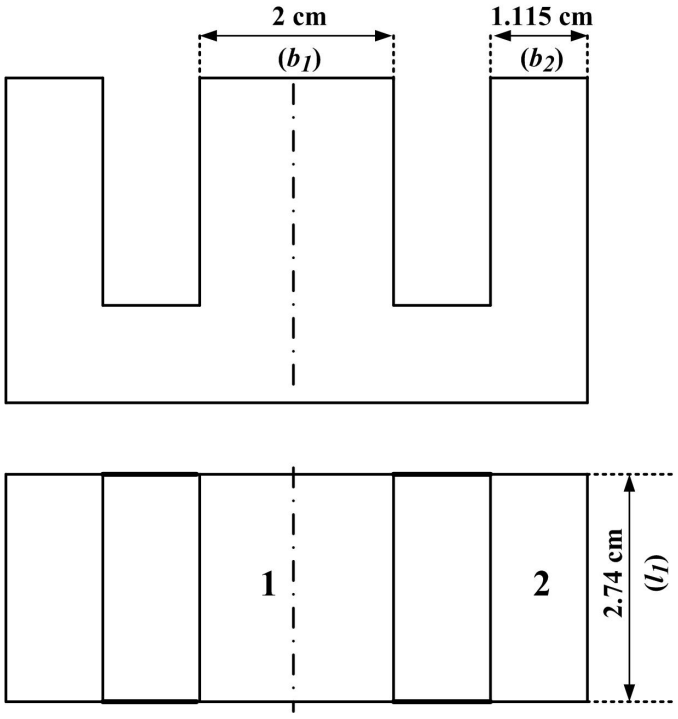


Figure 3.4: Dimension of the EE-65-27 ferrite core

Using the value of $l_{sa} = 0.182\text{cm}$ throughout (each air gap)

$$x = \frac{l_{sa}}{\pi k_{as}} \ln \frac{2.132H}{l_{sa}} \tag{3.60}$$

Where, k_{as} is the ratio between $\frac{l_1}{b_1}$ for (3.61) and $\frac{l_1}{b_2}$ for (3.62) (refer Fig. 3.4).

$H = H_{wi} + l_{sa}$, therefore, $H = 4.44 + 0.182 = 4.622\text{cm}$.

Therefore, for an increase in core dimension '*x*' on each side for area '1' (refer Fig. 3.4),

$$x = \frac{0.182}{\pi \text{x} \frac{2.74}{2}} \ln \frac{2.132\text{x}4.622}{0.182} = 0.168 \tag{3.61}$$

Similarly for increase in core dimension '*x*' on each side for area '2',

$$x = \frac{0.182}{\pi \text{x} \frac{2.74}{1.115}} \ln \frac{2.132\text{x}4.622}{0.182} = 0.0941 \tag{3.62}$$

Now, the fringing factor for area '1' can be expressed as:

$$\begin{aligned} F_1 &= (b_1 + (2x))(l_1 + (2x)) \\ F_1 &= (2 + (2\text{x}0.168))\text{x}(2.74 + (2\text{x}0.168)) = 7.185 \end{aligned} \tag{3.63}$$

The fringing factor for area '2' can be given as:

$$\begin{aligned} F_1 &= ((2b_2) + (2x))(l_1 + (2x)) \\ F_1 &= (2\text{x}1.115) + (2\text{x}0.0941))\text{x}(2.74 + (2\text{x}0.0941)) = 7.080 \end{aligned} \tag{3.64}$$

For inductance with multiple air gaps can be given as:

$$\begin{aligned} L &= \frac{0.4\pi N^2 \text{x} 10^{-8}}{\Sigma \frac{l_{sa}}{F_f}} \\ L &= \frac{0.4\pi \text{x} 59^2 \text{x} 10^{-8}}{0.182\left(\frac{1}{7.185} + \frac{1}{7.080}\right)} = 0.85\text{mH} \end{aligned} \tag{3.65}$$

3.4 Semiconductor Device Selection

3.4.1 MOSFET Selection

The section 3.3 has dealt with the inductor determination as well as the design parameters. The value of the inductance obtained from section 3.3.2 is vital and necessary for determining approximately the specification for the semiconductor device that can be

employed in the hardware prototype of the proposed DC-DC converter.

Therefore, for the switch selection i.e. MOSFET selection as already obtained from equation number (3.44) the peak current is $I_{pk} = 10.27\text{A}$.

Therefore, it is important to select the drain current of the MOSFET that is given by:

$$I_{DN} = I_{pk}\text{xS.F.xTemparature(S.F)}$$
$$I_{DN} = 10.27\text{x}1.5\text{x}1.5 = 23\text{A} \quad (3.66)$$

In (3.66) Safety Factor (S.F) is introduced. The safety factor implies that with its inclusion there is augmentation in the performance level over the semiconductor's entire operating life. This leads to the increase in reliability and efficiency of the device.

The temperature safety factor is important as the semiconductor device operates at varying temperature leading to thermal stress. Therefore, to reduce the degradation of the device a safety factor constant relating to the temperature level is employed.

In the equation number (3.66) a safety factor constant of 1.5 and a temperature safety factor constant used is 1.5.

The value of the drain to source voltage of the MOSFET can be expressed as:

$$V_{DS} = (V_i + V_o')\,\text{xV.S.F}$$
$$V_{DS} = (110 + 290)\,\text{x}\,2 = 800V \quad (3.67)$$

From equation number (3.37) the values of V_i and V_o' is obtained. The Voltage Safety Factor (V.S.F) used in the equation aids in enhancing the lifetime of the semiconductor device. A semiconductor device will last longer and operate satisfactorily when a V.S.F constant is included compared to a semiconductor device where it degrades at a much faster rate and becomes faulty when exposed to extremes of thermal stress and repetitive transient voltages. Here the safety factor constant used is 2.

In the selection of MOSFET it is of primary importance that it should have low $R_{DS(on)}$. The disadvantages of higher value of $R_{DS(on)}$ is broadly specified in the section 1.5.1.

The MOSFET selected for the operation of the proposed DC-DC converter is categorically specified in Appendix A.

3.4.2 Diode Selection

The selection diode is dependent on the ascertaining the average current of the DC-DC converter and the deriving the Peak Inverse Voltage (PIV). PIV is the indicator of the maximum reverse voltage that the diode may be put through during the reverse biased

interval before breakdown. Manufacturers of diode always specify the value of PIV of a diode in the datasheet. PIV of the diode is same as the peak reverse repetitive voltage also represented as V_{RRM} in the datasheet.

From the equation number (3.35) the average value of the current can be obtained as:

$$I_{avg} = I_o = 2.174\text{A}$$

Hence, the diode to be selected should possess the current specifications

$$= I_o \text{xS.F} = 2.174\text{x}2 \geq 4.35\text{A} \quad (3.68)$$

Here the safety factor constant is 2.

It is advised to select a diode with ampere rating of more than 6A as the proposed DC-DC converter would be subjected to higher value of source current as well as current into the converter during higher operating duty cycle.

The PIV rating is selected to be:

$$\begin{aligned} \text{PIV} &= (V_i + V_o')\,\text{xV.S.F} \\ \text{PIV} &= (110 + 290)\,\text{x}\,2 \geq 800\text{V} \end{aligned} \quad (3.69)$$

The PIV rating should be chosen higher than 800V for satisfactory operation of the diode in the DC-DC boost converter system. It would be ideal to select an Ultra Fast Recovery (UFR) diode to deal with the reverse recovery problem as mentioned in section 1.5.1. In UFR diodes the design of the component is such that it will make the reverse recovery time also known as t_{rr} smaller. The reverse recovery time is the instant at which the forward diode current becomes zero and the instant the reverse current is one-fourth of its reverse peak value. UFR are specifically designed for speed where the t_{rr} is about 25ns, which is very small in magnitude.

The diode selected for the operation of the proposed boost DC-DC converter is categorically specified in Appendix A.

3.5 Bode Plot for the Proposed DC-DC Converter

3.5.1 Introduction

In a feedback control system the stability analysis is built on the s-plane root location for the characteristic equation. The criterion for the system to be stable the roots identified should be on the left hand side of the s-plane. The clause for stability is that whenever any oscillations are brought about into the system with the application of input, dampening out the oscillations with respect to time will classify the system as a stable system. There are

various methods to estimate/evaluate the stability (absolute/relative) of the system.

In this section the Bode plot method for determination of stability is adopted. It is a graphical approach for calculating the stability of the control system which is based particularly on sinusoidal frequency response. In the transfer function of the system the Laplace operator 's' is substituted with '$j\omega$'. Therefore, it handles the frequency response of the system concurrently in the form of magnitude and phase angle. The Bode plot aids in acquiring the stability as well as determining the gain and the phase margin and can be useful in designing lead compensators.

3.5.2 Bode Diagram for the Proposed Converter

The Bode diagram for the proposed converter can be obtained from the transfer function of the proposed DC-DC converter deduced in equation number (3.34) in the section 3.2.

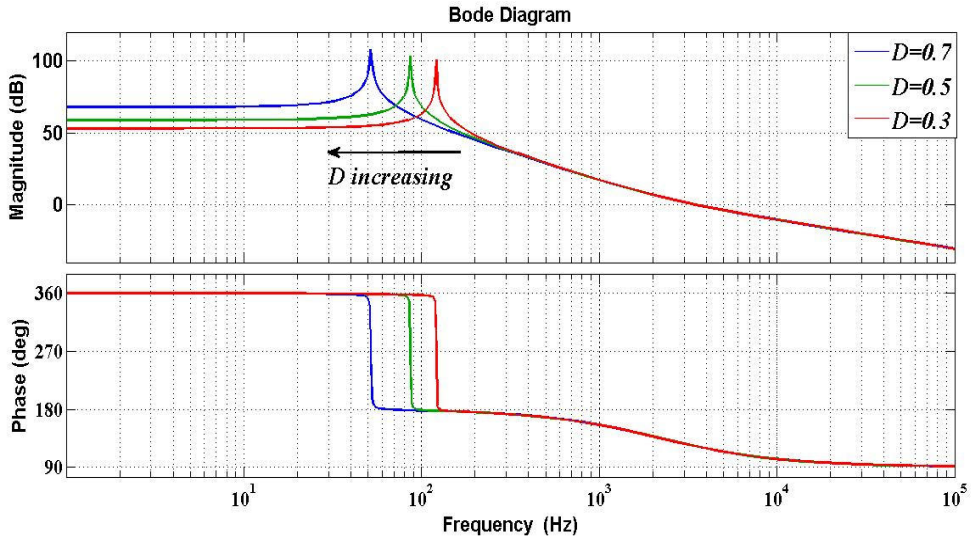


Figure 3.5: Bode diagram for the proposed converter

The Fig. 3.5 shows the Bode diagram for the proposed converter graphically plotted in the MATLAB platform. The figure represents the Bode plot for various duty cycles viz. D=0.3, D=0.5 and D=0.7. In the graphical plot the colors red, green and blue duly represent the duty cycles 0.3, 0.5 and 0.7 respectively.

In Fig. 3.6 the Bode diagram is shown with the peak gain response for duty cycles 0.3 and 0.7. In the graphical plot where the gain peaking frequency is indicated for the mentioned duty cycles, it can be vividly seen in the figure that with increase in duty cycle the gain peaking frequency reduces. The decrease in gain peaking frequency eventually leads to higher possibility of instability of the system in consideration.

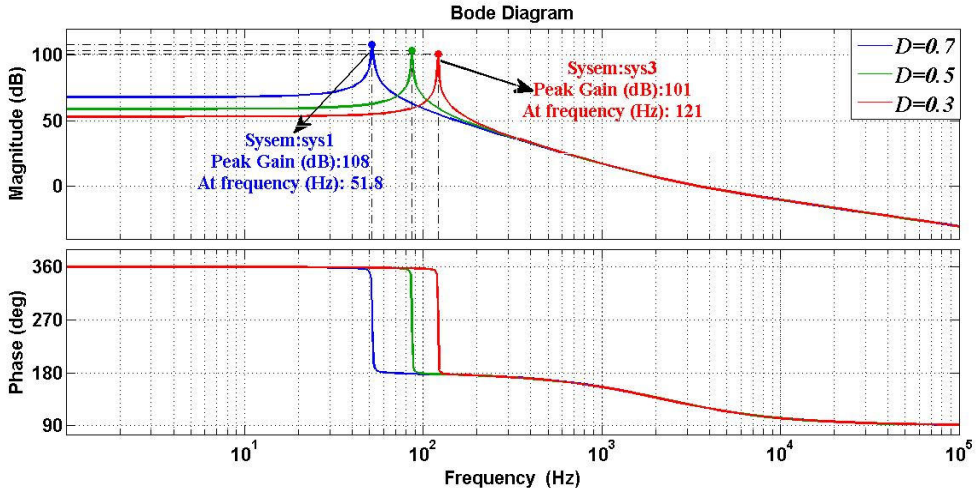


Figure 3.6: Bode diagram with gain peaking frequency

To determine the stability of the given system the pole-zero mapping can act as a major tool. The poles for a transfer function can be determined as, for e.g. $TF(s) = \frac{Num_1(s)}{Den_1(s)}$, the roots for $Den_1(s)$ of the said transfer function will provide the poles. Similarly, the zeroes are the roots of $Num_1(s)$ for the relevant transfer function. Therefore, from equation number (3.34) the pole-zero mapping can be obtained using the MATLAB platform.

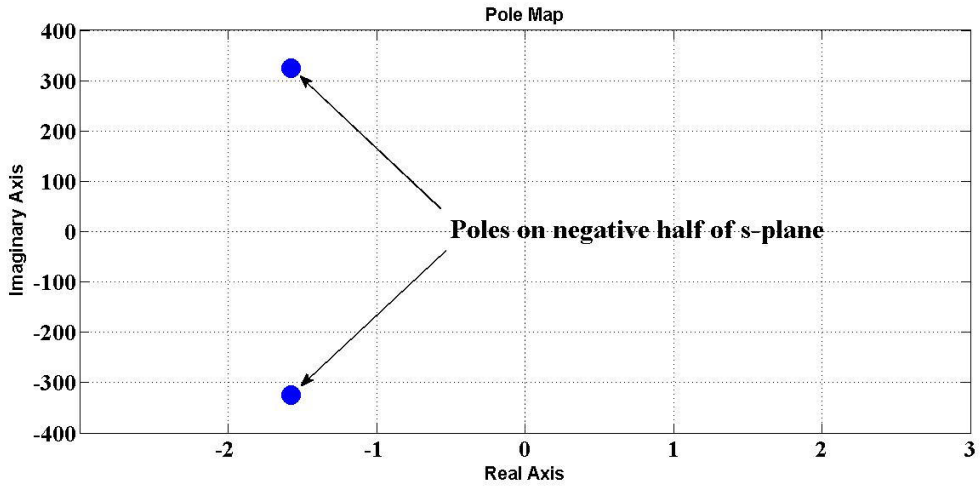


Figure 3.7: Pole mapping for the system transfer function

The location of the poles in the left half of the s-plane can be directly considered that the system is stable. The figure comprising of the pole mapping for the transfer function (3.34), the poles obtained are located on the negative half of s-plane. Hence, it can be stated that the system is stable. The location of zero for the transfer function (3.34) is clearly shown in

the Fig. 3.7.

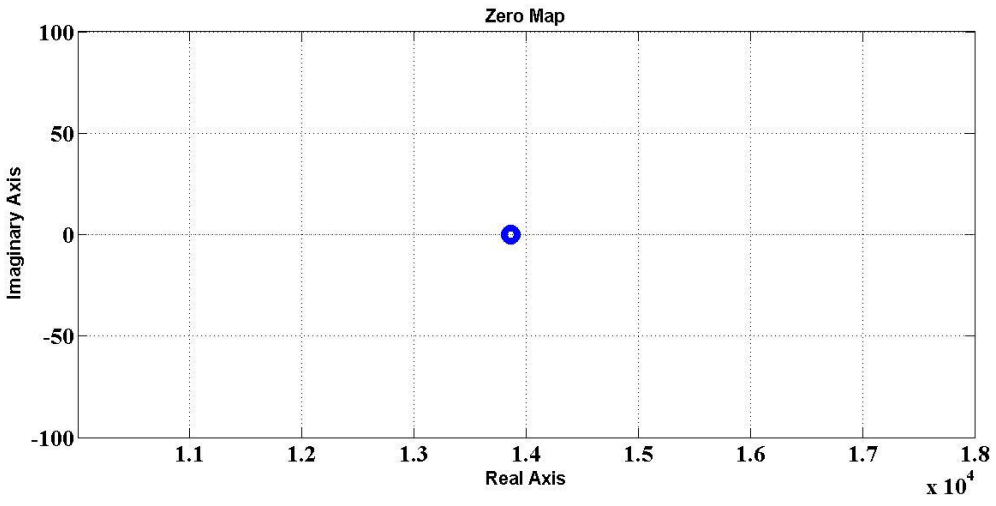


Figure 3.8: Zero mapping of the system

3.6 Simulation Results

3.6.1 Introduction

The section 3.3 has dealt with inductor value determination and design aspects and section 3.4 aids in selection of the specific semiconductor components that will be suitable for proper functioning of the proposed boost DC-DC converter. Therefore, from the assistance of these sections it is required to obtain the results for the proposed converter. The results i.e. simulation results run on MATLAB/Simulink platform and experimental results are of prime importance because it will finally indicate the validity as well as the practicality of the proposed scheme. In this particular section the simulation results will be provided for the converter system.

A MATLAB/Simulink model is established to study and analyze the proposed DC-DC converter. The experimental waveforms which will be shown in following section, has an input voltage V_i of 72V. The input DC voltage is chosen in a manner thinking of battery voltage i.e. 12V each. Hence, it can be assumed the input DC is series connection of six battery stacks. However, the input DC voltage can be increased to a higher level as the components are designed to operate at higher voltage levels as design specifications shown in sections 3.3 and 3.4 respectively. Therefore, in order to compare the experimental waveforms with the simulated results the converter is operated with an input DC voltage V_i of 72V.

The converter is selected to operate at various duty cycles, which is adjusted in discrete steps of 0.3, 0.5 and 0.7. The load regulation was also carried out for proper conduction of the converter at each value of *D*. A capacitor having a value of 1000μF was connected at the input DC bus so that major harmonic currents at the input level are bypassed from the source level. This will result in source current waveform to be a lot cleaner and smoother due to diminished value of harmonics present. The capacitor (C_a and C_b) value at the end of each sub-converter is chosen to be 1000μF each. The inductor (L_a and L_b) value for each sub-converter as determined from section 3.3 is taken as 0.85mH each.

3.6.2 Waveforms of the Converter

The simulation results for the duty cycle 0.7 for the proposed converter is shown in Fig. 3.9 to Fig. 3.14.

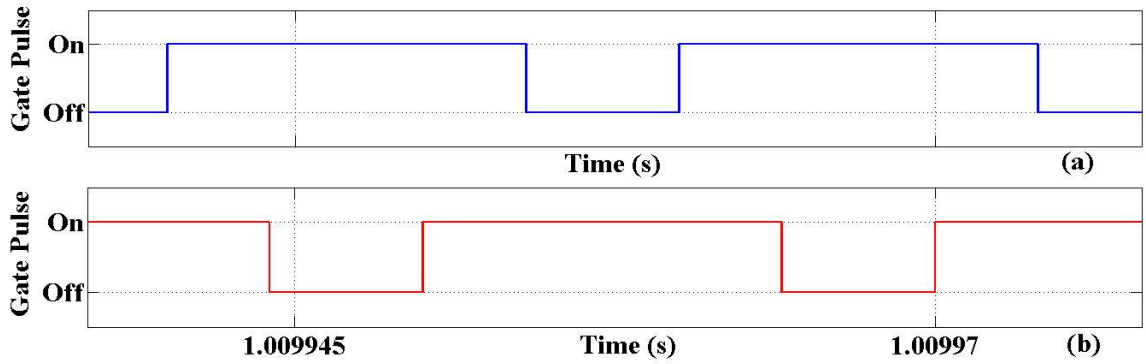


Figure 3.9: (*D*=0.7) (a) Gate pulse for switch S_a (b) Gate pulse for switch S_b

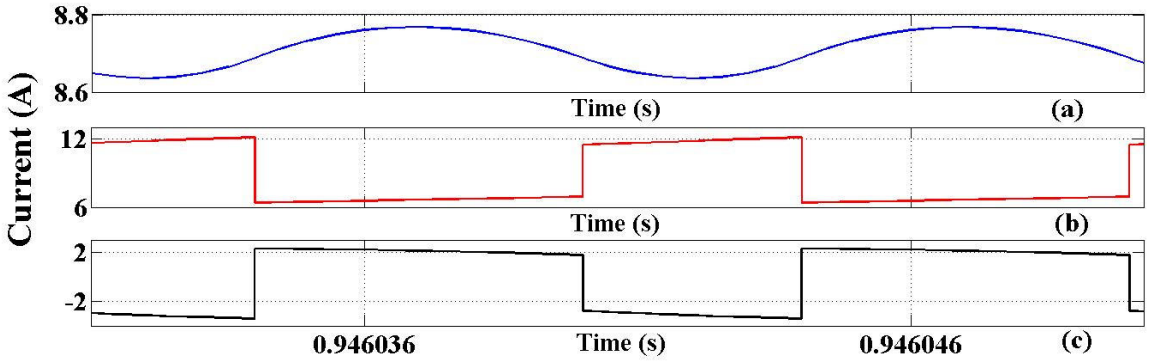


Figure 3.10: (*D*=0.7) (a) Source current (b) Converter input current (c) Current through the input capacitor

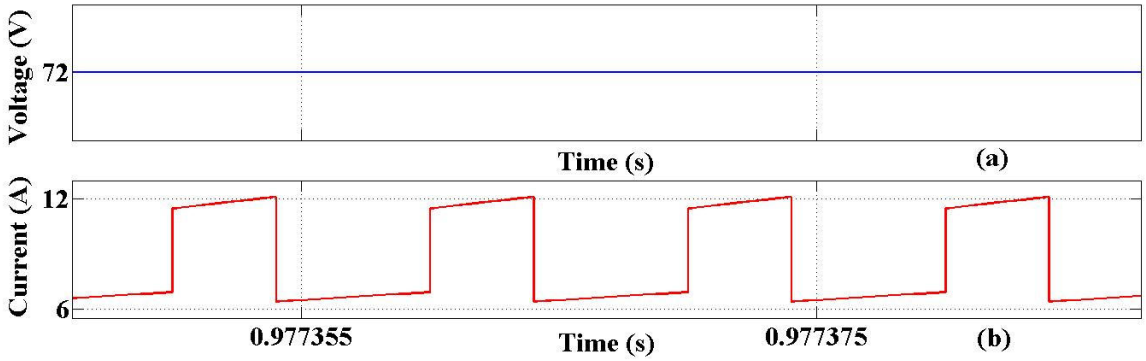


Figure 3.11: (D=0.7) (a) Input voltage (b) Converter input current

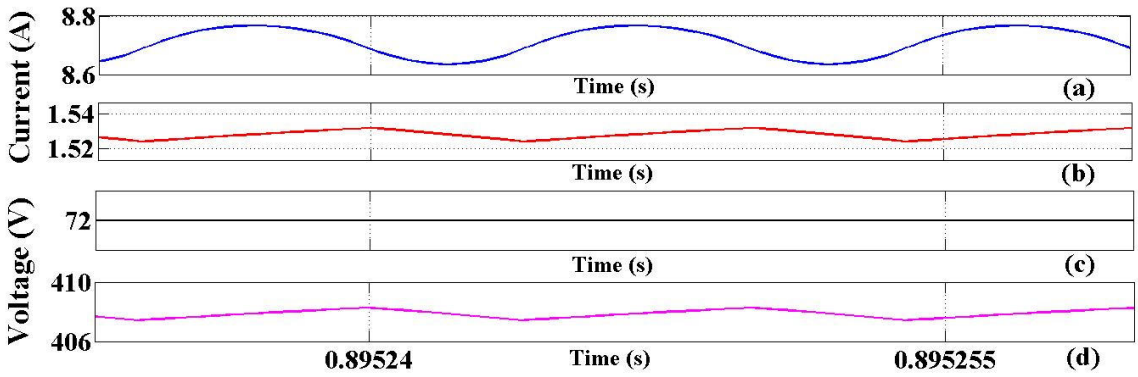


Figure 3.12: (D=0.7) (a) Source current (b) Load current (c) Input voltage (d) Total output voltage

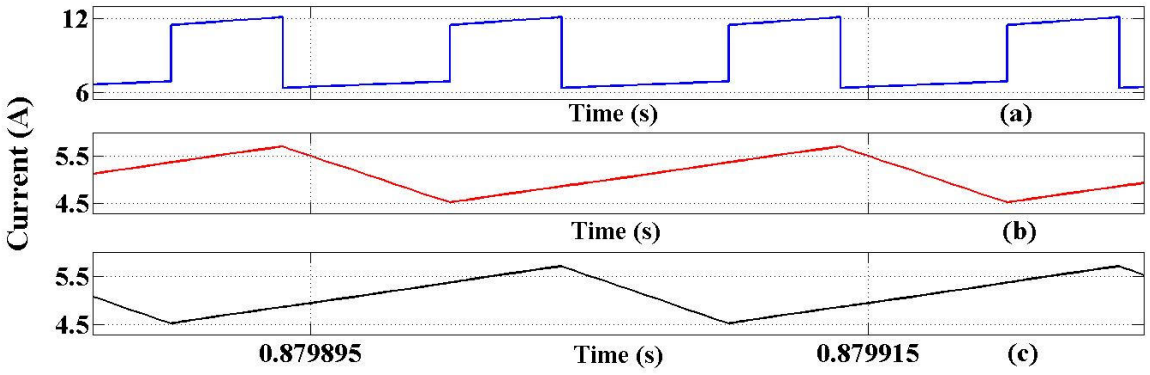


Figure 3.13: (D=0.7) (a) Converter input current (b) Inductor current for La (c) Inductor current for Lb

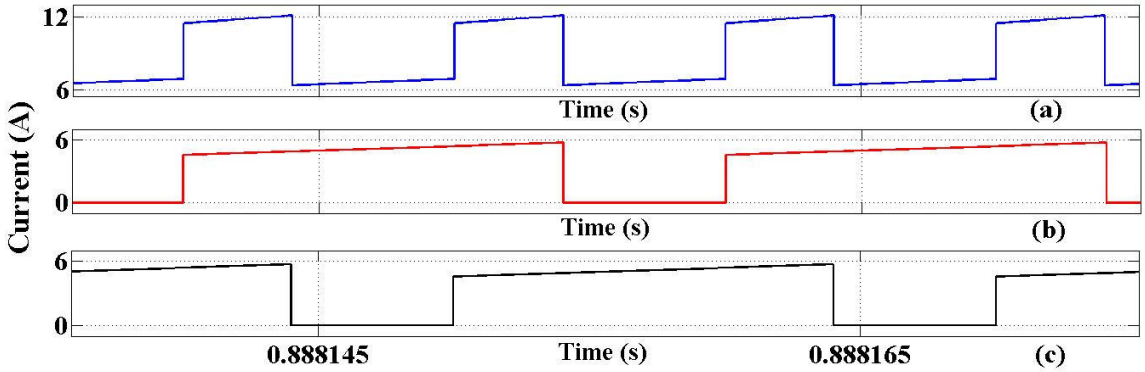


Figure 3.14: (D=0.7) (a) Converter input current (b) Switch current for S_a (c) Switch current for S_b

In the Fig. 3.9 (a) and (b) the gate pulses for the switches S_a and S_b are shown respectively. The Fig. 3.10 (a) represents the source current of the proposed converter. The current has diminished ripple content due to the presence of input capacitor (1000μF), as the input capacitor produces a filtering effect. Fig. 3.10 (b) shows the current into the converter i.e. after the input capacitor. Fig. 3.10 (c) shows the current passing through the input capacitor. The Fig. 3.11 (a) and (b) consists of the input voltage into the converter and the converter input current respectively. Fig. 3.12 (a), (b), (c) and (d) holds the source current, load current or the total output current of the converter, input voltage and the total output voltage of the converter respectively in one frame. The Fig. 3.13 (a) represents the converter input current. Fig. 3.13 (b) and (c) depicts the inductor current behavior for the inductors L_a and L_b respectively. From the behavior of the inductor current waveform it can be clearly seen that the proposed converter is operating in CCM. In Fig. 3.14 (a) the converter input current is clubbed along with the individual switch currents (for switches S_a and S_b) for the proposed converter in Fig. 3.14 (b) and (c) respectively.

The simulink waveforms are shown in the Fig. 3.15 to Fig. 3.20 for the proposed DC-DC converter at the specified duty cycle of 0.5.

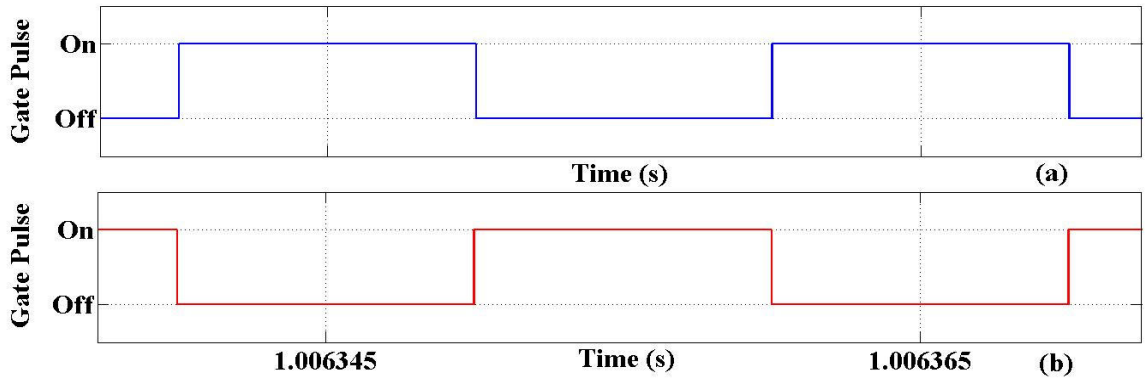


Figure 3.15: (D=0.5) (a) Gate pulse for switch Sa (b) Gate pulse for switch Sb

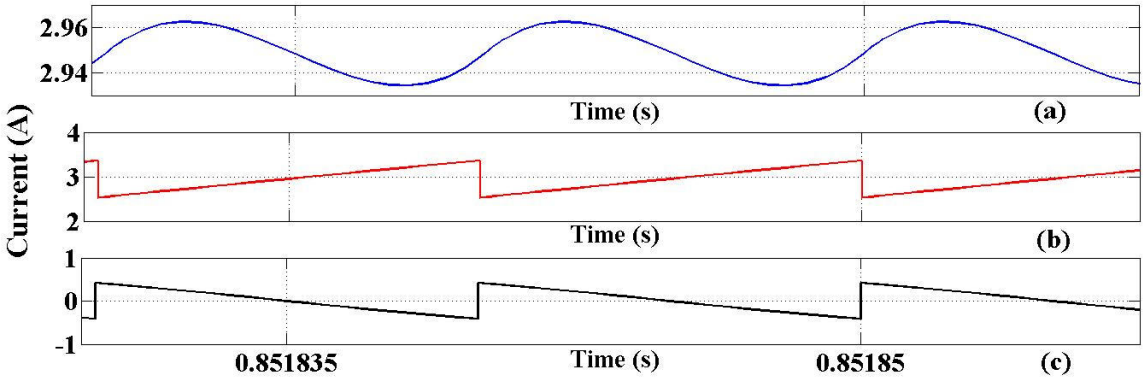


Figure 3.16: (D=0.5) (a) Source current (b) Converter input current (c) Current through the input capacitor

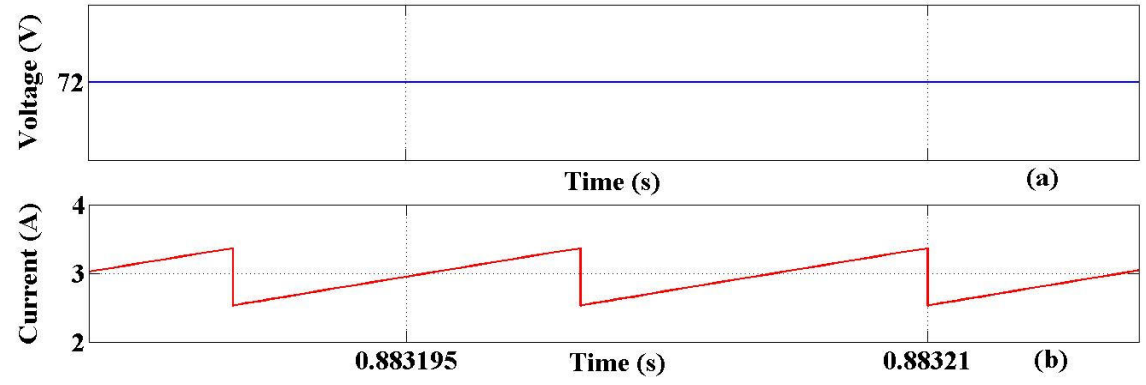


Figure 3.17: (D=0.5) (a) Input voltage (b) Converter input current

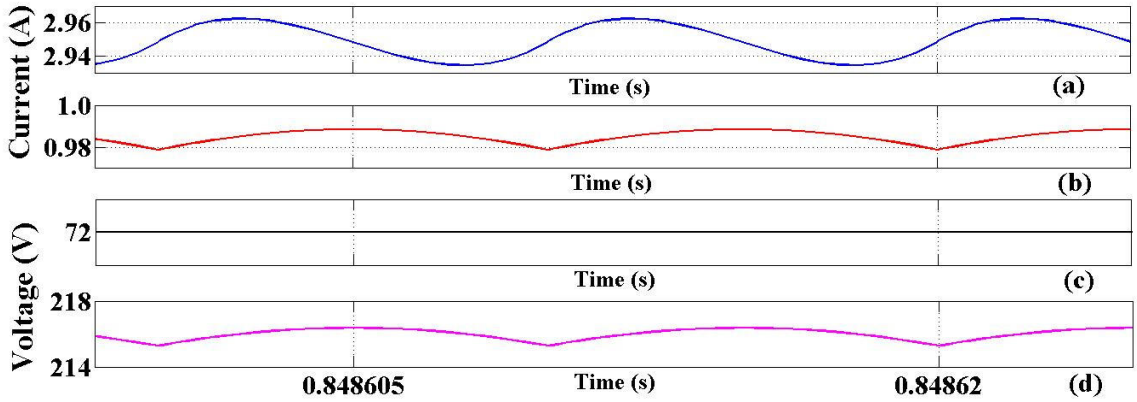


Figure 3.18: (D=0.5) (a) Source current (b) Load current (c) Input voltage (d) Total output voltage

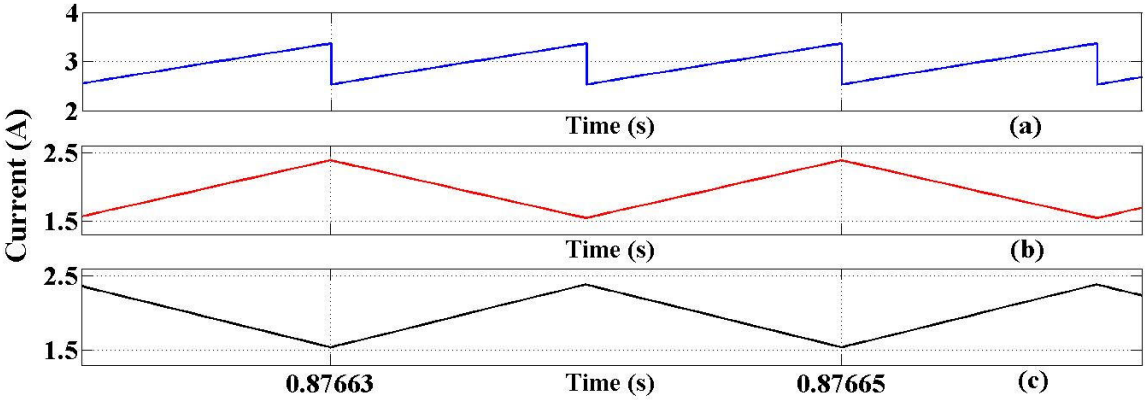


Figure 3.19: (D=0.5) (a) Converter input current (b) Inductor current for La (c) Inductor current for Lb

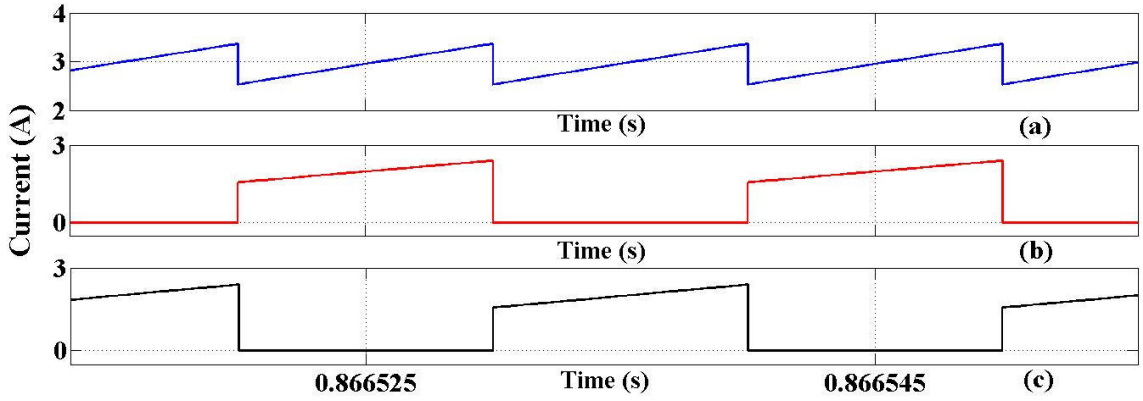


Figure 3.20: (D=0.5) (a) Converter input current (b) Switch current for Sa (c) Switch current for Sb

The Fig. 3.15 (a) and (b) shows the gate pulses at the switches of the converter. In Fig.

3.16 (a), (b) and (c) the source current, converter input current and the current through the capacitor is depicted respectively. Fig. 3.17 (a) consists of the input voltage and (b) represents the converter input current (after the input capacitor). Fig. 3.18 (a), (b), (c) and (d) comprises of the source current, output current/load current, input voltage and the total output voltage respectively. The point raised earlier in the section 2.2 that due to the interleaving of the two sub-converters voltage ripples and steady input voltage there is a considerable amount of reduction in ripple in the total output voltage can be clearly shown through the Fig. 3.18 (c) and (d). In Fig 3.19 (a), (b) and (c) the converter input current, the inductor (L_a) current and inductor (L_b) is shown respectively conducting in CCM. In Fig. 3.20 (a), (b) and (c) the converter input current, switch current (for switch S_a) and switch current (for switch S_b) is shown. From the figure the statement made earlier in section 2.2 can be further proved that at 50% duty cycle input current ripple is minimized due to the addition of each sub-converter input current and the load current (directly from input).

Similarly, the simulink waveforms are shown in the Fig. 3.21 to Fig 3.26 for the proposed converter at the specified duty cycle of 0.3.

The Fig. 3.21 (a) and (b) shows the gate pulses at the switches of the converter. In Fig. 3.22 (a), (b) and (c) the source current, converter input current and the current through the capacitor is depicted respectively. Fig. 3.23 (a) consists of the input voltage and (b) represents the converter input current (after the input capacitor). Fig. 3.24 (a), (b), (c) and (d) comprises of the source current, output current/load current, input voltage and the total output voltage respectively. In Fig 3.25 (a), (b) and (c) the converter input current, the inductor (L_a) current and inductor (L_b) is shown respectively conducting in Critical Conduction Mode i.e. the inductor current touches the zero point at one instant of the time interval and again rises, not staying at the zero interval. In Fig. 3.26 (a), (b) and (c) the converter input current, switch current (for switch S_a) and switch current (for switch S_b) is shown.

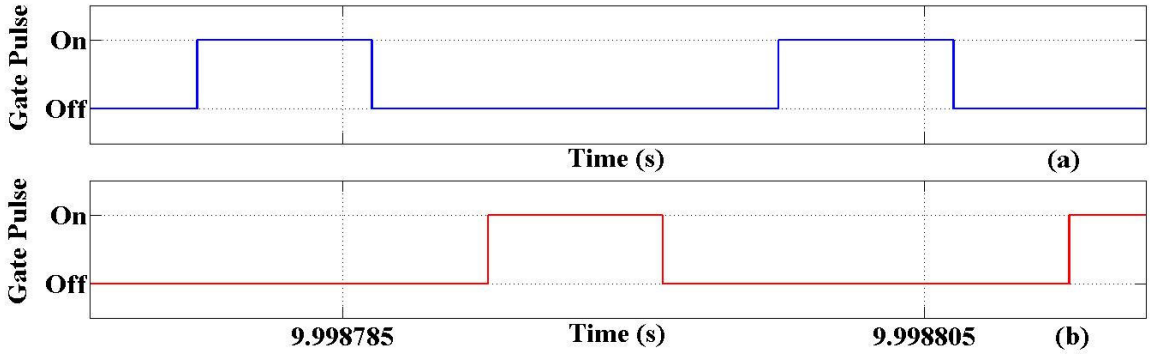


Figure 3.21: (D=0.3) (a) Gate pulse for switch Sa (b) Gate pulse for switch Sb

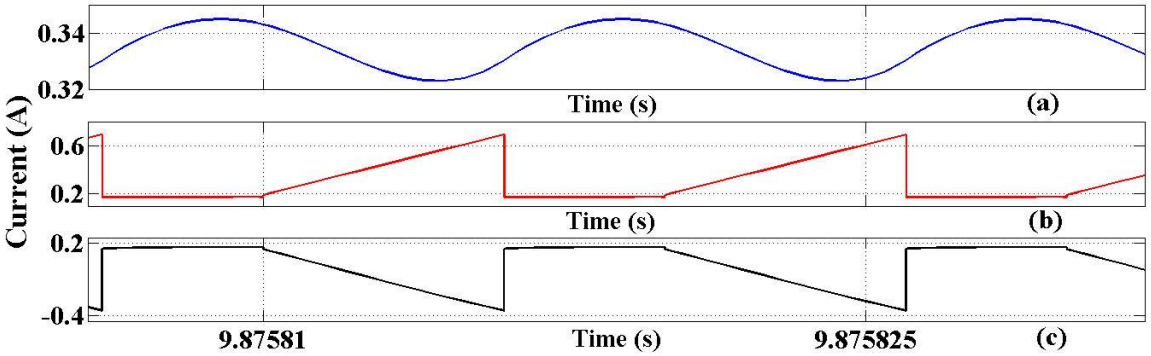


Figure 3.22: (D=0.3) (a) Source current (b) Converter input current (c) Current through the input capacitor

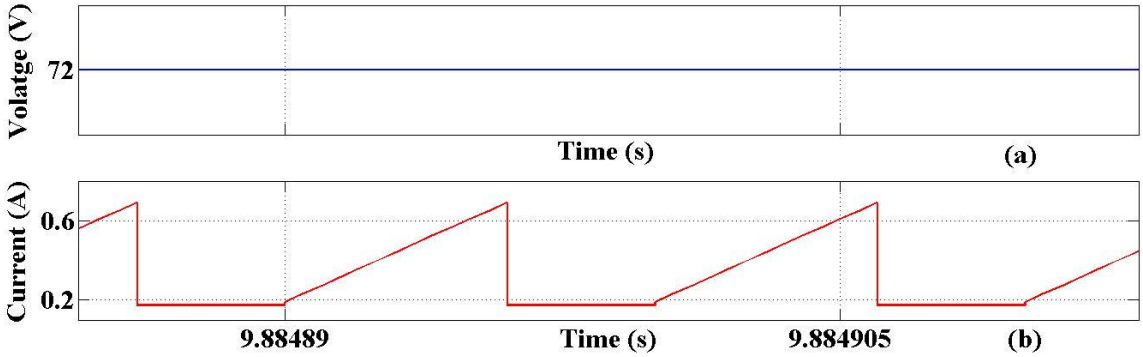


Figure 3.23: (D=0.3) (a) Input voltage (b) Converter input current

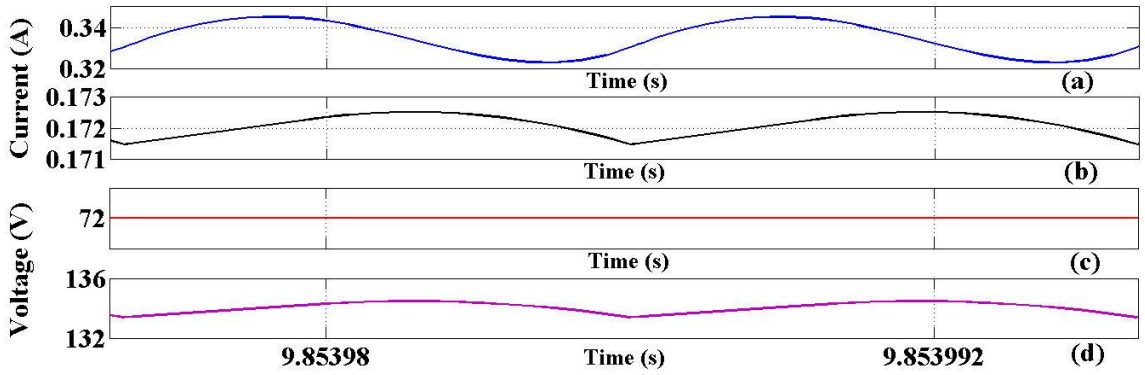


Figure 3.24: (*D*=0.3) (a) Source current (b) Load current (c) Input voltage (d) Total output voltage

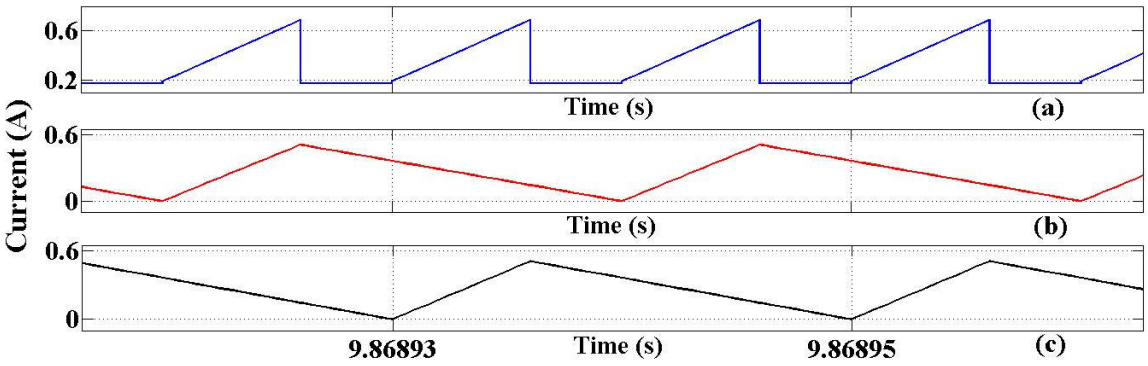


Figure 3.25: (*D*=0.3) (a) Converter input current (b) Inductor current for *La* (c) Inductor current for *Lb*

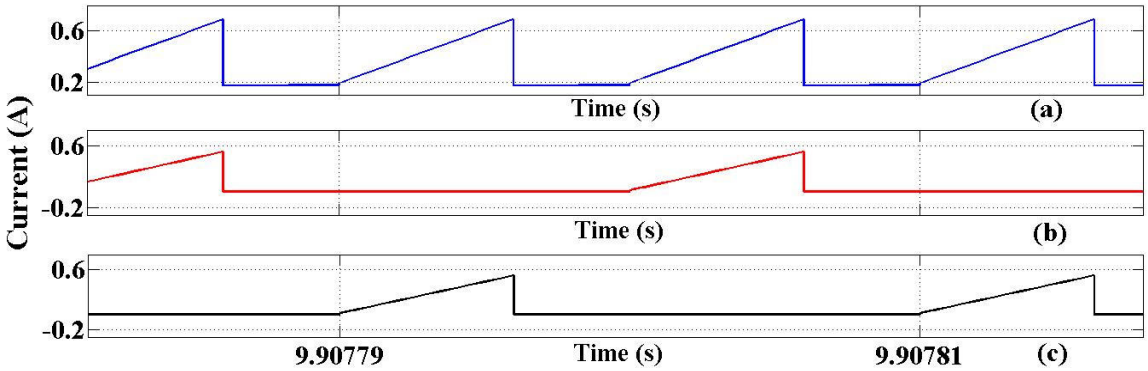


Figure 3.26: (*D*=0.3) (a) Converter input current (b) Switch current for *Sa* (c) Switch current for *Sb*

From the figures showing the converter input current at various duty cycle viz. *D*=0.7, 0.5 and 0.3, it can be vividly seen that it never reaches the zero value at any interval of time due to the steady current which is extracted by the load directly from the input.

3.7 Experimental Validation

A laboratory prototype is built for the proposed DC-DC converter. Two adjustable wire wound resistor of rating 160W, 500Ω, ±5%, were devised for the purpose of loading for the experimental validation of the proposed converter whose waveform is seen in the Fig. 3.27 to Fig. 3.44. The experimental results for the duty cycle D=0.7 is displayed in the Fig. 3.27 to Fig. 3.32. Similarly, the experimental results for D=0.5 and D=0.3 are depicted clearly in the Fig. 3.33 to Fig 3.38 and Fig. 3.39 to Fig. 3.44 respectively. The experimental figures clearly indicate that they very closely resemble their respective simulated figures in the section 3.6. This signifies the actual validation of the working principle and feasibility of the proposed DC-DC converter topology. It also authenticates the idea of higher voltage gain and higher output DC boost discussed in the earlier sections of the thesis.

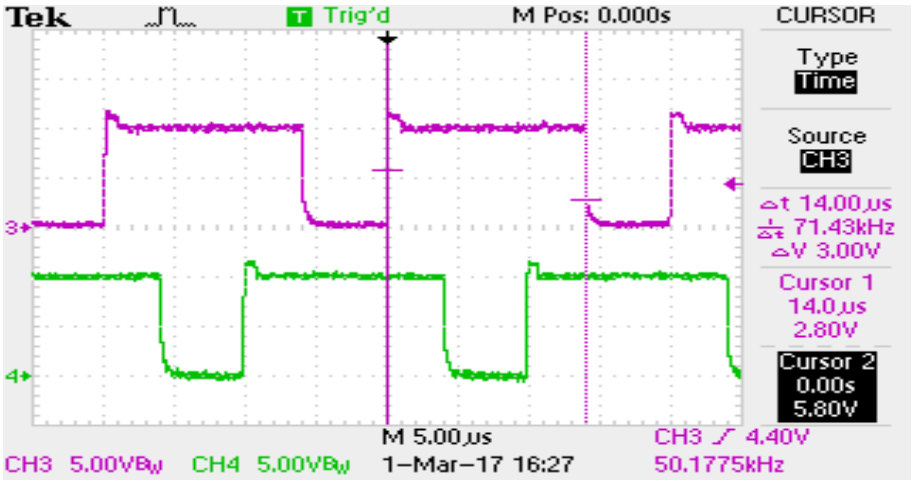


Figure 3.27: (D=0.7) Magenta (Top): Gate pulse for switch Sa Green (Bot): Gate pulse for switch Sb

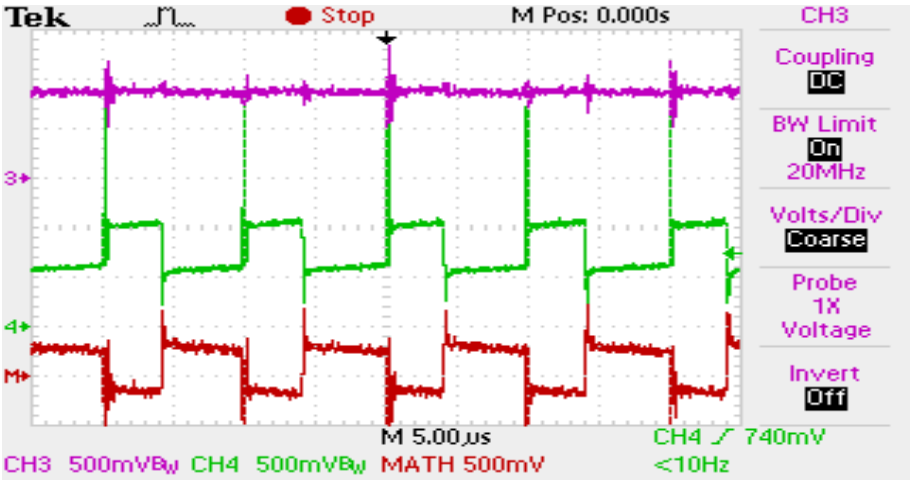


Figure 3.28: (D=0.7) Magenta (Top): Source current Green (Mid): Converter input current Red (Bot): Current through input capacitor

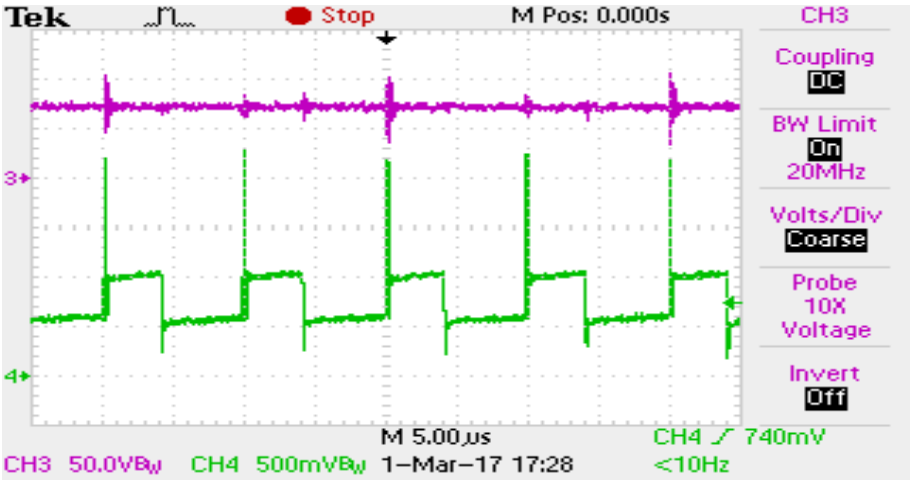


Figure 3.29: (D=0.7) Magenta (Top): Input voltage Green (Bot): Converter input current

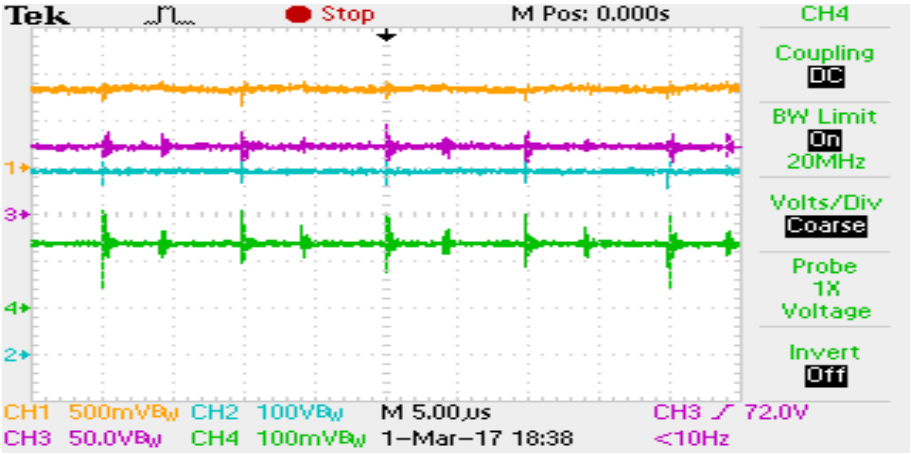


Figure 3.30: (D=0.7) Yellow (First): Source current Magenta (Second): Input voltage
Blue (Third): Total output voltage Green (Bot): Load current

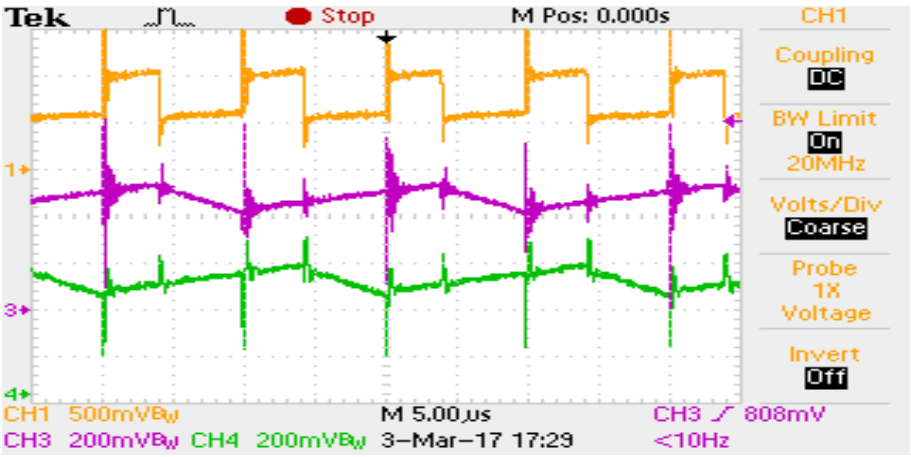


Figure 3.31 : (D=0.7) Yellow (Top): Converter input current Magenta (Mid): Inductor current for La
Green (Bot): Inductor current for Lb

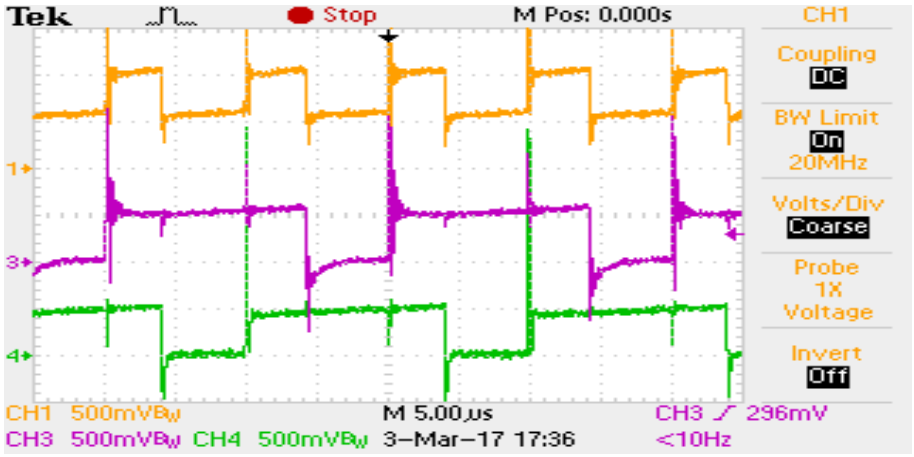


Figure 3.32 : (D=0.7) Yellow (Top): Converter input current Magenta (Mid): Switch current for Sa
Green (Bot): Switch current for Sb

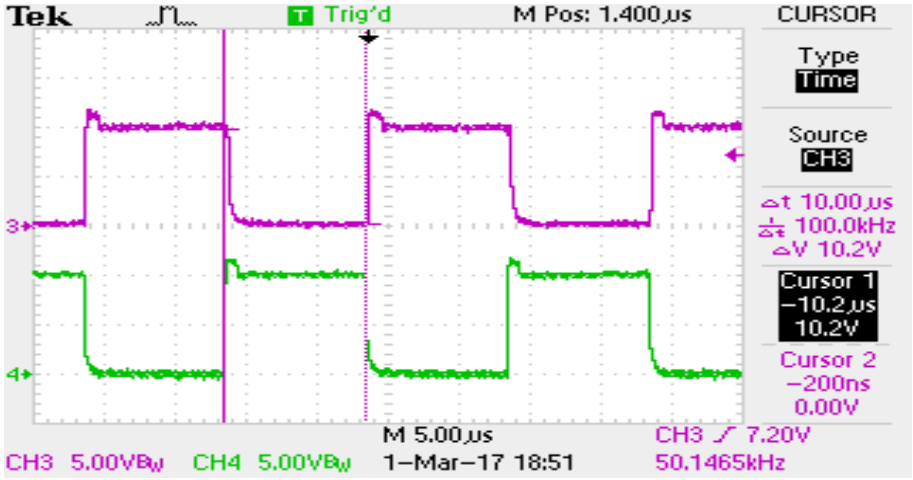


Figure 3.33: (D=0.5) Magenta (Top): Gate pulse for switch Sa Green (Bot): Gate pulse for switch Sb

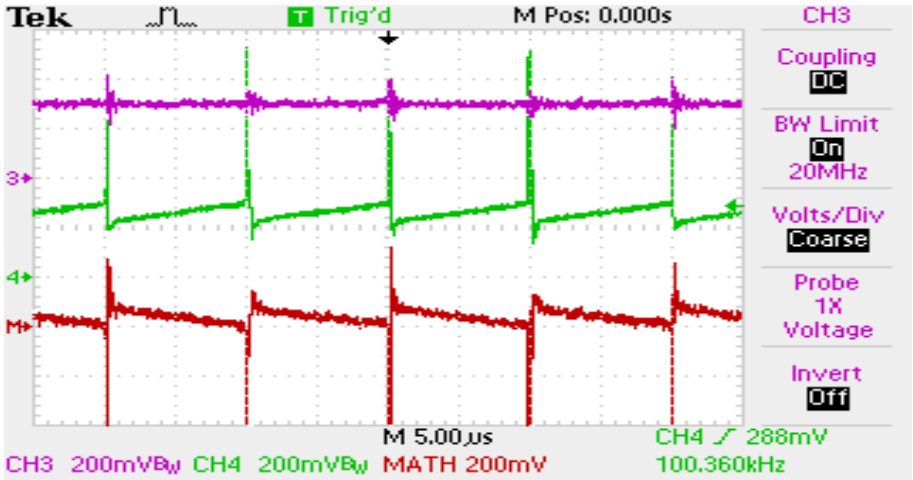


Figure 3.34: (D=0.5) Magenta (Top): Source current Green (Mid): Converter input current
Red (Bot): Current through input capacitor

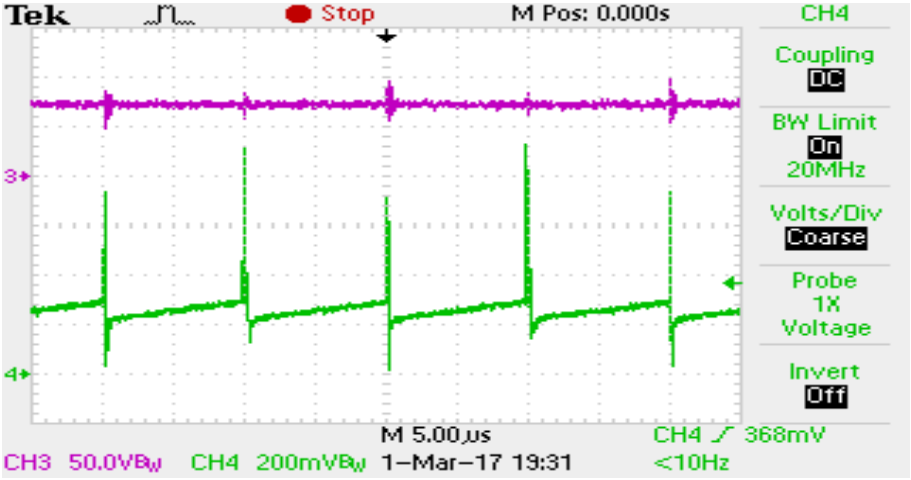


Figure 3.35: (D=0.5) Magenta (Top): Input voltage Green (Bot): Converter input current

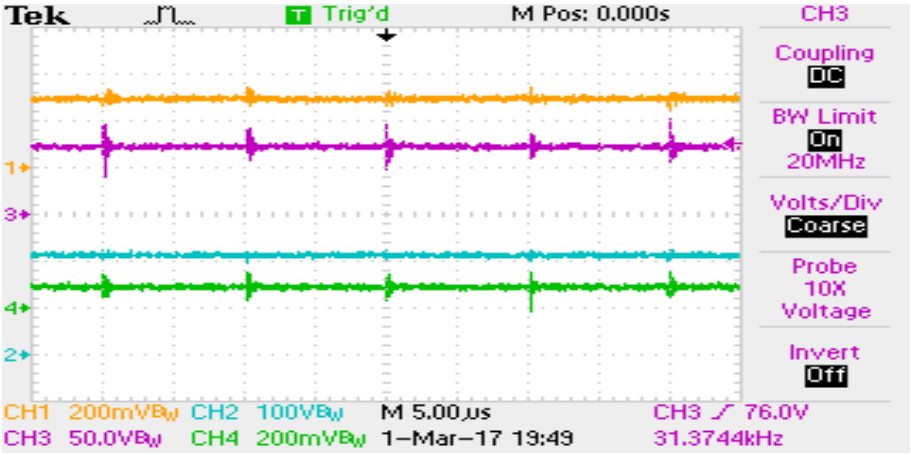


Figure 3.36: (D=0.5) Yellow (First): Source current Magenta (Second): Input voltage
Blue (Third): Total output voltage Green (Bot): Load current

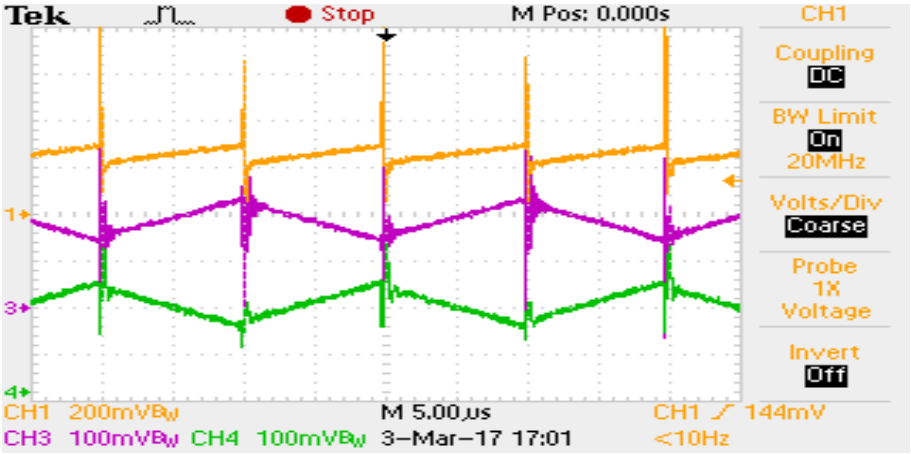


Figure 3.37: (D=0.5) Yellow (Top): Converter input current Magenta (Mid): Inductor current for La
Green (Bot): Inductor current for Lb

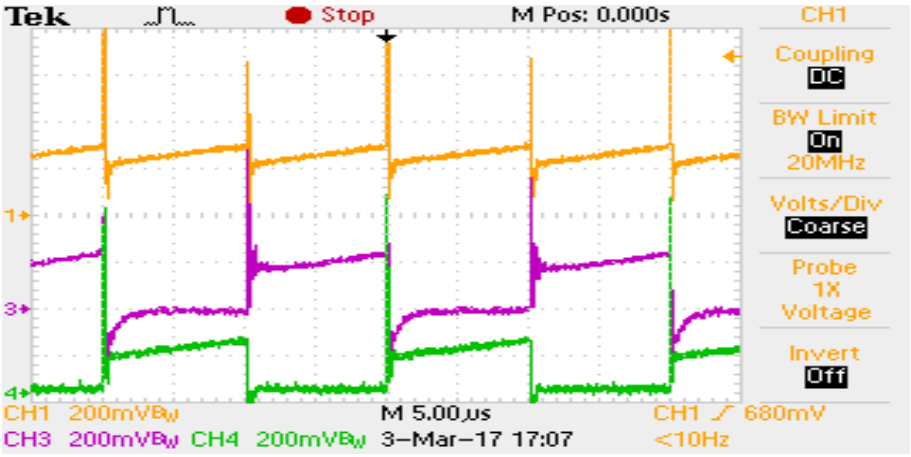


Figure 3.38: (D=0.5) Yellow (Top): Converter input current Magenta (Mid): Switch current for Sa
Green (Bot): Switch current for Sb

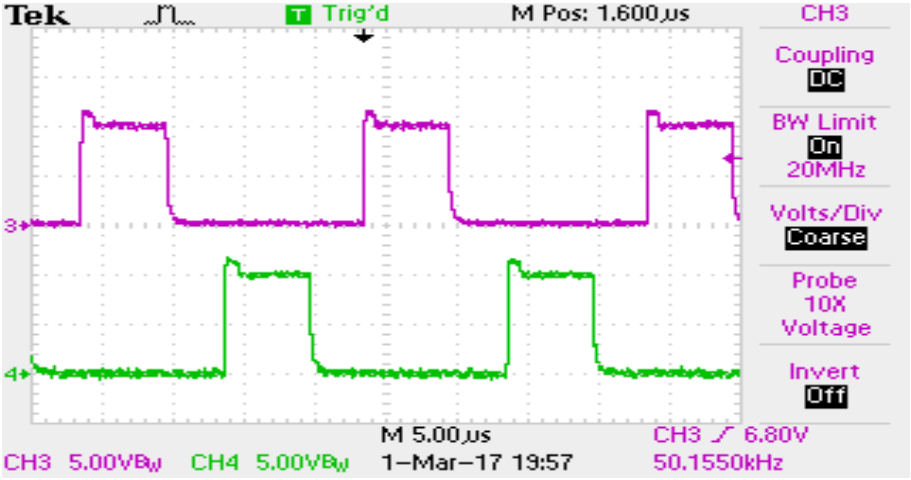


Figure 3.39: (D=0.3) Magenta (Top): Gate pulse for switch Sa Green (Bot): Gate pulse for switch Sb

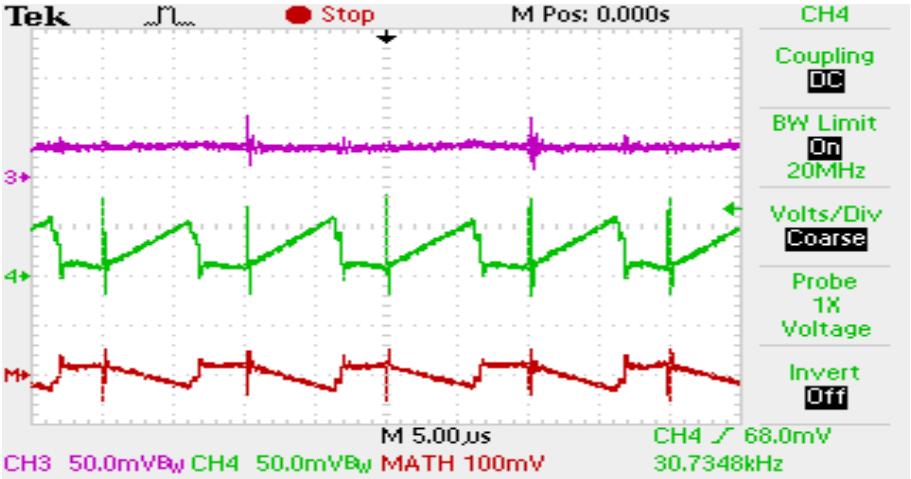


Figure 3.40: (D=0.3) Magenta (Top): Source current Green (Mid): Converter input current
Red (Bot): Current through input capacitor

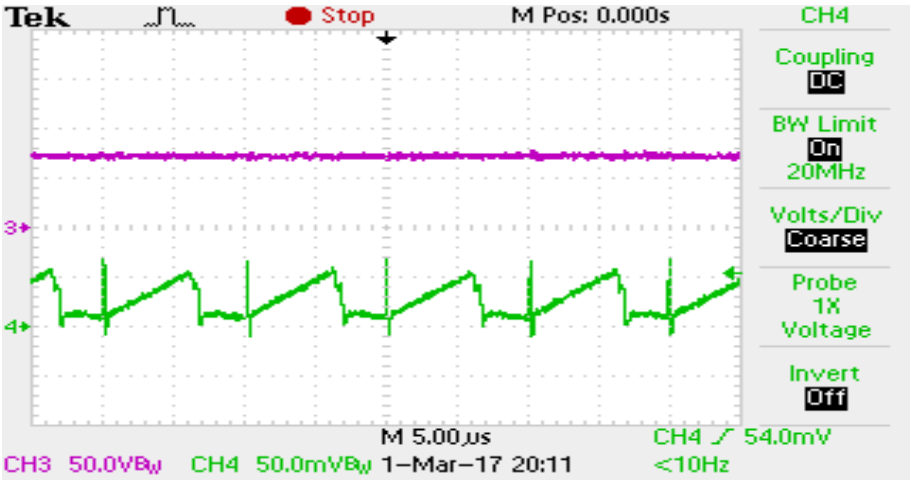


Figure 3.41: (D=0.3) Magenta (Top): Input voltage Green (Bot): Converter input current

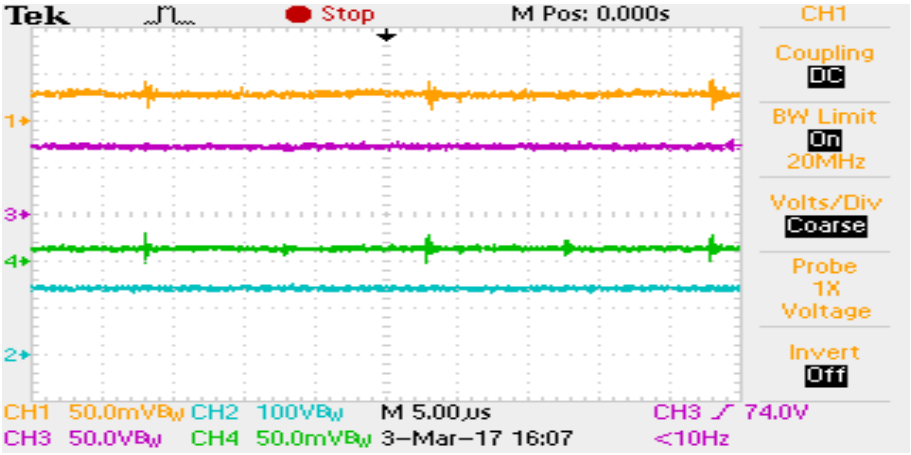


Figure 3.42: (D=0.3) Yellow (First): Source current Magenta (Second): Input voltage Green (Third): Load current Blue (Bot): Total output voltage

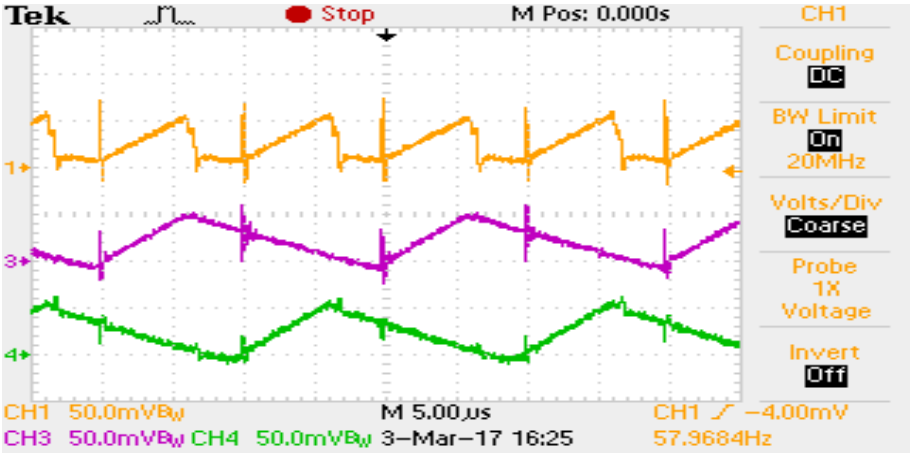


Figure 3.43: (D=0.3) Yellow (Top): Converter input current Magenta (Mid): Inductor current for La Green (Bot): Inductor current for Lb

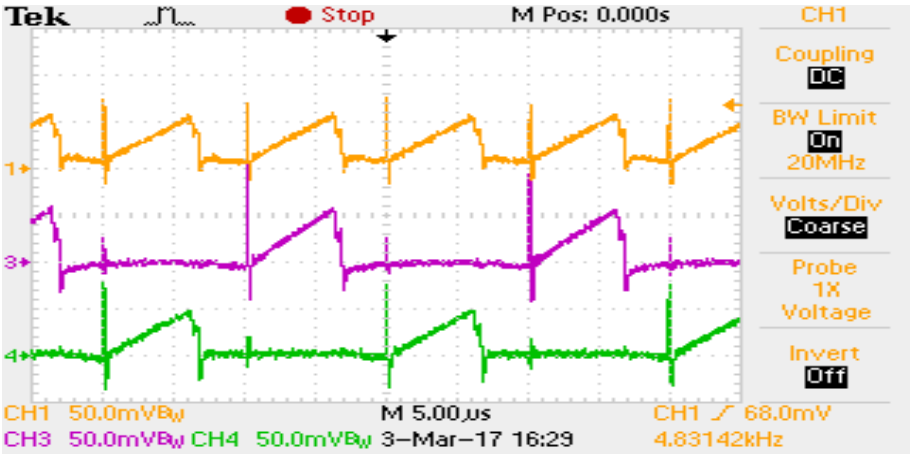


Figure 3.44: (D=0.3) Yellow (Top): Converter input current Magenta (Mid): Switch current for Sa Green (Bot): Switch current for Sb

For Fig. 3.27- Fig. 3.32: $R_o = 265\ \Omega$, Fig. 3.33- Fig. 3.38: $R_o = 220\ \Omega$ and Fig. 3.39 - Fig. 3.44: $R_o = 770\ \Omega$ (R_o ref. see Fig 2.1). The picture for the laboratory prototype comprising of both the power circuit as well as the control circuit is displayed in Appendix A.

3.8 Conclusion

In this chapter the state space averaging technique is applied to the converter operating states over the entire switching period. The derivation of the detailed transfer function is obtained for the entire converter from the small signal model. The power level inductor designing process is also shown. The inductor value is determined with the aid of parameters which are primarily assumed for the converter. The design process and the air gap calculation of the inductor used in the laboratory prototype is carried out and presented in detail. Selection of parameters regarding the semiconductor devices (switches and diodes) is put forward which is essential for building the experimental circuit. The Bode diagram for the converter is obtained in the simulink platform and presented. Pole-Zero mapping of the proposed DC-DC converter is also illustrated elaborately with the help of diagrams.

It is necessary to showcase the various waveforms at various duty cycles to check the actual practicality of the circuit proposed. Therefore, the waveforms obtained from simulation are closely compared with the experimental results obtained from hardware prototype to evaluate its efficacy. The results acquired from both the simulation platform and the laboratory prototype which closely mirrors each other at various operating condition, the proposed converter concept can be finally authenticated and confirmed for use as a high DC-DC boost converter topology. It can have wide applications in spheres of RES.

Chapter 4

Comparison with Other Boost Converters and Cascaded Representation of the Proposed Converter

4.1 Introduction

In this chapter the main focus is driven towards evaluating the performance of the proposed DC-DC converter with other boost DC-DC converter. The earlier chapters have proved the practicality of the concept of the proposed topology supported by experimental results. It is also required to confirm and establish the fact that the converter topology proposed has a better functioning capability and higher reliability leading to higher efficiency. The overall converter system needs to be compared with other classical DC-DC converters which aids in higher boost as well as converters of the recent research work assisting higher voltage gain leading to higher boost levels. The current and voltage parameters of various components of the converter topology are primarily compared with those of other high gain boost topologies.

4.2 Comparison with Classical Boost DC-DC Converter

As the main objective of the proposed converter is higher voltage boost, it is required to compare it with the classical boost DC-DC converter topologies at the initial level. This aids in pointing out the efficacy and reliability of the proposed converter. The CBC is extensively explained in the section 1.5.1 along with its working principle and its voltage gain equation in equation number (1.2). Another classical DC-DC converter that will be used for comparison purpose is the buck-boost converter. Therefore, a brief introduction to the topology is provided before advancing into the comparison sphere.

The buck-boost DC-DC converter is mainly applicable in regulated DC power supplies. The negative polarity output with respect to the common terminal involving the input voltage may be desired. The output obtained is either higher or lower than the input voltage. The working principle can be explained as, while the switch is operating at a certain time interval the diode becomes reverse biased and the input provides energy to the inductor. When the switch S_a is open then the stored energy in the inductor L is transferred to the

output stage via the diode *D*. Hence, no energy gets supplied from the input stage i.e. V_i at this interval. The inductor voltage v_L and the inductor current i_L waveform over a switching period is clearly shown and explained in the Fig. 2.4. The figure also helps in establishing the voltage gain equation of the buck-boost converter which is derived in the equation number (2.2). The schematic of the boost converter is clearly shown in the Fig. 1.4 and the diagram representing the buck-boost converter is shown in the Fig. 4.1 [17].

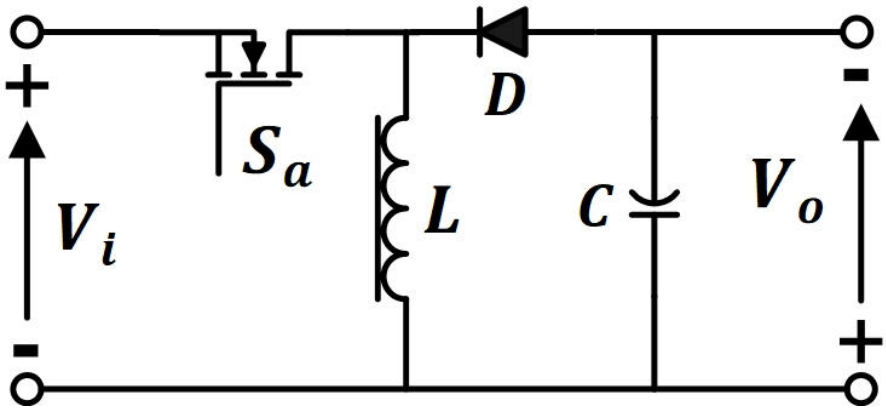


Figure 4.1: Schematic diagram of a Buck-Boost converter

The comparison carried out for the proposed DC-DC converter with classical DC-DC converters has component specifications given in tabular form. For the case of proposed converter the component specification represent for each sub-converter level. The input current ripple and the output voltage ripple when compared with other DC-DC classical converter is regarding the total converter.

In the comparison table the parameters considered are as follows:

The input voltage is $V_i = 100\text{V}$, the switching frequency is considered as $f_s = 50\text{kHz}$ and the output power is taken as $P_o = 1000\text{W}$.

The performance evaluation for all the DC-DC converters has been carried out on a simulation platform at three different specified output voltage conditions. The output capacitor values for all the converters are considered identical and the inductors are operating at critical conduction mode for all the converters so that the current ripple has the largest value. The size regarding the inductor solely depends on its Area Product which can be expressed as in the equation number (3.46). As the design consideration is same concerning the DC-DC converters the terms K_{wi} (the window utilization factor), B_{pk} (the

peak flux density in Wb/m^2) and J_c (Current density in A/cm^2) are assumed to be constant for all the converters in comparison. Therefore, the size of the inductor is represented as:

Size of the inductor $\propto LI_{pk}I_{rms}$ (4.1)

The table 4.1 to 4.6 will present the comparison of the proposed converter with that of the classical DC-DC converters (boost and buck-boost) under different working parameters specified.

Table 4.1 Table showing the comparison of proposed converter with boost and buck-boost converter for operating conditions with V_i=100V, V_o=566.7V, P_o=1000W

Component Specification	Classical Boost Converter	Classical Buck-Boost Converter	Proposed Converter (each sub-converter)
Duty Cycle	0.8235	0.85	0.7
Inductance (H)	82.35 μ H	72.25 μ H	119 μ H
Inductor Current (peak)	20A	23.53A	11.76A
Inductor Current (RMS)	11.61A	13.58A	6.818A
Inductor Size*	0.0190	0.02309	0.00951
Output Capacitor	1000 μ F	1000 μ F	1000 μ F
Capacitor Voltage	566.7V	566.7V	233.35V
Capacitor Current (RMS)	4.548A	4.948A	3.293A
Switch Current (peak)	20A	23.53A	11.8A
Switch Blocking Voltage	566.7V	666.67V	333.35V
Diode Blocking Voltage	566.7V	666.67V	333.35V
Diode Current (RMS)	4.878A	5.244A	3.734A

Component Specification	Classical Boost Converter	Classical Buck-Boost Converter	Proposed Converter (each sub-converter)
Diode Current (average)	1.762A	1.738A	1.76A

* As per equation number (4.1)

Table 4.2 Table showing total ripple value comparison for the specified operating condition specified in Table 4.1.

Component Specification	Classical Boost Converter	Classical Buck-Boost Converter	Proposed Converter
Input Current Ripple (pk-pk)	20A	23.53A	11.76A
Output Voltage Ripple (pk-pk)	0.028V	0.03V	0.016V

Table 4.3 Table showing the comparison of proposed converter with boost and buck-boost converter for operating conditions with V_i=100V, V_o=300V, P_o=1000W

Component Specification	Classical Boost Converter	Classical Buck-Boost Converter	Proposed Converter (each sub-converter)
Duty Cycle	0.667	0.75	0.5
Inductance	66.7 μH	56.24 μH	75.07 μH
Inductor Current (peak)	20A	26.67A	13.3A

Component Specification	Classical Boost Converter	Classical Buck-Boost Converter	Proposed Converter (each sub-converter)
Inductor Current (RMS)	11.55A	15.41A	7.683A
Inductor Size*	0.0154	0.02309	0.00768
Output Capacitor	1000 μ F	1000 μ F	1000 μ F
Capacitor Voltage	300V	300V	100V
Capacitor Current (RMS)	5.782A	6.951A	4.303A
Switch Current (peak)	20A	26.67A	13.3A
Switch Blocking Voltage	300V	400V	200V
Diode Blocking Voltage	300V	400V	200V
Diode Current (RMS)	6.68A	7.704A	5.431A
Diode Current (average)	3.32A	3.322A	3.314A

* As per equation number (4.1)

Table 4.4 Table showing total ripple value comparison for the specified operating condition specified in Table 4.3

Component Specification	Classical Boost Converter	Classical Buck-Boost Converter	Proposed Converter
Input Current Ripple (pk-pk)	20A	26.67A	13.3A
Output Voltage Ripple (pk-pk)	0.042V	0.05V	0.017V

Table 4.5 Table showing the comparison of proposed converter with boost and buck-boost converter for operating conditions with V_i=100V, V_o=185.7V, P_o=1000W

Component Specification	Classical Boost Converter	Classical Buck-Boost Converter	Proposed Converter (each sub-converter)
Duty Cycle	0.4615	0.65	0.3
Inductance	46.1 μ H	42.26 μ H	39 μ H
Inductor Current (peak)	20A	30.76A	15.4A
Inductor Current (RMS)	11.53A	17.73A	8.854A
Inductor Size*	0.0106	0.02309	0.00532
Output Capacitor	1000 μ F	1000 μ F	1000 μ F
Capacitor Voltage	185.7V	185.7V	42.85V
Capacitor Current (RMS)	6.544A	9.008A	5.126A
Switch Current (peak)	20A	30.76A	15.4A
Switch Blocking Voltage	185.7V	285.7V	142.85V
Diode Blocking Voltage	185.7V	285.7V	142.85V
Diode Current (RMS)	8.461A	10.47A	7.412A
Diode Current (average)	5.362A	5.349A	5.351A

* As per equation number (4.1)

Table 4.6 Table showing total ripple value comparison for the specified operating condition specified in Table 4.5

Component Specification	Classical Boost Converter	Classical Buck-Boost Converter	Proposed Converter
Input Current Ripple (pk-pk)	20A	30.76A	15.4A
Output Voltage Ripple (pk-pk)	0.056V	0.07V	0.0184V

From the above tables 4.1, 4.3 and 4.5 it is clearly observed that the ratings of the semiconductor components in all the given duty cycles of operation are considerably low for the proposed converter in comparison to the boost as well as the buck-boost converter.

To elaborate on the results obtained, firstly for the duty cycle value of the proposed converter it can be observed that for a much lesser value of duty cycle a higher voltage level can be obtained in comparison to the boost and buck-boost converters. This clearly indicates that the proposed converter is successful in achieving the required output voltage with a much lower duty cycle while the classical DC-DC converters reach their extreme duty cycle value in achieving higher voltage gain leading to reverse recovery problem of the boost diode, higher conduction losses to name a few. Secondly, it can be noticed that the inductor current peak value has a diminished value for the concerned DC-DC converter proposed for all the operating conditions. The particular phenomenon will ultimately lead to reduced peak to peak ripple content in the input current value. Whereas, it can be clearly noticed that the ripple content in the input current is on the higher side for the boost as well as the buck-boost DC-DC converter. Thirdly, it is seen that the output capacitor voltage concerning each individual sub-converter of the proposed system is lower when compared to other classical DC-DC boost converters. Therefore, it can be inferred that each sub-converter of the proposed DC-DC converter is handling only a fraction of the total output power. However, in case of boost and buck-boost converters the converters process the entire output power. As the sub-converters of the proposed system has to deal with lower level of power there is a direct impact on the voltage and current rating of the semiconductor devices which can be seen to have reduced value. Thereby, increasing the efficiency and reliability of the total

converter system parameters. To elaborate on this point the tables showing the value for switch current (peak), switch blocking voltage and diode blocking voltage for the proposed converter (each sub-converter) can be seen to be dealing with lower voltage and current levels. The individual converters of the proposed system is handling a lower level of voltage viz. semiconductor blocking voltage, whereas when it is seen with the case of boost and the buck-boost converter, they invariably has to block a much a higher level of voltage across their semiconductor devices.

The table 4.2, 4.4 and 4.6 shows a comparison for the ripple content in the input current and the total output voltage ripple for the proposed converter topology with that of boost and buck-boost converter. It can be clearly observed that the ripple value for both the total input current and the total output voltage concerning the proposed converter possess a very low value. This is the proof for the statement already made earlier in the section 2.2. It can be shown with the aid of the results that the there will be reduction in input current ripple due the addition of the input current of individual converter and the output current of the proposed DC-DC converter. Similarly, the minimization of the output voltage ripple is due to summation of the individual converter output voltage and the input voltage. There is reduction in ripple content due to interleaving phenomenon of the voltage ripples and the addition of the steady input voltage. From the results obtained it can be finally concluded that the proposed DC-DC converter has an enhanced performance level leading to higher efficacy level.

4.3 Comparison with Quasi-SEPIC and Interleaved Boost DC-DC Converter

In this section the comparison is put forward for the DC-DC converter proposed with Quasi-SEPIC converter [91] and Interleaved Boost DC-DC converter. The component specifications of semiconductor components as well as passive components are presented in tabular form. For the case of proposed converter and interleaved boost DC-DC converter the component specification are represented for each sub-converter level. The total input current ripple and the total output voltage ripple when compared is represented for the total converter.

The Quasi-SEPIC converter employs a coupled-inductor technique that enables it to achieve higher voltage gain. The power losses of the concerned DC-DC converter are on the lower side when used in low to medium power applications. The converter is primarily built

on the SEPIC DC-DC converter working principle. The voltage stress across the primary active switch is less. This leads to higher efficiency of the overall system. In [91] it is shown to have achieved a very high voltage gain. Therefore, it is utmost necessary to compare the concerned converter with the proposed converter to get a proper idea and prove the higher efficiency of the proposed device under similar operating conditions.

The interleaved boost DC-DC converter which is the next converter to be compared with the proposed converter is extensively explained and discussed in the section 1.5.5 along with its working principle, voltage gain derivation in equation number (1.16) and schematic diagram in Fig. 1.11. These two converters when compared with the proposed DC-DC converter can provide a clear perception regarding semiconductor and passive component voltage and current values as well the ripple content present at similar working condition. Therefore, the above discussed converters are chosen with high voltage gain properties to be compared with the proposed DC-DC converter system.

In the comparison table the parameters considered are as follows:

The input voltage is $V_i = 100\text{V}$, the switching frequency is considered as $f_s = 50\text{kHz}$ and the output power is taken as $P_o = 1000\text{W}$.

For the Quasi-SEPIC converter the turns ratio regarding the coupled-inductors is considered to be $n_{pr} : n_{se} = 1 : 0.5$, where n_{pr} is the number of primary turns and n_{se} is the number of secondary turns concerning the coupled-inductors.

The output capacitor values for all the converters are considered identical and the inductors are operating at critical conduction mode for all the converters as was considered in the comparison tables 4.1 to 4.6.

The Fig 4.2 shows the Quasi-SEPIC DC-DC converter.

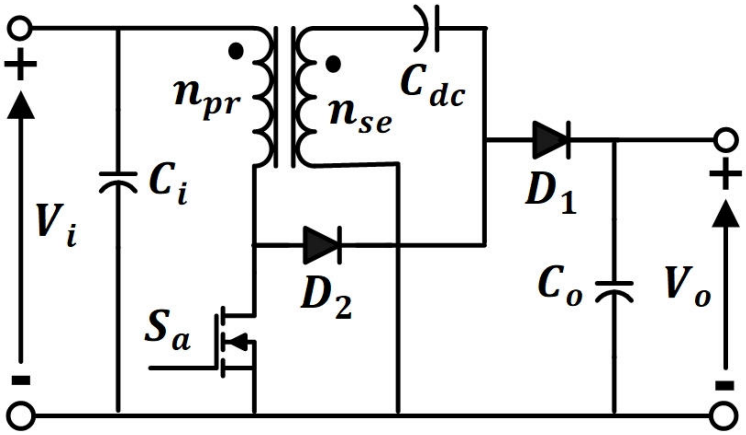


Figure 4.2: Schematic diagram of a Quasi-SEPIC converter

The voltage gain of the converter can be expressed as:

$$\frac{V_o}{V_i} = \frac{1+n}{1-D} \tag{4.2}$$

Where, V_i is the input voltage of the converter.

V_o is the total output voltage of the converter.

C_o is the output capacitor.

D_1 and D_2 represents the diodes.

and $n = \frac{n_{se}}{n_{pr}}$

The table 4.7 to 4.12 will present the comparison of the proposed converter with that of the Quasi-SEPIC converter and interleaved boost DC-DC converter under different working parameters specified for each table.

Table 4.7 Table showing the comparison of proposed converter with Quasi-SEPIC and Interleaved boost DC-DC converter for operating conditions with V_i=100V, V_O=566.7V, P_O=1000W

Component Specification	Interleaved Boost DC-DC Converter (each sub-converter)	Quasi-SEPIC Converter	Proposed Converter (each sub-converter)
Duty Cycle	0.7	0.735	0.7
Inductance (H)	119.04 µH	73.5 µH	119 µH
Inductor Current (peak)	11.76A	20A	11.76A
Inductor Current (RMS)	6.784A	11.6A	6.818A
Inductor Size*	0.009504	0.0169	0.00951
Output Capacitor	1000 µF	1000 µF	1000 µF

Component Specification	Interleaved Boost DC-DC Converter (each sub-converter)	Quasi-SEPIC Converter	Proposed Converter (each sub-converter)
Capacitor Voltage	333.3V	566.7V	233.35V
Capacitor Current (RMS)	3.277A	4.28A	3.293A
Switch Current (peak)	11.76A	20A	11.8A
Switch Blocking Voltage	333.3V	378V	333.35V
Diode Blocking Voltage	333.3V	D_1=186V D_2=559V	333.35V
Diode Current (RMS)	3.713A	D_1=4.8A D_2=4.18A	3.734A
Diode Current (average)	1.747A	D_1=4.83A D_2=2A	1.76A

* As per equation number (4.1)

Table 4.8 Table showing total ripple value comparison for the specified operating condition specified in Table 4.7

Component Specification	Interleaved Boost DC-DC Converter	Quasi-SEPIC Converter	Proposed Converter
Input Current Ripple (pk-pk)	11.76A	18A	11.76A
Output Voltage Ripple (pk-pk)	0.017V	0.03V	0.016V

Table 4.9 Table showing the comparison of proposed converter with Quasi-SEPIC and Interleaved boost DC-DC converter for operating conditions with V_i=100V, V_O=300V, P_O=1000W

Component Specification	Interleaved Boost DC-DC Converter (each sub-converter)	Quasi-SEPIC Converter	Proposed Converter (each sub-converter)
Duty Cycle	0.5	0.5	0.5
Inductance (H)	75.07 μH	50 μH	75.07 μH
Inductor Current (peak)	13.32A	20A	13.3A
Inductor Current (RMS)	7.664A	11.6A	7.683A
Inductor Size*	0.007689	0.0115	0.00768
Output Capacitor	1000 μF	1000 μF	1000 μF
Capacitor Voltage	200V	300V	100V
Capacitor Current (RMS)	4.294A	5.16A	4.303A
Switch Current (peak)	13.32A	20A	13.3A
Switch Blocking Voltage	200V	213V	200V
Diode Blocking Voltage	200V	D_1=100V D_2=304V	200V
Diode Current (RMS)	5.405A	D_1=6.61A D_2=6.06A	5.431A
Diode Current (average)	3.297A	D_1=6.6A D_2=3.22A	3.314A

* As per equation number (4.1)

Table 4.10 Table showing total ripple value comparison for the specified operating condition specified in Table 4.9

Component Specification	Interleaved Boost DC-DC Converter	Quasi-SEPIC Converter	Proposed Converter
Input Current Ripple (pk-pk)	13.32A	18A	13.3A
Output Voltage Ripple (pk-pk)	0.017V	0.06V	0.017V

Table 4.11 Table showing the comparison of proposed converter with Quasi-SEPIC and Interleaved boost DC-DC converter for operating conditions with V_i=100V, V_O=185.7V, P_O=1000W

Component Specification	Interleaved Boost DC-DC Converter (each sub-converter)	Quasi-SEPIC Converter	Proposed Converter (each sub-converter)
Duty Cycle	0.3	0.192	0.3
Inductance (H)	39 μ H	19.2 μ H	39 μ H
Inductor Current (peak)	15.4A	20A	15.4A
Inductor Current (RMS)	8.763A	11.6A	8.854A
Inductor Size*	0.005334	0.00443	0.00532
Output Capacitor	1000 μ F	1000 μ F	1000 μ F
Capacitor Voltage	142.85V	185.7V	42.85V
Capacitor Current (RMS)	5.149A	6.1A	5.126A

Component Specification	Interleaved Boost DC-DC Converter (each sub-converter)	Quasi-SEPIC Converter	Proposed Converter (each sub-converter)
Switch Current (peak)	15.4A	20A	15.4A
Switch Blocking Voltage	142.85V	133V	142.85V
Diode Blocking Voltage	142.85V	D_1=57.5V D_2=176V	142.85V
Diode Current (RMS)	7.286A	D_1=8.1A D_2=7.11A	7.412A
Diode Current (average)	5.335A	D_1=11.5A D_2=5.29A	5.351A

* As per equation number (4.1)

Table 4.12 Table showing total ripple value comparison for the specified operating condition specified in Table 4.11

Component Specification	Interleaved Boost DC-DC Converter	Quasi-SEPIC Converter	Proposed Converter
Input Current Ripple (pk-pk)	15.4A	19A	15.4A
Output Voltage Ripple (pk-pk)	0.018V	0.09V	0.0184V

From the tables 4.7 to 4.12 it can be seen that when compared with the Quasi-SEPIC converter the proposed converter has a much lesser inductor current peak and switch current peak value. This will lead to diminished value of peak to peak ripple content in the total input current. The switch blocking voltage and the diode blocking voltage for the proposed

converter is much lesser when compared with Quasi-SEPIC converter. This reduces the voltage stress on the semiconductor components in the proposed converter topology thereby reducing the semiconductor component rating as well. The Quasi-SEPIC converter topology employs a coupled-inductor to augment the voltage level. However, this practice will eventually lead to presence of considerable amount leakage inductance. This is due to the fact in practical scenario for coupled-inductors there will be non-ideal coupling present in both the inductors. This phenomenon will lead to the presence of high voltage spikes, ringing phenomenon in the parasitic components (resistor, inductor and capacitor) and losses which will reduce the efficiency and performance factor of the total converter. Snubber circuits (RCD) and clamping (diode capacitor) circuits can alleviate the issue but cannot totally eradicate the drawbacks of a practical topology employing a coupled-inductor.

For the interleaved boost DC-DC converter the component specification values are similar to that of the proposed converter. The value of the ripple content in the total input current and total output voltage for the interleaved boost DC-DC converter are similar to that of the proposed converter. However, as discussed in the section 1.5.4 for the interleaved boost DC-DC converter structures which comprises of interleaved boost modules, the total output voltage comprises of the addition of output voltages of the two individual sub-converters but with the total input voltage being subtracted (see equation no. 1.12 & 1.14). Whereas for the proposed DC-DC converter the total output voltage is the summation of each individual sub-converter with that of the input DC voltage (see equation no. 2.1). From the tables 4.7, 4.9 and 4.11 it can be vividly noticed that the output capacitor voltage value concerning each sub-converter module is way higher for the interleaved boost converter structure when compared with the proposed topology. The value reveals the fact that as the output voltage for each sub-converter level (interleaved boost converter) is on the higher side then each sub-converter also has to process more amount of power than what is actually required by the load, whereas in the proposed DC-DC converter each sub-converter has to process only a fraction of the power which leads to lower rating of the semiconductor devices. Therefore, it can be concluded that the proposed topology has an overall higher efficiency and reliability when compared with other recent boost topologies.

4.4 Efficiency Plot

It is necessary to present the graphical analysis regarding the efficiency estimation for the classical boost DC-DC converter topology and higher gain boost topologies with that of the

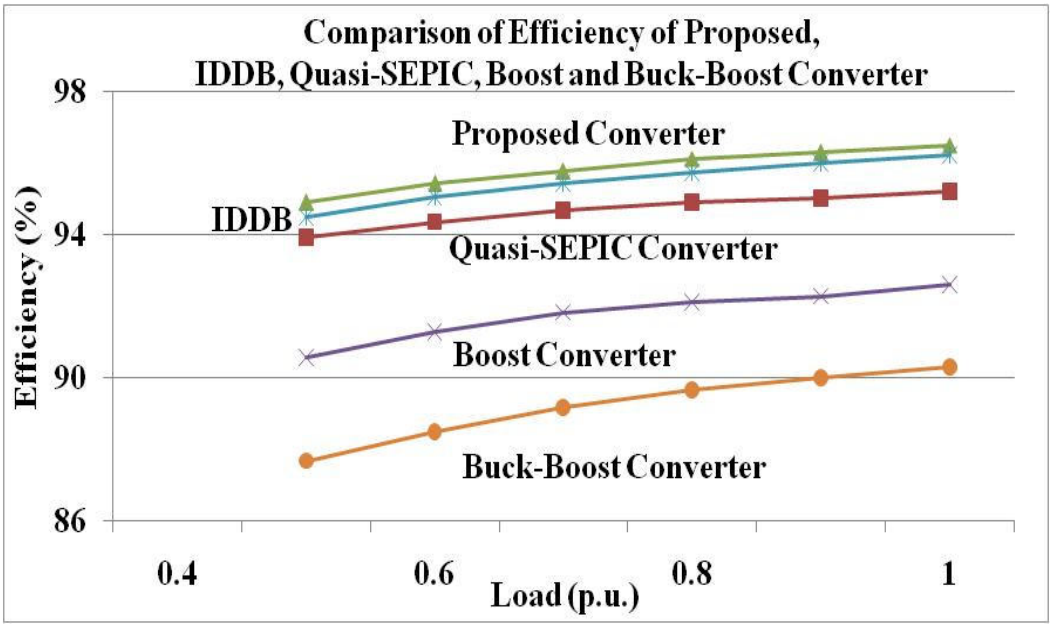


Figure 4.3: Efficiency plot of the proposed converter along with boost, buck-boost, quasi-SEPIC and interleaved boost DC-DC converter

DC-DC converter topology proposed.

The graphical analysis for efficiency estimation is vividly presented in the Fig. 4.3. Here the total power loss calculation concerning the active switches and diodes (semiconductor devices) is obtained from the simulation study which is performed with the aid of PSIM platform. The load interval selected for the simulation study for all the converter topologies is for the interval of 50% to 100%. It can be inferred and proved from the graphical analysis that the total power losses in all the semiconductor devices concerning the proposed converter are much less when compared to conventional DC-DC boost converter topologies such as boost and buck-boost converters. It is further shown in the graphical analysis that the efficiency for the proposed topology is higher when compared with recent high step-up boost converter topologies viz. quasi-SEPIC DC-DC converter and interleaved boost topology, while functioning under similar working parameters and condition. This is expected, as a part of the total output power is coming directly from the input, rather than the total power being converted as in other converters with which it is compared. From the plot it can be proved that the total power losses in all the semiconductor devices for the proposed converter are much less when compared to all similar high step-up converter topologies working under same parameters,

4.5 Cascaded Multi-Stage Extension

Here a detailed study will be conducted on how the proposed converter can be effectively designed in an internally cascaded multi-stage extension. The particular design of the proposed converter can accomplish a much higher voltage gain for two-stage configuration. The Fig. 4.4 portrays the schematic of the internally cascaded structure for two stages concerning the converter that is proposed.

The Fig. 2.1 shows the proposed DC-DC converter topology, here there is integration of the proposed topology with that of the internally cascaded structure. It consists of two interleaved buck-boost DC-DC converters. Which embodies two more switches i.e. S_c and S_d operating at 180^o phase shift along with their associated inductor, diode and capacitor. The cascaded structure which integrates with the positive bus contains switch S_c, inductor L_c, capacitor C_c and diode D_c. It will create a voltage V_c at the output which will get added to the input voltage V_i. Similarly, the cascaded structure which integrates with the negative bus comprises of switch S_d, inductor L_d, capacitor C_d and diode D_d. This will give rise to the negative bus voltage V_d which will also be summed up with the input voltage V_i. In the cascaded design the individual buck-boost sub-converter (second stage in Fig. 4.4) will derive its input value from the total output value of the earlier buck-boost sub-converter stage (first stage in Fig. 4.4). Thus, a fraction of the total output power of each sub-converter will directly derived from the input DC bus directly. The remaining value will be extracted from the previous stage sub-converter i.e. the first stage of the individual sub-converter shown in the Fig. 4.4.

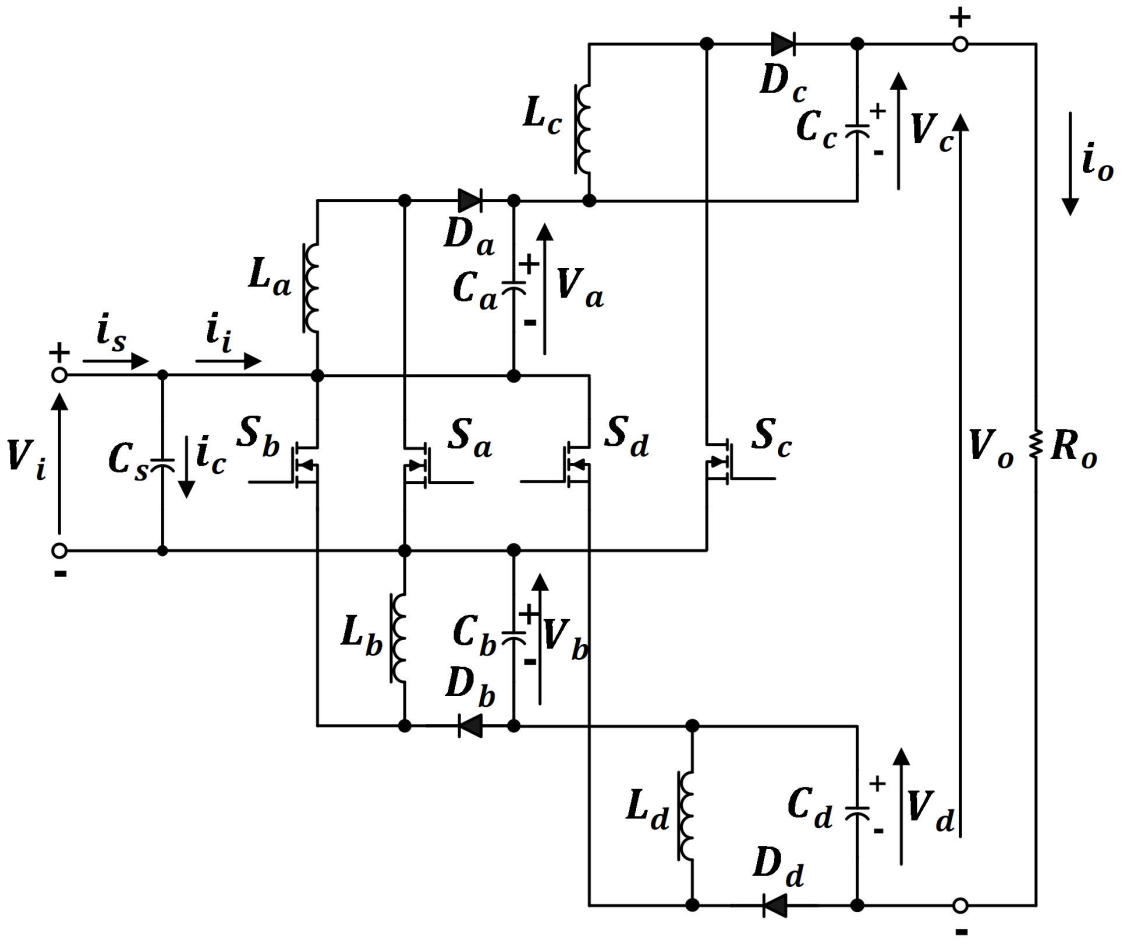


Figure 4.4: Schematic diagram of internally cascaded multi-stage extension of proposed boost converter with two-stages

4.5.1 Voltage Gain Equation of the Internally Cascaded Converter

In the general case, suppose '*n*' number of individual interleaved stages is used (2*n* sub-converters) then the voltage output of individual buck-boost sub-converters of the n^{th} stage can be expressed as:

$$\text{Let } \frac{D}{1-D} = z \tag{4.3}$$

$$\text{Therefore, } 1+z = 1+\frac{D}{1-D} = \frac{1}{1-D} \tag{4.4}$$

The Fig. 4.5 shows the n^{th} stage representation of the internally cascaded multi-stage extension of the proposed converter. Here the positive bus side extension is only presented

for simplicity and it will be easier to understand as well.

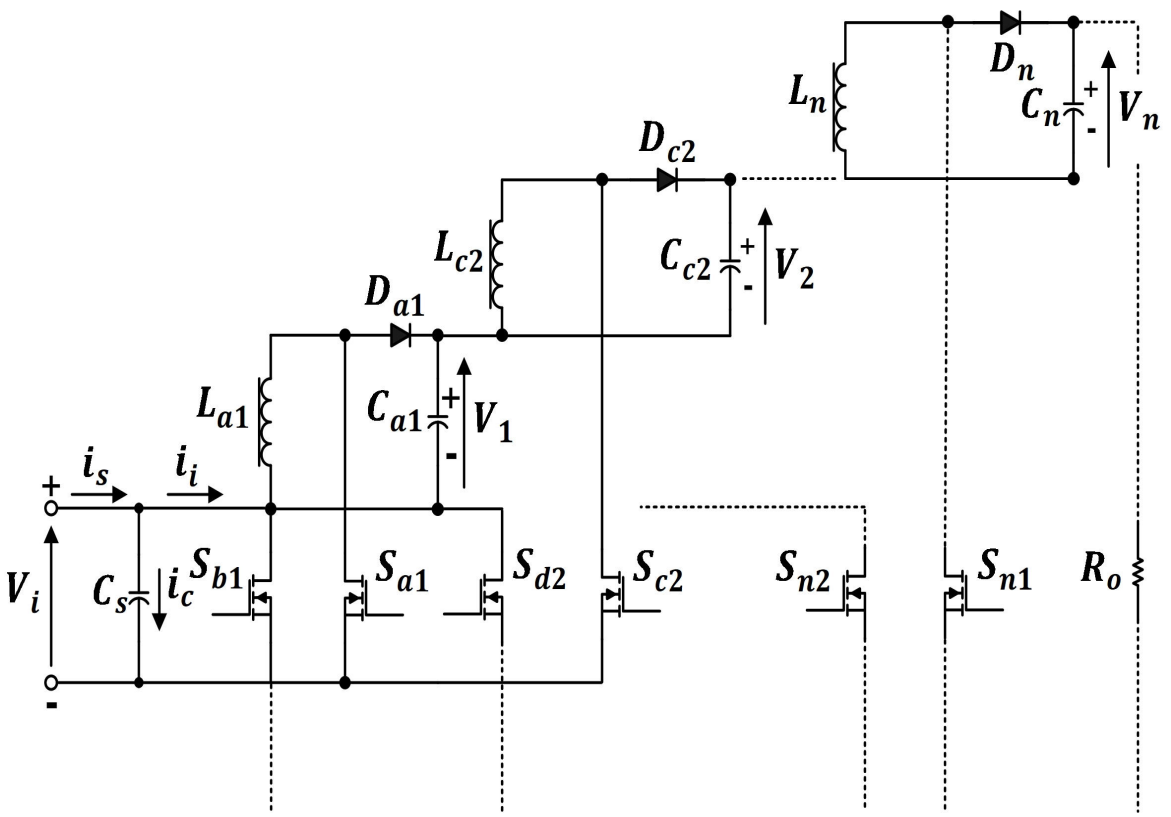


Figure 4.5: Schematic diagram of internally cascaded multi-stage extension of proposed boost converter for n^{th} stages

From the Fig. 4.5 the output voltages of each sub-converter up to n^{th} stage can be expressed as:

$$V_1 = V_i z \tag{4.5}$$

$$\begin{aligned} V_2 &= (V_i + V_1)z = V_i z + V_1 z \\ &= V_1 + V_1 z = V_1(1+z) \end{aligned} \tag{4.6}$$

$$\begin{aligned} V_3 &= (V_i + V_1 + V_2)z = V_i z + V_1 z + V_2 z \\ &= V_1 + V_1 z + V_2 z = V_2 + V_2 z = V_2(1+z) = V_1(1+z)^2 \end{aligned} \tag{4.7}$$

Similarly, $V_4 = V_1(1+z)^3$ (4.8)

Hence for output voltage after the n^{th} stage is:

$$V_n = V_1(1+z)^{n-1}$$

Therefore, $\sum_{n=1}^{n} V_n = V_1[1+(1+z)+(1+z)^2+....+(1+z)^{n-1}]$ (4.9)

$$\sum_{n=1}^{n} V_n = V_1 \frac{(1+z)^n - 1}{(1+z)-1} = \frac{V_i z[(1+z)^n - 1]}{z} \quad (4.10)$$

Substituting the value of z from equation number (4.3) in (4.10), it can be expressed as:

$$V_n = \left[V_i + \sum_{x=1}^{(n-1)} V_x \right] \left[\frac{D}{1-D} \right] \quad (4.11)$$

Where, V_x is the output voltage of each individual sub-converter (buck-boost) and expressed as:

$$V_x = V_a = V_b = \frac{V_i D}{(1 - D)} \quad (4.12)$$

The total output voltage of the n^{th} stage can be given by:

$$V_o = V_i + 2\sum_{1}^{n} V_n = V_i[1 + 2\{(1+z)^n - 1\}] \quad (4.13)$$

From the equation number (4.11) and (4.13), after simplification, the overall gain of the internally cascaded multi-stage converter can be expressed as:

$$\frac{V_o}{V_i} = \left[1 + 2\left\{ \frac{1}{(1-D)^n} - 1 \right\} \right] \quad (4.14)$$

or, $$\frac{V_o}{V_i} = \left[\frac{2}{(1-D)^n} \right] - 1 \quad (4.15)$$

The equation number (4.15) presents the n^{th} stage overall voltage gain of internally cascaded multi-stage extension of the proposed converter.

If a case is considered for a two stage converter i.e. n=2, and a comparison is done for a single stage converter. It can be noticed that at a specified duty cycle for example D=0.5 with a single-stage converter a voltage gain of three can be achieved. However, in the case of a two-stage converter system with the aid of the same duty ratio a much higher voltage gain is obtained i.e. voltage gain of seven. The single stage converter system can achieve the particular voltage gain with a duty ratio of D=0.75.

In the internally cascaded multi-stage extension it is not mandatory that all the multiple stages should possess the similar duty ratio. If the case of the two-stage converter is taken into consideration for voltage gain higher than three, the first-stage can be operated at a duty

cycle D=0.5 such that the current ripple is at the minimum level. The succeeding stages can now be operated at the required value of duty ratio so as to achieve the desired voltage gain value in order to reach the preferred output voltage value.

4.6 Simulation Results for Two-stage Cascaded Configuration

The actual feasibility of the statement made in the section 4.5.1 needs to be proved with the help of results. Therefore, the concept regarding the internally cascaded multi-stage converter is simulated on MATLAB/Simulink platform.

For obtaining the results parameters considered are as follows:

The input voltage is $V_i = 100\text{V}$, the switching frequency is considered as $f_s = 50\text{kHz}$ and the output power is taken as $P_o = 1000\text{W}$. The performance evaluation of the internally cascaded multi-stage DC-DC converter has been carried out on a simulation platform at three different duty ratios i.e. at D=0.7, 0.5 and 0.3. The output capacitor values for all the stages of the converter are considered identical i.e. 1000 μF and the inductors are operating at critical conduction mode for all the stages of the converter so that the current ripple has the largest value.

As the prime objective attained from the internally cascaded multi-stage converter is obtaining higher voltage gain from the same duty ratio with reference to the initial single-stage converter topology. Therefore, the figures (Fig. 4.6 to 4.11) depict the total input voltage supplied to the converter, the sub-converter voltage for single-stage as well as for the two-stage converter configuration (two-stage converter is considered for simulation). The results from simulation study also depict the voltage gain attained from the multi-stage system with a nominal amount input voltage supplied to the topology.

The Figures 4.6 and 4.7 represent the converter working at duty ratio, D=0.7. The Fig. 4.6 (a) represents the input voltage to the converter, Fig. 4.6 (b) and (c) presents the sub-converter output voltage after the single-stage converter system and two-stage converter system respectively. The total input voltage V_i=100V, the single-stage sub-converter output voltage V_a=233V and the two-stage sub-converter output voltage V_c=778V as obtained from the simulation study.

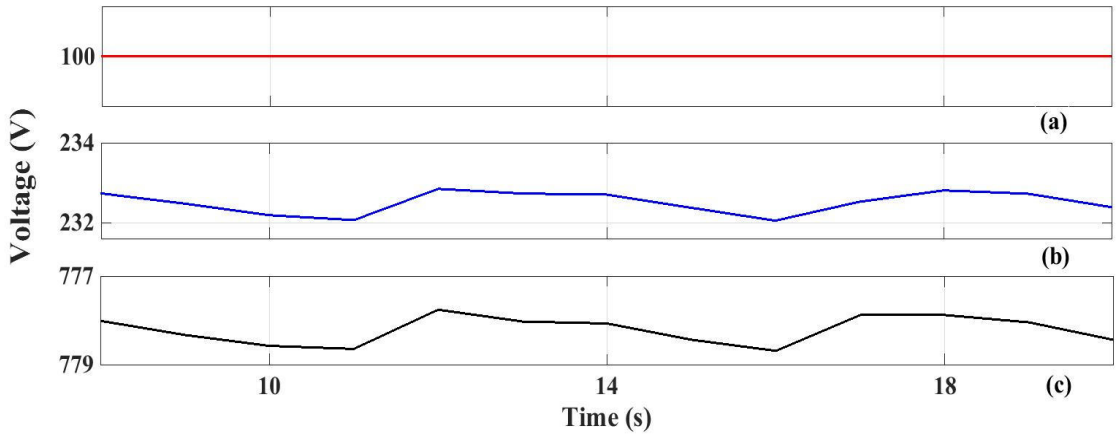


Figure 4.6: (D=0.7) (a) Input voltage (b) Single-stage sub-converter output voltage (c) Two-stage sub-converter output voltage

The Fig. 4.7 (a) represents the total input voltage and the Fig. 4.7 (b) presents the total output voltage of the converter. The total input voltage V_i=100V, the total output voltage V_o=2122V as obtained from the simulation analysis.

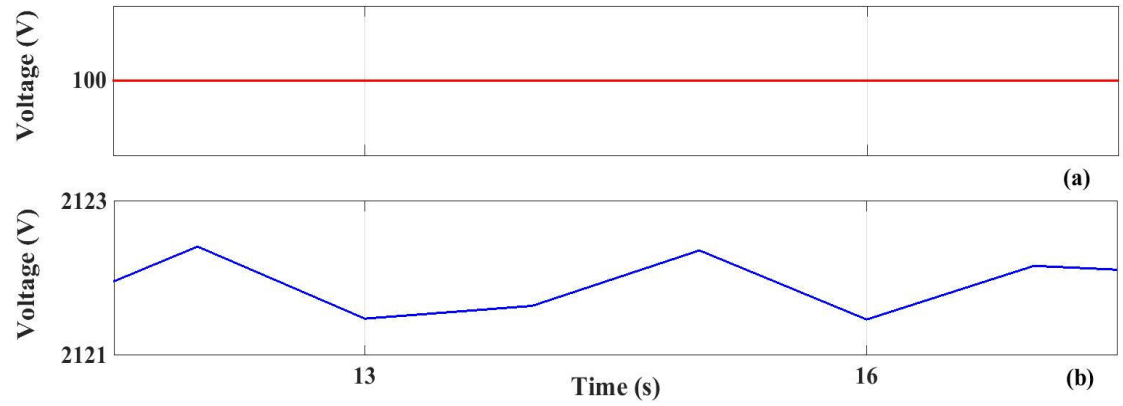


Figure 4.7: (D=0.7) (a) Input voltage (b) Total output voltage

The Figures 4.8 and 4.9 represent the converter working at a duty cycle, D=0.5. The Fig. 4.8 (a) represents the total input voltage to the converter, Fig. 4.8 (b) and (c) presents the sub-converter output voltage after the single-stage converter system and two-stage converter system respectively. The total input voltage V_i=100V, the single-stage sub-converter output voltage V_a=100V and the two-stage sub-converter output voltage V_c=200V as obtained from the simulation study.

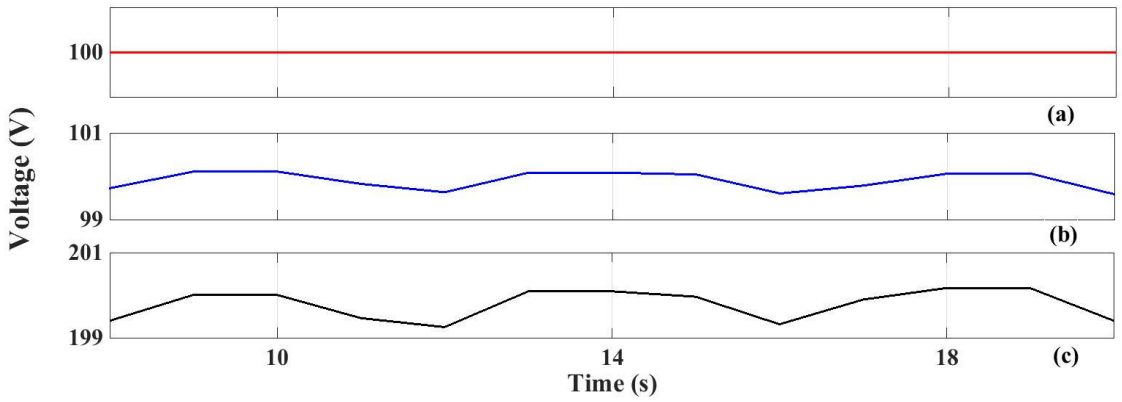


Figure 4.8: (D=0.5) (a) Input voltage (b) Single-stage sub-converter output voltage (c) Two-stage sub-converter output voltage

The Fig. 4.9 (a) represents the input voltage and the Fig. 4.9 (b) presents the total output voltage of the converter. The total input voltage V_i=100V, the total output voltage V_o=700V as obtained from the simulation analysis.

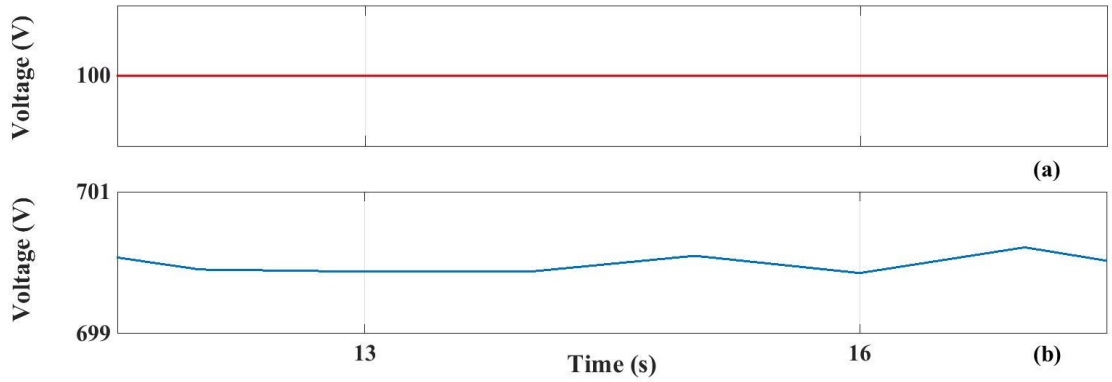


Figure 4.9: (D=0.5) (a) Input voltage (b) Total output voltage

The Figures 4.10 and 4.11 represent the converter working at duty cycle, D=0.3. The Fig. 4.10 (a) represents the total input voltage to the converter, Fig. 4.10 (b) and (c) presents the sub-converter output voltage after the single-stage converter system and two-stage converter system respectively. The total input voltage V_i=100V, the single-stage sub-converter voltage V_a=42.8V and the two-stage sub-converter voltage V_c=61.2V as obtained from the simulation study.

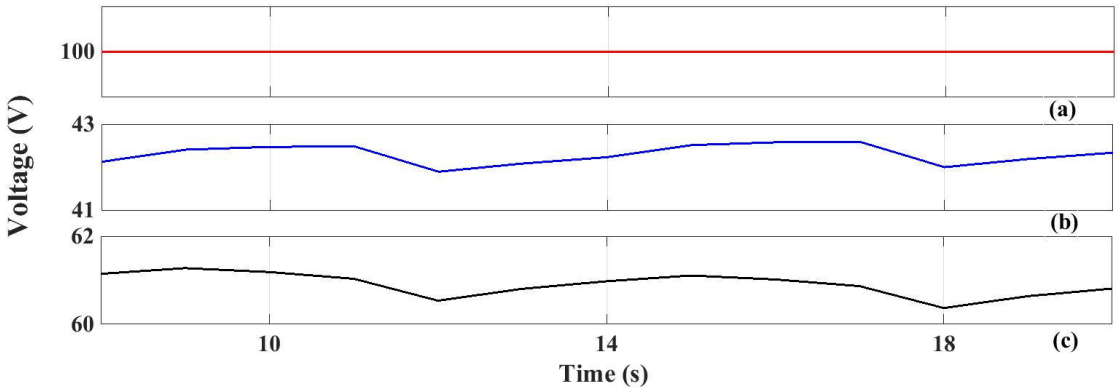


Figure 4.10: (D=0.3) (a) Input voltage (b) Single-stage sub-converter output voltage (c) Two-stage sub-converter output voltage

The Fig. 4.11 (a) represents the input voltage and the Fig. 4.11 (b) presents the total output voltage of the converter. The total input voltage V_i=100V, the total output voltage V_o=308V as obtained from simulation analysis.

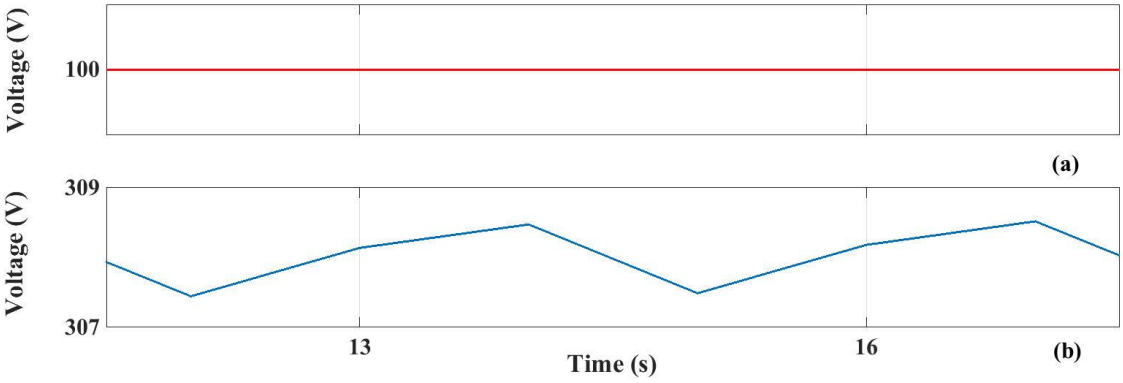


Figure 4.11: (D=0.3) (a) Input voltage (b) Total output voltage

4.7 Conclusion

In the particular chapter the focus was driven towards the comparison of the proposed DC-DC converter with other classical DC-DC converters as well as topologies with higher voltage gain properties which has been classified in the recent literature survey. In the first comparison sphere the proposed converter topology is compared with classical boost and buck-boost converter which are capable in achieving higher gain characteristics. In the comparison table it is vividly seen that the proposed DC-DC converter achieve the required output voltage at a much lower duty cycle when compared with the boost as well as buck-

boost converter. The inductor current ripple is also less which leads to lower peak to peak input current ripple of the converter. The converter also processes a lesser amount of power due to interleaving which leads to the higher efficacy and reliability of the total structure as the semiconductor ratings reduces due to handling lesser amount of power.

Similarly, the proposed converter is also compared with recent high-gain topologies i.e. Quasi-SEPIC DC-DC converter and the interleaved boost structure. The inductor peak value and the switch current peak value is much lower for the proposed boost structure when compared to Quasi SEPIC structure. In the proposed structure it is seen from the tables that it processes a fraction of power through each sub-converter when compared to sub-converter level of interleaved boost structure. The efficiency plot of the proposed boost configuration is done along with other classical DC-DC converter topologies and recent high-gain topologies. From the graphical analysis it has been noticed the semiconductor loss for the proposed converter is lesser compared to other high-gain topologies leading to higher efficiency.

The extension of the internally cascaded multi-stage converter topology is also presented in the chapter. The extended multi-stage structure is able to achieve a higher overall output voltage when compared to the single-stage proposed structure. The voltage gain for n^{th} stage is derived and analytically presented. Here in the chapter a two-stage internally cascaded structure is chosen to showcase the idea. The simulation results presenting the input voltage, the sub-converter voltage both at single-stage and two-stage is shown in the simulation result section. The overall output voltage is also depicted which clearly proclaims and ascertains the fact that the basic concept conceived is practical and functions properly. This brings to the conclusion that the idea generated for the internally cascaded multi-stage converter is applicable and its objective of attaining higher voltage gain is very much a reality when appropriately attached with the proposed converter system.

Chapter 5

Proposed Converter Application in a 5-Level Open-End Induction Motor Drive

5.1 Introduction

The main objective of the chapter is to promote the application of the proposed converter in various fields and spheres of machine drives. The inverter switching loss and the motor phase ripple current can be minimized with the aid of multilevel inverter. Specifically, the inverter levels higher than two are preferred in comparison to a two-level inverter. Voltage Source Inverter (VSI) is flexible and most commonly used mechanism for speed control of induction motor drives. In medium voltage (2.3kV-13.8kV) applications, a major challenge is to select a suitable topology so that the economical commercially available semiconductor devices can be used to withstand the DC voltage required by the drive. Multilevel inverter topologies are popular for Medium Voltage (MV) high power drive applications due to their higher efficiency [92] and reduced voltage rating of the individual switches [93, 94]. Though various hybrid multilevel topologies are popular in low voltage application, only Neutral Point Clamped (NPC), Cascaded H-Bridge (CHB) and Flying Capacitor (FC) inverter topologies are commercially used in MV drives. As an example, 3-level NPC inverter is used by Siemens in Sinamics SM150 [95], 5-level active NPC inverter is used by ABB in ACS2000 series [96] and CHB inverter is used by Siemens in Perfect Harmony series. For Medium Voltage High Power (MVHP) applications, multilevel inverter in open end configuration is gaining popularity for induction motor drives due to higher reliability, lower voltage distortion, and smaller individual power converter rating [97].

In the linear modulation range, the maximum fundamental voltage that can be generated across the motor terminal is less than the input AC voltage fed to the diode bridge rectifier. This reduction in voltage is caused by the voltage loss due to the practical limits of maximum modulation index in the linear operating range, voltage loss due to dead time, and voltage drop in the semiconductor switches, etc. Variable Speed Drive (VSD) supplied through long cables such as in the mines often faces the additional problem of significant line voltage

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Part of this work presented in this chapter has been accepted for publication in the paper entitled, "Performance Improved Multi-Level OEIM Drive with Voltage Boost through Unequal Levels", by K. Sarkar, A. Chakrabarti, P. Kasari, B. Das and S. K. Biswas, *IEEE Transactions on Industry Applications*, Early Access, June 2023.

drop [98]. Further, supply voltage can dip by about 10%, either momentary or long term, which are common. The combined effect of the above mentioned factors results in a substantial reduction in the motor terminal voltage and hence torque. Thus, it is essential to boost the DC bus voltage to maintain the rated AC voltage at the motor terminal despite the above-mentioned practical limitation [99]-[101]. A transformer on the input side of a VSD can be used to compensate for these voltage drops and may also provide galvanic isolation (which prevents leakage current due to CMV). However, the transformer contributes approximately 30-50% of the size, 50-70% of the weight, and substantially adds to the overall cost of the system [102]. A VSD without a dedicated transformer at its input is especially preferred in applications such as offshore platforms, mining, etc., where the size and weight of the drive system increase the structural requirements of the installation.

Single stage boost type active NPC topologies and switched capacitor based boost inverter topologies are popularly used for boosting the DC voltage in solar PV application [100][101]. In these topologies, the capacitors get charged in parallel to the input DC voltage and discharges in series with the input source. However, the voltage and current rating of the commercially available capacitor and device may not be sufficient to withstand the full DC link voltage in medium voltage applications. A two-stage topology with a fully rated DC-DC converter can be used to boost the DC voltage at the input of the VSI to its desired value [103]. However, the blocking voltage and current rating of the existing semiconductor devices does not permit the use of two stage topology in MVHP applications [104]. A fully rated DC-DC converter also substantially adds to the size and cost of the overall VSD system. A Z-source or a quasi Z-source inverter is a single-stage solution for boosting the output of the VSI efficiently [105]. However, large size of the passive elements, higher loss and poor dynamic response due to the presence of right half zero in a Z-source or quasi Z-source inverter limits its application in high-performance drives.

An open-end winding topology is a popular and suitable topology to work in medium voltage high-power applications e.g. traction, electric/hybrid vehicles etc. In an open-end winding the neutral of the Induction Motor is disconnected and two separate 3-ϕ inverters directly feed the stator winding of the motor from both ends. The primary focus is to supply the motor from both ends with a small number of levels in order to create a multilevel voltage across the motor's stator winding. The inverters connected at either ends of the stator winding can be of similar power and voltage rating and are able to operate at same switching frequency or they can have different rating (i.e. power/voltage) in which case it will operate

at different switching frequency. The 3-ϕ inverters are fed from sources (DC-link) that is of half the magnitude when compared with a conventional two-level inverter. In transformer-less dual inverter fed open end drives, both the inverters are supplied from a single DC source. As a result, a zero sequfence current due to common mode voltage may circulate through the motor winding without producing any torque but contributing to the machine losses. Hence it is important to eliminate common mode circulating current from an open end drive supplied from a common DC source. The existing techniques of eliminating common mode circulating current are effective only if all the voltage steps are equal in magnitude [106]-[109]. Further, the simultaneous balancing of capacitor voltage and common mode elimination in full modulation range is not possible for 4 or higher level VSI unless a separate hardware balancer circuit is used.

This article proposes a modified topology for efficiently boosting the DC bus voltage in a transformer-less 5-level NPC VSI based Open End Induction Motor (OEIM) drive. Out of the four separate voltage levels, common to both the VSI's, the two middle levels are obtained by dividing the input DC voltage using a capacitor voltage divider. A substantial amount of power consumed by the motor thus directly flows to the inverter through these two DC buses. The top and bottom voltage levels are obtained from the proposed DC-DC converter, whose generated voltages are kept just sufficient to cater to the boost need, resulting in low additional power loss in the process of boosting the voltage. This however, creates variable and unequal voltage at the input DC bus of the five levels, causing CMV generation that cannot be controlled through classical techniques. In this article, a new generalized technique is also proposed to restrict circulating current flow due to CMV in a 5-level inverter fed open-end drive supplied from a common DC source with unequal step height, while also permitting capacitor balancing. The performance of the proposed scheme with the proposed PWM method is evaluated through simulation and experimental study.

5.2 Proposed Scheme

In the proposed scheme, an OEIM drive is fed through two NPC inverters having a common DC source as depicted in Fig. 5.1. In the proposed DC-DC converter the output of the two partly rated DC-DC sub-converters is connected on either side of the input DC rail (proposed DC-DC converter shown in Fig 2.1 in section 2.2). In case the input DC voltage which is the output of the 3-ϕ rectifier drops below its rated value, the two partly rated DC-DC sub-converters generate the additional voltage required by the drive. With V_{DC} as the

incoming DC bus voltage and V_{FB} as the voltage generated by each DC-DC sub-converter, the total DC bus voltage (V_{DC_total}) for the inverter is given by:

$$V_{DC\_total} = V_{DC} + 2V_{FB} \tag{5.1}$$

The total DC bus voltage in the proposed scheme consists of four effective voltage sources (capacitor) which are connected in cascade. The top and bottom voltages are obtained from the proposed DC-DC converter and the other two in the middle is obtained by dividing the input DC into two equal parts using a capacitor voltage divider circuit as shown in Fig 5.1. These four effective voltage sources is the common input for the two 5-level NPC VSI of the OEIM drive. Since the boost voltage generated by the two DC-DC sub-converters of the proposed DC-DC converter are different from the voltage across the capacitor voltage divider circuit, the voltage generated by the five level NPC VSI has unequal step heights. The modified topology providing unequal step heights is of prime importance where it has the ability of catering to the voltage boost required in case of dip in the supply voltage.

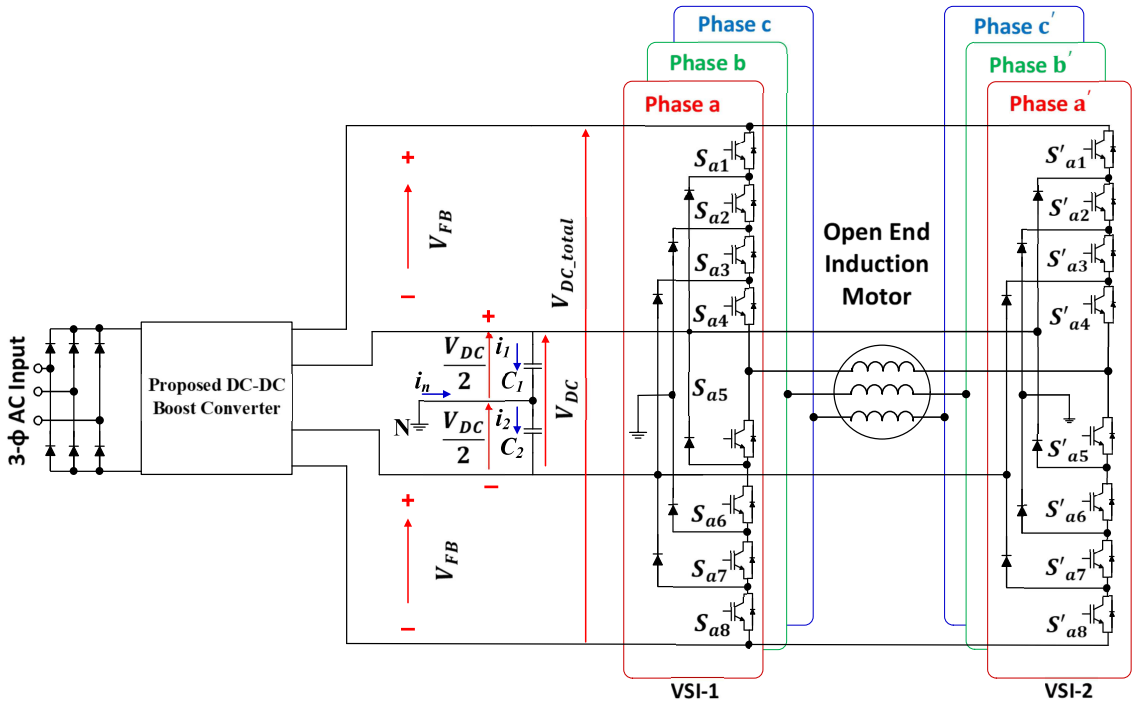

Figure 5.1: Proposed 5-level open end induction motor drive with unequal level and voltage boost capability

Existing carrier based scheme is popular for multilevel topologies where the step heights are of equal magnitude. However, existing carrier based PWM scheme cannot be implemented in this proposed 5-level OEIM drive. A carrier based PWM scheme is proposed in the section 5.7. which can restrict the flow of common mode circulating current even

though the voltage steps produced by the two VSI's are unequal and simultaneously can balance the capacitor voltage under dynamic operating condition.

5.3 Voltage Boost Generation using DC-DC Converter

A non-isolated DC-DC converter as depicted in Fig. 2.1 in section 2.2 is used to generate the desired boost voltage from the given DC bus. The input voltage to the proposed DC-DC converter which is the output of the rectifier as shown in Fig. 5.1 is V_i and the output is variable which depends upon the voltage boost required by the drive. The proposed converter is used to create four distinct DC voltage levels, as depicted in Fig. 5.1. In this case, the output voltages of the top and bottom levels are kept equal i.e. V_{FB}, as already explained in section 2.2 of Chapter 2 and $V_i = V_{DC}$. The output voltages of the individual sub-converters can be adjusted depending on the number of levels required and the voltage of each level (since input mid-point can be created by two capacitors C_1 & C_2 replacing C_S to create neutral point).

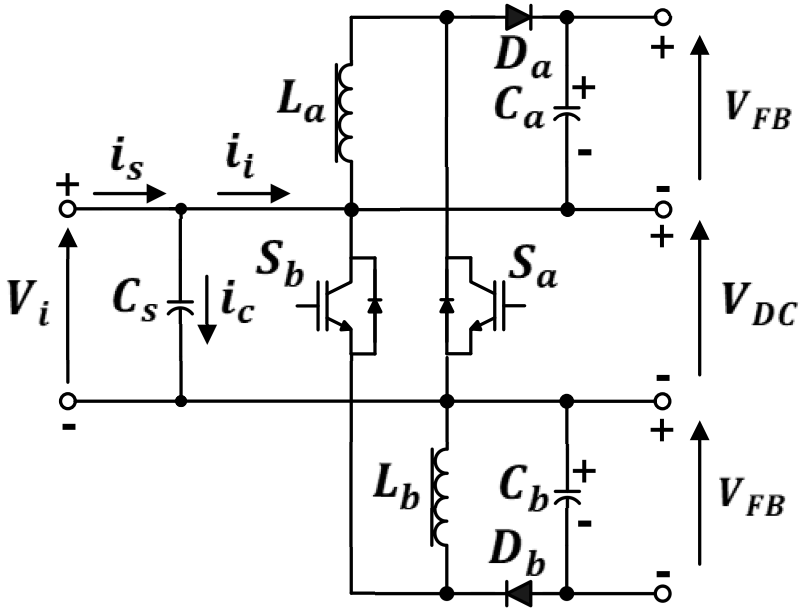

Figure 5.2: Proposed converter as source of multiple DC voltage levels

In order to elaborately understand the voltage boost requirement, it is seen in the Fig. 5.1 that an OEIM drive is being fed from two five-level Neutral Point Clamped (NPC) Voltage Source Inverter (VSI) having a common (DC) source. The DC source is obtained from the output of a 3-ϕ rectifier. The average value can be expressed as [110]:

$$V_{DC} = 1.35 V_{RMS-grid} \tag{5.2}$$

where $V_{RMS-grid}$ is the line-line RMS voltage which is fed to the input of the 3-ϕ rectifier. The maximum DC bus utilization for an OEIM drive operating under linear modulation range is 70.7% (for common DC source). Therefore, the maximum RMS voltage that is present across the motor winding can be expressed as:

$$V_{RMS-Motor} = 0.707 \text{x} 1.35 V_{RMS-grid}$$
$$= 0.954 V_{RMS-grid} \quad (5.3)$$

From (5.3) it is observed that the RMS voltage that is being generated across the motor terminals of the induction motor is 5% less than when compared to the grid voltage. A further 10% drop is allowable voltage loss due to dead time and practical limitation in modulation index in linear operating range [111], [112]. Therefore, the RMS voltage that is generated across the motor winding at the instant of the above mentioned voltage drops can be expressed as:

$$V_{RMS-Motor} = 0.90 \text{ x } 0.95 V_{RMS-grid} \quad (5.4)$$

Therefore, the expression can be further simplified as:

$$V_{RMS-Motor} = 0.85 V_{rated-grid} \quad (5.5)$$

From the above mentioned expressions (5.2) to (5.5) it can be shown that voltage boost required by the drive can be limited to 15% of the rated DC link voltage. Hence each of the individual DC-DC sub-converters of the proposed DC-DC converter is designed to generate maximum 7.5% of the rated DC voltage. Since the current flowing through the output of the DC-DC converter is same as the load current, the power rating of each of these converters will be 7.5% of the rated power of the machine. Since the voltage in the primary side of the converter is V_i, the current rating of the devices in the primary circuit will be 7.5% of the rated current of the inverter switches.

In the proposed 5-level OEIM drive with unequal voltage step height the voltage boost is generated in an energy efficient way. As stated earlier in the section the input DC bus is split equally with the aid of a capacitor voltage divider circuitry, the voltage across the capacitors are maintained at an equal magnitude with a voltage balancing algorithm which is discussed in the section 5.6. The voltage across the two capacitors connected in series is the contributor of around 80%-95% of the DC bus voltage available. It gets connected directly to two VSI's of OEIM drive without the involvement of any interfacing DC-DC converters. Therefore, there is a direct flow of the bulk power from the input DC bus towards the two VSI's without any loss occurring from any intermediate DC-DC converters.

The boost fraction of the voltage which is around 15% of the total DC bus voltage is being generated from the proposed DC-DC converter consisting of two sub-converters which are connected on either side of the positive and negative side of the input DC bus respectively. The sub-converters of the proposed DC-DC converter scheme only carry a fraction of the total input power. Hence, it can be stated that the size as well as the loss associated with the proposed DC-DC converter is much less when compared with topologies where a full rated DC-DC converter is utilized to boost the total DC voltage. At the instant when the speed is low or there is rated DC supply voltage, the requirement for voltage boosting of the DC bus is negligible, the switches S_{x1} and S_{x8} are turned OFF continuously. Whereas, S_{x4} and S_{x5} are switched continuously ON (where $(x \in (a,b \text{ or } c))$ and the other devices in the system operate in PWM mode. Under this operating condition power flows directly from the DC source toward the VSI. Due to this the loss associated with the proposed DC-DC converter consisting of two sub-converters is at a minimum range.

From the Fig. 5.1 it can be seen that the switches S_{x1} and S_{x4} (where $(x \in (a,b \text{ or } c))$ the voltage that is being boosted. The switches S_{x2} and S_{x3} has to withstand only half of the input DC bus voltage. However, the semiconductor devices (switches) generally consists of symmetrical devices which are two in number. Therefore, all the semiconductor devices in the proposed five level OEIM drive topology presented in the Fig. 5.1 has to have a rating of half the input DC bus voltage.

5.4 CMV Elimination in Drive with Unequal Voltage Step

The existing techniques for operating OEIM drive from a common DC source requires that the CMV produced by the individual VSI should be zero at all instant. This can be achieved using Space Vector Pulse Width Modulation (SV-PWM) technique or CB-PWM technique, however in both the techniques, it is essential that all the voltage levels in the pole voltage of the inverter should be of same height. Since V_{FB} is not necessarily equal to $V_{DC}/2$, voltage steps are of unequal height and hence existing PWM techniques cannot be used to restrict the circulating current in the proposed topology. To tackle the situation, a more general approach is used here such that the instantaneous CMV produced by two VSI is the same but not necessarily zero. In the proposed PWM scheme, the fundamental voltage generated by both the VSIs are phase shifted by 120° instead of a phase shift of 180° as in existing PWM technique of OEIM drive [113]. This approach can restrict the flow of circulating current due to CMV even when the voltage levels in the pole voltage of the

inverter are of unequal heights. With 120° phase shift between the two inverters of the OEIM drive, the motor winding voltage is:

$$V_m \sin(\omega t - \phi) = U_{1p} \sin(\omega t) - U_{1p} \sin(\omega t - 2\pi/3) - U_{CMV} \sin(3\omega t) - U_{CMV} \sin 3(\omega t - 2\pi/3) \quad (5.6)$$

where, V_m is the peak of the instantaneous voltage across the motor winding, ω is the angular frequency of the winding voltage, ϕ is the phase shift of the winding voltage with respect to the fundamental component of pole voltage of VSI-1, U_{1p} is the peak of the fundamental component of pole voltage generated by VSI-1 & VSI-2 while U_{CMV} is the peak of the CMV produced by VSI-1 & VSI-2. From (5.6), it can be seen that a shift of 120° in the fundamental voltage creates a 360° phase shift for the 3rd harmonic, which is a CMV. The voltage across the motor winding is thus given by:

$$V_m \sin(\omega t - \phi) = \sqrt{3} U_{1p} \sin(\omega t - \pi/3) \quad (5.7)$$

From (5.7) it can be concluded that when a phase shift of 120° is created between reference voltages of both the VSI's in an OEIM drive operating with same voltage levels, the CMV across the motor winding will be zero. As a result, no circulating zero-sequence current flows through the motor winding even when each VSI generates CMV. This technique can remove CMV in the proposed five-level NPC VSI based OEIM drive with unequal voltage levels.

From (5.7), it can be observed that the fundamental voltage across the motor winding is √3 times the voltage generated by each VSI. A 3rd harmonic voltage can be injected in the proposed PWM technique to increase the DC bus utilization by 2/√3 times [114]. Since the voltage at two ends of the OEIM drive is shifted by 120°, the 3rd harmonic voltage generated by the two VSI will be cophasal and hence no resultant 3rd harmonic current will flow through the motor winding. Considering this 2/√3 time increase in DC bus utilization, the fundamental voltage across the motor winding is given by:

$$\begin{aligned} V_m \sin(\omega t - \phi) &= \left(2/\sqrt{3}\right)\sqrt{3} U_{1p} \sin(\omega t - \pi/3) \\ &= 2U_{1p} \sin(\omega t - \pi/3) \end{aligned} \quad (5.8)$$

In the linear modulation range, DC bus voltage required to produce a peak pole voltage of U_{1p} at modulation index m, is:

$$U_{1p} = (0.5/m) V_{DC\_total} \quad (5.9)$$

Substituting the value of U_{1p} from (5.9) in (5.8), the winding voltage can be expressed as:

$$V_m \sin(\omega t - \phi) = (V_{DC\_total}/m) \sin(\omega t - \pi/3) \quad (5.10)$$

From (5.10) it can be concluded that the total DC bus voltage required in the proposed scheme is equal to the peak of the desired fundamental voltage across winding.

Existing SV-PWM schemes for OEIM drive eliminate CMV from both the inverters, which are operated with a 180° phase shift to maximize the winding voltage [115]. Due to the 180° phase shift, 3rd harmonic voltage injection is not permissible as it will result in 3rd harmonic current. Thus, the voltage generated across the motor winding using the existing SV-PWM schemes for OEIM drive is given by:

$$\begin{aligned} V_m \sin\left(\omega t - \phi\right) &= U_{1p} \sin(\omega t) - U_{2p} \sin(\omega t - \pi) \\ &= 2U_{1p} \sin(\omega t) \end{aligned} \tag{5.11}$$

Substituting the value of U_{1p} from (5.9) in (5.11) the winding voltage can be expressed as:

$$V_m \sin\left(\omega t - \phi\right) = (V_{DC\_total} / m) \sin \omega t \tag{5.12}$$

Comparing (5.10) and (5.12) it can be concluded that the proposed scheme requires the same DC bus voltage as in the SV-PWM technique. However, SV-PWM is applicable only when voltage steps are of equal magnitude, but the proposed scheme can eliminate CMV even if voltage steps are unequal.

5.5 Reference Signal Generation

Assume fundamental components of the reference signal generated by the motor control algorithm $(v_{as}, v_{bs} \text{ and } v_{cs})$ as:

$$\begin{aligned} v_{as} &= V_s \sin\left(\omega t\right) \\ v_{bs} &= V_s \sin\left(\omega t - 2\pi/3\right) \\ v_{cs} &= V_s \sin\left(\omega t + 2\pi/3\right) \end{aligned} \tag{5.13}$$

where V_s is the peak of the reference signal. The reference signals created for 3 phases of VSI-1 $(v_{a1s}, v_{b1s} \text{ and } v_{c1s})$ are:

$$\begin{aligned} v_{a1s} &= (1/3)\left(v_{as} - v_{bs}\right) = (1/\sqrt{3}) V_s \sin\left(\omega t + \pi/6\right) \\ v_{b1s} &= (1/3)\left(v_{bs} - v_{cs}\right) = (1/\sqrt{3}) V_s \sin\left(\omega t - \pi/2\right) \\ v_{c1s} &= (1/3)\left(v_{cs} - v_{as}\right) = (1/\sqrt{3}) V_s \sin\left(\omega t + 5\pi/6\right) \end{aligned} \tag{5.14}$$

The reference signals for three phases of VSI-2 $(v_{a2s}, v_{b2s} \text{ and } v_{c2s})$ are generated as follows:

$$\begin{aligned} v_{a2s} &= (1/3)\left(v_{cs} - v_{as}\right) = (1/\sqrt{3})V_s \sin\left(\omega t + 5\pi/6\right) \\ v_{b2s} &= (1/3)\left(v_{as} - v_{bs}\right) = (1/\sqrt{3})V_s \sin\left(\omega t + \pi/6\right) \\ v_{c2s} &= (1/3)\left(v_{bs} - v_{cs}\right) = (1/\sqrt{3})V_s \sin\left(\omega t - \pi/2\right) \end{aligned} \tag{5.15}$$

From (5.14) and (5.15), it can be observed that a phase shift of 120° is generated between the reference signals of VSI-1 and VSI-2. The effective reference signal for the motor winding is the difference between reference signals for both the VSI, and can be expressed as:

$$\begin{aligned} v_{a1s} - v_{a2s} &= V_s \sin\left(\omega t\right) = v_{as} \\ v_{b1s} - v_{b2s} &= V_s \sin\left(\omega t - 2\pi/3\right) = v_{bs} \\ v_{c1s} - v_{c2s} &= V_s \sin\left(\omega t + 2\pi/3\right) = v_{cs} \end{aligned} \tag{5.16}$$

From (5.13) and (5.16), it can be inferred that the effective reference signal for the motor winding is the same as generated by the motor control algorithm.

The reference signals generated for both the VSI are modulated with offset voltages to maximize the DC bus utilization [116]. This offset voltage ($v^1_{off\_x}$) is given by:

$$v^1_{off\_x} = 0.5\left(\max(v_{axs}, v_{bxs}, v_{cxs}) - \min(v_{axs}, v_{bxs}, v_{cxs})\right) \tag{5.17}$$

where x=1 for VSI-1 and x=2 for VSI-2. The function min(a,b,c) determines the minimum value and max(a,b,c) the maximum respectively, among the three variables. This offset voltage is added to the reference signals for VSI-1, as presented in (5.14), and reference signals for VSI-2, as presented in (5.15). The modified reference signals for the pole voltage of VSI-1 and VSI-2 thus obtained are:

$$\begin{aligned} v^*_{axp} &= v^*_{axs} + v^1_{off\_x} \\ v^*_{bxp} &= v^*_{bxs} + v^1_{off\_x} \\ v^*_{cxp} &= v^*_{cxs} + v^1_{off\_x} \end{aligned} \tag{5.18}$$

Another offset voltage $(v^2_{off\_x})$ is added to distribute the redundant voltage vector at the beginning and end of the switching period to reduce the harmonic distortion in the output voltage and is given by [117]:

$$v^2_{off\_x} = 0.5V_{dc}\left[0.5 - 0.5\left(M_x + N_x\right)\right] \tag{5.19}$$

where,

$$M_x = \max\begin{pmatrix} rem\left((v^*_{axp\_nom}+1),1\right), \\ rem\left((v^*_{bxp\_nom}+1),1\right), rem\left((v^*_{cxp\_nom}+1),1\right) \end{pmatrix}$$

$$N_x = \min\begin{pmatrix} rem\left((v^*_{axp\_nom}+1),1\right), \\ rem\left((v^*_{bxp\_nom}+1),1\right), rem\left((v^*_{cxp\_nom}+1),1\right) \end{pmatrix} \tag{5.20}$$

where the normalized value of the reference signal (v^*_{yxp}) is calculated as follows:

$$v^*_{yxp\_nom} = (v^*_{yxp} / 0.5V_{dc}) + 1 \tag{5.21}$$

The remainder functions used in (5.20) is defined as:

$$rem(a,b) = a - b\,\mathrm{int}(a,b) \tag{5.22}$$

where, {int(a,b)} returns the integer value when a is divided by b. The offset voltages obtained in (5.17) and (5.19) are added to the reference signals for VSI-1, as presented in (5.14) and reference signals for VSI-2, as presented in (5.15), to obtain the reference signal for pole voltage of VSI-1 and VSI-2, as:

$$v^*_{ypx} = v^*_{yxs} + v^1_{off\_x} + v^2_{off\_x} \tag{5.23}$$

5.6 Capacitor Voltage Balancing

In the proposed 5-level VSI, the input DC is split into two halves using two identical series-connected capacitors. At a steady-state, voltages across both the capacitors remain equal. During transient, a non-zero neutral current may flow through the center of the DC bus, causing the voltage across the capacitors to deviate. To maintain equal voltage across

the capacitor at all operating conditions, a non-zero neutral current of proper polarity has to be generated [116], [117].

Assuming the two capacitors in Fig. 5.1 to have a capacitance of C Farad each and voltage across these two capacitors to be V_{C1} and V_{C2} respectively, energy (E) stored in capacitors is:

$$E = 0.5\left[CV_{C1}^2 + CV_{C2}^2 \right] \tag{5.24}$$

It can be established that energy stored is minimum when $V_{C1}=V_{C2}$. Thus, the capacitor voltage balancing can be achieved if the rate of change of energy is zero or negative. This can be mathematically expressed as:

$$\left(V_{C1} - V_{C2}\right)\left(i_2 - i_1\right) \le 0 \tag{5.25}$$

where i_1 and i_2 are the currents through the capacitors C_1 and C_2. From Fig. 5.1, it can be seen that the current (i_n) through the middle of the DC bus is equal to:

$$i_n = \left(i_2 - i_1\right) \tag{5.26}$$

Substituting i_n in (5.25), the condition for balancing the capacitor voltage can be expressed as:

$$\left(V_{C1} - V_{C2}\right) i_n \le 0 \tag{5.27}$$

Thus, to balance the capacitor voltage, information about the polarity of the current through the middle of the DC bus is required. This current is a combination of currents generated by the three phases (i_{na}, i_{nb}, i_{nc}) and can be expressed as:

$$i_n = i_{na} + i_{nb} + i_{nc} \tag{5.28}$$

The current components i_{nx} $(x \in (a, b \text{ or } c))$ contributed by each phase, can be estimated as [117]:

$$\bar{i}_{nx} = \begin{Bmatrix} \left(rem\dfrac{\left(v^*_{yxp\_norm},1\right)}{1-G},1 \right) i_x & 0 < v^*_{yxp\_norm} < (1-G) \\ \left[1 - rem\dfrac{\left(v^*_{yxp\_norm} - 1 + G\right)}{1+G},1 \right] i_x & (1-G) \le v^*_{yxp\_norm} < 2 \end{Bmatrix} \tag{5.29}$$

where $G = (V_{C2} - V_{C1}) / (V_{dc})$

Once neutral current is determined $v_{off\_x}^2$ is modified to balance the capacitor as per the following four conditions:

If $\overline{i_n} > 0$ and $(v_1 - v_2) > 0$ then $v_{off\_x}^2 = -N$

If $\overline{i_n} > 0$ $\bar{\text{i}}_\text{n} > 0$and $(v_1 - v_2) < 0$ $(\text{v}_1\text{-v}_2) < 0$ then $v_{off\_x}^2 = M$

If $\overline{i_n} < 0$ $\bar{\text{i}}_\text{n} < 0$and $(\text{v}_1\text{-v}_2) > 0$ $(v_1 - v_2) > 0$ then $v_{off\_x}^2 = -N$

If $\overline{i_n} < 0$ $\bar{\text{i}}_\text{n} < 0$and $(\text{v}_1\text{-v}_2) < 0$ $(v_1 - v_2) < 0$ then $v_{off\_x}^2 = M$

5.7 Implementation of the Proposed Scheme

Let V_m be the rated peak fundamental voltage across the motor winding. From (5.10) it can be inferred that in open-end configuration, to generate the rated peak voltage across the motor winding, the DC bus voltage required is:

$$V_{DC}^* = V_m / m_{\max} \tag{5.30}$$

Assuming the DC bus voltage required for generating the desired peak voltage across the motor winding is more than the incoming DC voltage (V_{DC}), the additional DC voltage is generated by the sub-converters of the proposed DC-DC boost converter and is given by:

$$V_{boost} = V_{DC}^* - V_{DC} \tag{5.31}$$

This additional voltage (V_{boost}) is symmetrically generated by the sub-converters of the proposed DC-DC converter which act as the top and bottom voltage levels for the five-level VSI. Taking total DC bus voltage as the base value, the pu voltage generated by each sub-converter of the DC-DC converter (K_1) can be expressed as:

$$K_1 = (V_{boost} / 2V_{DC}^*) = (V_{FB} / V_{DC}^*) \tag{5.32}$$

Two capacitors connected in series across the incoming DC source act as the remaining two sources for the five-level NPC VSI. The pu voltage for each such source (K_2) is given as:

$$K_2 = 0.5(1 - 2K_1) \tag{5.33}$$

Thus, the four DC inputs for the proposed five-level NPC VSI are in the ratio of:

$$V_{FB} : 0.5V_{DC} : 0.5V_{DC} : V_{FB} = K_1 : K_2 : K_2 : K_1 \tag{5.34}$$

When the DC bus voltage needed for generating the desired peak voltage across the motor winding is less than the incoming DC voltage (V_{DC}), the DC-DC sub-converters may be kept at a minimum voltage with inverter output voltage reduction through PWM control to maintain 5-level VSI structure.

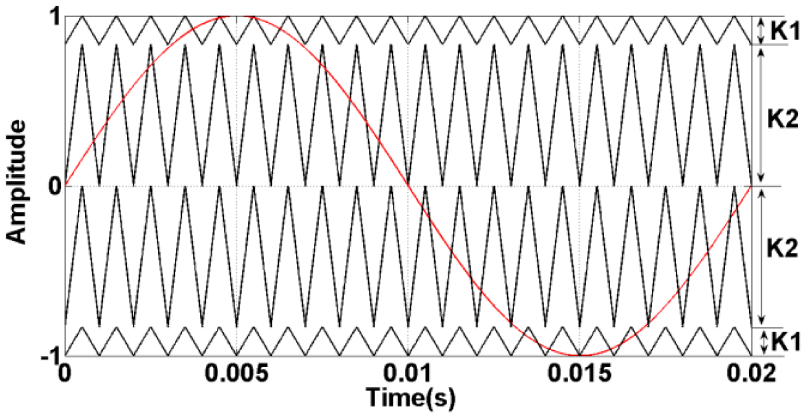

Figure 5.3: Possible multicarrier PWM scheme

Fig. 5.3 shows a possible multi-carrier PWM technique for 5-level NPC VSI, where the reference is compared with a level-shifted carrier wave, whose magnitude is proportional to the corresponding DC bus voltage. The generation of the carrier with variable amplitude through DSP consumes a lot of resources and thus is not a popular hardware implementation. Here, a modified reference signal is compared with a single carrier to generate the PWM gate pulses for the proposed 5-level NPC VSI. The reference signal is modified such that the same level shift and the same ratio between the peak of the triangular carrier and the reference signal are preserved as in the case of the multicarrier PWM technique.

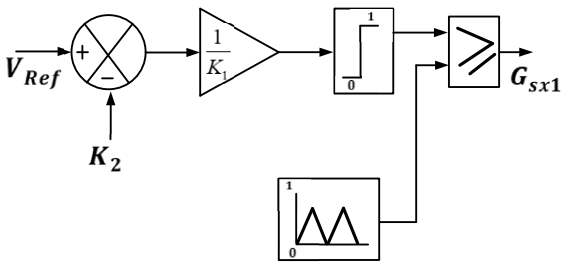

Figure 5.4 (a): Gate Pulse Generation for S_{x1}

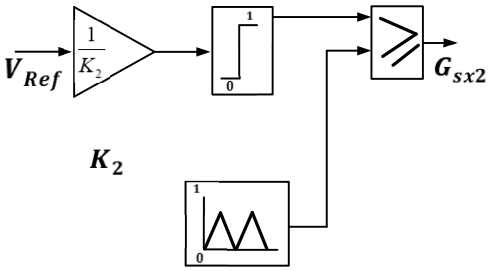

Figure 5.4 (b): Gate Pulse Generation for S_{x2}

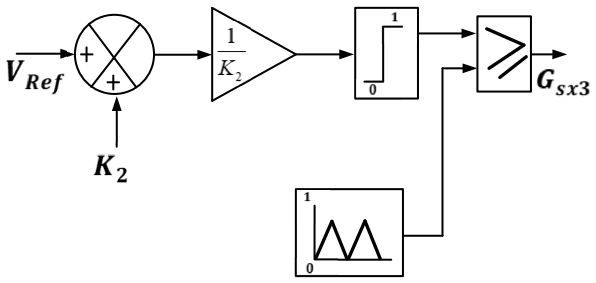

Figure 5.4 (c): Gate Pulse Generation for S_{x3}

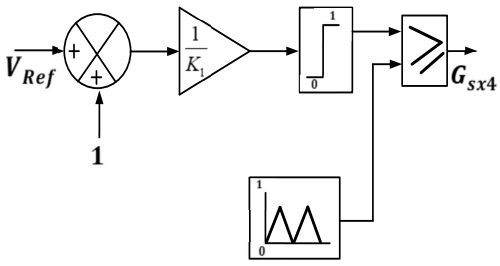

Figure 5.4 (d): Gate Pulse Generation for S_{x4}

In a multi-carrier PWM scheme as in Fig. 5.3, the gate pulse for the top switches (S_{x1}) are generated by comparing the reference signal with a triangular (carrier) wave having a height of K_1 and a level shift of K_2. For generating similar gate pulses using a single-carrier scheme where the magnitude of the triangular carrier varies from 0 to 1, K_2 is first subtracted from the reference signal, resulting in the same level shift between the carrier and the reference signal. The modified reference signal is divided by K_1 to obtain the same ratio between the magnitude of the triangular (carrier) wave and the reference signal as in the case of a multicarrier system. A schematic for obtaining the gate pulses for the switches S_{x1} using the single carrier wave scheme is presented in Fig. 5.4 (a).

For gate pulse generation of the switch S_{x2} using the multi-carrier scheme, the carrier signal initially starts from zero value and has a magnitude of K_2. For generating the same pulses from a single carrier scheme, the reference signal is divided by K_2 without offset addition as depicted in Fig. 5.4 (b).

To generate the gate pulses for devices S_{x3}, the triangular wave in the multi-carrier scheme for switch S_{x3} starts from a negative value of magnitude K_2. Hence, while converting it to a single-carrier scheme, an offset value of K_2 needs to be added as shown in Fig. 5.4 (c). The signal thus obtained is divided by K_2 and compared with a triangular (carrier) signal.

To generate the gate pulse for the switch S_{x4} the triangular (carrier) wave for the switches S_{x4} starts from -1 and has a magnitude of K_1 in a multi-carrier scheme. Hence, an offset value of 1 is added and the resultant signal is divided by K_1 to generate the gate pulses using the single carrier-based scheme as presented in Fig. 5.4 (d).

5.8 Complete Closed Loop System of the Proposed Scheme

The complete closed loop control system is shown in Fig. 5.5 for the entire proposed system. The error between the reference speed and the actual speed of the motor is processed through a speed controller to generate the reference voltage for the motor. Using equation (5.14) and (5.15), the reference signals for individual inverters are generated. Two offset voltages viz., (v_{off}^{1}) and (v_{off}^{2}) obtained from (5.17) and (5.19) are added to reference signal for the inverter to maximize the DC bus utilization and to minimize the harmonic distortion.

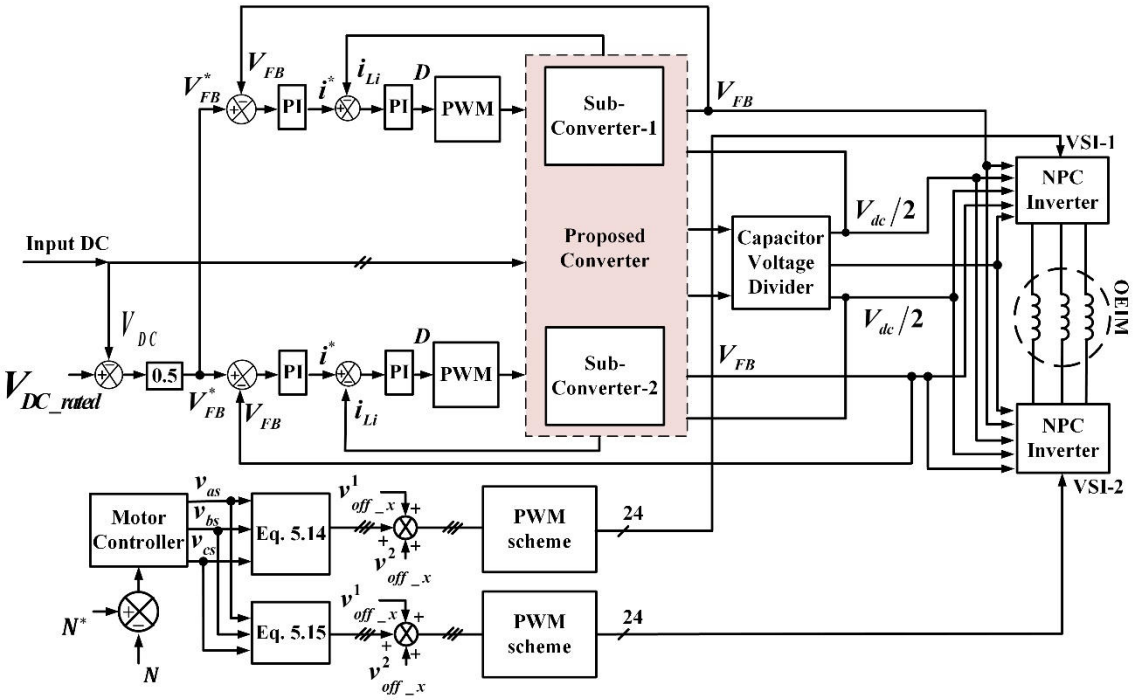

Figure 5.5: Complete Closed Loop Control System of the Proposed Scheme

From these reference signals the gate signals for the individual 5 level NPC inverters are generated. The voltage boost (V_{boost}) required at a given operating condition is the difference between the rated DC link voltage and actual input DC voltage and can be calculated using (5.31). Since this boost voltage is symmetrically generated by the sub converters of the proposed DC-DC boost converter the reference voltage signal (V^*_{FB}) to each of these converters is half of the total boost voltage. The voltage generated from the DC-DC sub-converters are connected on either side of the positive and negative bus of the input DC source to maintain a steady DC link voltage despite of supply voltage variation.

5.9 Performance Analysis

The proposed scheme is simulated in MATLAB/Simulink and is verified on a laboratory prototype. The system specifications are presented in table C.1 in Appendix-C.

5.9.1 Simulation Results

A model of an open-end induction motor is developed in MATLAB/Simulink and is supplied from two ends from two 5-level NPC VSIs with unequal voltage levels. A phase shift of 120° is maintained between the reference signal of the corresponding phases of the two VSIs and gate pulses are generated as explained in section 5.7.

Fig. 5.6 shows the performance of the proposed scheme under various dynamic condition

viz., change in input voltage, change in operating frequency as well as switching frequency, and load change. Initially the two VSI of the OEIM drive are supplied from rated input DC voltage and hence the output of the individual sub-converters of the proposed DC-DC converter is set to be zero. The motor accelerates from zero speed and reaches half the rated speed in 1s. During this dynamic operation it can be seen that the voltage across the capacitor has remained steady at 50% of input DC voltage.

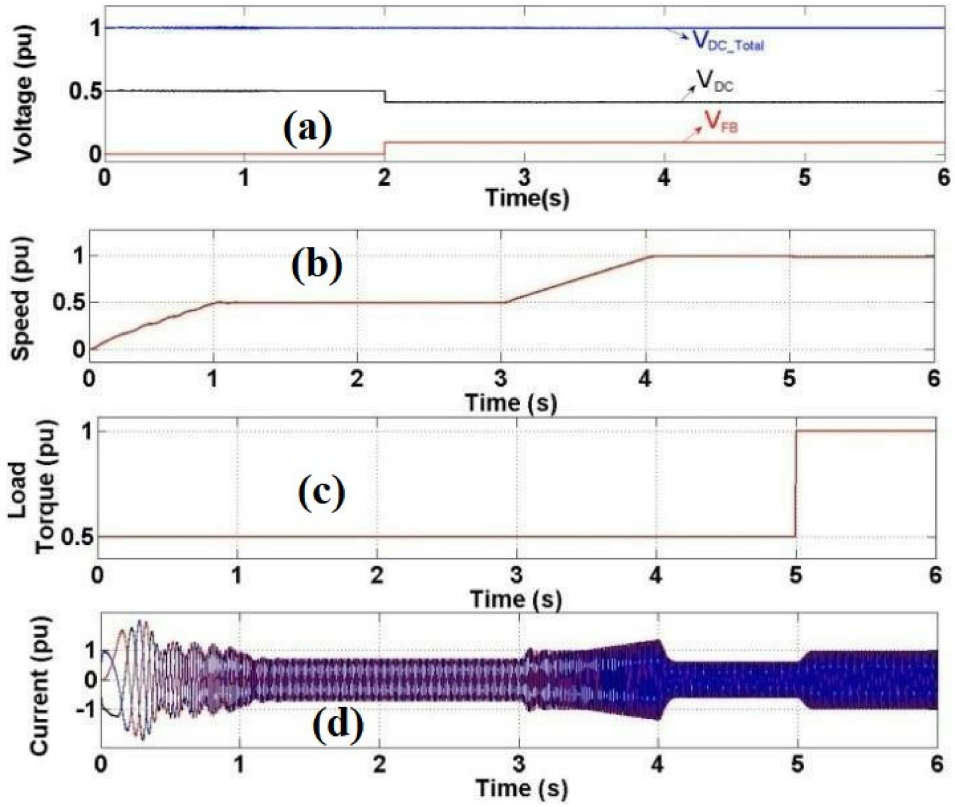

Figure 5.6: Simulation results under dynamic condition (a) Total DC link voltage, supply voltage and DC-DC converter voltage (b) Operating speed of the open end induction motor (c) Load torque of the motor (d) Motor winding current

At 2s, the input DC voltage dips by 15%. The voltage across the individual capacitor also reduces by 15% maintain equal voltage across the two capacitors. As per the proposed scheme, the proposed DC-DC boost converter generate 15% voltage boost which compensate for the voltage dip and maintain the total DC link voltage (V_{DC_total}) at rated value. From simulation result it can be seen that fall in the supply voltage has negligible effect on the total DC link voltage as well as on the speed response. At 3s, the speed command is changed and the machine accelerates to its rated speed. At 4s, the switching

frequency of the VSI is changed from 2.5kHz to 5kHz, and at 5s, rated load torque is applied, the latter causing a small deviation in the operating speed. However, no significant deviation between individual capacitor voltages is observed during these dynamic events, validating capacitor voltage balancing under each such event.

The pole voltage obtained from the proposed topology is a 5-level waveform with unequal voltage levels as shown in Fig. 5.7. The spectrum of pole voltage given in Fig. 5.7 shows the presence of 3rd harmonic, which is the CMV. Other harmonics up to twice the switching frequency are negligible.

The voltage generated across the motor winding contains nine distinct levels of unequal step heights as depicted in Fig. 5.8. The spectrum of the voltage across the motor winding presented in Fig. 5.8 shows that all lower-order harmonics up to twice the switching frequency, including the 3rd (which represents the CMV) are negligible. Thus, the proposed scheme can effectively eliminate CVM even if voltage steps are unequal. The voltage THD for both pole voltage and voltage across the motor winding remains high due to incorporation of harmonics around the switching frequency and twice switching frequency

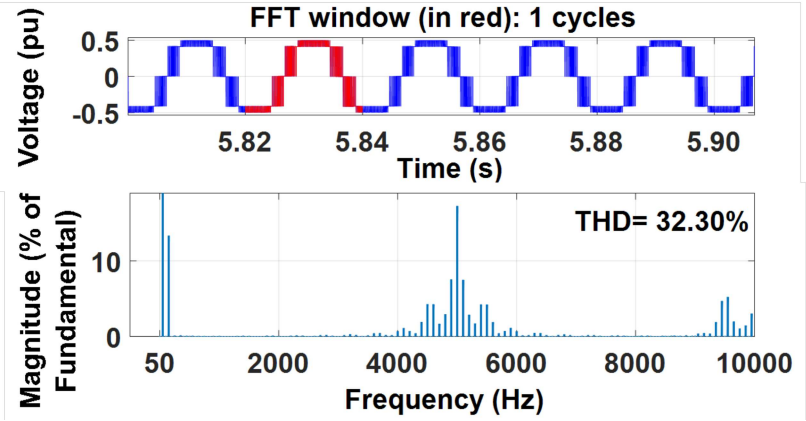

Figure 5.7: Pole Voltage in p.u. with rated DC bus voltage as base and its spectrum

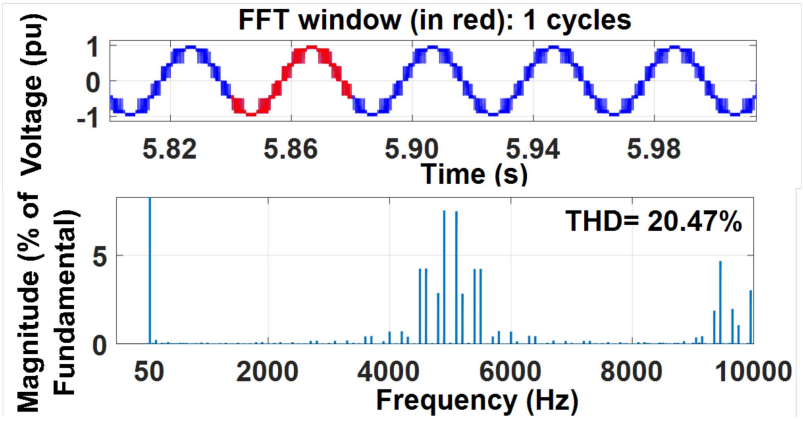

Figure 5.8: Voltage across motor winding in p.u. with rated DC bus voltage as base in open-end mode and its spectrum

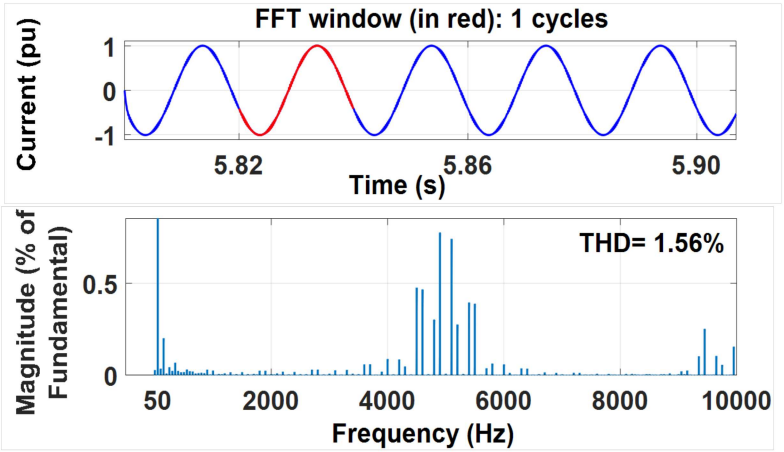

Figure 5.9: Winding current in p.u. with rated motor current as base and in open-end configuration and its spectrum

Fig. 5.9 shows the motor current and its spectrum at rated load. It can be observed that all lower harmonics of motor current including 3rd are negligible, supporting the theory that the proposed PWM strategy can restrict the flow of circulating current created by CMV. THD of motor current at rated load calculated up to twice the switching frequency is 1.56%.

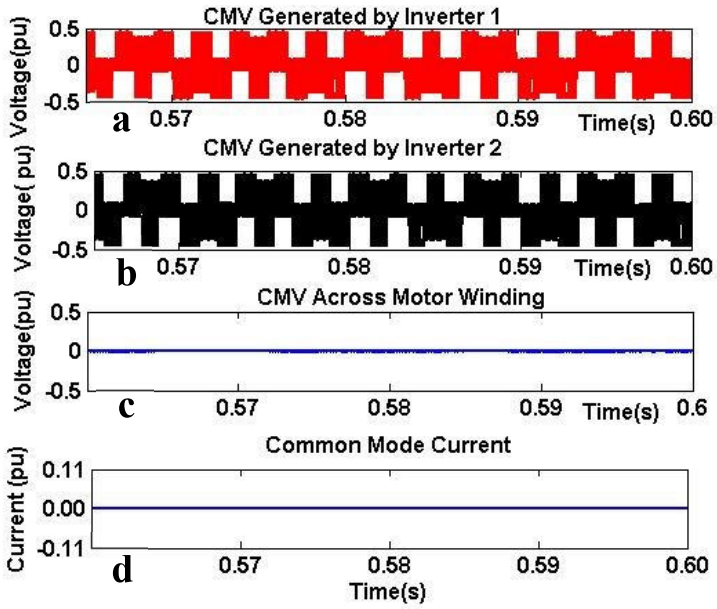

Figure 5.10: a) CMV generated by VSI-1 (b) CMV generated by VSI-2 (c) CMV across motor winding (d) Common mode current through the motor winding

Fig. 5.10(a) and Fig. 5.10(b) show the CMV generated by both the VSIs. Since the fundamental voltages generated by the two VSIs are mutually phase-shifted by 120°, the CMV produced by both the VSI has a mutual phase shift of 360° and hence becomes cophasal. Since the same PWM scheme and same DC bus voltage are used for both the VSI, the instantaneous CMV produced by both the VSIs is the same. Thus, CMV generated across motor winding shown in Fig. 5.10(c) and the resulting common mode current shown in Fig. 5.10(d) is zero. It can be inferred from the simulation result that CMV across the winding of an OEIM drive can be eliminated by creating a 120° phase shift between the fundamental components of two VSI across the winding even if the voltage steps are not equal.

5.9.2 Experimental Results

Two 5-level NPC VSIs are used to drive an OEIM from a common DC bus. The input DC is provided from a regulated DC power supply and the boost voltage is generated by the sub-converters of the proposed DC-DC converter as described in section 5.3. A carrier-based PWM scheme as explained in section 5.7 is implemented in TMS320f28335ez DSP and 12 PWM signals are generated for the switches. An external circuit generates the complementary signals along with a dead time of 4μs. The photograph of the experimental setup is shown in Appendix C.

Input DC voltage is divided into two equal parts using a capacitor voltage divider. Equal voltages are maintained across both the capacitors by the capacitor voltage balancing

algorithm without deviation of capacitor voltages which is already elaborately discussed in the section 5.6. If the voltage balancing algorithm is manually deactivated at t_1, the capacitor voltages diverge from the balanced condition as shown in Fig. 5.11. When the algorithm is reactivated at t_2, the capacitor voltages again converge to half of input DC bus, thus validating the balancing scheme.

The capacitor voltage balancing scheme is experimentally validated under different transient operating conditions viz., sudden change in (i) input voltage, (ii) switching frequency, (iii) operating frequency, and (iv) motor speed

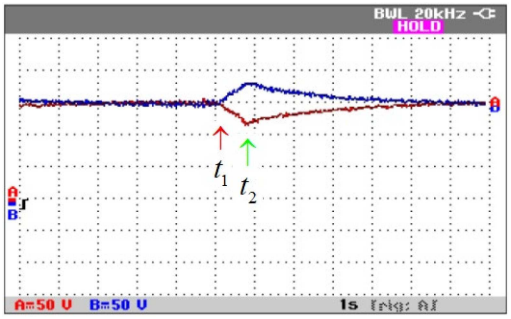

Figure 5.11: Capacitor Voltage Balancing with and without Balancing Loop

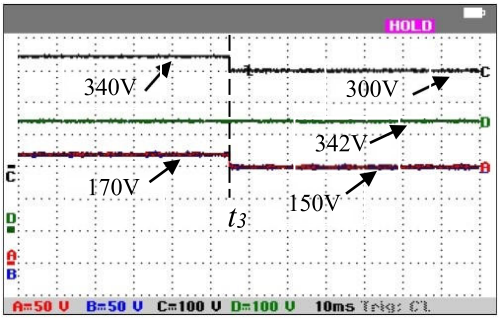

Figure 5.12: Experimental result of capacitor voltage balancing during sudden change in input voltage; Capacitor Voltage C1 & C2 (Trace A in Red and Trace B in Blue), input voltage (Trace C in Black) & Total DC voltage (Trace D in Green)

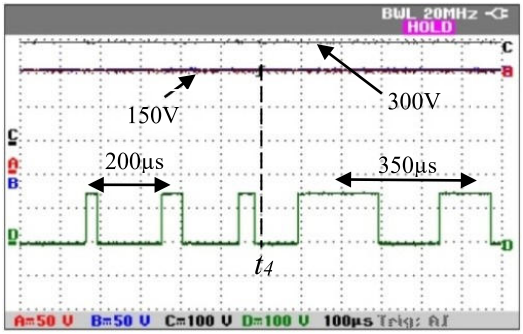

Figure 5.13: Experimental result of capacitor voltage balancing during change in switching frequency; Capacitor Voltage C1 & C2 (Trace A in Red and Trace B in Blue), Total input voltage (Trace C in Black) & Output voltage (Trace D in Green)

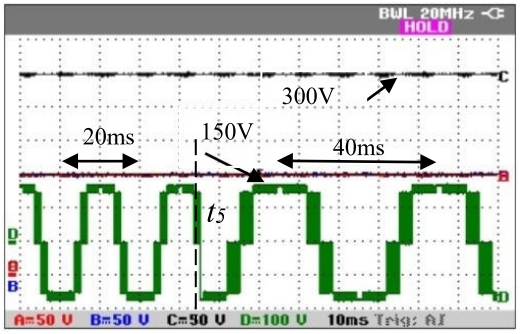

Figure 5.14: Experimental result of capacitor voltage balancing during sudden change in operating frequency; Capacitor Voltage (Trace A in Red and Trace B in Blue), Total input voltage (Trace C in Black), Pole voltage of Five level VSI (Trace D in Green)

Fig. 5.12 shows the performance of the proposed scheme during change in input voltage. The supply voltage is reduced suddenly at $t=t_3$ from 340V to 300V, depicted as Trace C (in black). Trace A and Trace B shows the voltage across the two capacitors remaining balanced during such voltage change along with the constant total DC voltage (Trace D: green).

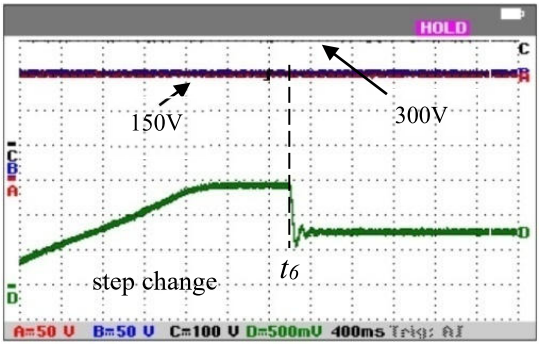

Figure 5.15: Experimental result of capacitor voltage balancing during dynamic speed change; Capacitor Voltage C1 & C2 (Trace A in Red and Trace B in Blue), Total input voltage (Trace C in Black) & Dynamic change in speed (Trace D in Green)

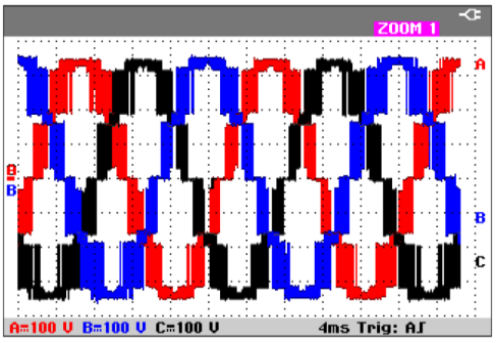

Figure 5.16: Voltage across the motor windings

In Fig. 5.13 the switching frequency of the VSI is changed from 5kHz to 2.85kHz at $t=t_4$. It can be observed that both the capacitor voltages (Trace A & Trace B) are balanced and are of equal magnitude during change in switching frequency.

In Fig. 5.14, Trace D shows the pole voltage of one leg of the inverter. At $t=t_5$, the operating frequency is changed from 50Hz to 25Hz and accordingly the fundamental period of the pole voltage changes from 20ms to 40ms as depicted in Fig. 5.14. However, from Trace A and Trace B it can be observed that both the capacitors maintain equal voltage at half of the input DC voltage (Trace C).

In Fig. 5.15, Trace D (Green) shows the motor speed during starting and step change in speed. The motor initially accelerates to its rated speed. At $t=t_6$, the speed is reduced to half of the rated value. During such dynamic speed changes, the capacitor voltages remain balanced and maintains equal voltage at 150V each (Trace A & Trace B).

Fig. 5.16 presents the experimental results for the voltage across motor winding and its spectrum is shown in Fig. 5.17. From the spectrum analysis, it can be seen that all lower-order harmonics including 3rd are absent in the voltage across the motor winding. The

fundamental voltage that is generated across the motor winding at modulation index of 0.95 is 224V. Thus, the DC bus utilization in the proposed scheme is 224/(0.95×342)×100=68.94%. This is approximately 1.8% less than the theoretical maximum limit of 70.70% and is caused by voltage loss due to dead time and device drop. The THD of voltage across motor winding measured up to switching frequency is 16.49% and the Weighted THD (WTHD) measured up to 50th order is 0.14%.

The OEIM drive is loaded to draw rated current. Fig. 5.18 & Fig. 5.19 show the 3-phase winding currents at rated load and its spectrum up to twice the switching frequency. From these, it can be observed that all harmonics up to twice the switching frequency are negligible. THD of the motor current calculated up to twice the switching frequency is 0.24%.

The pole voltages of all three legs of VSI-1 are acquired in real time and CMV produced by VSI-1 (V_{1CMV}) is calculated:

$$V_{1CMV} = (1/3)(V_{1a} + V_{1b} + V_{1c}) \tag{5.35}$$

Where V_{1a}, V_{1b}, and V_{1c} are the pole voltages produced by VSI-1. Fig. 5.20 (i) shows the experimental results of CMV produced by VSI-1. Similarly, pole voltages of all the three legs of VSI-2 are obtained and CMV produced by VSI-2 is calculated and plotted in Fig. 5.20 (ii). From these figures, it can be seen that the instantaneous CMV produced by both the VSI are identical.

The RMS value of CMV produced by both the VSI is approximately 82.4V. The voltages across the three motor windings are also acquired in real-time and the CMV across the winding is calculated and plotted in Fig. 5.20 (iii) which confirms that the CMV across the motor winding is almost zero. RMS value of CMV that appears across the motor winding is 2.3V, which is negligible.

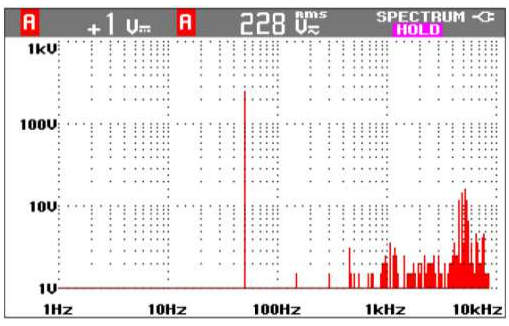

Figure 5.17: Spectrum of Voltage across the motor winding

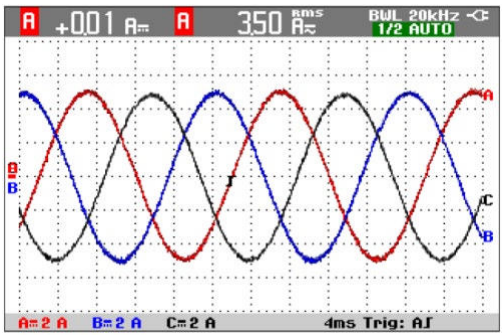

Figure 5.18: Motor Current at rated load

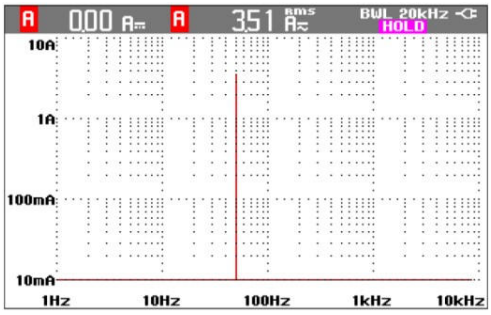

Figure 5.19: Motor current spectrum upto twice the switching frequency

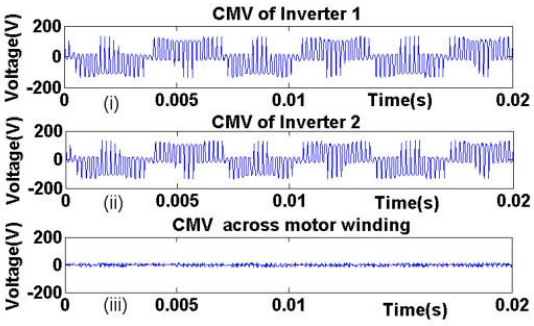

Figure 5.20: Experimental results of (i) CMV of VSI-1 (ii) CMV of VSI-2 (iii) CMV across motor winding

5.10 Efficiency Calculation

The power loss in the semiconductor devices of the proposed 5-level NPC VSI consist of two parts: conduction loss and switching loss. The instantaneous conduction loss for each of the device is given by:

$$p_{on} = \left[V_{ot} + R_{on} \left| i_L \right|\right] \left| i_L \right| \tag{5.36}$$

Where V_{ot} is the threshold voltage and R_{on} is the equivalent ON state resistance of the device. In (5.37) i_c is the load current and neglecting the harmonics, it can be approximated as:

$$i_c = I_m m \cos(\omega t - \phi) \tag{5.37}$$

The average conduction loss of a given switch in an interval [x~y] can be expressed as:

$$P_c = \frac{1}{2\pi} \int_x^y p_c D \, d(\omega t) \tag{5.38}$$

Where, D is the duty ratio of the conducting device in the interval [x~y], while x & y are the start and the end of conduction state of each IGBT. Similar approach is used for calculating the conduction loss of the DC-DC converter.

Switching losses occurs in IGBT and in the anti-parallel diodes. The turn on process of the diode is much faster compared to IGBT and hence diode turn on losses is neglected. The average turn off loss for diode and average turn on & turn off loss for each IGBT switch can be calculated as:

$$P_{D\_sw} = \frac{1}{2\pi} \int_0^{2\pi} E_{rev} . \left| i_c \right| f_c d\theta \tag{5.39}$$

$$P_{IGBT\_sw} = \frac{1}{2\pi}\int_{0}^{2\pi}\left(E_{on}+E_{off}\right)|i_c|\,f_c\,d(\omega t) \tag{5.40}$$

where f_c is the carrier frequency for the 5-level VSI. E_{rev} is the reverse recovery energy coefficient for the diode, E_{on} & E_{off} are the turn on and turn off energy coefficient for the IGBT.

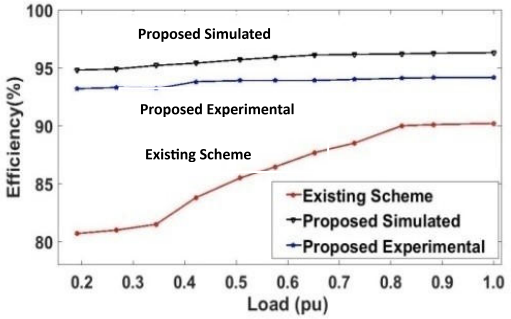

Figure 5.21: Comparative study of efficiency of the proposed scheme and existing similar boost inverter topology

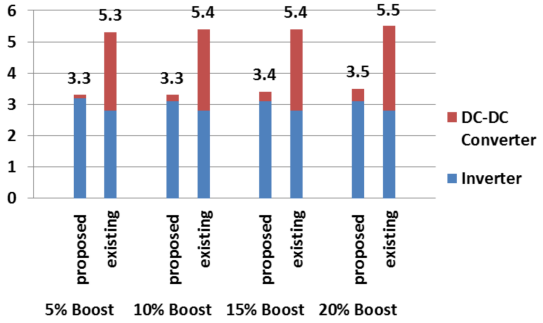

Figure 5.22: Power loss distribution between DC-DC converter and inverter for different values of voltage boost

The losses in 5-level VSI and DC–DC converter are evaluated from a simulation study in PSIM software and experimental validated in the laboratory prototype. Fig. 5.21 shows a graphical comparison between efficiency of the proposed topology and one existing 5-level topology [118]. From Fig. 5.21, it is seen that the loss in proposed topology is much small compared to existing topologies with similar operation.

Fig. 5.22 shows the distribution of power loss between the proposed DC-DC converter and inverter for different voltage boost. In the proposed scheme, only a small fraction of the total power flows through the proposed DC-DC converter and hence the power loss in the proposed DC-DC converter is smaller than the existing topologies where full power flows through the input DC-DC converter.

5.11 Comparative Study

Table 5.1 shows a comparison of proposed topology with existing multilevel topologies. Although the proposed topology requires larger number of switches compared to topologies presented in [118] and [119], the Total Standing Voltage (TSV) of these topologies is significantly higher than proposed topology. This restricts the use of these topologies in medium voltage application as the boost stage in these carries the full power and as a result

the efficiency of these topologies is lower than that of the proposed topology where only a part of the total power flows through the proposed DC–DC converter.

The number of devices and TSV of the proposed topology is comparable with different topologies suitable for MV high power drive [120]-[122]. Efficiency of the topologies reported in literature [121], [122] is marginally higher compared to that of the proposed topology. However, the topologies with better efficiency do not have voltage boost capability. When voltage boosting capability is incorporated, the efficiency of the proposed scheme is found to be better than the existing topology [104].

Table 5.1 Table showing the comparison of proposed converter with Existing topologies

Topology	Number of Levels	V_{dc} (kV)	Devices per phase	No. of Capacitors	Boosting feature	TSV	CMV	Control Complexity	PWM technique	Application	Reported Rated Efficiency
Hybrid [118]	5 level, 1-phase	0.31	6	2	Dynamic	$6V_{dc}$	--	Low	Nearest level control	Grid integration of RE	90% @ 300W
Hybrid [119]	9 Level, 1-phase	0.18	12	4	Yes	$8V_{dc}$	Low	Medium	Modified PDSPWM	Solar PV	96.5% @500W
Open end NPC [120]	9 Level, 3-phase	0.32	16	4	No	$2V_{dc}$	Zero	High	SV-PWM	----	----
Open end CHB [121]	19 level, 3-phase	0.64	18	10	No	$2.25V_{dc}$	Low	High	Level Shifted SPWM	Motor Drive	97.5% at 2.8kW
MMC [122]	7 level, 3-phase	7	16	24	No	$2V_{dc}$	--	High	Phase-shift PWM	Medium Voltage Drive	97.75@ 1MVA
IMMC [104]	--	16	-	8	Yes	--	--	--	--	Solar	95.2%@1MVA
Proposed	9 level, 3-phase	7	16	4	Dynamic	$2.15V_{dc}$	Zero	Low	CB-PWM	Medium Voltage Drive	96.8% @1MVA

5.12 Conclusion

The work proposes a boost inverter topology for medium voltage high power application in open end configuration. A 5-level NPC topology is selected so that multiple lower voltage rated device can be used to block the required DC link voltage of the drive. A further reduction in the voltage as well power rating of individual switches is obtained by using an open end configuration where two 0.5pu rated inverters are used to drive the motor. To

maintain the DC link voltage to the desired value despite of fluctuation of input AC supply, voltage boosting of DC link using the proposed DC-DC converter is proposed (see Fig. 5.2, section 5.1). The DC-DC sub-converters of the proposed DC-DC converter have a power rating each of 7.5% of the motor and hence can be realized using commercially available devices for medium voltage high power application. Common mode current circulating through the motor windings is a typical problem in open end topology with single DC bus.

In the proposed scheme the four DC buses for the 5-levels VSI are unequal and hence existing techniques for operating OEIM from single DC source cannot be applied. Thus, a carrier based PWM technique is proposed in this scheme to restrict the flow of common mode circulating current where the voltage step produced by the 5-level VSI are unequal. Simulation results supported by experiments on a laboratory prototype show that the proposed scheme for transformer-less OEIM drive is able to maintain DC link voltage at its rated value despite of drop in supply voltage. Harmonic analysis of winding voltage and current validates that CMV and circulating current due to CMV can be eliminated even though the voltage step heights are unequal.

Chapter 6

Conclusion & Future Scope

6.1 Conclusion

In this thesis a non-isolated DC-DC converter topology is proposed for boosting the available DC voltage with improved efficiency compared to existing solutions. The converter is suitable for application in non-conventional energy power sources or for multi-level inverters for drive system. The topology comprises of two buck-boost DC-DC sub-converters, arranged such that there is addition of individual output to either side of the input DC voltage bus without the utilization of any transformer. Interleaving the switching operation with 180° phase shift between the sub-converters creates considerable reduction in input current ripple due to parallel operation at input as well as output voltage ripple due to series operation at output. Since part of the load power flows in directly from the input, each sub-converter does not process the entire output power. This results in minimizing the current & voltage ratings of the semiconductor devices, improving the overall system efficiency. A higher voltage boost is generated than conventional DC-DC boost converter for identical duty cycle. Due to the symmetrical addition of voltages on both sides of the incoming DC bus, the proposed converter can be used to create multiple DC voltage levels for multilevel inverters.

The Continuous Conduction Mode (CCM) and the Discontinuous Conduction Mode (DCM) are studied and analyzed in details. Simulation and experimental study verifies the practicality of the proposed scheme with improved performance.

The thesis also presents the application of the proposed converter in an energy efficient 5-level NPC inverter based boost inverter topology for transformer-less medium voltage high power OEIM drive. A conventional boost circuit cannot be used in such drives as single semiconductor device may not be able to block the total DC link voltage and simultaneously carry full load current. In the proposed scheme, two partly rated DC-DC sub converters of the proposed DC-DC converter which generate only the required boost fraction of the voltage are connected in either ends of the input DC bus. The input DC is divided into two equal parts using a capacitor voltage divider circuit. These four effective voltage sources in

cascade serve as the four DC bus for the two five level NPC VSI of the OEIM drive. A substantial amount of power directly flows to the inverter through the capacitor voltage divider circuit and hence the size as well as power loss of the proposed DC-DC boost converter scheme is much smaller. The voltage generated from the DC-DC sub-converters is lower than the voltage in the capacitor voltage divider circuit, creating unequal step heights in the pole voltage of the 5-level NPC VSI. These unequal steps in the pole voltage of the two VSI of open end drive restrict the use of existing technique for operating an OEIM drive from a single DC source. In this article, a carrier based PWM technique is proposed to restrict the circulating current caused by CMV even when the voltage steps are unequal.

6.2 Future Scope

The proposed boost converter can be applied to boost the output voltage from a solar PV panel. The output DC bus may be fed to a grid connected inverter system for feeding power into the grid. The MPPT may be incorporated either in the DC-DC converter or in the inverter and the dynamics of the overall system studied. Due to the symmetrically balanced output voltage created over the SPV voltage, such a scheme is likely to be well suited for transformer-less applications when connected to the grid.

The proposed boost converter in cascade with an inverter may also be studied for boost inverters, as an alternative to the Z-source inverter. However, total losses and stability of the two systems are to be studied in details.

Analysis of fault tolerant performance of the proposed converter may be carried out in case one of the power switches or diodes or inductors fail in the open circuit mode or the switch gate driver fails. In such a case, unlike the conventional boost converter, the proposed converter can continue operation but without the capability to provide a boosted voltage.

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PUBLICATIONS

Journal

1. **K. Sarkar**, A. Chakrabarti, P. Kasari, B. Das and S. K. Biswas, "Performance Improved Multi-Level OEIM Drive with Voltage Boost through Unequal Levels", *IEEE Transactions on Industry Applications*, Early Access, DOI: 10.1109/TIA.2023.3290574.

2. A. Chakrabarti, **K. Sarkar**, P. Kasari, B. Das and S. K. Biswas, "A CB-PWM Technique for Eliminating CMV in Multilevel Multiphase VSI", *IEEE Transactions on Industrial Electronics*, Vol. 70, Iss. 9, September 2023, DOI: 10.1109/TIE.2022.319825.

Conference

1. **K. Sarkar**, A. Chakrabarti, and S. K. Biswas, "A Five-Level Boost NPC Inverter for Electric Vehicle," IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES), MNIT Jaipur, India, Dec. 2020, DOI: 10.1109/PEDES49360.2020.9379599.

2. A. Chakrabarti, **K. Sarkar**, and S. K. Biswas, "Generalized Carrier Based Technique for Eliminating CMV in 3-Phase n-level NPC Inverter," IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES), MNIT Jaipur, India, Dec. 2020, DOI: 10.1109/PEDES49360.2020.9379889.

Appendix-A

A.1 The photograph of the PCB board of the control circuit for the proposed converter is shown in the Fig. B.1 (Section 2.8, Chapter 2).

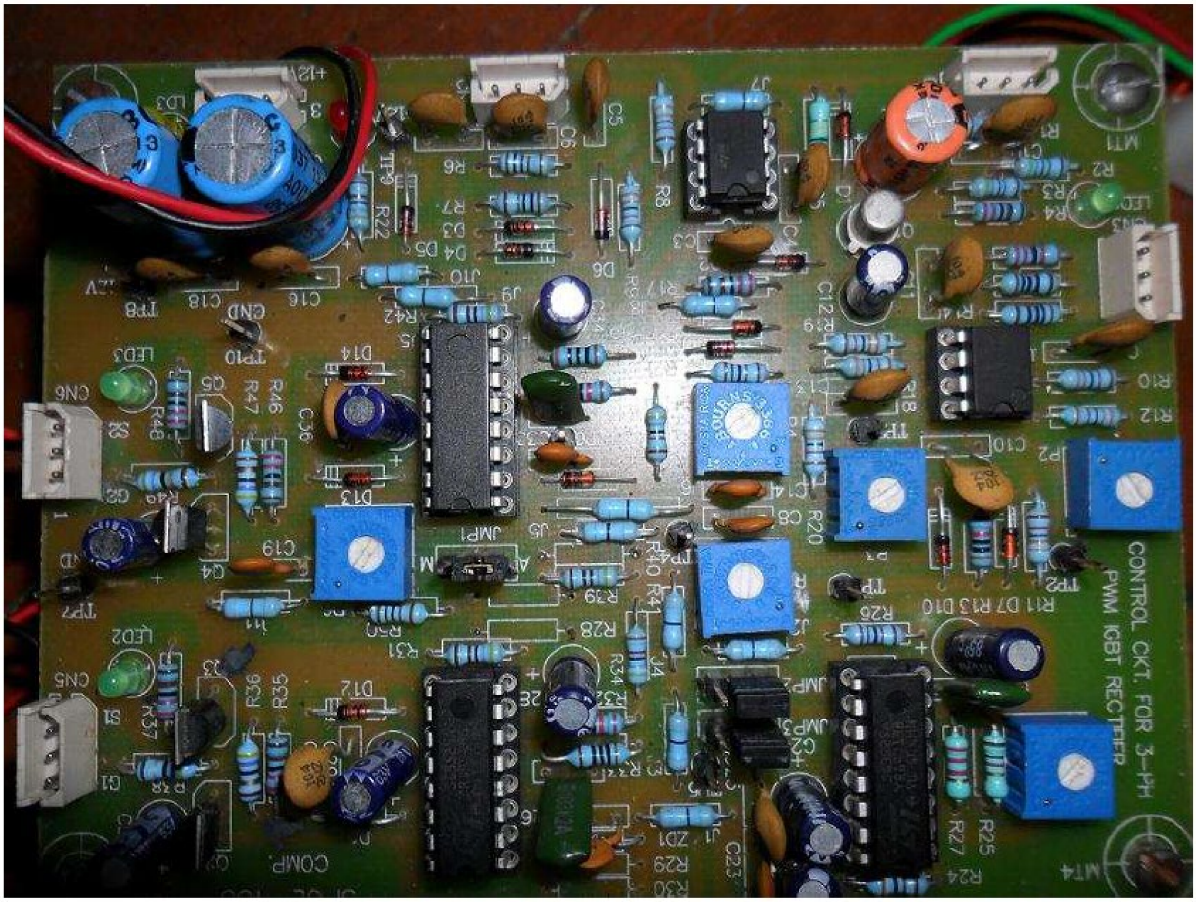


Figure A.1: Control Circuit PCB

A.2 The MOSFET selected for performing the experiment has the following specifications: (Section 3.4.1, Chapter 3).

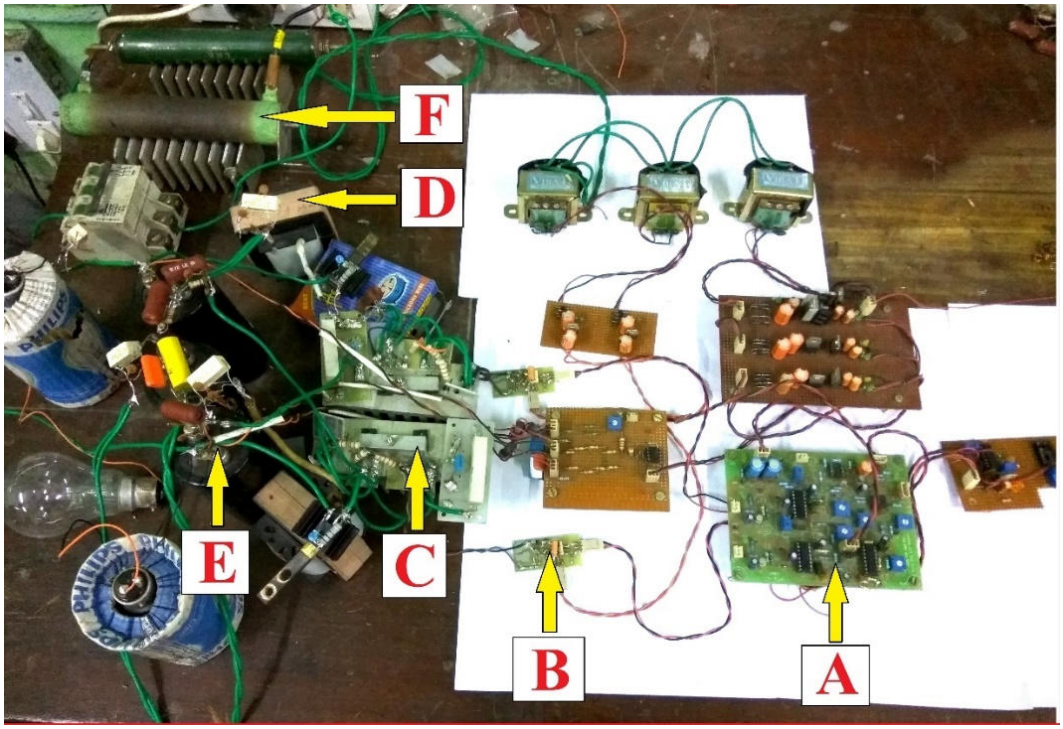
Silicon N-channel MOSFET- **TK10A80E** [123].

Sl. No.	Particulars	Value
1.	Drain Source ON Resistance $(R_{DS_{(on)}})$	0.7Ω
2.	Leakage Current (I_{DSS})	$10\mu A$ (max)
3.	Drain Current (I_D)	$10A$
4.	Drain Source Voltage (V_{DSS})	$800V$
5.	Power Dissipation (P_D) (25^0C)	$50W$

A.3 The diode selected for the operation of the proposed DC-DC converter has the following specifications: Soft Recovery Ultrafast Plastic Rectifier- **UF5400** [124]. (Section 3.4.2, Chapter 3)

Sl. No.	Particulars	Value
1.	Maximum average forward rectified current, $I_{F(AV)}$	$3.0A$
2.	Maximum repetitive peak reverse voltage, V_{RRM}	$50V$
3.	Maximum reverse recovery time, t_{rr}	$50ns$
4.	Maximum instantaneous forward voltage, V_F	$1.0V$
5.	Operating junction, T_J	-55 to +150 ^0C

A.4 The picture for the laboratory prototype comprising of both the power circuit as well as the control circuit of the proposed DC-DC converter shown: (Section 3.7, Chapter 3).



A-Control Circuit B-Gate Driver C-MOSFET
D-Inductor E-Capacitor F-Resistive Load

Figure A.4: View of the laboratory experimental setup (Proposed DC-DC converter)

Appendix-B

B.1 The MATLAB code for Bode plot for all the three duty cycles chosen for the proposed DC-DC boost converter is shown: (Section 3.5.2, Chapter 3).

```
s=tf ('s');
Vi=110;
La=0.85*10^-3;
C=1000*10^-6;
Ila=9.334;
Ro=317.38;
Lb=0.85*10^-3;
Ilb=9.334;
D1=0.7;
D2=0.5;
D3=0.3;
a=Vi/(La*C);
b=Ila/C;
c=1/(Ro*C);
d=((1-D1) *(1-D1))/(La*C);
dd=(a-b*s)/(s^2+s*c+d);
e=Vi/(Lb*C);
f=Ilb/C;
g=((1-D1) *(1-D1))/(Lb*C);
gg=(e-f*s)/(s^2+s*c+g);
sys1=dd+gg;
h=((1-D2) *(1-D2))/(La*C);
hh=(a-b*s)/(s^2+s*c+h);
i=((1-D2) *(1-D2))/(Lb*C);
ii=(e-f*s)/(s^2+s*c+i);
sys2=hh+ii;
j=((1-D3) *(1-D3))/(La*C);
jj=(a-b*s)/(s^2+s*c+j);
k=((1-D3) *(1-D3))/(Lb*C);
kk=(e-f*s)/(s^2+s*c+k);
sys3=jj+kk;
bode (sys1, sys2, sys3);
```

B.2 The MATLAB code for Pole Zero map for the transfer function (for a particular duty cycle) for the proposed DC-DC boost converter is shown: (Section 3.5.2, Chapter 3).

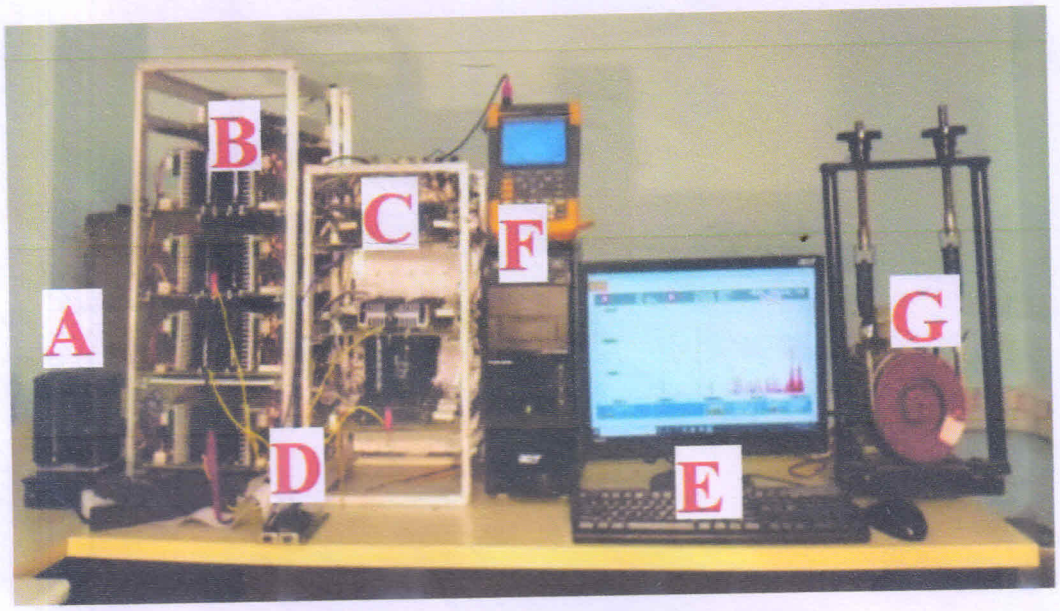
```
s=tf ('s');
Vi=110;
La=0.85*10^-3;
C=1000*10^-6;
Ila=9.334;
Ro=317.38;
Lb=0.85*10^-3;
Ilb=9.334;
D1=0.7;
a=Vi/(La*C);
b=Ila/C;
c=1/(Ro*C);
d=((1-D1) *(1-D1))/(La*C);
dd=(a-b*s)/(s^2+s*c+d);
e=Vi/(Lb*C);
f=Ilb/C;
g=((1-D1) *(1-D1))/(Lb*C);
gg=(e-f*s)/(s^2+s*c+g);
sys1=dd+gg;
pzmap(sys1);
grid on;
```

Appendix-C

C.1 Table C.1: Parameters for Simulation & Experimental Study (Section 5.9, Chapter 5)

Sl. No.	Parameter	Simulation	Experimental
1.	Input voltage range	6100-7000V	298-342V
2.	Total DC voltage	7000V	342V
3.	Rated power of 3-phase IM	1000kW	2 kW
4.	Rated winding voltage	2400V	230V
5.	Rated winding current	150A	3.7A
6.	Rated fundamental frequency	50Hz	50Hz
7.	No. of poles	4	4
8.	Rated kVA of 5-level VSI	500kVA	5kVA
9.	Switching frequency	5kHz	5kHz
10.	Rated power of the boost stages DC-DC Converter	75kW	500W
11.	Max input voltage of DC-DC converter	7000V	350V
12.	Boost Output voltage of DC-DC converter	0-525V	0-25V
13.	Switching frequency of DC-DC converter	15kHz	15kHz
14.	Current controller K_{cp}	0.000166	0.0498
15.	Current controller K_{ci}	0.037072	7.414
16.	Voltage controller K_{vp}	0.048	16.8
17.	Voltage controller K_{vi}	1.3341	333.35
18.	Capacitor for each boosted stage of DC-DC converter	3000μF	470μF

C.2 The photograph of the experimental setup explained in Chapter 5 is shown: (Section 5.9.2, Chapter 5)



A: DC-DC converter
B & C: VSI-1 & VSI-2
D: DSP
E: Host PC
F: Digital oscilloscope
G: Motor under test

Figure C.2: Photograph of the experimental setup (Proposed 5-level NPC VSI base OEIM drive)

Kaustav Sarkar