NATURAL MITIGATION OF VOLTAGE HARMONICS IN INVERTERS WITH HIGH DC BUS UTILIZATION

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ABSTRACT

Switching inverters are used to supply loads which normally require a sinusoidal voltage waveform. Any harmonic present in the supply from the inverter causes the flow of harmonic currents through the load, resulting in undesired behaviour from the load and additional kVA loading of the inverter. However, high efficiency power electronic inverters produce only flat-topped waveforms with sharp voltage rise and fall due to the switching mode of operation of the power semiconductor switches. Thus, additional low-pass filters are required at the inverter output to filter out the harmonic content in the generated voltage and deliver only the fundamental waveform to the load. However, filters only attenuate the harmonics and hence a large size of filter is often needed to bring down the Total Harmonic Distortion (THD) of the inverter voltage waveform to acceptable limits. Alternatively, special Pulse Width Modulation (PWM) schemes are used, that generate reduced voltage harmonics at the cost of reduced fundamental voltage output (reduced DC bus utilization).

Some researchers have demonstrated that instead of using a bulky filter, an additional power converter circuit can be connected in series with the inverter output to reduce its harmonic content. This additional circuit can be designated as a harmonic compensator, which generates exactly the same amount of harmonics present in the inverter output, but in phase opposition. Thus, the resulting final output to the load is free of harmonics. However, the additional converter requires an isolated power supply, being another switching power stage. As a result, several research work has been directed towards development of a power stage that does not require an additional power supply and the concept of Natural Compensation of harmonic voltages is an attractive issue.

The work envisaged in this thesis is directed towards investigating the techniques of Natural Mitigation of harmonics along with achieving higher fundamental voltage compared to the conventional schemes using Sinusoidal Pulse Width Modulation (SPWM). A new fixed frequency single phase sine wave inverter topology is investigated, having high DC bus utilization. The main inverter uses six IGBT switches operating at low frequency in over-modulation mode to create a five stepped voltage waveform, thus having low switching losses with high DC bus utilization. A series connected active compensator using power MOSFETs helps to remove the major harmonic voltages. No isolated DC power supply is required across the compensator as it is based on the principle of natural compensation. The DC bus voltage needed for the compensator is about half of the inverter, thus the compensator has low switching loss even at the designated switching frequency.

A three phase inverter system is investigated which produces a near sinusoidal three phase voltage output at fixed fundamental frequency with low switching loss. Since the inverter system comprises of fixed waveform, it is not possible to control the output voltage other than by adjusting the DC bus voltage of main inverter. However, introduction of low frequency Pulse Width Modulation permits output voltage adjustment within the inverter. Thus a new three phase inverter system at over-modulation with SPWM control scheme along with compensator is investigated to get high dc bus utilization and low THD. The switching frequency components of the compensator remains in the output as they are not compensated, necessitating the use of a small filter at the output to attenuate them. Thus the use of higher switching frequency in the compensator permits the use of a small filter at the output to attenuate the switching frequency components.