NATURAL MITIGATION OF VOLTAGE HARMONICS IN INVERTERS WITH HIGH DC BUS UTILIZATION

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Dedicated

To My Husband

ABSTRACT

Switching inverters are used to supply loads which normally require a sinusoidal voltage waveform. Any harmonic present in the supply from the inverter causes the flow of harmonic currents through the load, resulting in undesired behaviour from the load and additional kVA loading of the inverter. However, high efficiency power electronic inverters produce only flat-topped waveforms with sharp voltage rise and fall due to the switching mode of operation of the power semiconductor switches. Thus, additional low-pass filters are required at the inverter output to filter out the harmonic content in the generated voltage and deliver only the fundamental waveform to the load. However, filters only attenuate the harmonics and hence a large size of filter is often needed to bring down the Total Harmonic Distortion (THD) of the inverter voltage waveform to acceptable limits. Alternatively, special Pulse Width Modulation (PWM) schemes are used, that generate reduced voltage harmonics at the cost of reduced fundamental voltage output (reduced DC bus utilization).

Some researchers have demonstrated that instead of using a bulky filter, an additional power converter circuit can be connected in series with the inverter output to reduce its harmonic content. This additional circuit can be designated as a harmonic compensator, which generates exactly the same amount of harmonics present in the inverter output, but in phase opposition. Thus, the resulting final output to the load is free of harmonics. However, the additional converter requires an isolated power supply, being another switching power stage. As a result, several research work has been directed towards development of a power stage that does not require an additional power supply and the concept of Natural Compensation of harmonic voltages is an attractive issue.

The work envisaged in this thesis is directed towards investigating the techniques of Natural Mitigation of harmonics along with achieving higher fundamental voltage compared to the conventional schemes using Sinusoidal Pulse Width Modulation (SPWM). A new fixed frequency single phase sine wave inverter topology is investigated, having high DC bus utilization. The main inverter uses six IGBT switches operating at low frequency in over-modulation mode to create a five stepped voltage waveform, thus having low switching losses with high DC bus utilization. A series connected active compensator using power MOSFETs helps to remove the major harmonic voltages. No isolated DC power supply is required across the compensator as it is based on the principle of natural compensation. The DC bus voltage needed for the compensator is about half of the inverter, thus the compensator has low switching loss even at the designated switching frequency.

A three phase inverter system is investigated which produces a near sinusoidal three phase voltage output at fixed fundamental frequency with low switching loss. Since the inverter system comprises of fixed waveform, it is not possible to control the output voltage other than by adjusting the DC bus voltage of main inverter. However, introduction of low frequency Pulse Width Modulation permits output voltage adjustment within the inverter. Thus a new three phase inverter system at over-modulation with SPWM control scheme along with compensator is investigated to get high dc bus utilization and low THD. The switching frequency components of the compensator remains in the output as they are not compensated, necessitating the use of a small filter at the output to attenuate them. Thus the use of higher switching frequency in the compensator permits the use of a small filter at the output to attenuate the switching frequency components.

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List of Abbreviation

VSI	Voltage Source Inverter
CSI	Current Source Inverter
FFT	Fast Fourier Transform
AC	Alternating Current
DC	Direct Current
ASD	Adjustable Speed Drive
UPS	Uninterruptible Power Supply
RMS	Root Mean Square
IGBT	Insulated Gate Bipolar Transistor
EMF	Electro Motive Force
PWM	Pulse Width Modulation
HB	Half Bridge
FB	Full Bridge
EMI	Electro Magnetic Interference
SVM	Space Vector Modulation
SPWM	Sine Pulse Width Modulation
SCR	Silicon Controlled Rectifier
VFD	Variable Frequency Drive
EMC	Electro Magnetic Compatibility
CM	Common Mode
SHE	Selective Harmonic Elimination

THD	Total Harmonic Distortion
IM	Induction Motor
FC	Floating Capacitor
DVR	Dynamic Voltage Restorer
OEW	Open End Winding
MV	Medium Voltage
DG	Distributed Generation
NPC	Neutral Point Clamped
ANPC	Active Neutral Point Clamped
PV	Photo Voltaic
MLI	Multilevel Inverter
LSPWM	Level Shifted Pulse Width Modulation
SiC	Silicon Carbide
TPWM	Trapezoidal Pulse Width Modulation
RC-qTPWM	Reconstructed Carrier Quasi Trapezoidal Pulse Width Modulation
CPS_PWM	Carrier Phase Shifted Pulse Width Modulation
CHB	Cascaded H Bridge
TI	Transformer less Inverter
SC	Switched Capacitor
ASHCM-PWM	Asymmetric Selective Harmonic Current Mitigation PWM
MCPWM	Multicarrier Modulation
DPWM	Discontinuous Pulse Width Modulation
PSPWM	Phase Shifted Pulse Width Modulation
PSO	Particle Swarm Optimization
PCC	Point of Common Coupling

HE	Harmonic Elimination
NLM	Nearest Level Modulation
MMC	Modular Multilevel Converter
APF	Active Power Filter
NHC	Natural Harmonic Compensator
SAPF	Series Active Power Filter
MOSFET	Metal Oxide Field Effect Junction Transistor
VAR	Volt Ampere Reactive
FACTs	Flexible AC Transmission System
VSD	Variable Speed Dive

CHAPTER – ONE

Introduction

1.1 Power Electronics Inverter System

Power Electronics involves power and electronics to convert electrical power from one form to another in a proficient, clean, regulated, and economical manner for the further consumption by end user. Inverter is the heart of power electronics which defines a type of power conversion circuit that is fed from a dc voltage source or alternatively a dc current source to either ac voltage or ac current. Even though input to an inverter circuit is a dc source, it is a very common practice to derive this dc from an available ac source like utility grid. For instance, the major source of input power can be the utility grid supply which is transferred to dc by a rectifier and then 'inverted' back to ac using an inverter. Here, the frequency and magnitude of the ac output may be different than the input ac of the utility supply. The 'inverter' operation can also be used by a rectifier circuit provided the direction of flow of power is from load to source side. Though, in this chapter, irrespective of direction of flow of power, 'inverter' is defined as a power converter which is fed from a stiff dc voltage source and transforms it into ac output voltage source. When the dc input is a voltage source, the corresponding inverter is known as voltage source inverter (VSI). If the input is a current source, the inverter is called as current source inverter (CSI). The VSI is capable of control the output voltage directly while the output current is directly controlled by the CSI.

The voltage waveform of the output of an ideal VSI should not depend on connected load at its output. A common example of dc voltage source applicable to a VSI may be a battery containing multiple cells in series-parallel mode. Solar photovoltaic arrays may be a type of dc voltage source. DC voltage derived from an ac voltage supply, through rectification is also an effective voltage source. A stiff voltage source implies that the magnitude of the source voltage is independent of load connected to it.

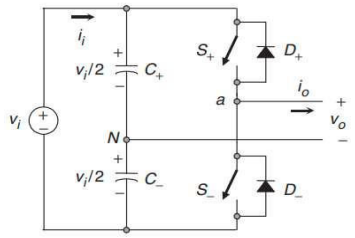
Few practical examples of voltage source inverters include uninterruptible power supply (UPS) modules, variable ac motor drives (VSD), frequency changer system etc. The commercially available models of inverter for use in our homes and work places to provide power to critical ac loads in case the unavailability of the utility grid. In these inverters, the input dc source is created by battery and the inverter circuit changes the dc into ac voltage at designated frequency. The ac voltage magnitude is controlled by the amplitude of dc input voltage. If the input dc voltage is lower than that required to meet the load voltage demand, then a step up transformer is used to meet the load demand.

1.2 Classification of Inverters

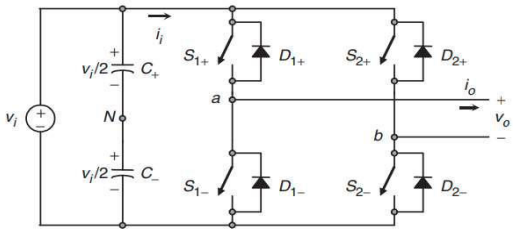
Inverters can be classified in a several ways. It can be a single-phase inverter or a three-phase inverter depending on whether the output is single-phase or 3-phase ac. As per the method of commutation it is classified as line commutated inverter and forced commutated inverter. A line commutated inverter operates with an ac system. The ac line voltage is used for commutation. As the ac voltage goes to zero crossings and reverses the polarity of voltage the thyristor is turned off. The force commutated inverters used mainly with dc system utilizes extra commutation circuit to turn off the devices. Another Classification of Inverters is as per the connections of thyristors and commutating elements such as series inverter, parallel inverter and bridge inverter. Another Classification of Inverters is voltage source inverters and current source inverters. A voltage source inverter is supplied by a constant dc voltage source while a current source inverter is excited by a constant current source.

1.2.1 Single phase Inverter

A single-phase square wave VSI generates square wave output voltage using a 1-phase load. Those inverters use simple control strategy and the power electronics devices to switch at a low switching frequency compared to some other types of inverters. The early generation inverters based on thyristors as switches, were mostly square wave inverters as thyristors had restricted switching frequency at a few hundred's of frequency. Alternately, the present day semiconductor switches like MOSFETs, IGBTs are having faster switching speed and used at switching frequencies up to few megahertz. Single-phase inverters are generally categorized as half bridge or full bridge configurations. Power circuits of these configurations are depicted in Fig. 1.1(a) and (b) for further discussions.



(a)



(b)

Fig. 1.1(a) Single-phase half bridge VSI, (b) Single-phase full bridge VSI

In this chapter, both the aforementioned configurations of inverters are illustrated assuming ideal source of voltage and ideal switches. In accordance, it is also assumed that the input dc voltage (V_i) has steady magnitude and the semiconductor switches are free of loss. In half bridge configuration the dc voltage input is divided in two equal halves across an ideal and loss-free capacitive voltage divider. The half bridge configuration contains one limb of switches whereas the full bridge topology has two such limbs. The mid-point of the semiconductor switches in each limb of the inverter acts as an output terminal for the load connection. In half bridge configuration the 1-phase load is connected across the mid-point of the input dc bus voltage and the mid-point of the two semiconductor switches as shown in Fig. 1.1(a). Such points are demarcated as 'a' and 'N' respectively. For simplicity, the semiconductor switches S_+ and S_- can be assumed to be adjusted as mechanical switches that will open and close in response to the switching signal. Now, if the switches S_+ and S_- are turned on alternately with duty ratio of 50%, the voltage across the load (V_{aN}) will become a square wave with a peak-to-peak amplitude equal to the voltage V_i of input dc bus voltage. Table 1.1 shows the switching states of 1-phase half bridge inverter.

Fig. 1.2 also shows the output voltage waveform of single phase half bridge and full bridge inverter. Fig. 1.2(a) depicts a typical waveform of load voltage supplied by a half bridge inverter. V_{aN} achieves an amplitude of $+0.5V_i$ when S_+ is on and the amplitude is $-0.5V_i$ when S_- is turned on. The two switches of the inverter limb are turned on alternatively. For a general purpose load, the switches should not be turned on turned off at the same time. Simultaneous turn-on of both the switches will make the input dc bus short circuited causing the switch currents to rise enormously. For an inductive load, one of the switches should be turned on to maintain continuous load current. For an inductive load, even though the switching frequency is very high as current cannot change instantly through an inductor. Hence, the switches must have bidirectional current carrying ability. Also Table 1.2 shows the switching states of single-phase full bridge (FB) inverter.

Table 1.1 Switching states for a HB single-phase VSI

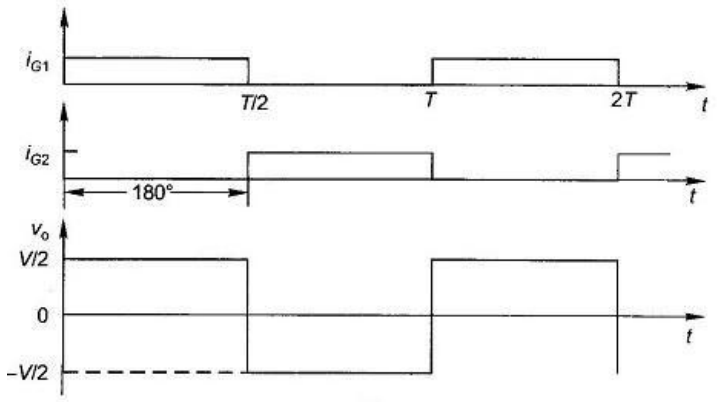
Output Voltage V_0	Switching State	Components Conducting	
$V_i/2$	S_+ is on and S_- is off	S_+	If $i_o>0$
		D_+	If $i_o<0$
$-V_i/2$	S_+ is on and S_- is off	D_-	If $i_o>0$
		S_-	If $i_o<0$
0	S_+ is on and S_- is off	D_-	If $i_o>0$
		D_+	If $i_o<0$

Table 1.2 Switch states for a full-bridge single-phase VSI

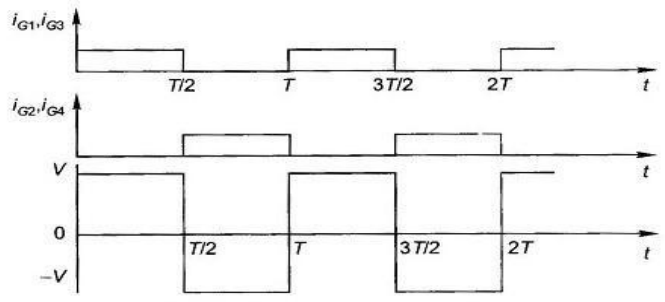
Output Voltage V_0	Switch State	Components Conducting		v_{aN}	v_{bN}
V_i	S_{1+} & S_{2-} are on & S_{1-} & S_{2+} are off	S_{1+} & S_{2-} D_{1+} & D_{2-}	If $i_o>0$ If $i_o<0$	$V_i/2$	$-V_i/2$
$-V_i$	S_{1-} & S_{2+} are on & S_{1+} & S_{2-} are off	D_{1-} & D_{2+} S_{1-} & S_{2+}	If $i_o>0$ If $i_o<0$	$-V_i/2$	$V_i/2$
0	S_{1+} & S_{2+} are on & S_{1-} and S_{2-} are off	S_{1+} & D_{2+} D_{1+} & S_{2+}	If $i_o>0$ If $i_o<0$	$V_i/2$	$V_i/2$
0	S_{1-} & S_{2-} are on & S_{1+} & S_{2+} are off	D_{1-} & S_{2-} S_{1-} & D_{2-}	If $i_o>0$ If $i_o<0$	$-V_i/2$	$-V_i/2$
V_i $-V_i$	S_{1-}, S_{2-}, S_{1+}, & S_{2+} are all off	D_{1-} & D_{2+} D_{1+} & D_{2-}	If $i_o>0$ If $i_o<0$	$-V_i/2$ $V_i/2$	$V_i/2$ $-V_i/2$

Harmonic Analysis of Load Voltage Waveforms

A square wave is the combination of several sine waves with odd multiple of the fundamental harmonics frequency. To know about the various elements of a complex waveform it is necessary to perform a spectrum (frequency) analysis. Analyzing signals may be carried out in a digital, analog or combined of both ways. Analog signal processing can be done with spectrum analyzers. It could be a group of filters having a variety of pass frequencies as well as narrow band filters that are tunable.



(a)



(b)

Fig. 1.2(a) Output of Half Bridge Inverter, (b) Output of Full Bridge Inverter

In digital signal processing, Fast Fourier Transform (FFT) is the most frequently used technique. A periodic signal is expressed by the form of a Fourier series is the equivalent of breaking down it into component functions which include the constant part a_0 as well as the harmonic components that have two factors: ω_1, 2 ω_1, 3 ω_1, …, n ω_1, where ω_1 is the fundamental content and $n\omega_1$ are the harmonic content, n is a natural number. The fundamental component is determined by the formula.

$$\omega = \frac{2\pi}{T} \qquad 1.1$$

Where, T – time period of the function

The equation expressing the periodic waveform x(t) by means of the Fourier series is given by

$$x(t) = a_0 + \sum_{n=1}^{\infty}(a_n \cos n\omega_1 t + b_n \sin n\omega_1 t) \qquad 1.2$$

The efficacy of Fourier series a_0, b_n are determined by analyzing the equation of the waveform is demonstrated based on the results of measurements made with the help of a harmonic analyzer. For example, a periodic signal that is in the form of a square waveform can be represented as an infinite trigonometric order that includes odd harmonics (1 3, 5, 7, …) with decreasing magnitudes. This is a demonstration of the signal in the time domain as shown in fig. 1.3.

$$x(t) = \frac{4A}{\pi}\left(\sin\omega_1 t + \frac{1}{3}\sin 3\omega_1 t + \frac{1}{5}\sin 5\omega_1 t + \frac{1}{7}\sin 7\omega_1 t + \ldots\right) \qquad 1.3$$

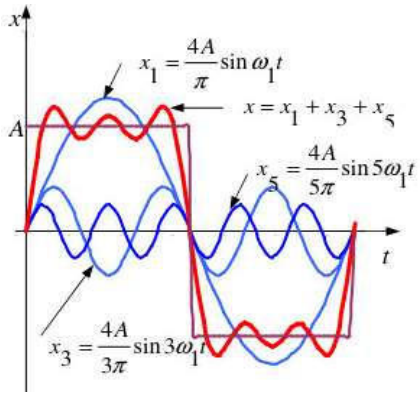


Fig. 1.3 Square waveform approximation with a limited number of harmonics

Periodic signals may also be graphically depicted within the defined frequency range. The x-axis is taken as frequency f. The length of the bars is proportional to the magnitude of the harmonics that are present in the signal being studied. The graph is referred to as the amplitude spectrum. Spectrums of the periodic signal components have discrete however (Fig. 1.4), spectrum of aperiodic signal (e.g. impulsive signal) is continuous. From the above amplitude spectrum it can be concluded that for a single phase square wave inverter, the peak amplitude of the fundamental ac output voltage is

$$\frac{4}{\pi}\frac{V_i}{2} \qquad 1.4$$

where V_i is the input dc bus voltage to the inverter.

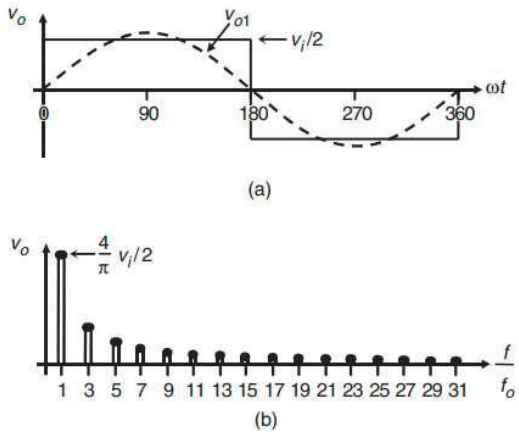


Fig. 1.4 Waveforms for ideal half-bridge voltage source inverter using square-wave modulating technique: (a) ac output voltage and (b) FFT spectrum of the output voltage

1.2.2 Three phase Inverter

The individual phase voltages w.r.t. the dc bus midpoint of the 3-phase bridge inverter are same with that of the square wave output as obtained by single-phase half bridge or full bridge inverters. Fig. 1.5 shows the power circuit of the three-phase inverter. Here, the three phase voltages are displaced in time by 120°. These phase voltages and three line voltages are shown in Fig. 1.6 (b) and (c) respectively. The horizontal axis of the waveforms in Fig. 1.6 is given in the style of 'ωt', where 'ω' is the angular frequency of the fundamental component of the square wave voltage and 't' is the time in second. Referring to Fig. 1.6 (b) & (c) the phase sequence of the phase voltages is taken as V_{aN}, V_{bN} and V_{cN}. Also Table 1.3 shows the switching states of 3-phase full bridge inverter.

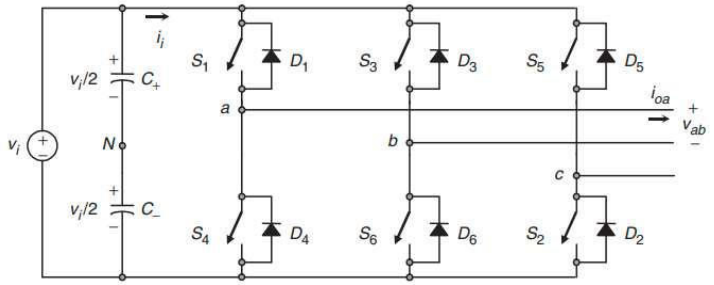
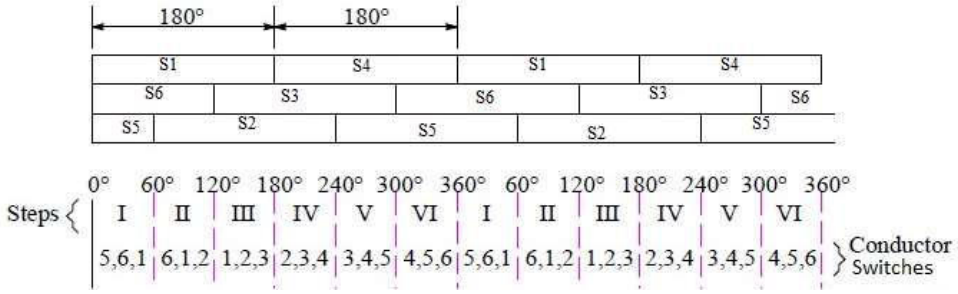


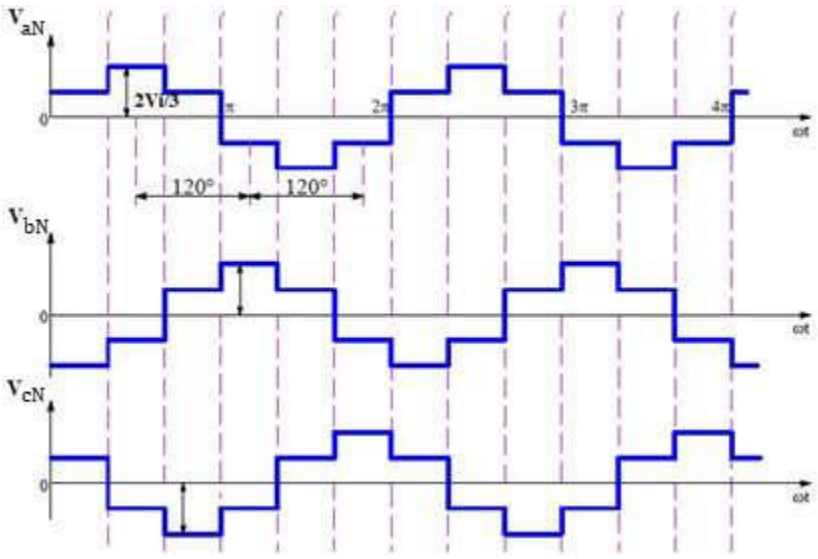
Fig. 1.5 A 3-phase Voltage Source Inverter (VSI) feeding a balanced load

Table 1.3 Switch states for a three-phase VSI

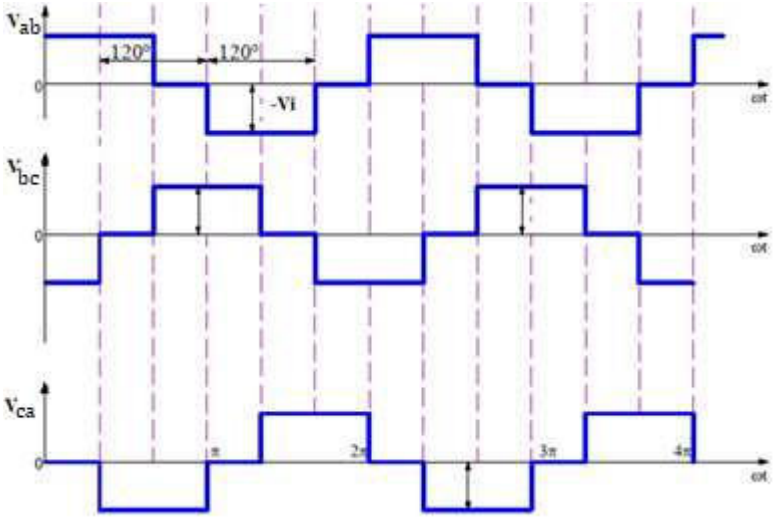
State		V_{ab}	V_{bc}	V_{ca}
On State	Off State	V_i	0	$-V_i$
S_1,S_2,S_6	S_4,S_5,S_3	0	V_i	$-V_i$
S_2,S_3,S_1	S_4,S_5,S_6	$-V_i$	V_i	0
S_3,S_4,S_2	S_1,S_5,S_6	$-V_i$	0	V_i
S_4,S_5,S_3	S_1,S_2,S_6	0	$-V_i$	V_i
S_1,S_2,S_6	S_3,S_4,S_5	V_i	$-V_i$	0
S_6,S_1,S_5	S_3,S_2,S_4	0	0	0
S_4,S_6,S_2	S_1,S_3,S_5	0	0	0



(a)



(b)



(c)

Fig. 1.6 (a) Timing diagrams of the switches in three phase inverter;(b)Phase voltage waveforms of a 3-phase square wave VSI; (c) Line voltage waveforms of a 3-phase square wave VSI

The switches have been numbered, it is necessary to observe the conduction period of the switches marked in Fig. 1.6 (a). It will be observed that with the chosen numbering the switches turn on in the sequence:- S_1, S_2, S_3, S_4, S_5, S_6, S_1, S_2, ….and so on. Recognizing the fundamental repetition time as 360° (2π radians), each switch operates for 180° and the turn on of the adjacent switch is displaced by 60°. In each limb of the inverter, the upper and lower switches operate in a complementary manner. If the output phase sequence is to be reversed, the switching sequence must be altered. From the symmetry style of the switch conduction, it may be observed that at any time three switches will conduct. The sequence may involve two from the of switches of the top group connected to positive dc input, and one from bottom

group i.e., two from upper group and one from lower group. As per the conduction pattern depicted in Fig. 1.6 (a) six combinations of conducting switches exists over one complete input cycle. Each of these combinations of switches conducts for 60 degrees as per the above mentioned sequence to create output phase sequence of a, b, c. The phase voltages across load, V_{aN}, V_{bN} and V_{cN} can be obtained from the sequence of conduction of the switches in the inverter. Concerning to Fig. 1.7, it can be noted that for $0 \leq \omega t \leq \pi/3$, conduction exists for switches Sw5, Sw6 and Sw1. Assuming that the switches are ideal, Fig. 1.7(a) depicts the equivalent model of inverter and load circuit for the interval $0 \leq \omega t \leq \pi/3$. Looking into the equivalent circuit, the non conducting switches are ignored and the conducting switches are represented by a cross (X) sign. The instantaneous phase voltage waveforms for a balanced 3-phase load are given below for the two conditions (i) when a purely resistive load is connected and (ii) when a load, comprising of a resistance in series with an inductance and a back e.m.f. in each phase. In both the cases, Fig. 1.7(a) is the equivalent circuit referred to obtain the expression for load-phase voltage.

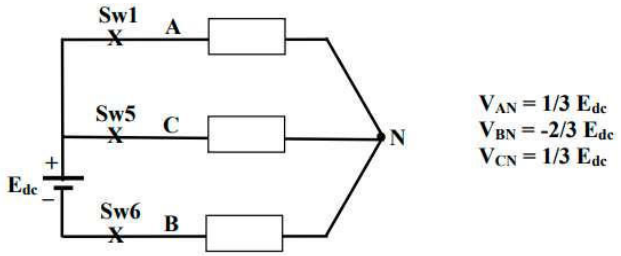


Fig. 1.7(a) Equivalent load circuit during conduction of Sw5, Sw6 and Sw1

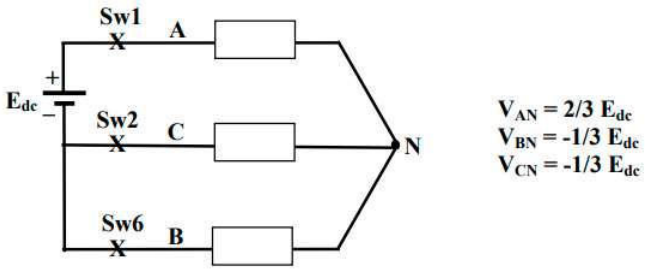


Fig. 1.7(b): Equivalent load circuit during conduction of Sw6, Sw1 and Sw2

For case (i), with a balance resistive load, it is simple to observe that for $0 \leq \omega t \leq \pi/3$, the instantaneous phase voltages shall be expressed by $V_{AN} = 1/3\ E_{dc}$, $V_{BN} = -2/3\ E_{dc}$, $V_{CN} = 1/3\ E_{dc}$. Fig. 1.7(b) depicts the equivalent circuit for case (ii) during $\pi/3 \leq \omega t \leq 2\pi/3$, when the switches Sw6, Sw1 and Sw2 are in conduction. The voltages across load phase instantaneous values can be determined to yield $V_{AN} = 2/3\ E_{dc}$, $V_{BN} = V_{CN} = -1/3\ E_{dc}$.

For other switching combinations, the load phase voltage waveforms may be determined in a similar approach. Two phase voltages, V_{aN} and V_{bN}, and line voltage V_{ab} have been shown in Fig. 1.6(c). It will be observed that voltage V_{bN} is similar to V_{aN} but lags it by 120°. Further, it may be proved that the voltage across the load phase V_{aN} also has a similar waveform to the other two voltages across phases but displaced in time by 120°. The waveform of voltage V_{cN}

leads V_{aN} by 120°. It is clear that the phase voltage waveforms will contain a balanced fundamental components of 3-phase voltage with a phase sequence A, B, C. The output phase sequence can be altered by suitably controlling the switching pattern. The phase voltage waveforms shown in Fig. 1.6 (a) depicts six steps in one output cycle which is also known as the six-stepped waveform.

The 3-phase inverter as explained above may be used to create balanced 3-phase ac voltages at fundamental frequency. On the other hand, the 5^{th}, 7^{th} and other odd harmonic voltages of fundamental frequency pollute the output voltage. Such distortions in output voltages may not be tolerable in many cases and the use filter circuits to eliminate the harmonic voltages may also not be desirable.

1.3 D.C. Bus Utilization of Inverter

DC Bus utilization is a performance index which measures how efficiently the input dc voltage can be utilized at the output of an inverter.

For an example if input dc is V_d=100 V, then to obtain 100% dc bus utilization, the RMS fundamental ac voltage of the inverter (V_{01}) is to be 100 V.

1.3.1 Square Wave Operation

In single phase square wave inverter, to control the amplitude of ac output of inverter the input dc has to be varied as the width of the square pulse cannot be adjusted except the frequency of the ac output. During square wave switching mode, each switch of the inverter limb of Fig 1.1(a) is turned on for one half cycle of the desired output frequency, hence a square wave is formed as shown in Fig 1.2. By Fourier-Series analysis, the maximum value of the fundamental component and harmonics in the output waveform of the inverter can be given by:

$$V_{aN} = \frac{4V_i}{2\pi} = 1.273\frac{V_i}{2} \quad 1.5$$

$$V_{aNh} = \frac{V_{aN}}{2\pi h} \quad 1.6$$

where, the harmonic order *h* takes on only odd values. It should be obtained that the square wave switching is a particular case of the sinusoidal PWM switching with modulation index unity. The maximum DC bus utilization can be achieved by a square wave. The output voltage is independent of modulation index m_a in the square wave area of the graph as shown in Fig. 1.8.

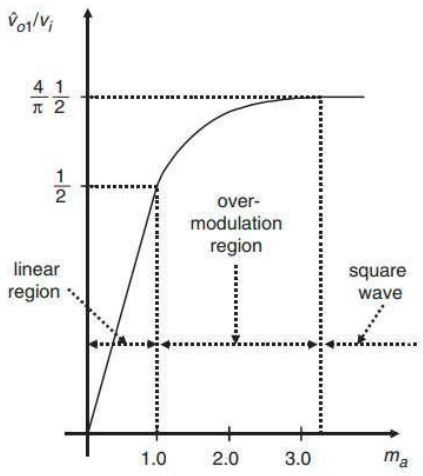


Fig. 1.8 Voltage control by varying m_a

The major advantages of the square-wave switching operation are that each inverter switch alters its state only two times per cycle that is required for a high power applications where the switching speed of the power semiconductor devices are small. The major problem with square wave switching is non availability of output ac voltage magnitude adjustment.

In three phase inverter, with square wave switching output ac voltage magnitude cannot be controlled. Hence control of input dc voltage is the only option for the variable ac output. Using this scheme dc bus utilization can be higher but contains many harmonics. Here each switch conducts for 180˚ and three switches are turned on at any instant. In three phase inverter operating in square wave mode, the line to line fundamental RMS voltage is

$$V_{LL1} = \frac{\sqrt{3}}{\sqrt{2}} * \frac{4V_i}{2\pi} = 0.78V_i \qquad 1.7$$

1.3.2 PWM Operation

The main purpose of pulse width modulation is to control the magnitude of ac output voltage of the inverter and to vary the frequency as well. By controlling the width of the PWM pulses the wave-shape of the output voltage becomes a near sinusoid. To create a pure sinusoidal output voltage at a designated frequency, a modulating control signal at the desired frequency is compared with high frequency carrier signal. The frequency of the carrier signal (e.g. triangular signal) decides the inverter switching frequency at which the inverter switches are switched. A control signal $v_{control}$ at fundamental frequency f_1 is used to modulate the inverter switches by comparing with the carrier signal at the switching frequency f_s. Thus a PWM sine wave is produced as shown in Fig. 1.9. The modulation index m_a is defined as

$$m_a = {}^{V_{control}}/_{V_{tri}} \qquad 1.8$$

where, $v_{control}$ is the maximum amplitude of the control signal.

v_{tri} is the maximum amplitude of the carrier signal.

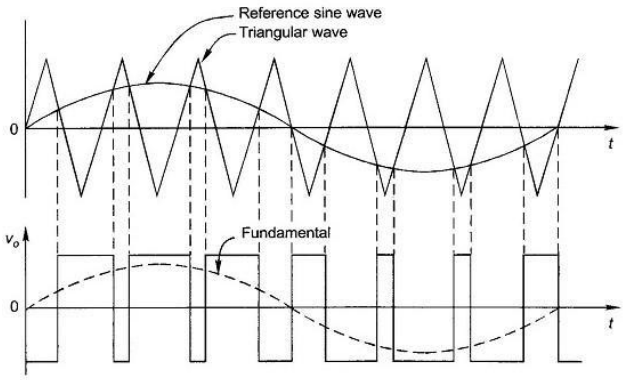


Fig. 1.9 Pulse width modulation scheme

For a single phase inverter at under-modulation, the peak amplitude of the fundamental voltage component as shown in Fig. 1.9 (dotted line) is expressed as

$$V_{o1} = m_a \frac{V_i}{2} \quad \text{, for HB inverter}$$

$$V_{o1} = m_a V_i \quad \text{, for FB inverter}$$

Which shows that the amplitude of the fundamental output voltage of the inverter varies linearly with m_a. Thus the linear region of the modulation index lies between 0 and 1. Hence , the RMS value of the fundamental voltage during under-modulation by a half bridge and full bridge inverter is $0.3535V_i$ and $0.707V_i$ respectively if the modulation index is unity. Therefore less DC bus utilization can be achieved as compared to square wave switching in which the RMS of fundamental voltage is 90% of the input dc bus voltage as shown in Table 1.4.

Table 1.4 Comparative study on DC bus utilization of a single phase FB inverter

Type of Switching	**Input dc (V_d)**	**RMS value of fundamental voltage(V_{01})**	**Observation**
Square Wave switching	100 V	$V_{01} = \frac{4V_{dc}}{\pi\sqrt{2}} = 0.9V_d$	Maximum dc bus utilization but contains many harmonics
SPWM switching	100 V	With $m \leq 1$, $V_{01} = \frac{m_a}{\sqrt{2}} V_d = 0.7V_d$	Harmonic content is low with reduced dc bus utilization
	100 V	With m>1, $\frac{V_d}{\sqrt{2}} < V_{01} < \frac{4Vd}{\pi\sqrt{2}}$	Over-modulation increases the amplitude of the fundamental frequency component but low frequency harmonics is increased.

In the previous discussion, it is seen that during under-modulation, in spite of having less harmonic contents, the dc bus utilization is also reduced causing notches at the output waveform. In order to increase the dc bus utilization, m_a is increased further beyond 1.0

causing the output voltage to contain many harmonics as the fundamental component of output ac voltage of the inverter does not vary linearly beyond m_a=1as shown in Fig 1.8. Also, the modulation index cannot be increased to large values (say, 3 i.e. the optimum value beyond of which the PWM inverter behaves like a square wave inverter) which decomposes the PWM inverter into a square wave inverter again and thus gives more harmonic contents.
Practical inverters are far away from the ideal one as normally constant dc is not obtained at the input to the inverter. Generally this dc is a pulsating as obtained from the rectifiers connected to the grid. Also a large capacitor filter is connected across the dc output of rectifier to remove the ripples in the dc voltage. The capacitor voltage ripple, which is also the voltage ripple across the inverter input, is due to (1) the output of rectifier is not a pure dc, (2) the current drawn by the inverter from the dc source is also not a constant signal, Thus contains second harmonic current along with high switching frequency components. This 2nd harmonic causes ripple in the capacitor voltage as the ripple due to high frequency switching component is negligible.

Similarly, in three phase voltage source inverters, pulse width modulation is used to maintain the balanced three phase output voltages in amplitude and frequency. To create the wave shape a pure sinusoid, it is essential to compare a high frequency triangular wave with the three sinusoidal modulating signals which are 120˚ phase displaced by each other as shown in Fig 1.10.

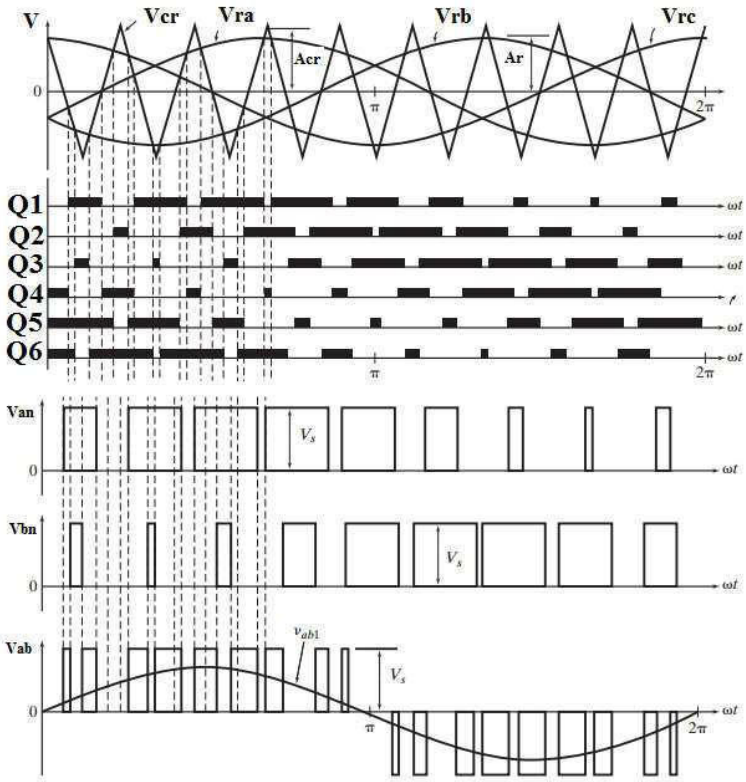


Fig. 1.10 PWM in three phase inverter

In any three phase inverters, the line to line voltages containing the harmonics are of major concern whereas the harmonics present in the phase voltage concerning the dc bus midpoint is identical to that obtained by single phase inverter. In the linear region where m_a is less than equal to unity, the fundamental component in the output voltage varies linearly with the amplitude modulation ratio m_a. The peak value of the fundamental component of phase voltage is given by:

$$V_{an1}=m_a*(V_s/2) \quad 1.9$$

Also, the line to line rms voltage at fundamental frequency can be expressed as

$$V_{LL1}= (\sqrt{3}/\sqrt{2})* V_{an1} \quad 1.10$$
$$= 0.612 m_a V_s$$

In over modulation (m_a>1), the peak of the modulating signal is higher than the carrier wave. Thus, in this mode of operation the fundamental voltage will not change with the increase of modulation index as shown in Fig. 1.11.

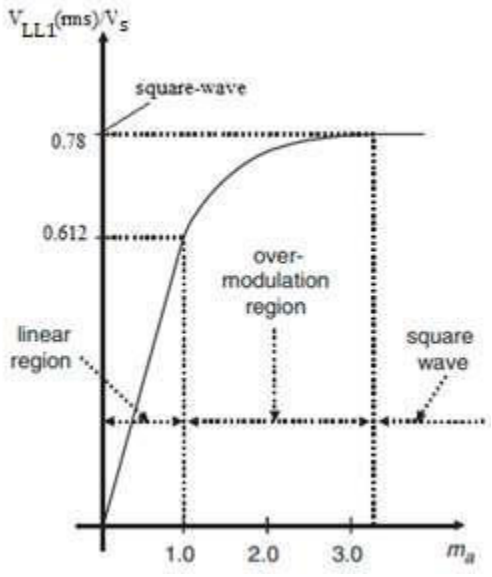


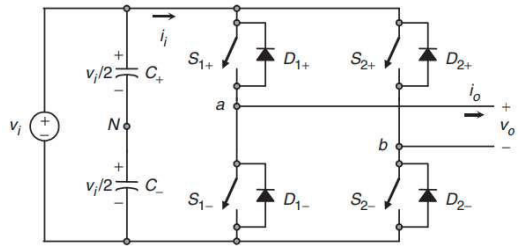
Fig. 1.11 V_{LL} vs m_a curve of three phase inverter

Thus it is found that in three phase inverter, dc bus utilization is maximum (line to line RMS fundamental voltage is 78% of V_s) with square wave switching as compared to the PWM switching technique (line to line RMS fundamental voltage is 61.2% of V_s at under-modulation).

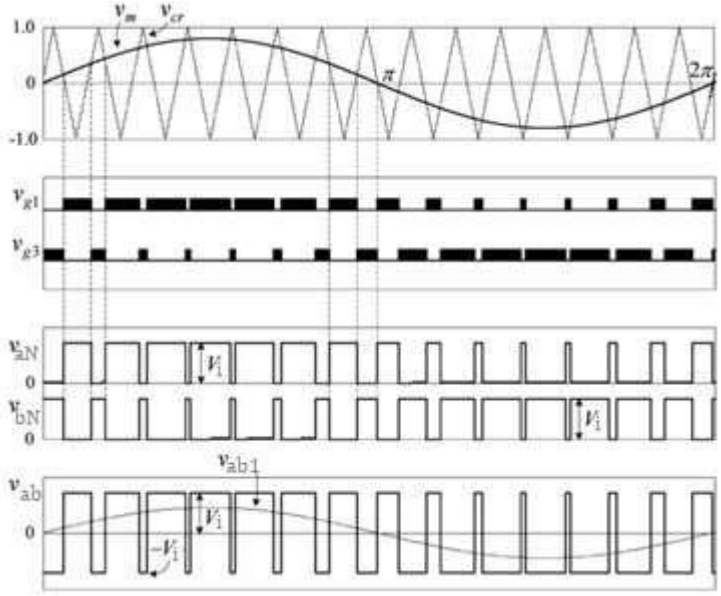
- **PWM with bipolar voltage switching**

In an inverter, the upper and the lower half switches in a limb work in a complementary fashion with alternate switches turned on at a time. Hence only two independent gating signals are required to be provided to the two switches S_{1+} and S_{1-} i.e. v_{g1} and v_{g3} which are

generated by comparing sinusoidal modulating signal v_m and triangular carrier signal v_{cr}. The inverter terminal voltages are obtained denoted by V_{aN} and V_{bN} and the inverter output voltage $V_{ab} = V_{aN}-V_{bN}$. As the voltage waveform of V_{ab} alternates between positive and negative dc bus voltage, this technique is called bipolar PWM which is shown in Fig. 1.12.



(a)



(b)

Fig. 1.12 Single phase inverter with sinusoidal PWM scheme; (a) Full bridge inverter, (b) Bipolar PWM scheme

- **PWM with uni-polar voltage switching**

The uni-polar modulation basically uses two sinusoidal waveforms v_m and v_{m-} as modulating waves which are of same amplitude and frequency but 180˚ phase opposition. These two modulating signals are compared separately with a common triangular wave (carrier) v_{cr} to generate two gate signals v_{g1} and v_{g3} to be provided to the upper two switches S_{1+} and S_{2+}. It must be noted that the upper two switches do not change state simultaneously, which makes it different from the bipolar PWM where all the four switches are switched simultaneously. The output voltage of inverter changes between zero and $+V_i$ in the positive half cycle or between zero and $–V_i$ in the negative half cycle of the fundamental frequency. Hence, this modulation logic is called uni-polar modulation as shown in Fig.1.13. The uni-polar switched inverter

supports reduced switching losses and creates less EMI. In terms of efficiency, it seems that the uni-polar switched inverter has an advantage. Over-modulation happens when modulation index m_a is higher than unity. It results in reducing the number of pulses present in the line to line output voltage waveform causing the presence of lower order harmonics. Further, the notch and pulses near the centre of positive and negative half cycle tend to disappear. To accomplish the switching operations of the switch, minimum notch and pulse widths must be controlled. When minimum width notches and pulses are dropped, there will be some switching transient at the load current.

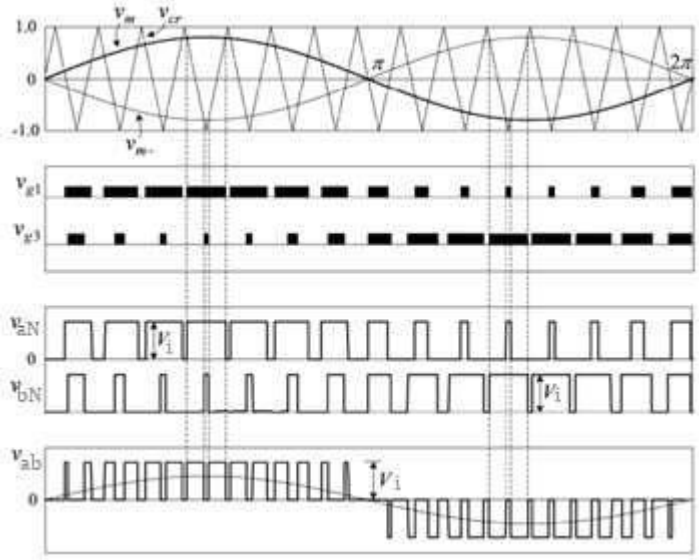


Fig. 1.13 Single phase full bridge inverter with uni-polar sinusoidal PWM scheme

1.4 Voltage Control in Inverters

It is highly essential to control the output voltage of inverters (1) to overcome the variations of dc voltage, (2) for voltage regulation of inverters, (3) for constant volts/frequency control demand. There are different techniques by which the magnitude of output ac voltage of the inverter can be controlled. The widely applicable techniques include:

i. Single Pulse Width Modulation Technique
ii. Multiple Pulse Width Modulation Technique
iii. Sinusoidal Pulse Width Modulation Technique (SPWM)
iv. Space Vector Modulation Technique (SVM)

1.4.1 Single Pulse Width Modulation Technique

Single pulse width modulation technique involves only one pulse per half cycle and to adjust the inverter output voltage the width of the gate pulse is to be varied. Here the switching signals are created through comparison of a pulsed signal E_r (reference signal) with a

triangular signal E_c (carrier). The carrier signal frequency decides the frequency of the fundamental output voltage. The pulse width P can be varied from 0 to 180˚ by varying E_r from 0 to E_c as shown in fig. 1.14. The ratio of E_r to E_c is the modulation index and is expressed as

$$m = \frac{E_r}{E_c} \qquad 1.11$$

and the RMS output voltage can be given as

$$E_L = E_{dc}\sqrt{\frac{P}{\pi}} \qquad 1.12$$

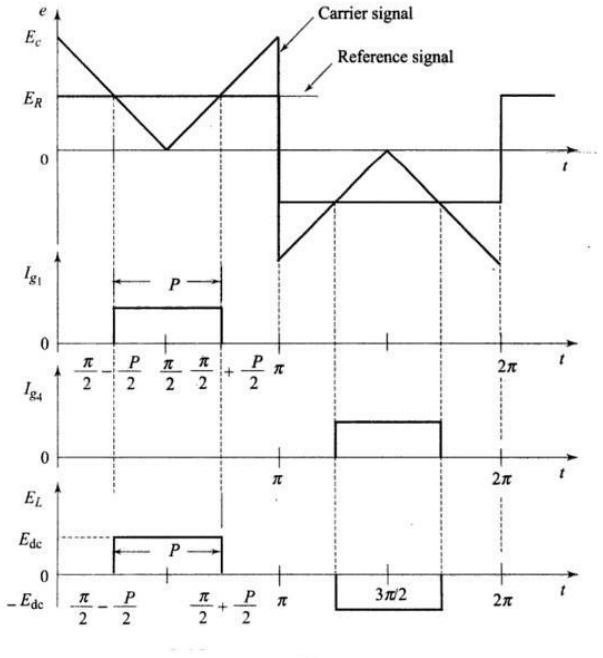


Fig. 1.14 Single pulse width modulation

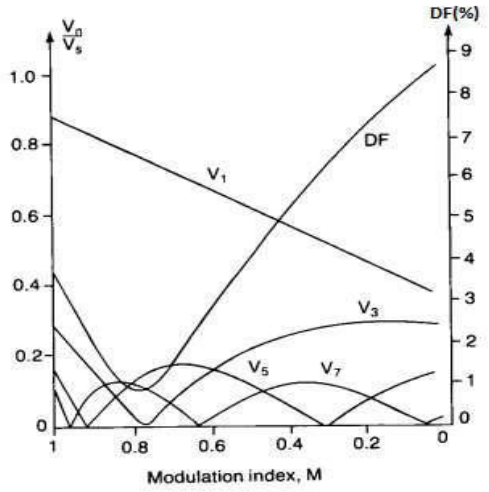


Fig. 1.15 Harmonic profile of single pulse width modulation

Fig. 1.15 shows the harmonic profile of single pulse width modulation. The graph shows that the dominant harmonic content is the third harmonic and the distortion factor increases significantly at a low value of output voltage.

1.4.2 Multiple Pulse Width Modulation

This modulation allows the output ac voltage to be controlled by modulation index. The frequency of reference waveform decides the frequency f_0 of the fundamental output and the carrier frequency determines the number of pulses per half cycle (N). The harmonics may be mitigated by using multiple pulses within each half cycle of the output voltage. The firing pulses to turn on and turn off the power electronics switches are shown in fig. 1.16.

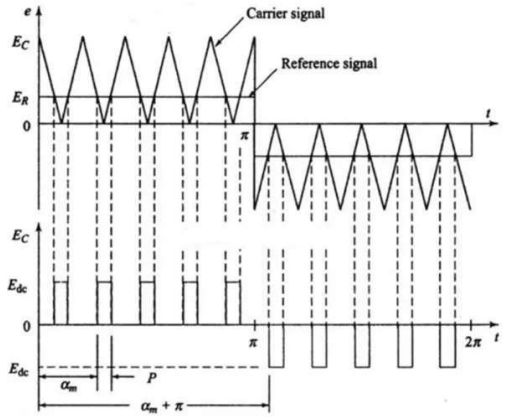


Fig. 1.16 Multiple pulse width modulation

The number of pulses per half cycle is expressed as

$$N = \frac{f_c}{2f_o} \qquad 1.13$$

The modulation index (m) lies between 0 to 1 which varies the pulse width 0 to π/N and the output voltage from 0 to E_c The output voltage for a single phase bridge inverters is shown in Fig. 1.16. If P is the width of each pulse, the RMS output voltage is given by

$$E_c = E_{dc}\frac{\sqrt{NP}}{\pi} \qquad 1.14$$

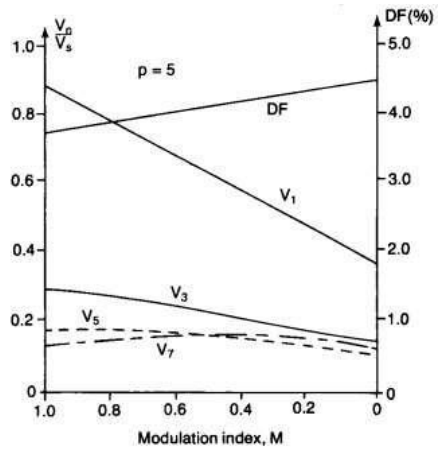


Fig. 1.17 Harmonic profile of multiple pulse width modulation

Fig. 1.17 depicts the harmonic characteristics with respect to the modulation index to have five pulses in one half cycle. The distortion factor is less in this case concerning to single pulse modulation. But due to the fast switching of the semiconductor devices the switching losses are increased. The amplitudes of lower order harmonics are less with the increase of p. But the magnitude of some higher order harmonics can be present which can be further reduces with the small size passive filter.

1.4.3 Sinusoidal Pulse Width Modulation (SPWM)

This technique is superior as compared to the above two techniques in terms of the distortion factor and lower order harmonics. Here, the size of each pulse is varied in ratio to the magnitude of a sine wave measured at the centre of the same pulse. The control signals as shown in Fig. 1.18 are created by comparing a sinusoidal reference waveform (f_r) with a high frequency carrier signal (f_c). This type of modulation scheme has many industrial applications. The frequency of reference signal defines the fundamental frequency f_0 of the output and its maximum amplitude A_r decides the modulation index (m) and the RMS output voltage V_0. The number of cycle per half cycle depends on the carrier frequency.

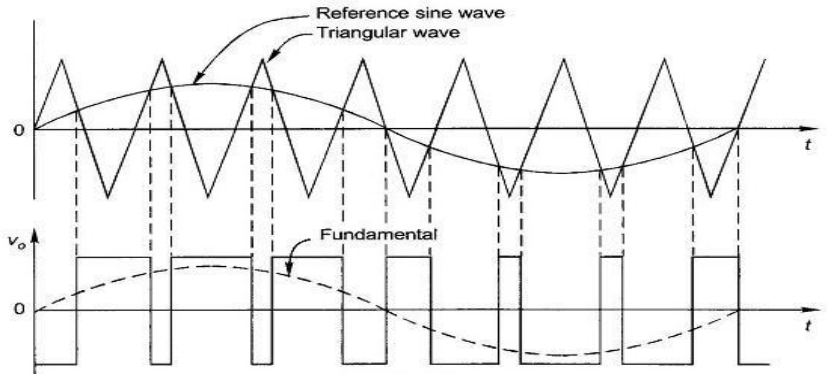


Fig. 1.18 Sinusoidal pulse width modulation

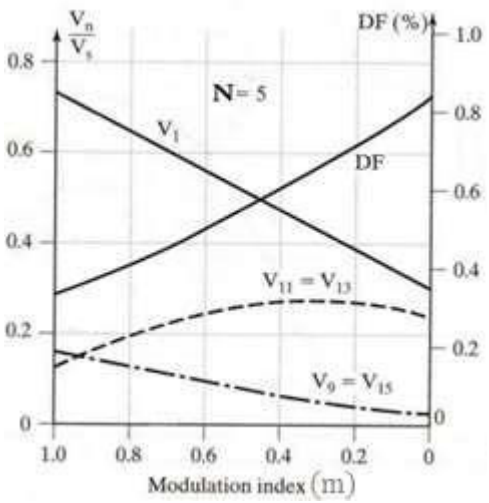


Fig. 1.19 Harmonic profile of sinusoidal pulse width modulation

The RMS output voltage can be changed from 0 to V_s by adjusting the modulation index (m) from 0 to 1. Fig. 1.19 depicts the harmonic characteristics with respect to the variation of modulation index for five pulses per half cycle.

1.4.4 Space Vector Modulation Control

Presently, in the digital systems the modulation technique to control the switches in any power converter system is most suitable one. The space vector modulation is an effective method to develop PWM signals as the line voltages which are on an average similar to the line voltages across a load. This is accomplished in each interval of sampling by suitably adopting the switching states obtained from the conventional ones of the VSI as shown in Table 1.3. and through calculation of the value of time periods correctly. The selected and calculated time periods are based on the Space Vector transformation.

A. Space-vector Conversion

A 3-phase set of data which sum up to zero in the abc stationary frame may be expressed in a complex plane using a complex vector which consists of a real (α) as well as an imaginary (β) part. As an example, the 3 phase line-modulating signals $v_c^{abc} = [v_{ca}\ v_{cb}\ v_{cc}]^T$ can be expressed by the complex vector $\dot{v_c} = v_c^{\alpha\beta} = [v_{c\alpha} v_{c\beta}]^T$ through the following transformation:

$$v_{c\alpha} = \frac{2}{3}[v_{c\alpha} - 0.5(v_{cb} + v_{cc})] \quad 1.15$$

$$v_{c\beta} = \frac{\sqrt{3}}{3}[v_{cb} - v_{cc}] \quad 1.16$$

Assuming the line-modulating signals v_c^{abc} are balanced three sinusoidal voltage waveforms which attribute a magnitude $\hat{v}c$ at an angular frequency ω, the ensuing signals used for modulation in the αβ stationary frame provides a vector $\overrightarrow{v_c}$= $v_c^{\alpha\beta}$ at fixed module $\hat{v_c}$, that

rotates with a frequency ω (Fig. 1.20). Also, the SV transformation is applicable to the line voltage signals of the eight states of the VSI normalized concerning v_i as given in Table 1.3, that creates the eight space vectors ($\overrightarrow{v_i}$, i = 1, 2, ... , 8) in Fig. 1.20. As accepted, $\overrightarrow{v_1}$ to $\overrightarrow{v_6}$ are non-null line-voltage vectors $\overrightarrow{v_7}$ and $\overrightarrow{v_8}$ are null line-voltage vectors.

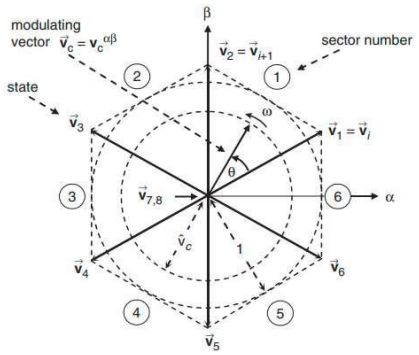


Fig.1.20 Space-Vector representation

The objective of the space vector modulation scheme is to estimated the line-modulating space vector $\overrightarrow{v_c}$ using the eight space vectors ($\overrightarrow{v_i}$, i = 1, 2, ... , 8) presented in VSIs. On the other hand, if the modulating signal $\overrightarrow{v_c}$ lies between the random vectors $\overrightarrow{v_i}$ and $\overrightarrow{v_{i+1}}$, only the closest two non-zero vectors ($\overrightarrow{v_i}$ and $\overrightarrow{v_{i+1}}$) and one zero space vector ($\overrightarrow{v_z}$ = $\overrightarrow{v_7}$ or $\overrightarrow{v_8}$) can be used. Hence the highest load line voltage is increased and the frequency of switching is reduced. To certify that the developed voltage in one time period T_s of sampling (made up of the voltages produced by the vectors $\overrightarrow{v_i}$, $\overrightarrow{v_{i+1}}$, and $\overrightarrow{v_z}$ used at times T_i, T_{i+1}, and T_z) is on an average same as to the vector $\overrightarrow{v_c}$,the subsequent equation must hold:

$$\overrightarrow{v_c}.T_s = \overrightarrow{v_i}.T_s + \overrightarrow{v_i} + 1.T_i + 1 + \overrightarrow{v_z}.T_z \qquad 1.17$$

For a line-load voltage that features an amplitude restricted to $0 \leq \hat{v}_c \leq 1$, the solution of the real and imaginary parts of Eq. (1.15) gives

$$T_i = T_s.\hat{v}_c.\sin(\frac{\pi}{3} - \theta) \qquad 1.18$$

$$T_{i+1} = T_s.\hat{v}_c.\sin(\theta) \qquad 1.19$$

$$T_z = T_s - T_i - T_{i+1} \qquad 1.20$$

The previous equations represent that the magnitude of the highest line-voltage fundamental magnitude is unity for $0 \leq \theta \leq \pi/3$. This is created an improvement over the SPWM method which gains a $\sqrt{3}/2$ highest value of magnitude of line-voltage fundamental under the linear operating area. While, space vector modulation (SVM) strategy decides on the vectors usable and their turn-on times, it does not decide the sequence at which they are used, the choice of the zero space vector, and the normalized sampled frequency. As an illustration, if the modulating line-voltage vector is in segment 1 (Fig. 1.20), the vectors $\overrightarrow{v_1}$, $\overrightarrow{v_2}$, and $\overrightarrow{v_z}$ is to be taken within a sampling time by time intervals denoted by T_1, T_2, and T_z, respectively.

However, whether the sequence, or any other sequence should actually be used, remains a question.

(i) $\overrightarrow{v_1} - \overrightarrow{v_2} - \overrightarrow{v_z}$,

(ii) $\overrightarrow{v_z} - \overrightarrow{v_1} - \overrightarrow{v_2} - \overrightarrow{v_z}$,

(iii)$\overrightarrow{v_z} - \overrightarrow{v_1} - \overrightarrow{v_2} - \overrightarrow{v_1} - \overrightarrow{v_z}$

(iv)$\overrightarrow{v_z} - \overrightarrow{v_1} - \overrightarrow{v_2} - \overrightarrow{v_z} - \overrightarrow{v_2} - \overrightarrow{v_1} - \overrightarrow{v_z}$

However, the method does not clarify if $\overrightarrow{v_z}$ should be $\overrightarrow{v_7}$, $\overrightarrow{v_8}$, or a combination of both.

B. Space-vector patterns and Zero Space-vector optimization

The sequence followed for the line-voltages of load which characterize quarter-wave symmetry for minimizing undesired harmonics (even harmonics). In addition, the zero SV optimization must be carried out to reduce the switching frequency. Even though there is no systematic process to develop sequence for SV, a graphical presentation depicts that the sequence $\vec{v}_i$, $\vec{v}_{i+1}$, $\overrightarrow{v_z}$ (where $\overrightarrow{v_z}$is alternately chosen from $\overrightarrow{v_7}$ and $\overrightarrow{v_8}$) can provide improved performance in terms of reducing undesired harmonics and minimizing the switching frequency.

C. The Normalized Sampling Frequency

In three-phase carrier based PWM schemes, the normalized carrier frequency m_f is opted to be an odd multiple of 3 (m_f = 3*n, where, n = 1, 3, 5, ...). Hence, it is possible to remove non-intrinsic harmonics from the PWM waveforms. For the SVM technique, a similar process may be used to reduce uncharacteristic harmonics. Thus, it is obtained that the normalized frequency of sampling f_{sn} must be an integer multiple of 6. Such a case arises because to provide symmetrical line voltages, all the sectors (total of 6) must be equally used in one time period.

1.5 Harmonics in Inverters

In today's world, with the growing utilisation of power electronics switches, the quality of electrical power, towards the energy efficiency, has become a major challenge. The main issues of power quality are the harmonic distortion, voltage unbalance, voltage sag/swell which represents the deviation between the ideal sinusoidal signal of the network voltage or the load current should have, and what really it is as depicted in Fig. 1.23. The word harmonics can be defined in the following three ways.

I. "Harmonics are voltages and/or currents present in an electrical network at some multiple of the fundamental frequency."

II. "Harmonics are any frequency that exists in the system except the fundamental frequency".

III. "In other words, harmonics appear as the distortion in the desirable sinusoidal waveform in power line".

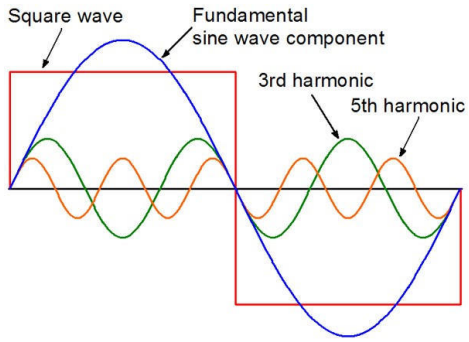


Fig. 1.21 Harmonics in Power System

1.5.1 Source of Harmonics in Inverters

Power electronic inverters produce flat-topped wave-shapes with sharp voltage rise and fall due to switching operation of the semiconductor switches, injecting substantial harmonics into the load that lead to its undesired behaviour.

Also, non-linear load which creates a current waveform differed from the applied voltage wave causes Harmonics in the power converter. The non-linear load involves power semiconductor switches such as diodes, thyristors, SCRs, or transistors etc.

A non-linear load changes its impedance value with the change of instantaneous applied voltage, causing a non-sinusoidal current to be drawn. Alternately, this type of load does not have a constant relation between current and voltage along the alternating time period. The simplest circuit to express a non-linear load is a diode-rectifier, with its different topologies (half-wave diode rectifier, full-wave diode rectifier). Few more examples of non-linear loads, capable of injecting harmonics are as follows: industrial equipments (welding, arc furnace), variable frequency drives (VFD), line-switched rectifiers, switch-mode power supplies, lighting ballasts and also modern electronic equipments, at low load levels, even they could be designed to optimize efficiency around it's rated working value. All these circuits contain semiconductor power switches such as diodes, thyristors (SCR's), transistors etc.

1.5.2 Problems Caused by Inverter Harmonics

Harmonic currents aggravate the RMS current in electrical network and degrade the supply voltage quality. They offer stress to the electrical network and indirectly damage the connected appliances. This may also hamper the normal operation of the devices and enhance operating costs. Also, power factor degrades as the input current wave shape changes from

sinusoidal to some distorted signal causing large amount of harmonics. Thus the overall system efficiency and voltage regulation are reduced significantly.

1.5.3 Techniques of Harmonic Elimination

Few major techniques of harmonic mitigations are explained below:

- **Passive Filters:**

Now days at the receiving end those who consume electrical power is transmitted to various electronic modules say AC- DC conversion device, adjustable motor drive unit, various switch mode power supply unit. All the above mentioned systems are operated on power semiconductor switches which provide the nonlinear characteristics & because of this non linear attributes, the receiver will inject large amount of harmonics in the distribution system & will also influence the other consumers by this contamination of harmonic in system. Generally, harmonic filter is reasonably vital for the enhancement of power quality of the system. Harmonic deformation in the system is very cosmic problem for the entire power electronic researcher & they continuously worked upon the improvement of harmonic component in the system to construct an efficient & clean consumer based electrical utilities in very determinant, with high voltage regulation & maximum efficiency. Passive filters are quite useful for lessening of harmonic component & used conventionally. Passive filters are the most traditional process for the improvement of harmonic in the electrical power system over decades & there has been constant development in this regard for the optimal use of filter & modification of their features to achieve the optimal approach of consumption with reduced cost & rating. They can be used in six pulse three phase converter for the elimination of harmonic component & also gives the reactive power compensation to improve the power quality. Hence by doing so the cost of the extra needed capacitor for the supply of extra kVAr in the line to balance the reactive power will be reduced and thus power quality issues resolves.

Passive series filter-

A passive type series filter has characteristics of both purely inductive type or LC tuned features. The main element used in passive series filter are AC line reactor & DC link filter.

Passive shunt filter-

This has been the most usual method for the elimination of harmonic content in distribution system. Such filter is basically designed as either single tuned or band pass filter technique. In accordance with the name, shunt filters are connected in the system shunted with the load. Such passive filter gives a very low impedance in the circuit at the tuned frequency to switch all the related current & at given tuned frequency. The problem is that passive filter always offers some reactive power in the line, hence the design of passive shunt filter serves the two

purposes- one is the filtration purpose & other one is to support reactive power compensation for correcting the power factor in the network in a proper manner. The benefit of passive shunt type filter is that it carries only a fraction of load current, thus the overall power losses are less as compared to series type filter [47].

- **Stepped wave Inverters:**

In this method pulses of different width and height are superimposed to create a resultant stepped waveform with low THD. The stepped wave inverters can be fed from a single dc source. The turns ratio of the two transformers used in this type of inverter may have different ratings as shown in Fig. 1.22. Low switching frequency stepped wave inverters produce higher DC bus utilization with lower switching loss at the cost of higher amount of lower order harmonics.

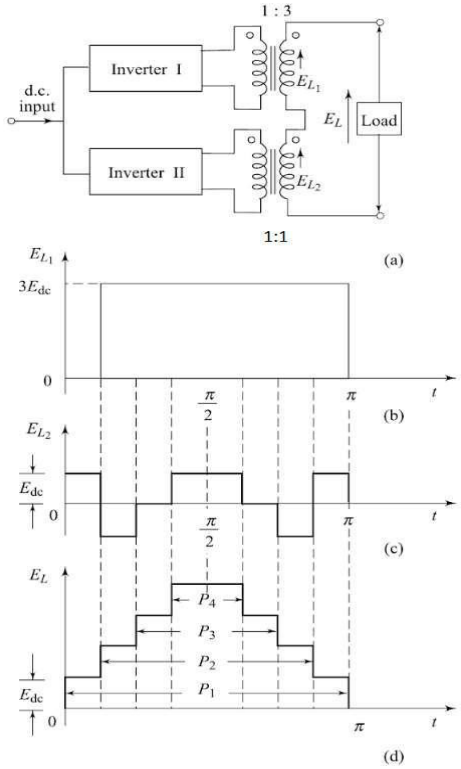


Fig. 1.22 Stepped wave inverters

- **SPWM scheme:**

In SPWM scheme, in order to generate 120˚ displaced sinusoidal load voltages, three modulating signals which are 120˚ displaced by each other are to be used. Fig. 1.23 depicts the ideal waveforms of 3-phase VSI SPWM can be developed using a triangular signal as a carrier signal has been taken to illustrate PWM technique. Thus, all three phase voltages (v_{aN} , v_{bN} , and v_{cN}) are same but 120˚ displaced with the absence of even harmonics; however,

triplen harmonics are uniform in magnitude and phase displacement in all phases. As an example, 9th harmonic in phase aN is

$$v_{aN9}(t)=v_9\sin(9\omega t) \quad 1.21$$

the ninth harmonic in phase bN will be

$$v_{bN9}(t) = v_9\sin[9(\omega t - 120^\circ)] = v_9\sin(9\omega t - 1080^\circ) = v_9\sin(9\omega t) \quad 1.22$$

Hence, the line-line ac voltage $v_{ab} = v_{aN} - v_{bN}$ will not include the ninth harmonic. For example, the identical conclusions can be made for the operation in the 1-phase topologies. However, as the highest magnitude of the fundamental component of phase voltage is $v_i/2$ in the linear region ($m_a \leq 1$), the highest magnitude of the fundamental component of ac output line voltage is $\sqrt{3}v_i/2$. Thus,

$$\hat{v}_{ab1} = m_a\sqrt{3}\frac{v_i}{2}, \quad 0<m_a\leq 1 \quad 1.23$$

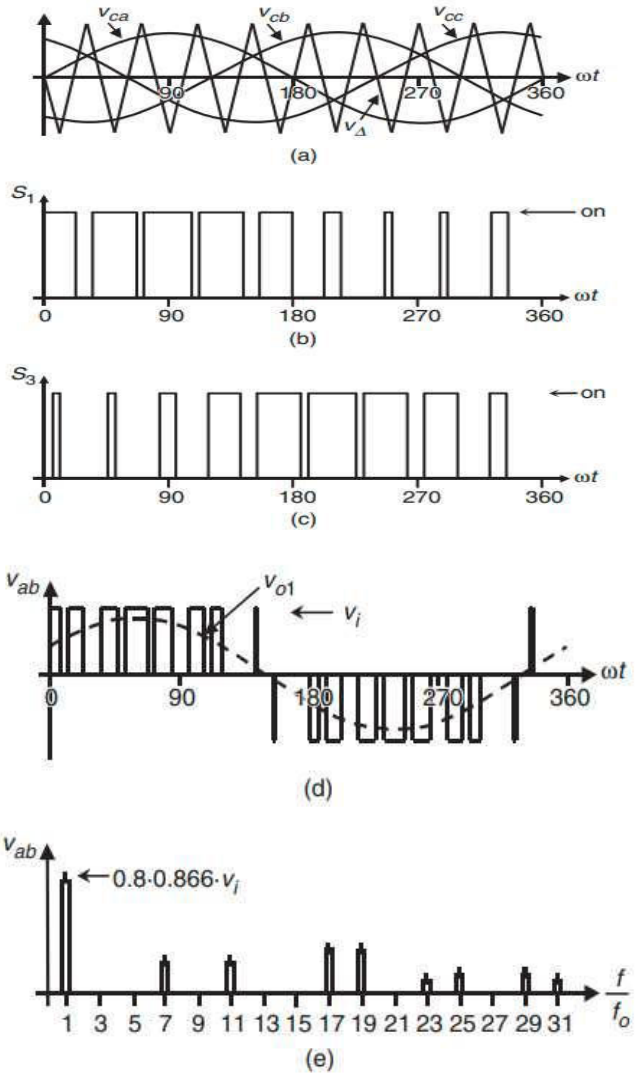


Fig. 1.23 Ideal waveforms for three phase SPWM- VSI: (a) modulating and carrier waveforms; (b) state of switch S_1 state; (c) state of switch S_3 state; (d) line-line output voltage; (e) spectrum of output voltage

If the magnitude of the load voltage is to be increased further, the modulating signal v_c peak is to be increased beyond the magnitude of the carrier signal v_Δ, resulting in over-modulation. The relationship between the magnitude of the output ac line voltage fundamental and the input dc bus voltage is non-linear as in the case of 1-phase VSIs. Thus, at over-modulation region [6], the range of the line voltages lies between

$$\sqrt{3}\frac{v_i}{2} < \hat{v}_{ab1} = \hat{v}_{bc1} = \hat{v}_{ca1} < \frac{4}{\pi}\sqrt{3}\frac{v_i}{2}, \quad 1.24$$

Special Pulse Width Modulation (PWM) techniques are used to obtain low voltage harmonics at the cost of low fundamental output voltage and high switching loss.

- **Multilevel Inverters:**

Several industrial applications involve higher voltage rating apparatus in present days. In medium voltage applications it is very difficult to connect only one power semiconductor switch directly. A utility grid connected application supports few MW's power rating. Hence, a multilevel converter topology has been developed as an alternative solution in high power and medium voltage applications. A multilevel converter is suitable for use with renewable energy sources like photovoltaic, wind, and fuel cells, which can easily be connected to a multilevel configuration in high-power application. The multilevel concept started with the three-level structure. Consequently, numerous multilevel converter topologies have been studied practically. However, the main aim is to attain higher power using a series of power semiconductor devices with several dc sources of lower voltage to execute the conversion of power by creating a staircase voltage waveform. Capacitors, battery banks, and photovoltaic sources may be incorporated as the dc voltage sources. The switching method of the power semiconductor switches aggregates these multiple dc sources to attain high voltage at the output; however, the voltage rating of the power semiconductor devices depends only on the magnitude of the dc voltage sources. A multilevel inverter has many advantages over a classical two-level inverter using pulse width modulation (PWM) with high switching frequency. The attractive features of a multilevel converter are described as follows.

• **Staircase waveform facility**: Multilevel inverters provide output voltage with low THD because of its staircase waveform facility across the load. Also they can reduce the dv/dt stresses, electromagnetic compatibility (EMC) issues etc.

• **Common-mode (CM) voltage gain**: Common mode voltage gain is the key factor of the multilevel inverters. They offer less CM voltage, less stress to the bearings of a motor. In addition, CM voltage can be mitigated by using advanced modulation techniques.

• **Input current wave-shape**: Multilevel converters can provide input current with low THD.

• **Switching frequency of the devices**: Multilevel inverters are suitable to operate at both fundamental switching frequency and high switching frequency PWM. It can be stated that low switching frequency corresponds to less switching loss and high efficiency. However, multilevel inverters have some demerits. The main issue is higher number of switches. Though, lower voltage rating devices can be incorporated in a multilevel inverter, but in that case switches require specific gate drive circuit causing the overall cost of the system to be more [6]. Fig. 1.24a shows a single-phase topology of an m-level cascaded inverter and Fig. 1.24b depicts the phase voltage waveform across the load of a 11-level cascade H-bridge inverter using five separate dc sources.

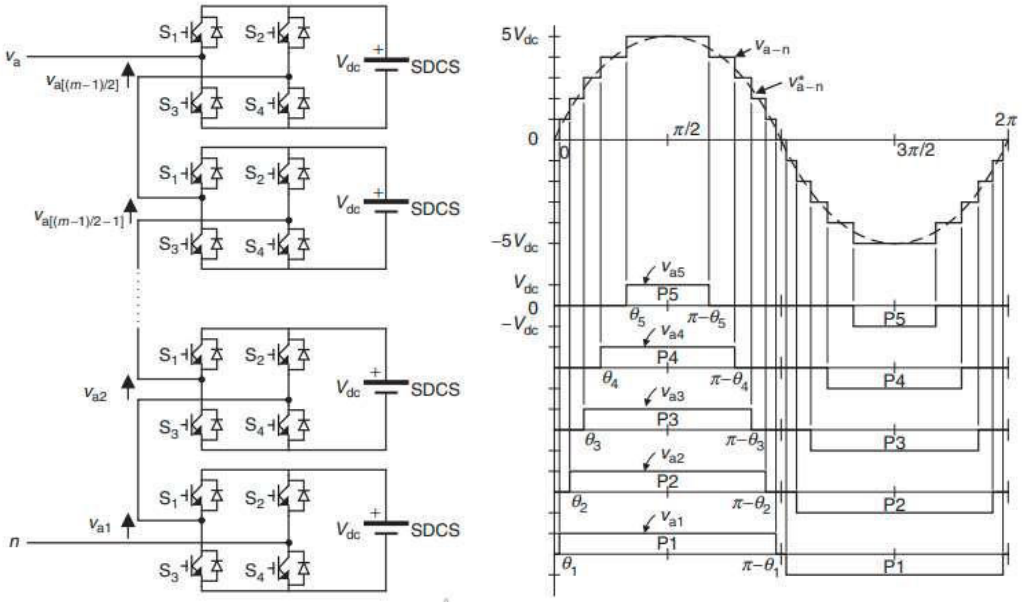


Fig. 1.24 a) Single-phase structure of a multilevel cascaded H-bridge inverter, b) Output ac phase voltage of a 11-level cascaded inverter with isolated dc sources

- **SHE PWM Scheme:**

As in 1-phase VSIs, the Selective Harmonic Elimination (SHE) technique can be implemented in 3-phase VSIs. For this case, the power switches in each limb of the inverter are turned on and off so as to mitigate a specific given harmonics and to adjust the amplitude of fundamental component of phase voltage. In most uses, the desired output voltages of line must be balanced and displaced by 120˚ from each other. The harmonics which are multiples of 3 (h = 3, 9, 15, ...), may exist in the voltages of phases (v_{aN} , v_{bN} , and V_{cN}), but may be absent in the load voltages (v_{ab}, v_{bc}, and v_{ca}). Hence, it is not necessary to mitigate such harmonics and the suitable switching angles are used to remove only the odd harmonics h = 5, 7, 11, 13, ... as desired [6].

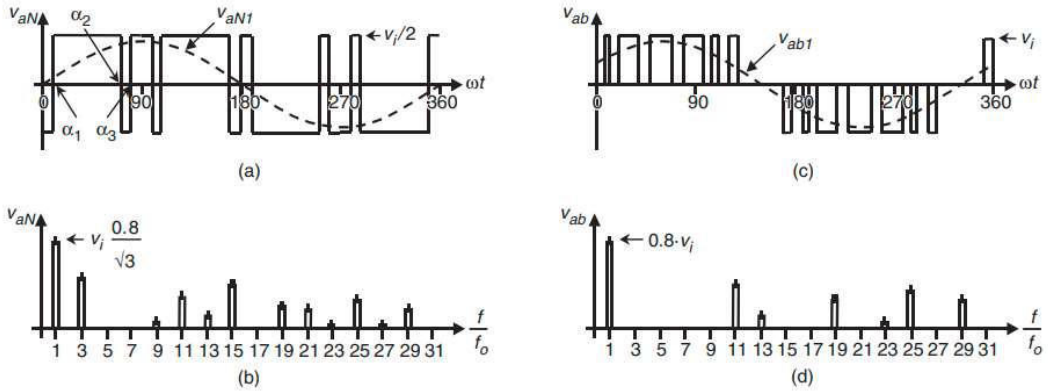


Fig. 1.25 Waveforms for ideal three-phase VSI with SHE modulation: (a) phase voltage V_{aN} for 5th & 7th harmonic elimination; (b) phase voltage spectrum; (c) line voltage V_{ab} for 5th & 7th harmonic elimination; (d) line voltage spectrum.

The mathematical equations for minimizing a specified number of harmonics are the same as used in 1-phase inverters. As an example, to remove the 5th and 7th harmonics and exercise control over the fundamental magnitude (N = 3), the equation involved are:

$$\cos(1\alpha_1) - \cos(1\alpha_2) + \cos(1\alpha_3) = (2 + \frac{\pi \hat{v}_{aN1}}{v_i})/4$$

$$\cos(5\alpha_1) - \cos(5\alpha_2) + \cos(5\alpha_3) = 1/2$$

$$\cos(7\alpha_1) - \cos(7\alpha_2) + \cos(7\alpha_3) = 1/2 \qquad 1.25$$

where the angles α_1, α_2, and α_3 are defined as shown in Fig. 1.25a. Fig. 1.25b depicts that the 3rd, 9th, 15th, etc., harmonics all exist in the phase voltages; though, they do not exist in the voltages across the lines (Fig. 1.25d).

Selective Harmonic Elimination (SHE) techniques can be used for high dc bus utilization and low switching losses but only selected lower order voltage harmonics are eliminated while output voltage control is not possible.

- **Auxiliary Inverter:**

A square-wave inverter at low-frequency with a series-connected pulse-width modulated (PWM) inverter can be suited in high-power applications. This series connected inverter is called as auxiliary inverter. The series compensator produces only the required harmonic voltages but in phase opposition such that the net output voltage is sinusoidal with higher order PWM switching harmonics only. To control the dc bus voltage of this auxiliary converter, external dc source is not required. Hence there will be no consumption of active power by the series inverter. [44].

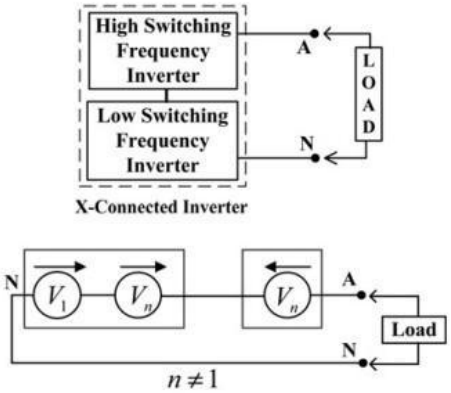


Fig. 1.26 Equivalent circuit of one limb of the inverter in series with a auxiliary inverter

When the four switches of one inverter are switched at low switching frequency, the four switches of the auxiliary inverter operate at higher switching frequency as shown in Fig. 1.26. The four switches from the auxiliary inverter are switched such that the switching pattern nullify the low-frequency harmonics, causing a pulse-width modulation (PWM) voltage with less amount of low-order harmonics at the output. By selection of the suitable PWM pattern, the magnitude of fundamental output voltage produced can be maximum as compared to sinusoidal PWM from the same dc bus input voltage, without bothering about its inherent lower-order harmonics as they would be compensated anyway. Hence, it is possible to establish maximum possible dc bus utilization theoretically [46]. Here, the load current contains the fundamental component predominantly; this current draws active power only from the input dc source using the switches utilized in the low switching frequency inverter which offers only fundamental voltage. Switches used in the high switching frequency PWM series inverter, along with capacitor across the series inverter, provides reactive power only as they do not generate any fundamental voltage. Thus, it can be rationally assumed that the average charge on capacitors in the PWM inverter shall remain same, if the internal losses are neglected.

1.6 Closed Loop Operations of Inverter

Inverters provide adjustable ac output from a constant dc power source, for example, adjustable ac speed drives system. With the change of load specifications, the output voltage also need to be adjusted with these changed conditions. Also, no dc power supply is ideal and the dc voltage value is also not constant in practice, the inverters need to be functional for such variations. Suitable adjustments may be incorporated automatically through a closed-loop control technique. This closed loop system can be made by two ways in the inverter operations. The process of adjustments can be done by the feedback and the feed-forward approaches [6]. The feedback process can balance for both the disturbances (input dc variations) as well as load parameter variations (e.g. load torque changes). Though, the feed-forward technique is more efficient in removing disturbances as it protects its negative effects

from the side of load. These problems are examined in 3-phase inverters as shown below, also the same results are found for single-phase VSIs.

The input dc bus voltage in VSIs is actually considered a constant voltage source v_i. Practically the dc bus voltage is obtained using diode rectifier as given in Fig. 1.27, the dc bus voltage comprises of lower order harmonics such as the 6^{th},12^{th}, ... (due to six-pulse diode rectifiers operation), and the second problem is that the input ac voltage contains unbalanced voltage too. In addition, if the 3-phase load is not balanced, as in UPS applications, the inverter input dc current contains the 2nd harmonic, which in turn causes creation of a second harmonic voltage in the dc bus. Feed-forward approaches are basically meant to sense the disturbances and accordingly change the input so as to nullify its effect. Thus, the dc bus voltage is to be first sensed and then the modulation technique is to be consequently adapted.

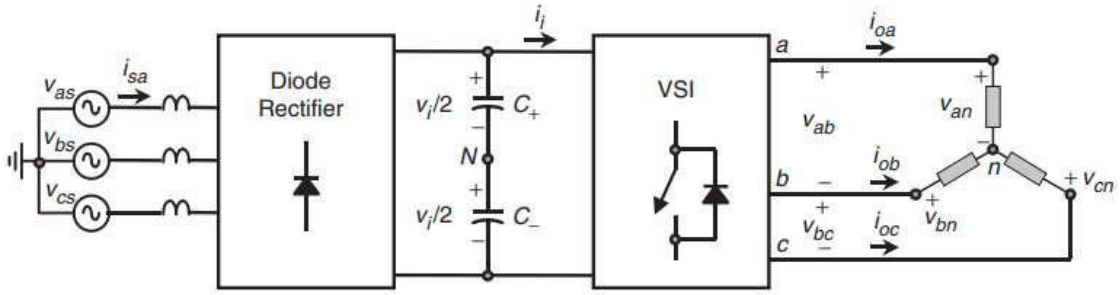


Fig. 1.27 Three-phase VSI topology with a diode-based front-end rectifier

1.7 Outline of the Thesis

The proposed work motivated towards the novel approach for achieving highest dc bus utilization to create maximum fundamental ac voltage with reduced THD in switching inverters. In the above section several techniques are discussed to mitigate harmonics but at the cost of less dc bus utilization in inverter circuits. In contrary there are suitable control schemes by which effective dc bus utilization can be attained but contains large lower order harmonics. Hence the fundamental objective of this research work focuses on the generation of maximum RMS ac output voltage with reduced harmonic contents. By the principle of natural compensation, both the single phase and three phase switching inverter systems were examined to have high dc bus utilization and more fundamental output voltage at over-modulation i.e. modulation index greater than unity.

The thesis is organized as follows:

Chapter two presents a review of the different techniques of harmonic mitigation in order to have maximum fundamental ac output voltage with effective dc bus utilization.

Chapter three introduces a new topology of the single phase inverter with series active power filter in order to generate a pure sinusoidal signal. Supporting simulation results are furnished to justify the performance of the new inverter system using natural compensation. The proposed scheme is also verified using experimental results.

In chapter four, a new three phase PWM inverter with the auxiliary inverter was investigated to reduce the lower order voltage harmonics and more fundamental ac output voltage as compared to conventional PWM inverter. Simulation and experimental results are also shown to substantiate the theoretical findings.

In chapter five, a three phase inverter system at over-modulation was investigated using natural harmonic compensation to achieve less THD but the output ac voltage control facility is not available. Finally simulation studies are furnished to justify the proposed concept.

Overall conclusion and summarization of the work presented in the thesis is given in Chapter six along with future scope of work.

CHAPTER – TWO

Review of Techniques for Mitigation of Voltage Harmonics and Improved DC Bus Utilization in Inverters

2.1 Introduction

For any research work, the literature review is the primary task that any researcher must do. This study helps one to go into the deep of the researches that had been investigated on that specific area. In this section such research domains are highlighted and explained thoroughly which are relevant towards the mitigation of voltage harmonics with high dc bus utilization in inverters. Various types of inverter topologies are also studied concerning to the mitigation of harmonics and to create more fundamental RMS voltage at the output of the inverter system.

2.2 Different Configuration of Inverters

A new technique of over-modulation scheme is presented using the application of space vector modulation. The system can be implemented to an application of open end winding induction motor drive. Here a two level conventional inverter is connected at one end of open end winding and the other end of the winding is connected to a 2-level inverter in series with a capacitor fed H bridge cell. This above mentioned configuration of five level inverter system using SVM scheme is more reliable as compared to the neutral point clamed inverter by the elimination of eighteen clamping diodes of different ratings. Alternately, this topology requires a single capacitor bank per phase whereas the number of capacitor bank is more than one in flying capacitor based inverter for the same five level output ac waveform across the load. In addition this topology can be worked as a three level inverter if there is any problem in the capacitor fed H bridge inverter. [1].

Another inverter system of thirteen level output having a three level inverter cascaded with a half-bridge inverter and a three level floating capacitor in each phase. The ratio of the two floating capacitors is calculated such that the higher levels can be generated across the output voltage. A suitable PWM scheme is used to maintain the balance between the dc bus capacitor voltages. This topology is well suited for the grid tied converter as because here the number of switch count is less per phase to improve the power quality. To create more fundamental ac output by this system, the modulation scheme is extended by injecting common mode voltages. [2].

A new topology of multi-level inverter with the flying capacitor played an important role for the excellent features. In this work a seven level output is presented using pulse width modulation scheme. Mainly the flying capacitor based inverters used in industrial applications

are analysed with a simple control strategy at transient state. It is demonstrated that by changing the modulation index, the dynamic responses of the dc-link can be understood with a high performance index [3].

In medium voltage applications, the cascaded multilevel inverters are popular to develop ac output voltage using a series connection of multiple power cells at suitable low voltage rating devices. The output power quality and the input current waveform have shown excellent characteristics [4].

Nowadays, Dynamic Voltage Restorer (DVR) plays a very important role in many power system applications to overcome several power quality issues. In power electronics, problems of voltage sag or voltage swell or any unbalance in the grid voltage can be solved using series connected inverters. The open end winding transformer connection can be implemented through this inverter system to avail the operation of a DVR connected with the inverter output. This above mentioned system is superior as compared to a conventional inverter in terms of harmonic distortion, fault tolerance level and the converter losses [5].

Another research work discovered that a shunt active power filter can be designed using two converters having three limbs connected to three phase open end winding transformer in order to generate multilevel output. The main advantage of the system is to reduce switching losses and harmonic distortions [7].

Sine wave inverters with fixed frequency are used in several applications as backup power supply to critical equipment or synchronized to the AC grid for power support as distributed generation (DG) from renewable energy sources [8,9].

This work developed a new topology of the inverter where three inductors are coupled to form impedance source inverter like Y-source or delta-source configurations. This system improves the output quality by reducing the active switches. However, in this case, the boosting level decreases with the increase of modulation index. Hence, the dc bus utilization is greatly affected for large gain applications. Also, it is found that the leakage inductance present in this system causes the sudden change in the induced current which in turn generates a large voltage spike. Thus by utilizing a buffer circuit, this problem can be resolved and the spike in the voltage waveform can be minimised [10].

2.3 Techniques for Improved DC Bus Utilization

In high power and medium voltage applications multilevel inverters are widely used. They reduce the size of bulky inductors in the filter circuit to create good power quality at the output. But the major problem is that to avail half of the dc bus voltage, two times ac maximum voltage is needed. In large power application, the input dc bus voltage to be high which causes to select switches and the passive components with very high voltage rating. Also, sometimes to improve the dc bus utilization a front end rectifier or a dc-dc boost converter is required. Thus to improve the dc bus utilization, this work introduced a new inverter topology in addition to a T-type network with four active devices just before the dc

link capacitor. Hence, the requirement of input dc voltage is less which in turn increases the output voltage levels of the [11].

A new method is studied for a transformer less inverter topology for effective dc bus utilization. In PV based inverter application this type of inverter having switched capacitor can be implemented. These capacitors improve the PV voltage by two times. A special PWM technique is used to create a five level output voltage. The leakage current related issues and EMI problems can be avoided by this topology. A level shifted sinusoidal PWM helps to provide more dc bus utilisation with a single dc source and with zero leakage current [12].

A new voltage balance theory using floating capacitor (FC), is introduced with the extended modulation index to get more ac output as compared to the conventional inverter. This proposed three phase thirteen level inverter using a single dc voltage source can provide dc bus utilization of 63% of the dc input voltage at unity power factor. But is seen that the above mentioned system is not suitable to balance the FC voltage for the wide modulation range compared to the conventional capacitor voltage balance theory [13].

Another work proposed that three phase inverter with less switching devices can produce infinite level output. A simple PWM technique is used with no additional filter circuit to create cost effective inverter system. In this system one switch per phase will operate at high frequency to provide less switching stress and reduced switching loss. Since the system utilizes input voltage source of low rating, in this work, the dc bus utilisation is improved as compared to other PWM inverters. Also, third harmonic injection PWM theory extended the dc bus utilization to create a sinusoidal output ac voltage [14].

Nowadays, multilevel inverters are popular topic in power electronics applicable to different kind of renewable energy sources. This proposed work describes that the new topology of inverter system has a feature of producing more ac fundamental voltage as compared to the conventional multilevel inverters like neutral point clamped, flying capacitor based and cascaded H bridge inverters. Here the self balancing floating capacitors are used. However the control logic is complex in this but the dc bus utilisation is two times what we get by the conventional multilevel inverter topology [15].

This research area has evolved a new topology of the three phase inverter system which can be suitable to a frequency conversion device. The dc bus utilization of a three phase standard SPWM inverter is 0.866 which can be extended to unity using a special space vector modulation. The proposed technique utilized the principle of selective harmonic elimination (SHE) theory along with the immune algorithm. This modulation technique produced dc bus utilization of 1.022 with a small voltage and current harmonics [16].

Another work described about a new model of nine level inverter system suitable for renewable energy applications. Only ten numbers of switching devices and a flying capacitor are used here. To create an efficient system, this topology uses the hybrid configuration of SiC based inverter provides high dc bus utilization that is 2.5 times that of conventional multilevel inverters [17].

In this work, in order to have effective dc bus utilization, a new technique based on reconstructed carrier quasi-trapezoidal pulse width modulation (RC-qTPWM) is described. The topology is suitable to have more dc bus utilization and less total harmonic distortion. The proposed unit can be implemented to overcome the problem of power imbalance amongst H bridge model. The proposed modulation strategy provides improved DC voltage utilization, better efficiency, less line voltage, low current THD, and enhanced power balance as compared to conventional TPWM methods [18].

A new topology of three phase inverter suitable foe solar PV based system is introduced for improved dc bus utilization. A special modulation theory, using the principle of third harmonic injection is explained in a work. The proposed configuration can help to enhance the constraint range of the power balance between the units of cascaded PV inverter utilizing the concept of carrier phase shifted pulse width modulation (CPS-PWM) scheme [19].

Another research work introduced a hybrid topology of inverter system which provides nine-level output. The inverter topology improves the dc-bus utilization with low amount of lower order harmonics. The system is operated at over modulation range to enhance the dc-bus utilization as compared to conventional multilevel inverters. The above mentioned inverter comprised of a cascaded structure of an H-bridge (HB) module and a T-type network of 5-level output. However, capacitor voltage balancing is accomplished using inserting an offset to the reference sine-wave. The pulse width modulation technique is utilized here to increase the maximum value of the fundamental voltage (phase voltage) from $0.577V_{dc}$ to $0.625V_{dc}$ at unity power factor load and to $0.637V_{dc}$ at 0.82 power factor load [20].

A new five level inverter topology described in this research work to create more DC bus voltage utilization using a single DC source and a capacitor fed H-bridge (CHB) modules. A carrier-based modulation scheme is utilised here for the enhancement of the DC bus utilization. Here, the new topology of inverter is introduced using CHB module of three level output with a neutral point clamped (NPC) inverter connected with each limb. The above mentioned modulation process provides the inverter to improve the DC bus utilization upto 0.63 times of input dc voltage keeping the power factor unity. Though the modulation range is linear but using a low value of the DC bus voltage and thus, the inverter topology is suitable to operate with a reduced value of lower order harmonics [21].

A low cost and high efficiency PV based inverter circuits are more popular now a days. A Transformer less (TIs) inverter configurations are not very useful because the parasitic capacitance of PV array produces leakage currents, thus the control scheme becomes more complex. In this work, a switched-capacitor (SC) based inverter topology is used to generate such that the leakage current is zero. Additionally, industrial half-bridge modules can be utilized directly with the proposed inverter in industrial applications. The aforementioned configuration has the characteristics that the switched capacitor with a self-voltage balancing mechanism van be used to compensate the reactive power and to improve dc-bus utilization [22].

A new three phase induction motor based ac drives applicable for domestic ceiling fan is proposed in this research work with extended dc-bus utilization. The proposed system is fed from a 50Hz single phase ac power source using a flyback-based power factor correction rectifier circuit, which results in 100Hz voltage ripple in the dc-link. The voltage ripple is considerable (nearly 10%) as a low value of capacitor is used to avoid high system cost. By using special carrier based space vector modulation (SVM) strategy the motor performance can be made immune to this voltage ripple but it limits the dc-bus utilization considerably. In this paper this problem is addressed by introducing an appropriate phase difference between the reference vector of the SVM and the dc-link voltage ripple. This phase difference is calculated by aligning the peaks of the modulation signal and the dc-link voltage ripple. It is shown that by doing so the dc-bus utilization can be increased. In the proposed case the dc-bus utilization is achieved to be 61% whereas any existing PWM strategy with ripple free dc-link voltage cannot have more than 57.7% dc-bus utilization [23].

2.4 Techniques for Mitigation of Voltage Harmonics

In power system applications, harmonic distortion is the major problem which pollutes the power quality of the entire network. Conventionally, Passive filters are very much useful for elimination of harmonic contents from the system. Several research works introduced passive filter over the last three decades for the reduction of harmonic to have the optimum approach with reduced rating & cost. [47].

A novel PWM control scheme is introduced for a multilevel inverter. The low-frequency hybrid modulation concepts are projected in this work for cascaded multilevel converter topologies to mitigate the harmonics. Here, two types of pulse width modulation schemes are used. They are a phase shift pulse width modulation (PS-PWM) and an asymmetric selective harmonic current mitigation-PWM (ASHCM-PWM). In the proposed work, the cascaded H-bridge (CHB) converter operates such that using the control schemes PS-PWM and ASHCM-PWM the IEEE 519 harmonic tolerance band can be expected [24].

In cascaded H bridge inverters, the traditional switching scheme produces lower order harmonics across the load. This causes discontinuous output current leading to a severe threat to the ac drive system. Hence a special pulse-width modulation (MCPWM) technique using a multicarrier scheme is proposed which minimizes the amplitude of harmonic voltage from the inverter output. This system analyses with continuous output current at low peak amplitude. The proposed concept involves an elimination mitigation algorithm that opts the switching angles of the MCPWM pulse to satisfy the real time adjustment of the modulation index and the switching frequency of the semiconductor switches. The main objective is to eliminate the fifth, seventh, and eleventh order harmonics from the inverter output voltage and to decide a new range of switching sequences such that the switching harmonics have less magnitude. In this work, estimation of switching pattern in real time domain is more popular than solving the complex nonlinear equations [25].

A cascaded H-bridge (CHB) converter suitable to grid-tied applications at low frequency modulation schemes introduced as per power quality standards. Simultaneously, the harmonics at the grid voltage affects the current harmonics of the CHB converters. Also, the dc link voltages of grid connected converters need to be controlled. In this proposed work, an asymmetric selective harmonic current mitigation pulse width modulation (ASHCM-PWM) scheme is used to have the limits of current harmonic using the standard of power quality. To control the dc bus voltage, a voltage balancing theory based on the average power of each cell is defined to adjust dc link voltages of the CHB converters. The cost of the proposed voltage balancing technique, do not need any complicated dc link voltage controllers. [26].

Another research work explained about a simple switching mechanism to reduce the harmonics from the system. This proposed technique is suitable for a grid connected Photo Voltaic (PV) inverters, wind and water turbines. To create a good quality of power different modulations schemes are there in power electronics. In this work a phase shift switching scheme is implemented, in order to have less current distortion even while there is any unbalance in the grid. Though the control mechanism is simple, at the end, a suitable filter circuit is to be designed to eliminate the further harmonic contents from the circuit [27].

A typical multilevel inverter is proposed in this work to remove harmonics from the system using unequal dc sources. Selective harmonic Elimination method is implemented here in conjunction with the principle of fuzzy logic control system and particle swarm optimization (PSO) technique. Fuzzy is that intelligence system which is utilized to obtain the appropriate switching instants. PSO is the intelligence based algorithms which is used in the proposed work to create the optimum values of the switching angle from the selected data set in order to mitigate harmonic distortion [28].

This document describes a technology that operates at fundamental frequency to obtain switching angles for the proposed converter topology. A single phase 9-level converter is utilized here to mitigate the third and odd multiple of the triplen harmonics and to eliminate lower order harmonics, in order to have a reduced total harmonic distortion (THD). The switching instants can be obtained by using the adjustment of DC bus voltages supplying the converter, equal in magnitude, but controllable. The switching angles are not dependent on modulation index [29].

The cascaded H-bridge converter (CHB) is a versatile process in like flexible ac transmission systems and motor drives. In the proposed work, the discontinuous pulse-width modulation (DPWM) by adding some power cells is introduced. This is incorporated in the CHB as it allows minimizing the switching losses in the power switches. However, this method generates a large distortion of harmonic in the CHB output voltage as compared to the conventional phase-shifted PWM (PS-PWM) method of switching. If the number of clamping cells increased, then this process is not hold good. Hence, a generalized CHB model analysis is applied to the DPWM method with multiple clamped cells. The proposed method can be operated in two ways, first to eliminate the basebands harmonic, secondly, a variable-angle

PS-PWM scheme is implemented to the CHB in order to remove the sidebands harmonics [30].

Another work introduced the concept of phase shifting process of the carrier for eliminating the harmonics in systems having asymmetrical inverters connected in parallel, applicable for the DG network. The research work illustrates the operation in a decentralized manner and provides an optimal solution in minimizing the cost for the improvement of power quality. The proposed work indicates the principle of optimal carrier phase shifting technique for the reduction of lower order harmonics in power system. Compared to all the existing centralized methods, the proposed technique has a feature of decentralized option which includes the advantages of the robust and cost effective solution [31].

The renewable energy based solution is becoming popular day by day as it provides clean, sustainable and energy efficient technologies. Hence, in a distributed generation (DG) network connected to the power grid, it is highly essential to have a good quality of power at the point of common coupling (PCC). In distributed generation circuit, first it is required to eliminate the harmonics generated by power semiconductor switches which includes higher order harmonics at the multiple of carrier frequency of the DG connected inverter. This work mentioned that these harmonics can be mitigated with the help of passive LC filters connected at the inverter output. Another cause of generation of the harmonics is generated by the nonlinear elements in the utility grid of the system, which are very common generated at the multiples of the fundamental frequency. In the proposed work an advanced control scheme is reviewed for the mitigation of such harmonics in the DG connected inverter system [32].

Power quality issues are major challenges nowadays to have efficient power electronics converters in many applications. For instance, adjustable speed drive (ASD) system is required to operate by a suitable control scheme such that the system is free of harmonics. In distribution networks, three phase traditional diode bridge rectifiers are widely used in three-as the grid connected converters. They have a cost-effective solution, simple control logic, and reliable characteristics. In the proposed work, a three-phase bridge rectifier with harmonic elimination property using an electronic inductor is introduced. The proposed methodology can remove current harmonics as developed by other traditional rectifiers connected with the same point of common coupling (PCC) [33].

In power electronics, multilevel inverters are the great solutions in terms of their ability to generate higher number of levels in the output voltage waveform. In many applications like uninterruptable power supply, adjustable speed drive systems and piezoelectric transducer, these converters play an important role towards different switching control schemes. Several modulation techniques have introduced by multiple research works. To control the output voltage of the multilevel converters, it is found that the space vector modulation is a better solution amongst the other harmonic elimination (HE) techniques. Multilevel inverters may have equal or unequal value input dc bus voltage. However, this work presents a DC bus voltage with unequal values towards the mitigation of harmonics [34].

This study introduces a new topology of converter using the technique increased nearest level modulation (NLM) mechanism to enhance the THD factor and improve the output voltage of the modular multilevel converters (MMCs) topology. The proposed work can be suitably applicable for offshore wind farms which require connections from onshore grids, and this can be achieved by using MMC by developing higher number of levels. The aforementioned technology possesses the benefits of the traditional NLM approach in terms of simple control logic and less switching loss [35].

The proposed work introduced a new topology of the multilevel inverters which can be utilized in high power industrial applications and grid tied renewable energy conversion networks. The proposed topology is advantageous as it minimizes the blocking voltage stress, lower order harmonics, size of the filters. In this work, a quasi-nested topology is being implemented which makes the system more attractive as compared to the conventional MLIs. A special discontinuous modulation scheme is introduced in order to control the voltage unbalancing of the input dc bus voltage. The main advantage of the proposed topology is that by employing an additional level to a four-level inverter configuration with the same number of semiconductor switches as used in the conventional three-level multilevel inverters such as NPC and ANPC, the output voltage with less THD can be obtained as compared to the other clamped inverters [36].

The work proposes the outcomes obtained from a single-phase series connected active power filter (APF) using a special control scheme. A modified hysteresis control technique is introduced in the work which can operate with the variation of both the limited and unlimited maximum switching frequency but at the cost of large number of higher order harmonics in the load voltage waveform [37].

This study proposed a control scheme implemented to the series APF for mitigation of harmonics and to compensate the dynamic voltage. Here a voltage source inverter is required to connect across the secondary side of the transformer and the utility grid to be connected with the primary side. According to the amount of the harmonic current, the switching sequences are to be designed. The voltage sag/swell of the grid power will also define how the switching to be done. Hence, the VSI is capable of reducing the voltage deviation in the line with reduced THD [38].

This work introduced the simple control logic operated for the active filter. A variable source can be utilised by this active filter. Though it is mainly used as controlled impedance, it compensates the harmonic voltages as described in the work by connecting linear or nonlinear loads with a improved power quality [39].

The quality of electrical energy is a prime concern nowadays to a consumer. Different bodies are paying more attention to the production of good quality of power because that includes the rate of productivity and economical profit. Hence, it is essential to find some solutions which eliminate the issues related to this problem. Active Power Filters (APFs) are power electronic devices that are capable of mitigating power quality issues. But there are few challenges working with this active power filter such that its high cost. This work proposed a new

configuration with suitable control algorithms implemented to a single-phase SeAPF supplied directly to the utility grid without using any coupling transformers and extra dc voltage sources [40].

A study of several pulse width modulation (PWM) methodologies is proposed in this research work suitable to a three phase inverter. A cascaded H-Bridge (CHB) type multilevel inverter is selected for this work. Today, multilevel inverters (MLIs) are mostly being used in medium and high voltage networks due to several characteristics to produce improved power quality is a major concern. The pattern of the modulation scheme proposed here is a simple one i.e. carrier based PWM signals are developed by using the modulating signal. The study involves calculation of various parameters like switching losses, conduction losses, harmonic distortion factor and DC bus utilization of inverter output with two different modulation techniques i.e. the continuous and discontinuous PWM techniques [41].

Another research area proposes the idea of sub- harmonic elimination technology. The control strategy is well established to a six step operation of a three phase inverter. Actually the sub-harmonics generated because of the switching sequences of the power electronics switches causing the dc offset. Thus, the proposed work designed a control technique for this three phase inverter topology to mitigate the sub-harmonic contents [42].

2.5 Natural Compensation of Harmonics

In power converters the fundamental objective is to make the system harmonics free so that the efficiency of the converter is improved. In this regard, the natural voltage balancing theory is becoming popular to create a pure sinusoidal ac output voltage waveform. The multi-cell converter topologies are more suitable option for the aforementioned principle. The key factors related to this technique include the selection of switching frequency, load characteristics and the harmonic voltage signal. To reduce the lower order harmonics of the proposed multi-cell inverter the system utilises a new PWM technique [43].

In this work two inverters connected in series are investigated for high-power applications. One of them is a square wave inverter at low switching frequency and the other one is a PWM inverter at high switching frequency. The second converter is known as harmonic compensator which produces only the required harmonic voltages in the opposite phases as that obtained by the main inverter. To have the final output voltage near sinusoidal with less PWM high switching frequency harmonic components, a suitable control scheme for the natural compensator is explained here. This principle of operation decides the dc bus voltage across the compensator at the appropriate level. To control the dc bus voltage of the later converter, no external dc voltage source is required [44].

In this work, a hybrid converter is presented for medium-voltage applications like reactive-power compensation. The main converter is a square wave inverter operated at high-voltage. This inverter creates a fundamental reactive current. The proposed square wave inverter is connected to multiple cells consists of single-phase full-bridge converters to mitigate

harmonic voltages. The input voltage signal of the different cells proposed here will be adjusted using this hybrid converter topology presented here. In this proposed work different PWM techniques are implemented to satisfy the operation of the inverter [45].
A new inverter topology with reduced lower order harmonic voltages can be explained by the principle of natural harmonic compensation. Here one set of switches will be operated with low frequency and the other set of switches from the same limb will be operated at high frequency. Two input capacitors are connected across the input. The inverter topology will be operated using the PWM scheme such that all the lower order harmonics get nullified and only high frequency PWM components will be appeared across the load. A suitable PWM technique is proposed in this work to have more fundamental output ac voltage and improved dc bus utilization as compared to a standard SPWM inverter [46].

2.6 Conclusion

In the earlier sections several research works are explained related to different types of inverter systems in applications like renewable energy, power supply, variable speed drives etc. Many researchers developed novel configurations of inverters to create high DC bus utilization but at the cost of large switch counts. Various researches are demonstrated inverters to create less number of lower order harmonics with reduced fundamental RMS voltage at the output. Many have demonstrated different complex topologies of inverter to mitigate harmonics in which wide range of voltage variation scheme is not available. Thus, in order to have all the benefits, a special type of control scheme is implemented to the new topology of an inverter system in the next sections of this thesis report.

CHAPTER – THREE

Sine Wave Inverter with High DC Bus Utilization Using Natural Harmonic Compensation

3.1 Introduction

Sine wave inverters with fixed frequency are used in several applications as backup power supply to critical equipment or synchronized to the AC grid for power support as distributed generation (DG) from renewable energy sources [8, 9]. To create the desired sinusoidal voltage wave-shape from the DC supply with voltage control, several techniques are used, of which Sinusoidal Pulse Width Modulation (SPWM) techniques are the most popular. The SPWM method is selected to reduce the magnitude of the lower-order harmonics so that the remaining higher-order harmonics can be easily filtered out using small-size low-pass LC filters [6]. However, this process results in the use of high switching frequency in the power semiconductor switches, which causes increased power loss in them. At the same time, the RMS magnitude of AC fundamental voltage obtained from the given DC supply (DC bus utilization) without using a transformer is not very high.

High DC bus utilization has been a matter of research since it yields a higher output sine-wave voltage from a given DC voltage input, which results in the need for lower input DC voltage for a particular AC voltage output. For the same DC bus input & same power output, higher DC bus utilization reduces the current through the semiconductor switches. Several inverter topologies have evolved to improve the DC bus utilization of inverters [11,12]. Multilevel voltage source inverters provide high DC bus utilization with reduced harmonics and without the transformers or series-connected harmonized switching devices [14,20]. In multilevel inverters, the harmonics of the output voltage are reduced by increasing the number of levels. However, this also demands large numbers of switching devices in the inverter system and several isolated DC power supplies in different multilevel structures, which is a major concern [13, 21].

Several researches carried out using an auxiliary pulse width modulated (PWM) inverter in series with the main inverter in the form of the series active power filter (SAPF) has been effective in removing voltage harmonics from the output of an inverter. One such example of 1-phase SAPF uses a transformer coupled PWM bridge (with a separate DC supply) in series with the main inverter to produce good quality voltage but at the cost of limited switching frequency and some higher order harmonics in the load voltage waveform [37]. Another work describes a SAPF using a transformer coupled PWM bridge, but without the use of a separate DC supply [38]. The principle, operation and control strategy of a SAPF was described to reduce voltage harmonics for linear or non-linear load without using any transformer or DC

supply, but using a complex control circuit [39]. Another research work has also been presented [40] that developed a 1-phase SAPF without using any transformer or DC supply. However, the use of a complex control circuit to maintain the voltage on the DC bus of the SAPF has always been a deterrent. Several techniques have been adopted to overcome the above problem, of which, the principle of natural compensation of harmonics is an interesting area [44, 45]. This technique permits the creation of lesser switching loss in the main inverter and high DC bus utilization [46].

The work presented here combines a low switching frequency multi-level inverter along with a transformer-less series active power filter to yield a new combined structure for a 1-phase inverter system with advantages of both, such that there is no need for a separate power supply for the SAPF. The combination permits over 20% higher DC bus utilization while maintaining similar efficiency and Total Harmonic Distortion (THD) of voltage when compared to an SPWM inverter of the same power rating, even though using a higher number of switches. In this proposal, a 1-phase 5-level main inverter is operated at a low switching frequency with over-modulation to obtain low switching loss along with high DC bus utilization. A 2-level 1-phase series active power filter using high switching frequency is used for compensation of voltage harmonics but does not require a separate DC bus supply. The SAPF is operated in a simple feed-forward control mode (instead of complex feedback control) to maintain its own DC bus voltage based on the principle of natural compensation. Further, due to the use of a multi-level main inverter, the lower order harmonics are low; hence required DC bus voltage of the SAPF is low, permitting the use of lower voltage devices like power MOSFETs with lower losses at a given switching frequency. A small L-C filter is used at the final output to remove switching frequency components of the auxiliary inverter and create a low THD sinusoidal output voltage with a magnitude higher than that obtained through a standard PWM inverter.

3.2 Proposed Scheme

The proposed 1-phase inverter scheme is depicted in Fig. 3.1. It comprises of a 1-phase 5-level inverter operating from its DC voltage input (V_{dc}), switching only at low frequency, with the desired fundamental frequency output voltage. The output voltage from this inverter is a stepped waveform without any high-frequency modulation, unlike normal multi-level inverters, thereby creating a high DC bus utilized output waveform (that has a large amount of fundamental AC voltage) with low switching losses. This inverter however has a significant amount of harmonics in its output voltage and a limited range of output voltage adjustment through adjustment in its pulse widths.

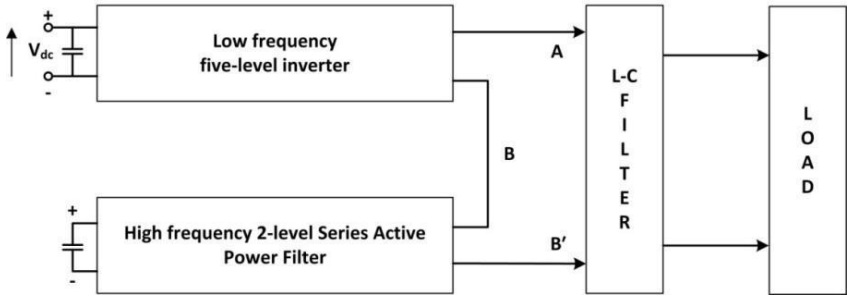


Fig. 3.1 Proposed scheme of sine-wave inverter using a multi-level inverter with a series active power filter

A separate 1-phase 2-level PWM inverter with only a capacitor bank connected across its DC bus (without a separate power supply) has its output AC terminals connected in series with the 5-level inverter. This is referred to as the series active power filter (SAPF) or the compensator. This produces a specially controlled PWM voltage waveform across its output, that has the equal order and amplitude of voltage harmonics as that was generated by the main inverter, but in phase opposition, without any content of the main inverter fundamental voltage. This compensating voltage waveform, when connected in series with the main inverter, as depicted in Fig. 3.1, results in the cancellation of the harmonic voltages of the main inverter across the total output. Thus, the resultant voltage available across the output is only the fundamental content of the main inverter with added PWM switching frequency component of SAPF. Hence, a small LC filter is sufficient to provide an acceptable sinusoidal voltage waveform across the connected load.

The major contribution of this work is to initially create a stepped voltage waveform with maximum DC bus utilization, without regard to voltage harmonics as they would be removed effectively by the series active power filter. For example, a 1-phase square wave has a theoretical fundamental root-mean-square (RMS) AC voltage magnitude of 90% of the DC voltage, which provides the maximum possible DC bus utilization but has significant low-order voltage harmonics that would require a large filter for removal. On the other hand, a 1-phase SPWM waveform has reduced lower-order harmonics but the maximum fundamental RMS voltage is only about 70.7% of the DC bus voltage. Thus, the generation of a stepped voltage waveform with two steps in a half cycle (operating in SPWM mode with over-modulation) facilitates high DC bus utilization combined with voltage adjustments while having low switching losses. However, a high amount of low-order harmonics in such a voltage waveform created by the main inverter needs large filtering. Elimination of harmonics is accomplished here through a SAPF, based on an auxiliary inverter switching at a higher frequency, but with a lower DC bus voltage, without any separate DC power source, based on a simple feed-forward principle instead of a complex feedback system.

The output voltage generated across the points A & B by switches of the main inverter can be expressed as:

$$v_{AB} = \sum_{k=1,3,5,7,\ldots}^{\infty} V_k \sin k(\omega t - \phi_k) \qquad 3.1$$

where, ω is the fundamental angular frequency, ϕ_1 is assumed to be zero (as the reference) and V_k is the amplitude of the k-th order voltage harmonic component. This comprises a fundamental amplitude V_1 along with several harmonics of k-th order with magnitude V_k.
The voltage generated by the SAPF across points B & B′, can be expressed as:

$$v_{BB'} = -\sum_{k=3,5,7,..}^{\infty} V_k \sin k(\omega t - \phi_k) \quad 3.2$$

Since the magnitude and phase of the harmonics developed in the series active power filter is controlled to be equal to that of the main inverter, considering the series connection of the two voltages, the final output voltage across points A & B′ can be expressed as:

$$v_{AB'} = v_{AB} + v_{BB'} = V_1 \sin \omega t \quad 3.3$$

Thus, only fundamental voltage will be present, with all other harmonic voltages (including lower-order harmonics) canceled without the use of any LC low-pass filter.
Following effective compensation of voltage harmonics at load terminals, the series current through the inverter and SAPF is predominantly due to the fundamental. However, as the SAPF is not generating any fundamental component of voltage across it, there will be no fundamental active power exchange with the latter. Thus, its DC bus capacitor once charged up through auxiliary paths, can maintain its voltage by natural balance through a simple feed-forward control process, without getting discharged, without the need for a separate energy supply to its DC bus. However, considering system losses, a small amount of energy is required to maintain its DC bus voltage, which is automatically executed.
The above is based on the principle of Natural Harmonic Compensation (NHC) [16] as applied here. During normal operation, if any harmonic voltage generated by the main inverter is not compensated by the same harmonic created by the SAPF, then the resulting harmonic voltage sends a corresponding harmonic current through the load circuit. This harmonic current, along with the corresponding harmonic voltage across the SAPF, transfers energy through the switches of the SAPF, charging up its DC bus capacitor until the compensated harmonic voltage is identical to that of the main inverter when power flow due to the harmonic stops naturally. In similar fashion, the opposite action takes place while the harmonic voltage developed by the main inverter is overcompensated by the corresponding harmonic generated by the SAPF. Thus, the average state of charge of the DC bus capacitor of SAPF remains steady, offered that there is a minimum harmonic current path existing through the load such that power can flow to/from the DC bus capacitor of SAPF at a rate similar to or more rapidly than the internal loss in the SAPF.
It may be noted that the naturally controlled DC bus voltage of the series active power filter is automatically adjusted to create the right magnitude of compensating harmonic voltage. Since the output voltage waveform of the main inverter having steps already has a reduced magnitude of lower-order harmonics, the corresponding DC bus voltage of SAPF is lower than that of the main inverter. This aspect is used to advantage in this work by using lower blocking voltage rating devices in the SAPF and thus achieve lower switching losses.

3.3 The Operation of Proposed Inverter

The complete circuit diagram of the proposed 1-phase inverter system is presented in Fig. 3.2. It consists of a neutral point clamped main inverter generating a five-level voltage output at the fundamental frequency with two steps in each half-cycle, whose width can be modulated to control the fundamental voltage. To compensate for the voltage harmonics of the main inverter, a 1-phase high-frequency two-level auxiliary inverter working as a SAPF (based on natural compensation) is connected in series, creating opposing harmonic voltages. Finally, a small L-C filter is used to remove all voltage transients and switching frequency components to create a low THD voltage waveform with high DC bus utilization.

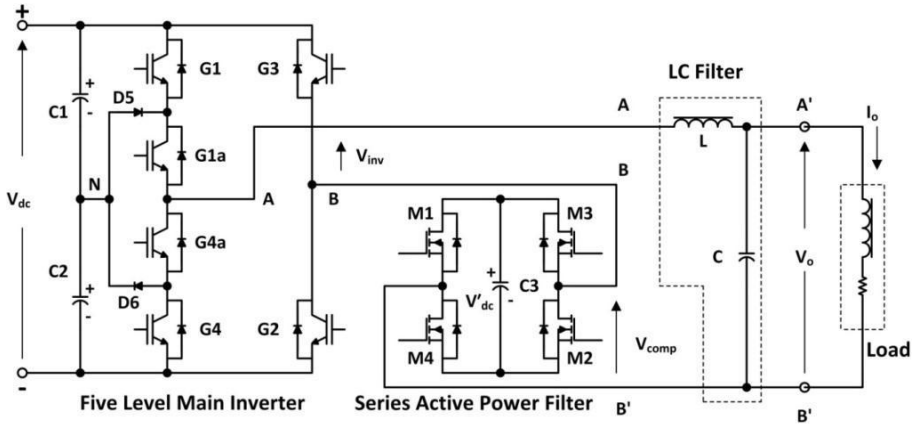


Fig. 3.2 The proposed 1-phase sine-wave inverter power circuit

3.3.1 Principle of Operation of Main Inverter

The diode-clamped 5-level main 1-phase inverter provides multiple voltage levels from the single DC bus divided into three levels by the series connection of two identical capacitors C1 & C2 that create a DC neutral point N. The first limb has four IGBTs (G1, G1a, G4, G4a) connected in a string across the input DC bus and has two diodes D5 & D6 connecting the string at different symmetrical points to the DC bus neutral. When the switches G1 and G1a are turned on, the output point A is connected to the positive DC bus. When the switches G4 and G4a are turned on, the output point A is connected to the negative DC bus. When the switches G1a or G4a are turned on while all other switches of the same limb are off, the output point A is connected to the mid-point of the DC bus through the diodes D5 or D6 depending on the current polarity. Thus, the first limb creates a 3-level voltage output (V_{AN}) at the desired fundamental frequency at point A concerning the DC bus neutral N, with one pulse per half cycle (without high-frequency modulation) as shown in Fig. 3.3. The switches G1, G1a, G4, G4a of the first limb creates voltage levels with respect to this mid-point as $(+0.5V_{dc}, 0, -0.5V_{dc})$. It is to be noted that the minimum blocking voltage of switches G1, G1a, G4 & G4a is required to be only half that of the DC bus (V_{dc}), hence the switching losses in

these devices are also lower than any device that faces full DC bus blocking voltage.
The second limb has two switches G2 and G3 connected to the input DC bus without any connection to the bus mid-point. When switch G3 is turned on, the output terminal B is connected to the positive DC bus, and while switch G2 is turned on, the output terminal B is connected to the negative DC bus. The operation of these two switches produces a 2-level output as V_{BN} at the desired fundamental frequency (as square wave) without any PWM control at point B with respect to the DC bus neutral N. The second limb thus creates voltage levels with respect to the DC bus mid-point as $(+0.5V_{dc}, -0.5V_{dc})$. However, its fundamental is kept displaced from the fundamental at terminal A by 180° as depicted in Fig. 3.3 to create the highest fundamental voltage (V_{AB}) across the output terminals A and B after taking the difference between the two limb voltages. The minimum blocking voltage of switches G2 and G3 is required to be that of the DC bus (V_{dc}).

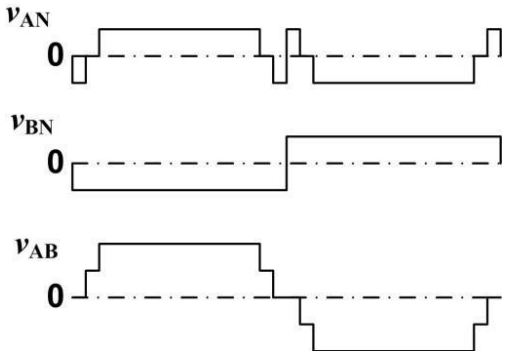


Fig. 3.3 Schematic of stepped wave voltage generation in proposed inverter

Thus, the total output voltage created from the main inverter has the levels $(+V_{dc}, +0.5V_{dc}, 0, -0.5V_{dc}, -V_{dc})$ as the difference between the voltages of the two limbs. Hence, the resultant waveform (VAB) created across the output terminals A and B is 5-level as depicted in Fig. 3.3. This waveform comprises fundamental voltage as well as harmonics. The operation of the switches is controlled through a low-frequency SPWM strategy in over-modulation mode using two steps per half cycle to control switching losses as well as achieve high DC bus utilization (yield more fundamental output voltage from a given DC bus voltage) combined with a restricted degree of voltage adjustments. The range of Modulation Index m used is:

$$1.5 \le m \le 3 \qquad 3.4$$

This range of modulation index calculation is shown in Appendix A1.1.

3.3.2 Principle of Operation of SAPF

The series-connected active power filter or compensator uses a 1-phase H-bridge comprising of four MOSFETs (M1 to M4) with an isolated DC bus capacitor C3. Assuming that the DC bus capacitor C3 is fully charged, the compensator generates a conventional two-level

waveform (which is a pulse width modulated signal at high frequency) between points B and B′. The minimum blocking voltage of switches M1, M2, M3, and M4 is required to be that of the auxiliary inverter DC bus (V'_{dc}).
In order that the SAPF creates an effective compensating waveform, the constituent devices must switch at a frequency higher than that of the main inverter. This justifies the use of MOSFETs to restrict switching loss. On the other hand, the use of MOSFETs restricts the magnitude of its own usable DC bus voltage across C3. In this case, since the output of the main inverter produces a five-level waveform, thereby reducing the height of each step, the DC voltage required across the capacitor C3 is lower than the input DC bus voltage (as explained in section 3.4), hence permitting easy application of MOSFETs (with lower blocking voltages) in the compensator circuit. Since no significant real power is drawn from the series active power filter, it does not require an active power source on its DC side.

3.3.3 Maintenance of Charge across Capacitor of SAPF

When the capacitor C3 across the SAPF dc bus as shown in fig 3.2, is fully discharged, there will be no compensating voltage harmonics by the semiconductor switches M1, M2, M3 and M4. This develops a current flowing through the load which contains harmonics as generated by the main inverter switches. Simultaneously, the switches of SAPF are trying to generate the same voltage harmonics as developed by the main inverter but with opposite phase, hence a real power is developed with this harmonic current through the load and the voltage harmonics across the SAPF which keeps the capacitor C3 charged always until the compensating harmonic voltage is similar to that of the main inverter. The capacitor charging will be stopped when these two harmonic voltages are equal. If voltage harmonics generated by SAPF is more, the capacitor charge will remain same if harmonic current through the load is enough. It means that a suitable harmonic current to be flown through the load always to maintain the capacitor voltage. Again the load current depends on the load impedance, hence for a purely resistive load or with a very small load inductance value, the charge across the capacitor may fall which in turn causes an imperfect sine wave across the load.

3.3.4 Principle of Operation of Low Pass L-C Filter

A small LC filter is finally used to remove the switching frequency components of the compensator as well as voltage spikes and smooth the output voltage waveform in order to obtain a low THD voltage output. The calculated value of L and C for the LC filters used in the proposed inverter system is shown in Appendix A1.2.

3.4 Control Pulse Generation Scheme

The block schematic of the control pulse generator for the proposed inverter system is shown

in Fig. 3.4. Since the main inverter has a stepped output waveform, a sine wave of variable magnitude (depending on the set value of modulation index) but frequency same as that of the inverter output is compared with a set of four level-shifted triangular waves of constant magnitude but double the frequency.

The lowest step per half-cycle is created at the intersection of the sine wave v_{sine} with the triangular wave v_{t2} or v_{t3}, depending on the positive or negative half-cycle respectively concerning Fig. 3.5(a). The highest step per half-cycle is created at the intersection of the sine wave v_{sine} with the triangular wave v_{t1} and v_{t4} depending on the positive or negative half-cycle respectively. This results in two sets of quasi-square waveforms whose widths are controlled by the magnitude of the sine wave v_{sine}. The control pulses are derived from this using appropriate logic such that the required switching pulses for switches G1, G1a, G4a, and G4 of the main inverter of Fig. 3.2 are generated to produce the desired voltage between points A and N as shown in Fig. 3.3. The switching instants of switches G2 & G3 are created by detecting the zero crossings of the sine wave to create two square waves as shown in Fig. 3.3.

The control of output voltage harmonics is by a feed-forward control strategy of the SAPF. To generate the control pulses of the SAPF, first, the hypothetical 5-level output waveform is synthesized in the control circuit from the pulses generated, as shown in Fig. 3.5(b). The fundamental component of this waveform v_{fund} is extracted through a band-pass filter and then the same fundamental is subtracted from the synthesized 5-level output waveform to yield the hypothetical harmonic content waveform v_{har} as shown in Fig. 3.5(b).

This resulting waveform is to be synthesized across the output of the SAPF and thus serves as the reference for the SAPF. It is to be noted that after subtraction of the fundamental, the peak-to-peak magnitude of this reference waveform created is about half of that of its original peak-to-peak waveform. This assures the reduced DC bus voltage requirement of the SAPF (V'_{dc}), which is needed to create only the waveform of v_{har} across its output terminals. This is one advantage of the proposed scheme in creating reduced switching losses in the overall system.

The reference waveform of v_{har} is compared with a separate higher frequency triangular carrier as depicted in Fig. 3.4 to create the PWM pulses for the SAPF (or compensator). These pulses are to be given to the switches M1, M2, M3 & M4 in sequence to generate v_{comp}, a PWM version of v_{har}, across points BB′ of the inverter in Fig. 3.2.

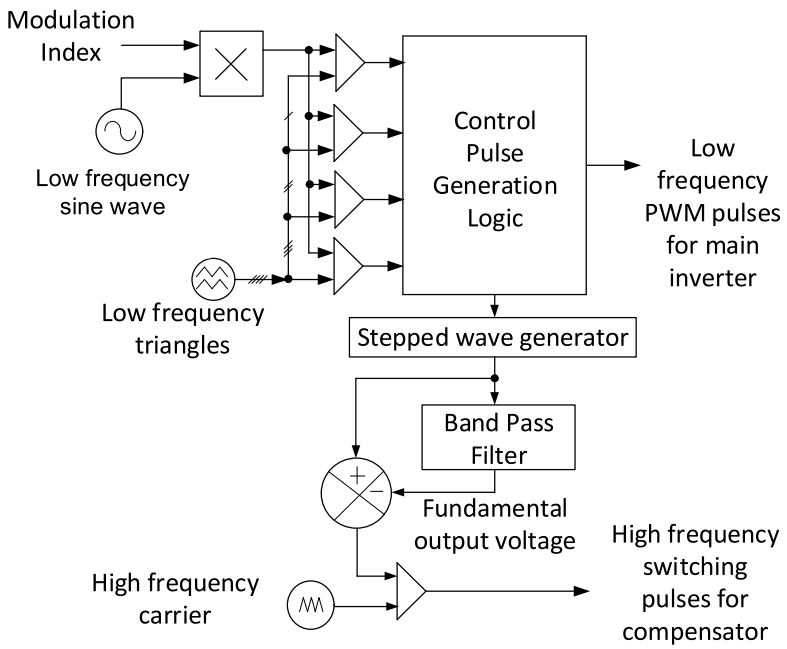


Fig. 3.4 Block diagram of the scheme for gate pulse generation scheme

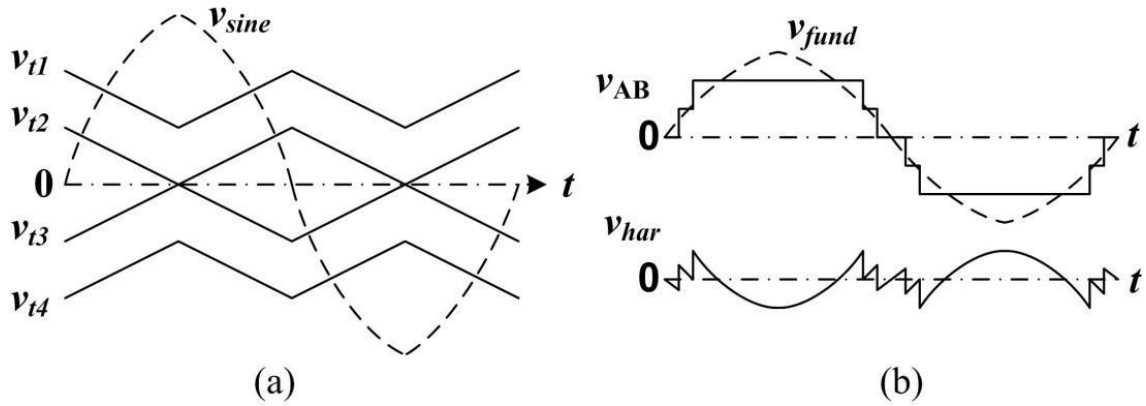
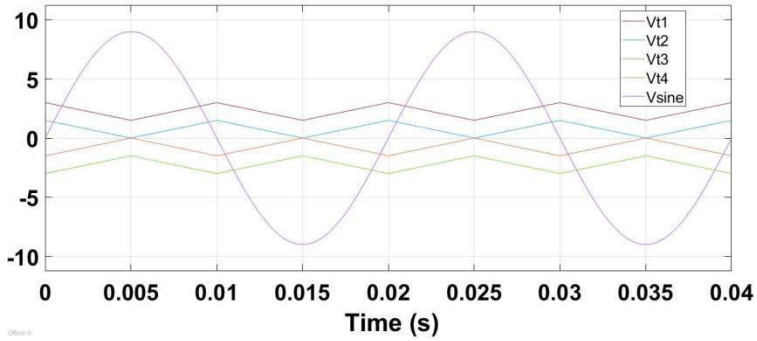


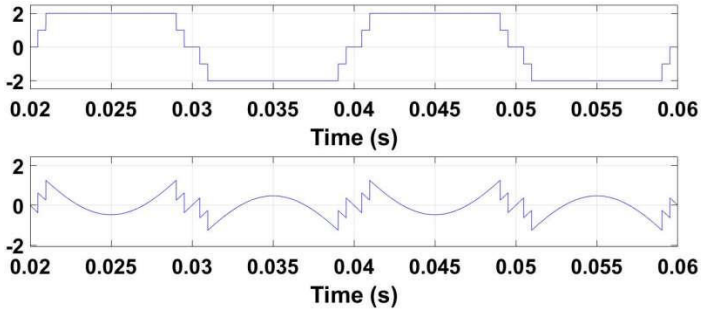
Fig. 3.5 (a) Principle of over-modulated SPWM pulse generation for the main inverter control; (b) Principle of reference generation for SAPF (or compensator)

3.5 Simulation Results

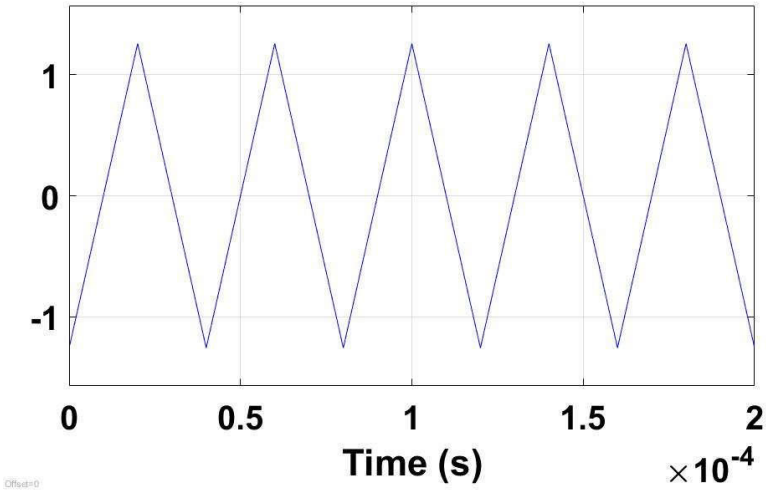
The 5-level inverter in series with 2-level series active power filter is simulated using MATLAB SIMULINK. The first limb of the low-frequency inverter is worked with a two-stepped PWM technique at m=3, whereas the second limb is operated with square pulses. In the simulation the low frequency sine wave with magnitude of 3pu becomes 9V after getting multiplied by modulation index of 3 and is used as the modulating signal with triangular waveforms of 1.5pu magnitude (3V) for the PWM pulses generation of the Main inverter switches. The major control circuit waveforms taken at different points using MATLAB simulation are shown below in Fig. 3.6.


Vt1
Vt2
Vt3
Vt4
Vsine
10
5
0
-5
-10
0
0.005
0.01
0.015
0.02
0.025
0.03
0.035
0.04
Time (s)

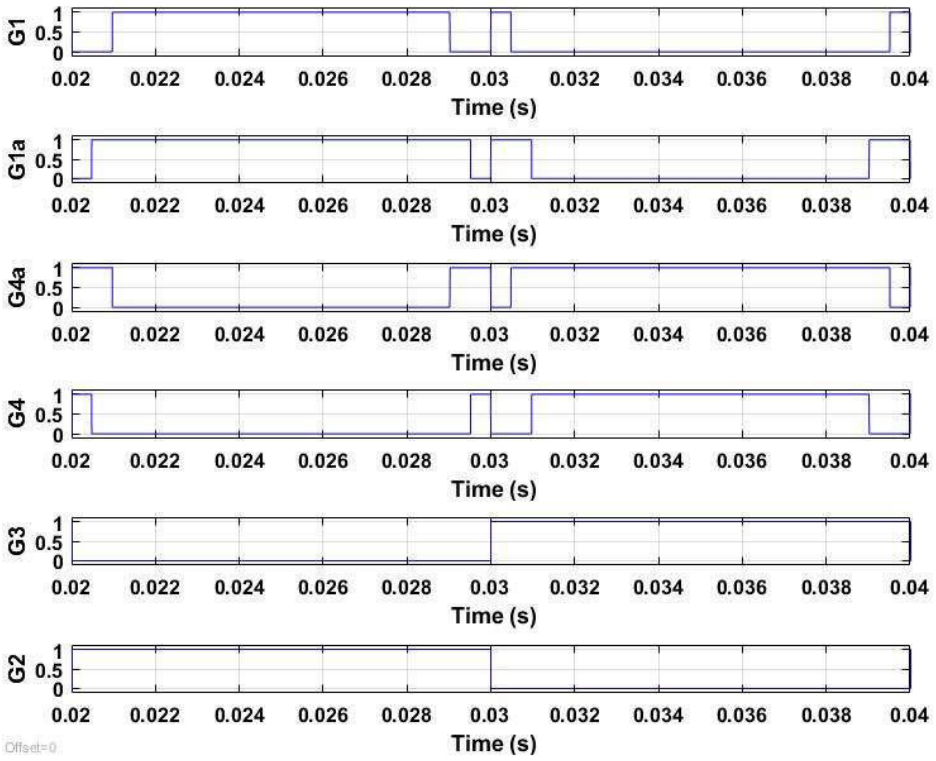
(a)


2
0
-2
0.02
0.025
0.03
0.035
0.04
0.045
0.05
0.055
0.06
Time (s)
2
0
-2
0.02
0.025
0.03
0.035
0.04
0.045
0.05
0.055
0.06
Time (s)

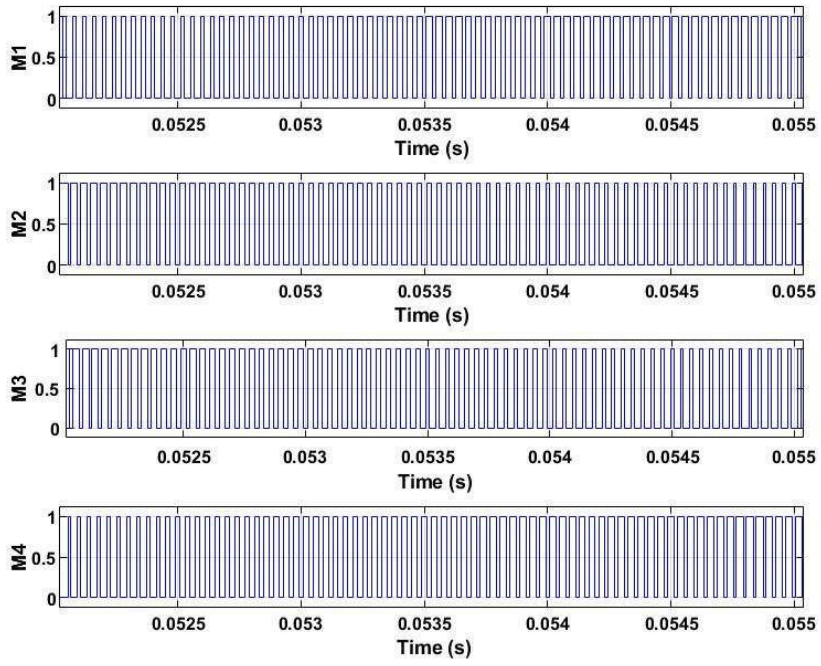
(b)


1
0
-1
0
0.5
1
1.5
2
Time (s)
×10-4

(c)



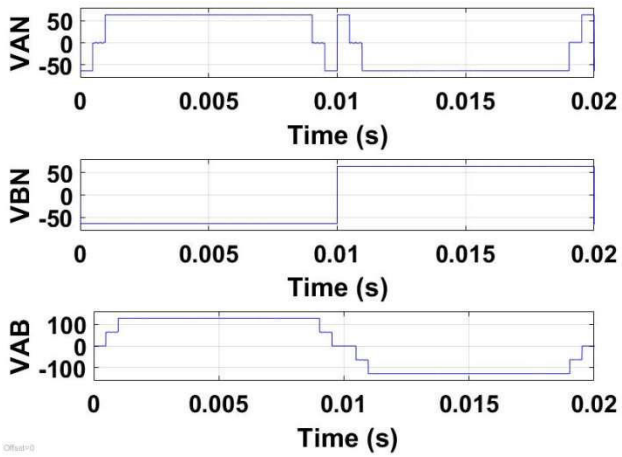
(d)



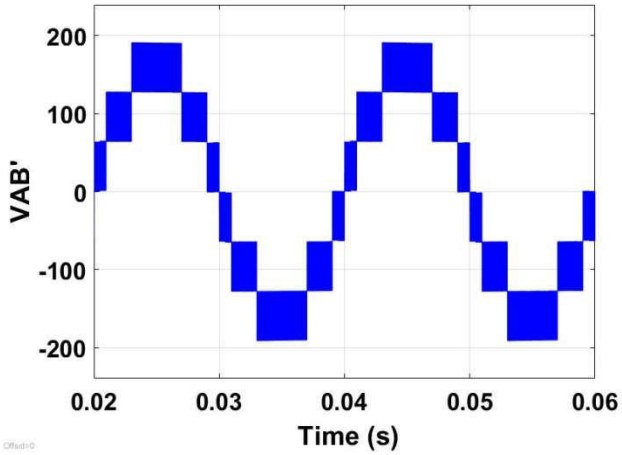
(e)

Fig. 3.6 Simulated waveforms: (a) modulating and carrier signal for pwm in main inverter; (b) top: reference signal for pwm in SAPF; bot: modulating signal for pwm in SAPF; (c) carrier signal for SAPF; (d) different gate signals of the six IGBTs in main inverter; (e) different gate signals of the four MOSFETs in auxiliary inverter

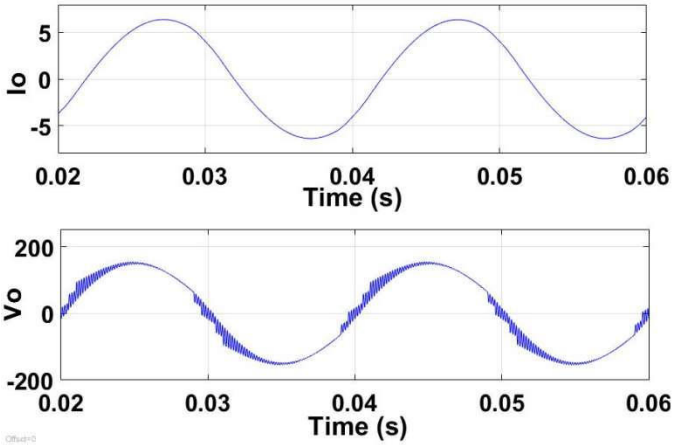
Power Circuit waveforms taken at over-modulation and switching frequency of 25 kHz and THD analysis from the FFT spectrums are shown in Fig. 3.7.



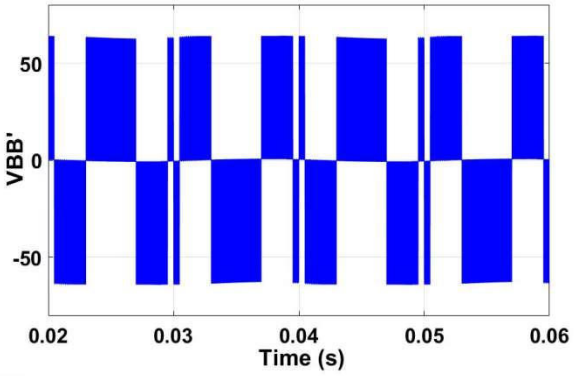
(a)



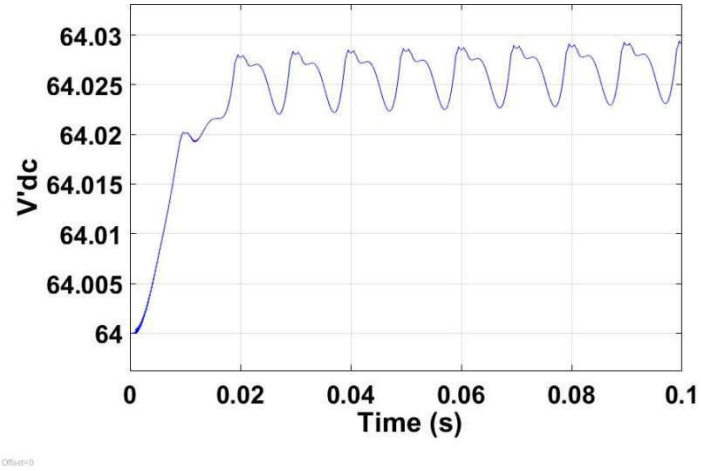
(b)



(c)



(d)



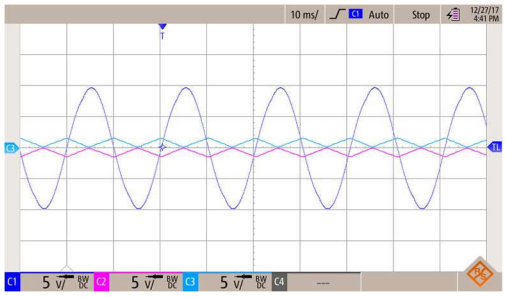
(e)

Fig. 3.7 Simulated waveforms: (a) top: voltage across terminals A & N; mid: voltage across terminals B & N; bot: voltage across terminals A & B; (b) voltage across terminals A & B′; (c) top: load current; bot: output voltage across load; (d) voltage across terminals B & B′ ; (e) output voltage across C3

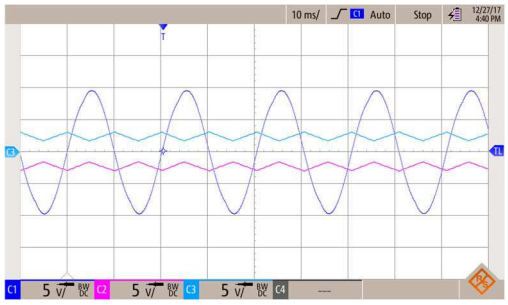
It is observed that the fundamental RMS value of the output voltage of the proposed inverter at no-load is about 112 volts, which is about 87.5% of the DC bus input, depicting the high DC bus utilization.

3.6 Experimental Validation

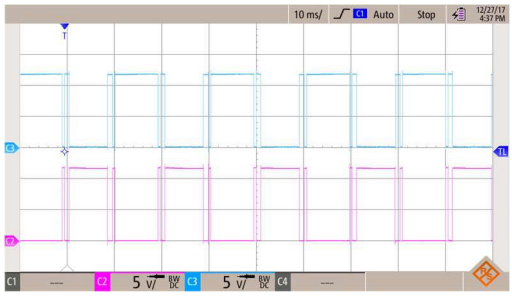
For the experimental verification, a prototype was built in the laboratory with parameters as close as possible to those under simulation as in Table 3.1. The control circuit for the proposed single-phase 5-level main inverter and the 2 level SAPF are attached in Appendix A1.4 and A1.5 respectively. The major control circuit waveforms taken at different points during the time of experimentation are shown below:


10 ms/
Auto
Stop
12/27/17
4:41 PM
C1 5 V/
C2 5 V/
C3 5 V/
C4

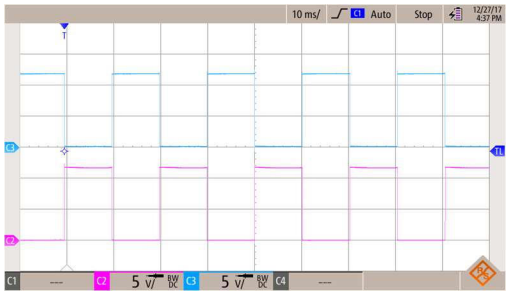
(a)


10 ms/
Auto
Stop
12/27/17
4:40 PM
C1 5 V/
C2 5 V/
C3 5 V/
C4

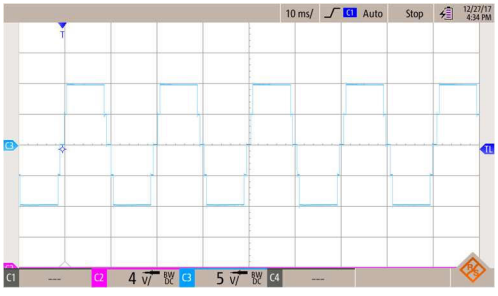
(b)


10 ms/
Auto
Stop
12/27/17
4:37 PM
C1
C2 5 V/
C3 5 V/
C4

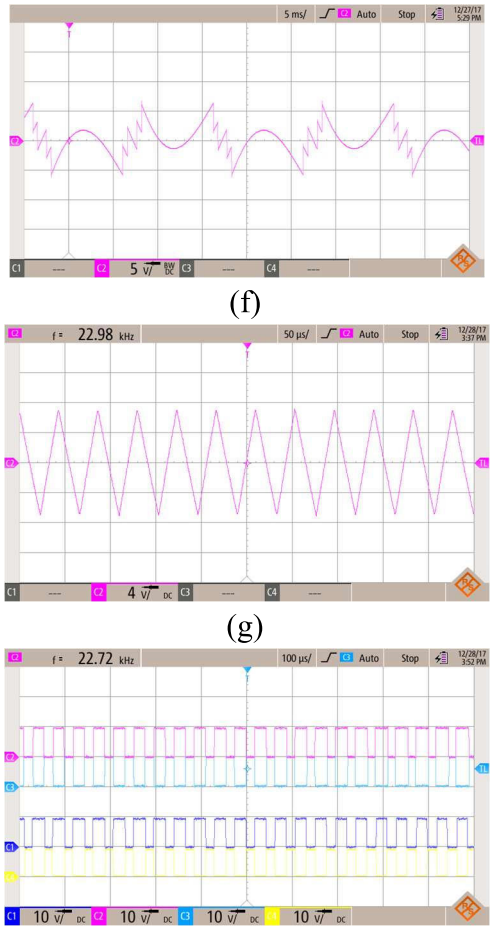
(c)


10 ms/
Auto
Stop
12/27/17
4:37 PM
C1
C2 5 V/
C3 5 V/
C4

(d)


10 ms/
Auto
Stop
12/27/17
4:34 PM
C1
C2 4 V/
C3 5 V/
C4

(e)



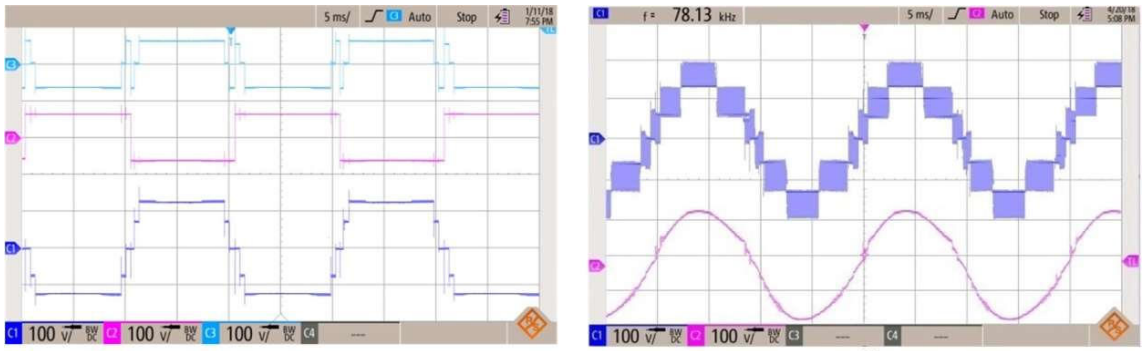
(f)

(g)

(h)

Fig. 3.8 Experimental waveforms: (a) Modulating Signal and Triangular Signal (v_{t2}, v_{t3});(b) Modulating Signal and Triangular Signal (v_{t1}, v_{t4});(c) Gate signals for G4, G1a in Main Inverter;(d) Gate signals for G3, G2 Main Inverter;(e) Reference Signal for SAPF(f) Modulating signal for PWM in SAPF;(g) Carrier Signal for PWM in SAPF;(h) Gate signals for the MOSFETs in SAPF

The experimental waveforms using the parameters of Table 3.1 are shown in Fig. 3.9.



(a) (b)

Fig. 3.9 Experimental waveforms: (a) top: voltage across terminals A & N; mid: voltage across terminals B & N; bot: voltage across terminals A & B; (b) top: voltage across terminals A & B′; bot: output voltage across load

Fig. 3.9 shows the waveforms at different points of the power circuit. Fig. 3.9(a) depicts the voltages of the main inverter, with the top waveform being between terminals A & N, the middle being between terminals B & N and the bottom waveform shows the resulting 5-level waveform across the output of the main inverter. The voltage waveform across the terminals of the main inverter (VAB) is found to have a THD of 28.3%. Fig. 3.9(b) depicts the voltage after compensation, where the top waveform shows the superimposed high-frequency PWM onto the stepped waveform. The voltage THD across this waveform after compensation (VAB′) is found to have a THD of 4.6%, clearly demonstrating the effective removal of voltage harmonics. The bottom waveform of Fig. 3.9(b) shows the filtered sinusoidal output voltage across the load with a THD of 4.5%.

The experimental results are observed to be quite similar to the simulated ones. It is observed that the fundamental output voltage is moderately high as compared to the SPWM inverter. The experimental voltage output has low THD content (4.56%) but has slightly less magnitude than the simulated value due to actual voltage drops in the inverter, compensator, and filter choke. The experimental setup in the laboratory is shown in Fig. 3.10. All the circuit diagrams referred to the hardware modeling are shown in Appendix A1.3

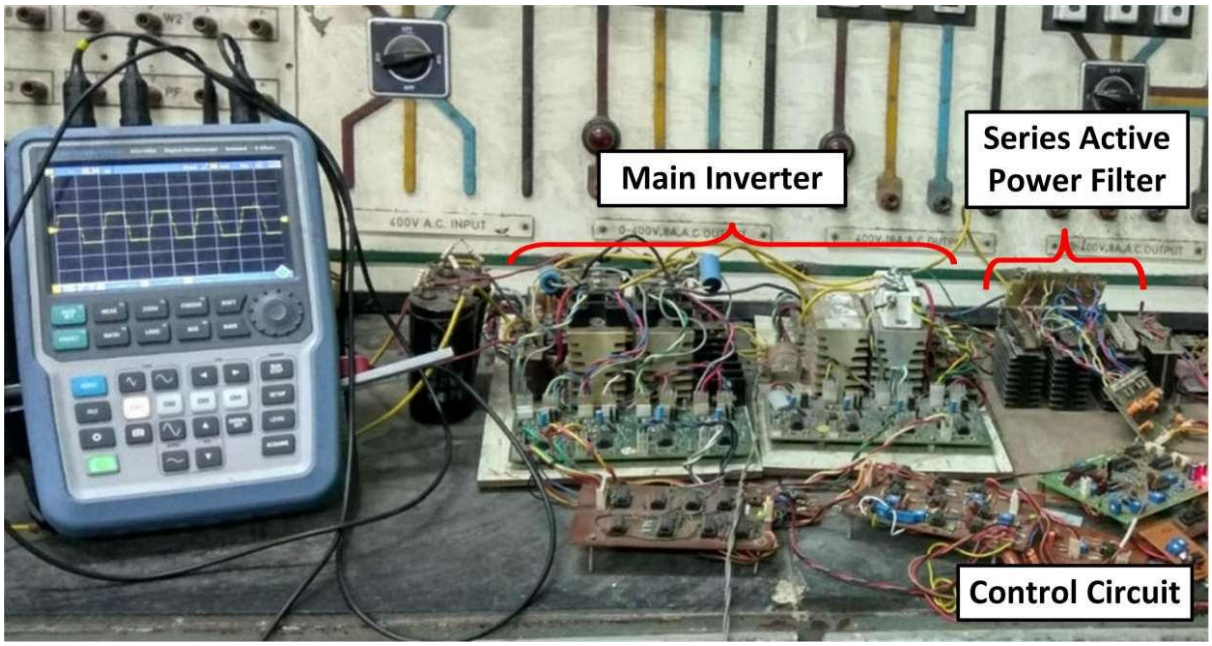


Fig. 3.10 Experimental setup

3.7 Efficiency Calculation

The efficiency (η) of the single-phase inverter is given by

$$\eta = \frac{P_o}{P_i} \qquad 3.5$$

Where, P_o is the output power of the inverter; P_i is the input to the inverter.

Also,

$$P_i = P_o + Loss \quad (3.6)$$

Where, P_o= p.f. x RMS value of fundamental load voltage x RMS value of fundamental load current. Considering the parameter values as shown in table 3.1 and 3.3, a conventional single-phase SPWM inverter is simulated in PSIM software to evaluate the loss and the efficiency of the overall system. For a 500 VA, single phase inverter at 0.8 p.f., the RMS output voltage is 90 volts if the input dc voltage is 128 volts. Assume that the switching frequency is 12 kHz and all the IGBTs used in the inverter circuit will be supported by 128 volts. Considering load current 4.55 A and p.f. 0.8, the load resistance and load inductance are calculated as 19.38 Ω and 46.24 mH using the following equations 3.7 and 3.8.

$$\text{Impedance(Z)} = \frac{\text{Fundamental RMS load voltage}}{\text{Fundamental RMS load current}} \quad (3.7)$$

$$p.f. = \frac{R}{Z} \quad (3.8)$$

Therefore, P_o=0.8x90x4.55=325.51 watt and loss=16.96 watt (see Appendix A). Hence, from equation 3.6, P_i can be calculated as 342.43 watt and efficiency is 95.1% using equation 3.5. Similarly, for the 5-level proposed inverter with a SAPF, using the same load current, the output RMS ac voltage is obtained as 111 volts. Here, four IGBTs in limb one of the main inverter are supported by 64 volts at the switching frequency of 100 Hz and the two IGBTs used in the second limb will be supported by 128 volts at the switching frequency of 50 Hz. The MOSFETs used in the SAPF will be supported by reduced voltage of 64 volts each at the switching frequency of 25 kHz. Hence, from equation 3.6, P_o can be calculated as P_o=0.8x111x4.55=404.04 watt and Pi can be calculated as 426.2 watt (P_i=404.04+22.16=426.2 watt) respectively where loss is 22.16 watt (see Appendix A), and thus efficiency is 94.8% using equation 3.5.

3.8 Comparison of Performance

To evaluate the performance of the proposed inverter, its parameters and components were fixed as given in Table 3.1.

Table 3.1 Values of Parameters and Component Ratings of System Studied

Parameter	Value	Component	Rating
Input DC voltage (V_{dc})	128 V	IGBTs	20 A, 400V
Main inverter fundamental frequency	50 Hz	DC bus capacitors C1 & C2 (each)	2200 µF
Main inverter switching frequency	100 Hz	MOSFETs	20 A, 150V
DC bus voltage of SAPF (V'_{dc})	64 V	DC bus capacitors C3	2200 µF
SAPF switching frequency	25 kHz	Filter inductor L	350 µH
Load VA	500	Filter capacitor C	2 µF
Load power factor	0.8	Load resistance	19.4 Ω
		Load inductance	46.3 mH

The simulated results are compared with those from experimentation in Table 3.2. The results will be observed to be close to each other.

Table 3.2 Comparison between Simulation and Experimental results

Parameter	Simulation Results	Experimental Results
Input DC voltage (V_{dc})	128 V	128 V
Main inverter fundamental voltage	112 V	111 V
SAPF DC bus voltage (V'_{dc})	64 V	64.1 V
Load voltage	111 V	109.5 V
Load current	4.55 A	4.54 A
Output voltage THD	4.51 %	4.56 %

Table 3.3 Comparison with Conventional SPWM Inverter

Parameter	SPWM Inverter	Proposed Inverter
Input DC voltage	128V	128V
Number of switches	4 IGBTs to support 128V	2 IGBTs to support 128V + 4 IGBTs to support 64V + 4 MOSFETs to support 64V
Switching frequency	All switches at 12kHz	2 switches at 50Hz, 4 switches at 100Hz, 4 switches at 25kHz
Output AC RMS voltage (after the filter)	90	111V
Output voltage THD (after the filter)	4.45 %	4.51 %
Load Current	4.55 A	4.55 A
Efficiency	95.1%	94.8%

The performance of the proposed inverter is compared with that of a conventional SPWM inverter under simulation. The results are tabulated in Table 3.3. It will be observed that the proposed inverter is far superior in terms of DC bus utilization, providing a 123% higher

output fundamental voltage than the SPWM inverter from the same DC supply while maintaining almost the same efficiency and same output voltage THD.
Even though the proposed inverter has a higher number of switches that increases the total conduction losses, overall total losses are comparable to the SPWM inverter. This is because of all the switches in the proposed inverter scheme, several of them switch at a low frequency only, while several face only an approximate 50% blocking voltage when compared to all the switches in the SPWM inverter, thereby creating lower switching losses.

3.9 Applications

In this work, the main inverter topology utilizes one limb at square wave switching and the second limb uses four switches to create a 5 level output with higher dc bus utilization than conventional SPWM inverters. Thus switching losses are low but conduction losses are higher, resulting in almost comparable efficiency with conventional SPWM inverters. A special technique of natural harmonic compensation brings down the THD within tolerable limit by IEEE 519 standard. Thus the overall system is a replacement for SPWM inverters wherever high dc bus utilization with low THD output voltage is required. The proposed inverter system at fixed frequency can be used in several applications as backup power supply to critical equipment or synchronized to the AC grid for power support as distributed generation (DG) from renewable energy sources.

3.10 Conclusion

A new 1-phase sine-wave inverter system with high utilization of DC bus is presented along with a series active power filter controlled through feed-forward control based on natural harmonic compensation, operating from a single DC source. This inverter can generate higher fundamental voltage than traditional simple inverters due to operation in over modulation mode with voltage THD less than 5% and comparable efficiency, using a simple control strategy. The main inverter uses six IGBT switches with low switching frequency and PWM with only two steps per half cycle to reduce its switching losses. A resulting 5-level output voltage controls the lower order harmonics in output voltage along with high DC bus utilization. The series active power filter uses four MOSFET switches at higher switching frequencies to create a composite harmonic voltage across its output to cancel those in the main inverter output when connected in series. Due to the use of the principle of natural compensation, the charge on the compensator capacitor can be maintained naturally using a simple feed-forward control only without an external DC voltage supply or complex feedback control. The DC bus voltage build-up in the compensator is less than the DC voltage input, which is possible due to the stepped nature of the inverter voltage waveform. The series active power filter thus has low switching loss due to its own DC voltage being only about 50%

compared to the input DC. A small LC low-pass filter is used to remove components of SAPF PWM switching frequency and residual voltage waveform imperfections due to higher harmonics that are not tackled by the SAPF circuit. The complete inverter system with a higher AC voltage from a given DC voltage input is directly suitable for fixed frequency backup power supply and also for other applications like renewable energy connection to the power grid.

CHAPTER – FOUR

Three Phase PWM Inverter with High DC Bus Utilization using Natural Harmonic Compensation

4.1 Introduction

The dc-ac power converters are utilized in variable speed drives (VSDs), flexible ac transmission systems (FACTSs), static VAR compensators, active power filters, uninterruptible power supplies (UPSs), and auxiliary voltage compensators [38, 39]. Almost in all ac drives, sinusoidal ac outputs are needed in which the magnitude, frequency, and phase of the output ac has to be adjusted. These topologies are the most commonly used as they behave naturally as voltage sources which may be required by several industrial applications, eg., VSDs, that are one of the most accepted application of inverters (Fig. 4.1a) [6]. Similarly, such configurations may be located as current-source inverters (CSIs) with the output ac as a controlled current waveform. A Pulse Width Modulated (PWM) voltage waveform is drawn in Fig.4.1c. Since, sinusoidal wave is not seen as expected in (Fig. 4.1b), its fundamental component should behave like that. This action should be ensured by a modulation technique that regulates the amount of time and the switching states. The modulating schemes are mostly used as the carrier-based technique (e.g. selective-harmonic-elimination (SHE) technique, sinusoidal pulse-width modulation (SPWM) and the space-vector (SV) modulation technique, as discussed in chapter 1. Also a capacitor at load side creates voltage spikes and to reduce these, an inductor filter between inverter output and ac load should be connected.

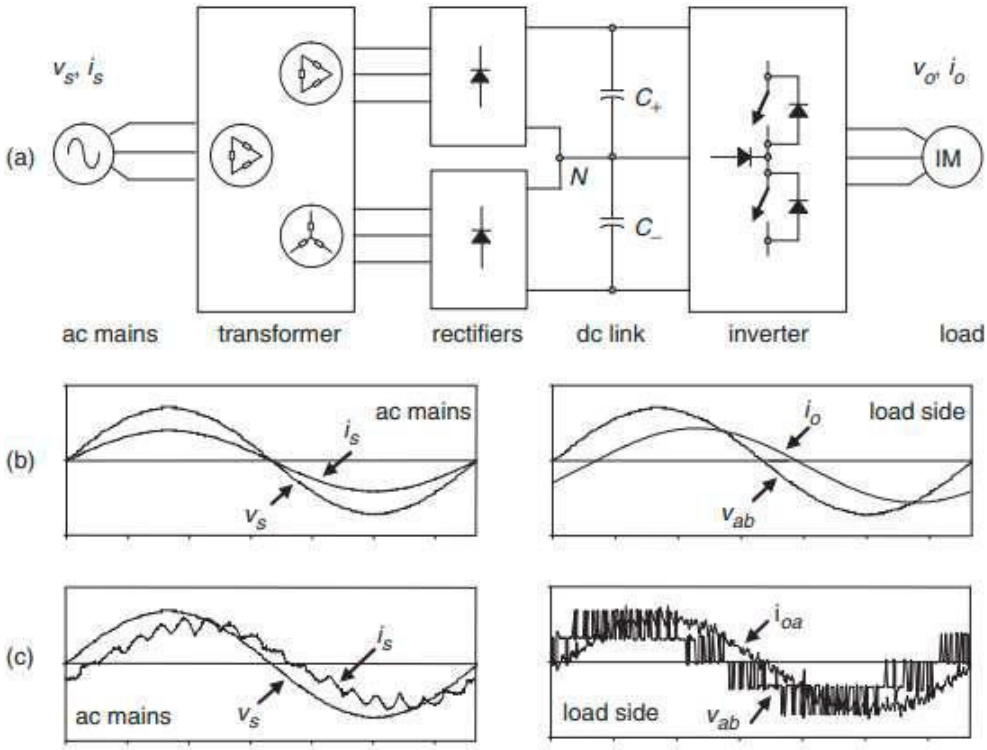


Fig. 4.1 Waveforms of an adjustable speed drive system: (a) block diagram of electrical power conversion; (b) the ideal input and output waveforms; and (c) the actual input and output waveforms

All practical inverters produce non sinusoidal output voltage waveforms which contains harmonics. Square wave and quasi square wave inverters are popular in low and medium power applications and hence not used in transformer and motor loads as it would heat up the core material because of its large harmonic content. To control the ac output voltage an index called the modulation index is defined as

$$m = \frac{V_1}{V_{dc}} \qquad 4.1$$

where V_1 is the maximum value of the fundamental component; V_{dc} the value input DC. The harmonic index h_n for the nth harmonic is defined as

$$h_n = \frac{V_n}{V_1} \qquad 4.2$$

where, V_n is the maximum value of the nth harmonic; V_1 the maximum value of the fundamental component.

The objective of pulse width modulation in three phase inverters is to create near sinusoidal waveform. In three-phase PWM inverters the balanced three phase output can be obtained by comparing three sinusoidal voltages which are 120˚ phase apart using a single triangular voltage waveform as shown in Fig. 4.2(a).

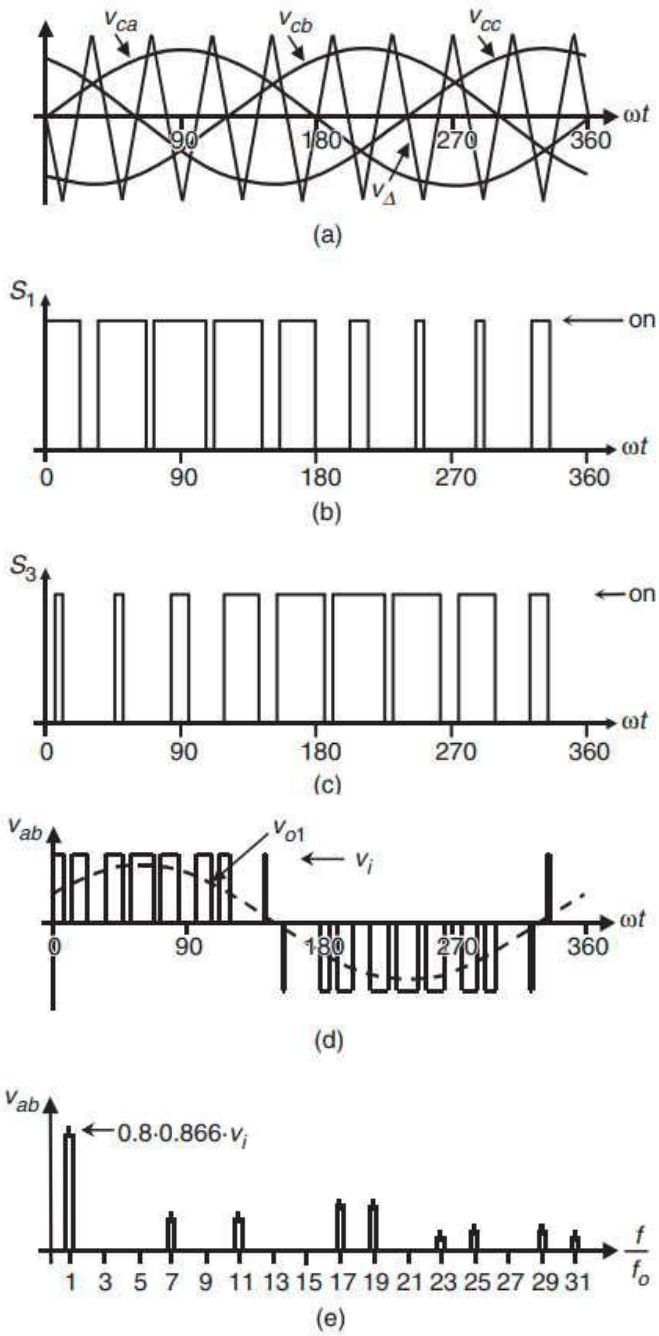


Fig. 4.2 Ideal waveforms for the SPWM in 3-phase VSI. (m_a = 0.8): (a) modulating and carrier signals; (b) state of switch S_1; (c) state of switch S_3; (d) output ac voltage; (e) spectrum of line voltage

Figure 4.2(b) and (c) shows the switching patterns of the switches S_1 and S_3 in a three phase inverter respectively as shown in Fig. 1.5. Fig. 4.2 (d) depicts the line to line voltage V_{ab} waveform which is a SPWM signal. Fig. 4.2(e) presents the harmonic spectrum of the signal V_{ab} which gives the maximum value of the fundamental ac output signal as $m_a(\frac{\sqrt{3}}{2})V_i$.

Thus it can be stated that the peak of the fundamental line voltage is expressed as

$v_{ab1} = m_a\sqrt{3}\frac{V_i}{2}$, $0<m_a\leq 1$ 4.3

In the over-modulation region, the line voltage lies between

$$\sqrt{3}\frac{V_i}{2} < V_{ab1} = V_{bc1} = V_{ca} < \frac{4}{\pi}\sqrt{3}\frac{V_i}{2} \quad 4.4$$

The PWM considerations in three phase inverter can be summarized in following ways:

A. Linear modulation ($m_a\leq 1.0$):

From Fig. 4.2 (d), the maximum value of the fundamental voltage in one limb of the inverter is given by

$$V_{ab1} = m_a\left(\frac{V_i}{2}\right) \quad 4.5$$

Therefore, the line to line RMS can be given as

$$V_{LL1} = \frac{\sqrt{3}}{2\sqrt{2}} m_a V_i = 0.612 m_a V_i \quad 4.6$$

B. Over-modulation ($m_a>1.0$):

Sinusoidal PWM in linear range pushes the harmonics to high frequency range around the switching frequency or its multiples. But the major demerit is the reduction of amplitude of fundamental voltage which creates notches in the output waveform. Thus with the increase in m_a linearly, fundamental frequency increases. Also it is seen from Fig. 4.3 that the amplitude of fundamental frequency component does not vary linearly. At over-modulation, PWM inverter acts like a square wave inverter resulting V_{LL1} (peak) equal to $0.78V_i$. Since the dominant harmonics may not have the large amplitude as compared to linear modulation, the power loss in the load at harmonic frequencies may not be high.

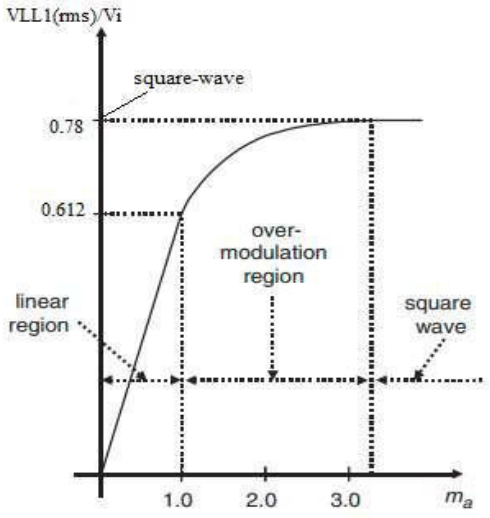


Fig. 4.3 V_{LL1}(rms)/V_i as a function of m_a in three phase inverter

Fig. 4.4 depicts the waveforms of the three-phase ideal VSI with SVPWM as discussed in chapter 1.4.4. Assuming the inverter has no loss it can be illustrated that

$$v_i.i_i = v_{ab}.i_a + v_{bc}.i_b + v_{ca}.i_c \quad 4.7$$

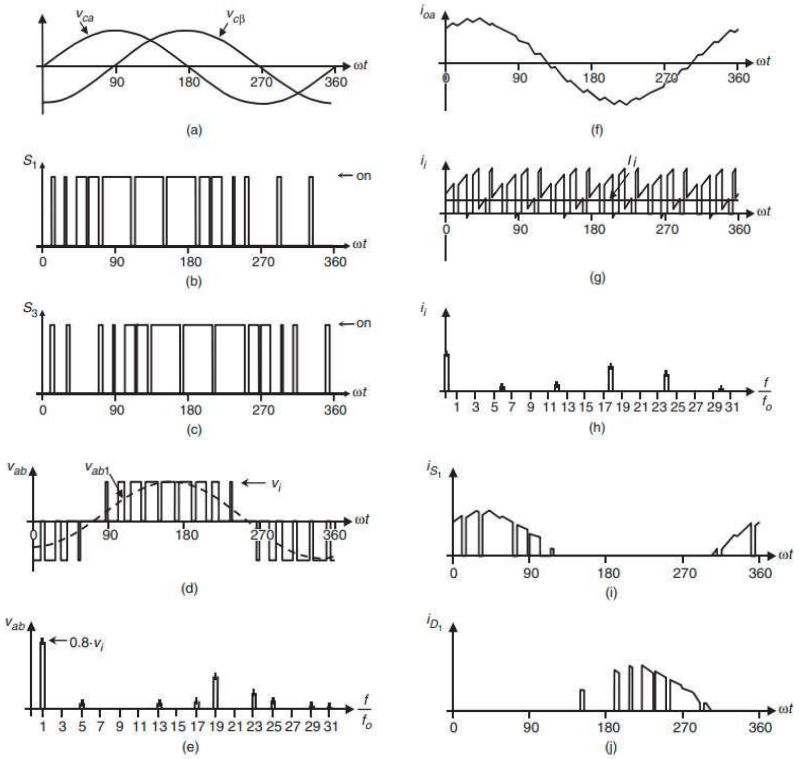


Fig. 4.4 Ideal waveforms with SVPWM in 3-phase VSI,: (a) modulating waveforms; (b) state of switch S_1; (c) state of switch S_3; (d) output ac voltage; (e) voltage spectrum of output ac; (f) output ac current; (g) input dc current; (h) spectrum of dc current; (i) current through switch S_1; and (j) current through diode D_1

where i_a, i_b, and i_c are the per phase currents as drawn in Fig. 4.5. Assuming the load inductive and the dc input voltage is considered fixed at $v_i = V_i$, Eq. (4.7) can be reduced to

$$i_i = \frac{1}{V_i}\left[\sqrt{2}V_{o1}\sin(\omega t).\sqrt{2}I_o\sin(\omega t-\varphi)+\sqrt{2}V_{o1}\sin(\omega t-120°).\sqrt{2}I_o\sin(\omega t-120°-\varphi)+\sqrt{2}V_{o1}\sin(\omega t-240°).\sqrt{2}I_o\sin(\omega t-240°-\varphi)\right] \quad 4.8$$

Where, V_{o1} is the RMS value of the ac line voltage fundamental component, Io is the RMS value of the load current, and φ is the power factor of load. Thus, the expression for the input current is as

$$i_i = 3\frac{V_{01}}{V_i}I_0\cos(\varphi) = \sqrt{3}\,\frac{V_{01}}{V_i}I_l\cos(\varphi) \quad 4.9$$

where $I_l = \sqrt{3}Io$ is the RMS value of load current.

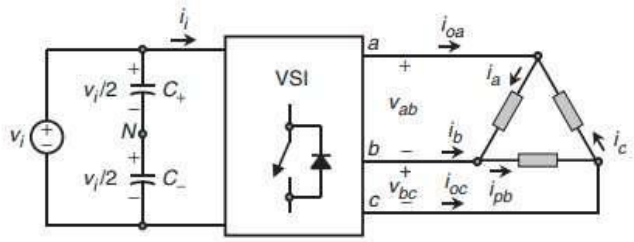


Fig. 4.5 A VSI with a load connected in delta

The star connected load is used as shown in Fig. 4.6 and voltages across load can be given as

$$\begin{bmatrix} v_{ab} \\ v_{bc} \\ v_{ca} \end{bmatrix} = \begin{bmatrix} v_{an} - v_{bn} \\ v_{bn} - v_{cn} \\ v_{cn} - v_{an} \end{bmatrix} \quad 4.10$$

The above may be given as a function of the phase voltage vector $[v_{an}\ v_{bn}\ v_{cn}]^T$ as

$$\begin{bmatrix} v_{ab} \\ v_{bc} \\ v_{ca} \end{bmatrix} = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \end{bmatrix} \quad 4.11$$

Eq (4.11) can be further expressed as

$$\begin{bmatrix} v_{ab} \\ v_{bc} \\ 0 \end{bmatrix} = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ 1 & 0 & 1 \end{bmatrix} \begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \end{bmatrix} \quad 4.12$$

which is not singular and hence,

$$\begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \end{bmatrix} = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ 1 & 0 & 1 \end{bmatrix}^{-1} \begin{bmatrix} v_{ab} \\ v_{bc} \\ 0 \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 2 & 1 & 1 \\ -1 & 1 & 1 \\ -1 & -2 & 1 \end{bmatrix} \begin{bmatrix} v_{ab} \\ v_{bc} \\ 0 \end{bmatrix} \quad 4.13$$

that can be further simplified to

$$\begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 2 & 1 \\ -1 & 1 \\ -1 & -2 \end{bmatrix} \begin{bmatrix} v_{ab} \\ v_{bc} \end{bmatrix} \quad 4.14$$

Figure 4.7 depicts the line and phase voltages respectively using Eq. (4.14).

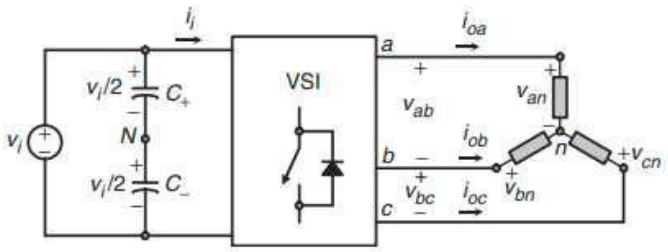


Fig. 4.6 A VSI in a star connected load

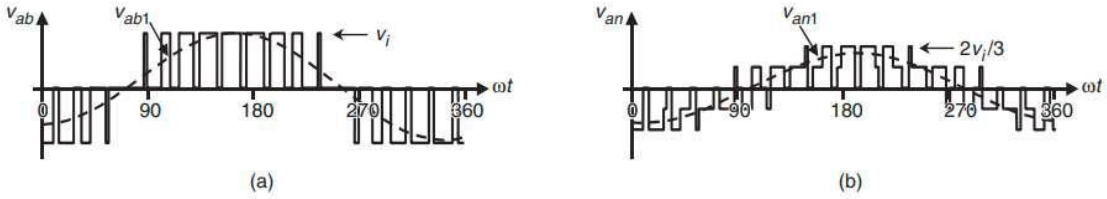


Fig. 4.7 Line- and phase voltages of the three-phase VSI.: (a) line voltage Vab ; (b) phase voltage Van

From the above discussion it can be said that three phase inverters with pulse width modulation scheme produce a voltage at the output whose fundamental RMS value is lower than the DC bus input voltage. This implies ineffective DC bus utilization. Further, harmonics generated by the inverter are attenuated at the final output by the use of low-pass LC filters to create near-sinusoidal voltage. In order to reduce the size of the filter, the switches are operated at higher switching frequency, causing higher switching losses. On the other hand, low switching frequency stepped wave inverters produce higher DC bus utilization with lower switching loss at the cost of higher amount of lower order harmonics.

Several research works had undergone to reduce THD with high dc bus utilization in three phase inverters [10, 15, 23, 42]. Three phase infinite level inverter with third harmonic injection scheme can be used to increase dc bus utilization as compared with PWM inverters [14]. Harmonics can be eliminated using Multi-level inverters, but at the expense of more number of switches and separate dc bus voltages [1-4]. Six pulse modulation schemes in three-phase inverter as compared to SPWM technique also improve dc bus utilization. Selective Harmonic Elimination (SHE) techniques can be used for high dc bus utilization and low switching losses but only selected lower order voltage harmonics are eliminated while output voltage control is not possible.

A square wave inverter has the lowest switching frequency with highest DC bus utilization, but has high harmonic content. The concept of using a high switching frequency inverter in series with the main inverter was introduced to eliminate the harmonics of a square wave inverter [43-46]. This resulted in high dc bus utilization with moderate overall switching loss. However, the dc bus of the additional inverter needs an isolated supply. The principle of mitigation of harmonics using the natural process of maintaining the DC bus of the series connected high switching frequency inverter introduced a new method for generation of sinusoidal voltages without use of separate floating dc supply for the series compensator.

The proposed new three-phase PWM inverter system comprised of presented here is based on

the principle of natural compensation of a stepped waveform, resulting in high dc bus utilization and a small filter to achieve a low THD voltage waveform output. Due to the use of stepped waveform, the DC bus voltage of the compensator is required to be less than that of the inverter DC bus, permitting the use of lower voltage, higher switching frequency devices in the compensator in order to achieve low switching loss. Such inverter is proposed to be used in three phase Dynamic Voltage Restorers (DVR) [5] for boosting of sagging supply line voltages.

4.2 The Proposed Three Phase Inverter

The topology of the proposed 3-phase inverter system is presented in Fig. 4.8. The proposed inverter uses three numbers of 1-phase half bridge inverters, operating in parallel from a common dc source, each phase output being connected in series with a two level active compensator providing natural compensation of the major harmonics generated by the inverters using feed-forward mode.

The R-L load is star (or Y) connected and the inverter control is designed to produce a stepped voltage waveform across each phase of the load. This ensures high DC bus utilization and low switching frequency of inverter IGBT switches, as explained later.

The series connected compensators uses a single phase H-bridge using four MOSFETs with a dc bus capacitor. The devices in the compensator circuit must switch at a frequency higher than that of the main inverter in order to achieve compensation of the main inverter output.

A small L-C low pass filter is connected across each phase of the final compensated output, in order to smoothen the voltage waveform by removing the compensator switching frequency component. Hence the filter size is quite small compared to what would have been needed to extract a sine wave from the basic stepped waveform of the inverter.

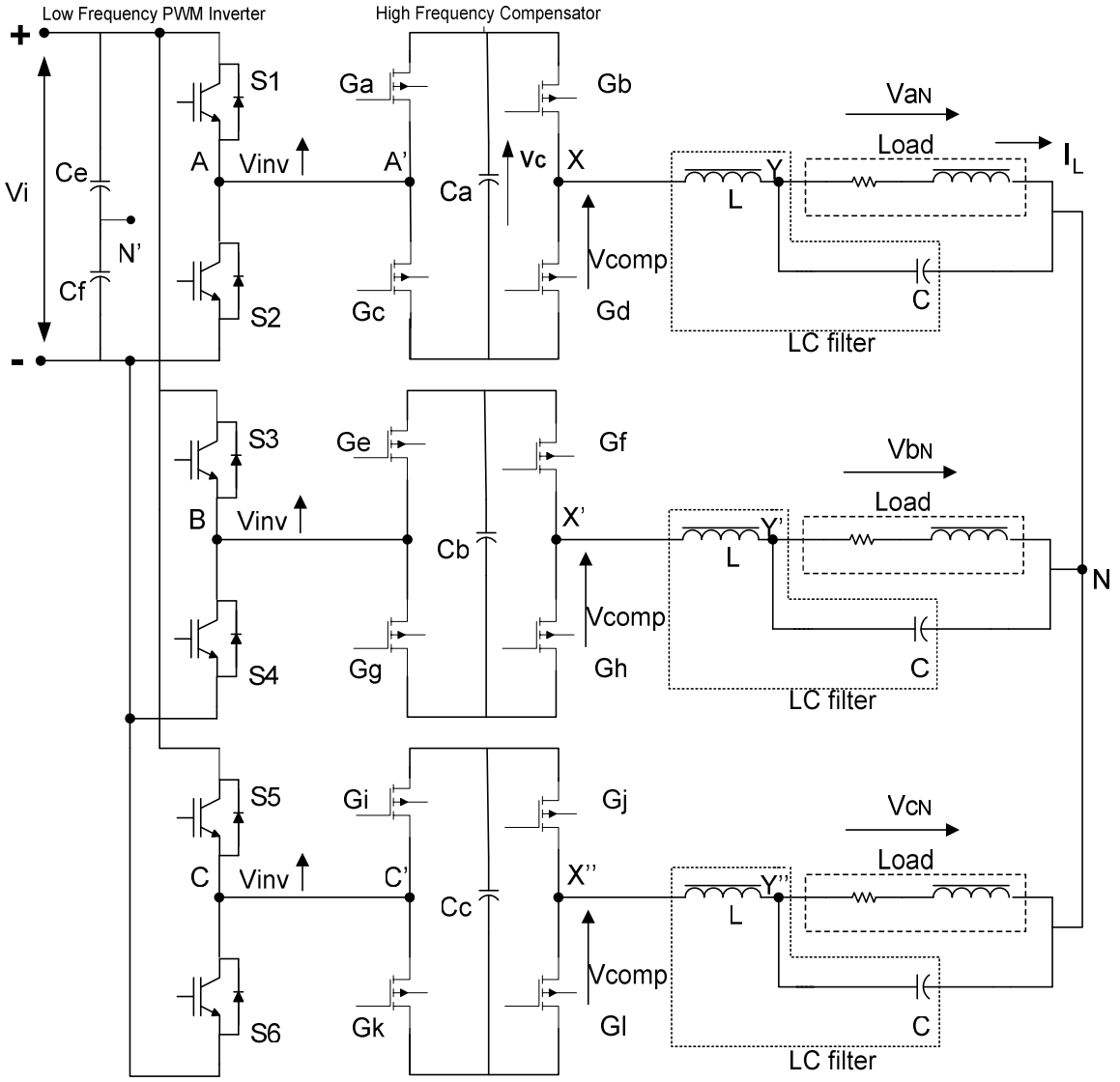


Figure 4.8 Power circuit diagram of proposed three phase PWM inverter

4.3 The Operating Principle of Proposed Inverter

Consider the three phase main inverter to be made up of three numbers of single phase half bridges, using two switches and output of each limb is connected to a series compensator followed by a small low-pass filter as shown in Fig. 4.9.

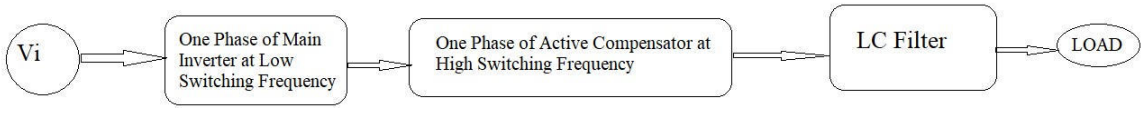


Figure 4.9 Single line diagram of one phase of proposed inverter system

The voltage created by switches of one phase of main inverter, with respect to load neutral,

can be given in terms of its fundamental and harmonics as:

$V_f = \sum_{n=1,3,5,..}^{\infty} V_{nm} \sin n\omega t$ 4.15

The voltage generated by switches of the harmonic compensator, can similarly be given in terms of its harmonics as:

$V_h = \sum_{n=3,5,..}^{\infty} V_{nm} \sin n\omega t$ 4.16

When the magnitude of the harmonics present in the two waveforms are equal and opposite to each other, the final output can be given as:

$V_{out} = V_f - V_h = V_{1m} \sin(\omega t)$ 4.17

The harmonics generated by main three phase inverter will thus be compensated through the presented technique without the need for a large low-pass filter at the output, creating a final voltage which is the sinusoidal fundamental generated by the low frequency switching of the main three phase inverter. This waveform can be fed to a three phase induction motor, with resulting near-sinusoidal current waveforms. However the use of an added small size low-pass filter to remove the switching frequency components, creates a good quality sine-wave for other three phase applications.

The principle of natural compensation [43-46] permits the use of only a charged dc bus capacitor Ca to maintain the output waveform of the compensator, without the use of separate dc supply. This can be explained by assuming that if only fundamental current is now flowing through the load due to complete compensation, then at the compensator output, no active power is contributed by the harmonic voltages only that are created by the compensator.

Since the voltage harmonics of inverter are compensated before reaching the load, it is possible to create fundamental of large amplitude than what can be generated by conventional PWM control from the same DC bus. Hence, a special modulation scheme per phase is chosen in this work to achieve highest DC bus utilization with minimum switching loss. For three phase PWM operation at over-modulation with low switching PWM scheme, the waveform is decomposed into a square wave and hence, line to neutral voltage is stepped in nature like a square wave inverter, having a theoretical fundamental amplitude of $2/\pi$ times DC bus voltage (i.e., RMS phase voltage is 45%) and the line to line voltage has a fundamental of theoretical magnitude of $2\sqrt{3}/\pi$ times DC bus voltage (i.e., RMS phase voltage is 77.9%).

Since the line to neutral voltage is stepped in nature, it permits the dc bus capacitor of the compensator to maintain lower input dc bus voltage across it [45-46]. This permits the use of lower voltage, higher frequency switching devices than what is needed in the main inverter. Due to the lower operating voltage of the compensator, its switching loss will not be very high.

A square wave-shape of the voltage of magnitude $\pm V_i/2$ is created at the midpoint of each half-bridge inverter with respect to the input dc bus mid-point. All three units are connected with the same input dc bus to develop similar square outputs at the midpoint of the limbs but shifted by $2\pi/3$ radians in order to achieve a three phase balanced output voltage across the output.

When the top switch S1 of the first half bridge limb is turned on, the bottom switch S2 must

be turned off as shown in Fig. 4.10. The logic is same for the other two units. A small dead band is provided between the switching to prevent unwanted shoot-through fault due to simultaneous on-condition of both the switches.

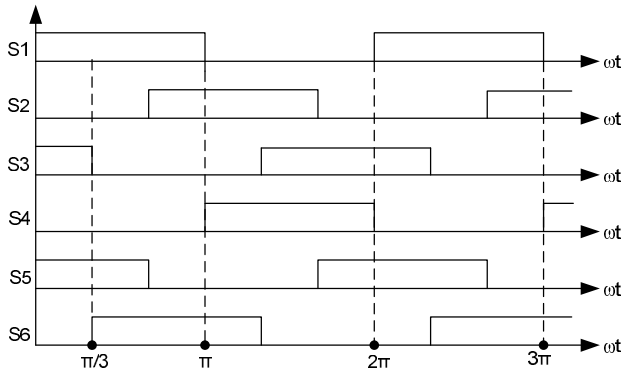


Figure 4.10 Switching pulses for the three phase inverter

Since the load is balanced and star connected, the voltage at the output of each inverter phase with respect to the load neutral (across the terminals A′& N of Fig. 4.8) appears as a stepped waveform as shown in Fig. 4.11. The step heights are $V_i/3$ and $2V_i/3$.

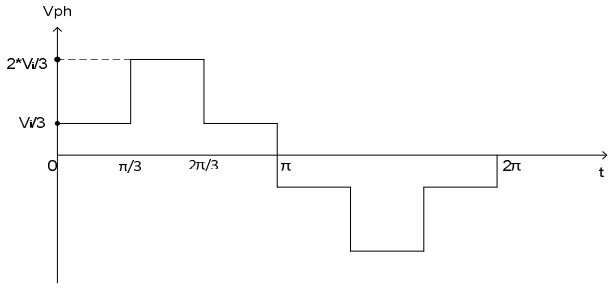


Figure 4.11 Stepped voltage waveform across terminals A′ & N

The phase voltage thus created at the output of main inverter comprises of fundamental as well as harmonics. The harmonics are removed by using a series connected active compensator at the output of each phase. The active compensator comprises of switches Ga to Gd, that creates a two level waveform (which is pulse width modulated at a frequency higher than that of inverter) between points A′ & X, consisting of identical order and magnitude of harmonics that was generated between A′ & N, other than being opposite in phase. This cancels the voltage harmonics in series opposition, leaving the fundamental voltage and the added switching frequency component between the terminals X & N.

The high PWM switching frequency component of the switches Ga to Gl of compensator will be however also present across the load and a small filter is needed to attenuate it in order to obtain a cleaner waveform.

As the load current is almost sinusoidal, due to the fundamental component, active power is

drawn only from the dc source through the output of three phase main inverter comprising of switches S1, S2′, S3, S4, S5 and S6 as it contains fundamental voltage. The active compensator comprising of switches Ga, Gb, Gc and Gd operating from an energy storage dc bus capacitor Ca, does not generate any fundamental voltage and hence cannot provide active power. Thus, the average charge on capacitor Ca remains constant at a value depending on the modulation of compensator, amount of harmonic and the input dc supply. Charging and maintenance of charge is automatic [46].

4.4 Control Pulse Generation Scheme

The two cascaded switching circuits are used for different objectives and hence switch in different modes. Switches of the main three phase inverter are operated at low frequency to create a desired fundamental content. Switches of the series compensator are operated at higher frequency PWM so as to nullify the lower order harmonics generated by the main 3-phase inverter.

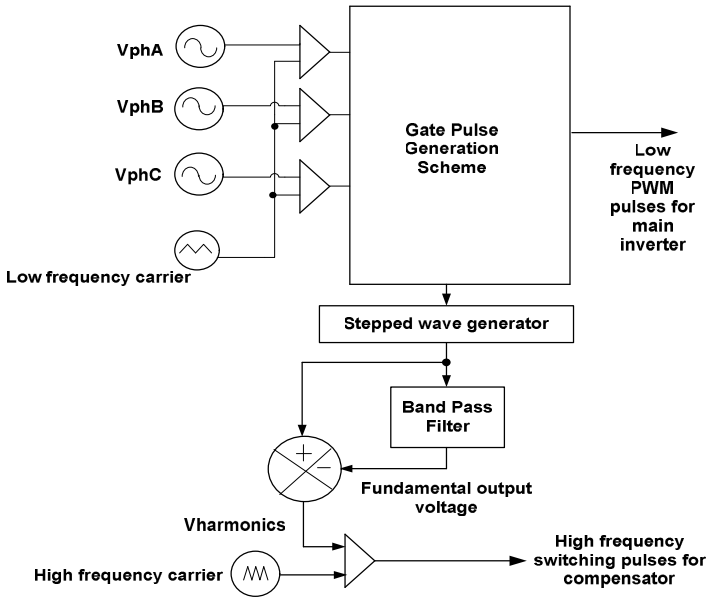


Figure 4.12 Block diagram of control scheme for generation of gate pulses for main inverter and compensator

Fig. 4.12 presents the block schematic of the control scheme for generation of gate pulses for one phase of the proposed system. First a low frequency triangular wave is compared with a sine wave at power frequency to generate PWM switching pulses of the main inverter (say, phase A). Then a reference stepped waveform for the low switching frequency inverter is generated. From the reference waveform for the main inverter, the output line to load neutral voltage waveform is synthesized within the control circuit. Then, the fundamental content of the synthesized waveform is extracted using a band pass filter and further subtracted from the reference waveform, thereby leaving only the harmonics ($V_{harmonics}$). This resulting waveform

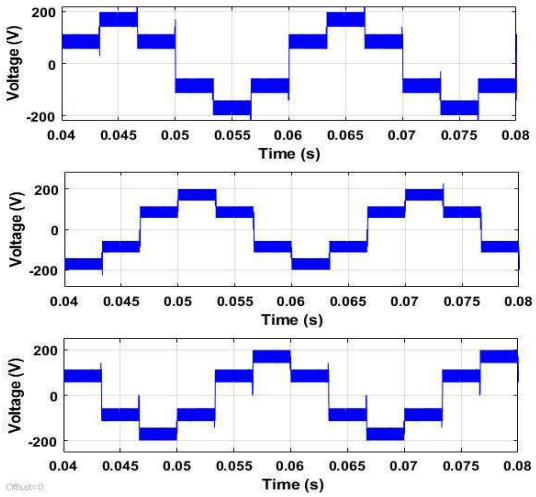
is used further as the reference signal to create the power waveform that will be created across the terminals A & X of the active compensator. This is now compared with a high frequency triangular carrier to generate the switching pulses for the switches Ga, Gb, Gc and Gd. The control pulses of the other two phases are generated in a similar way.

4.5 Performance Analysis

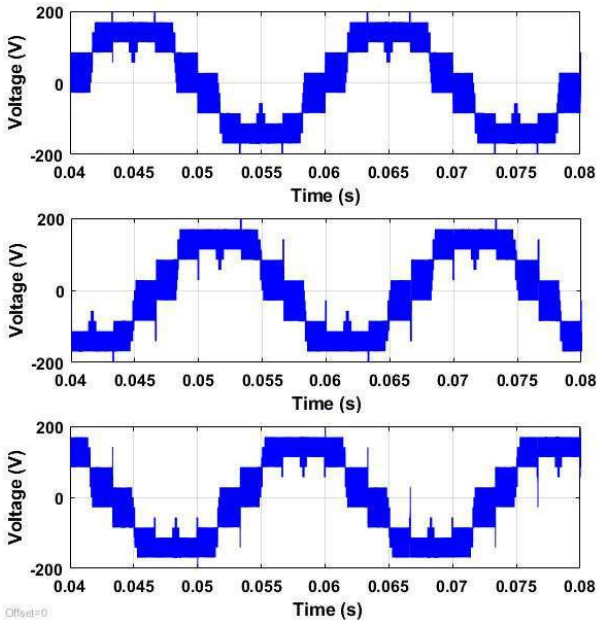
The simulation and experimental validations are explained in this section.

4.5.1 Simulation Results

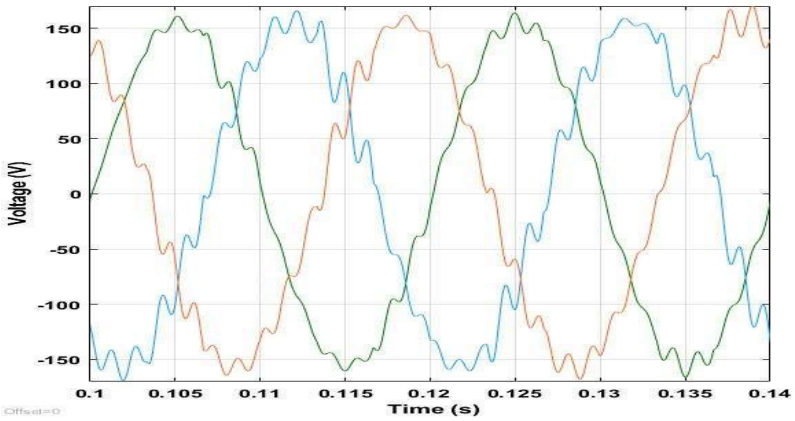
The three phase PWM inverter system comprising of the main inverter in series with the harmonic compensator with feed-forward control simulated using MATLAB software. Each limb of the half-bridge inverter is operated with the low frequency PWM pulses with switching frequency of 50 Hz at over-modulation to achieve high RMS ac fundamental output voltage. The supply frequency of the inverter in this simulation is 50 Hz. The harmonic compensator is operated with switching frequency at 25 kHz. The dc input voltage is 255 V, whereas the star (Y) connected load consists of a resistance of 29.04 Ω and inductance of 69.3 mH for each phase. Fig. 4.13, 4.14 and 4.15 are representing waveforms at different points of the power circuit control circuit and harmonic spectrum, of the proposed inverter respectively at over-modulation.



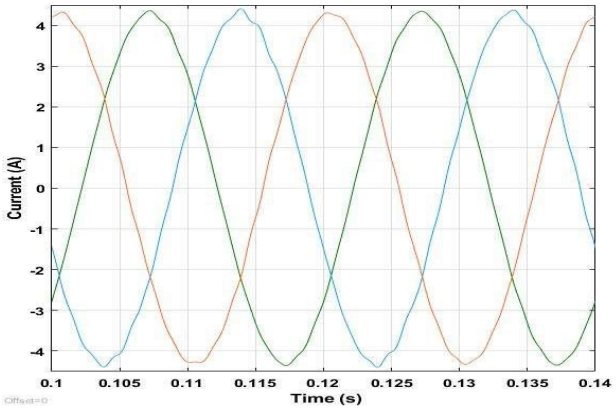
(a)


Voltage (V)
200
0
-200
0.04 0.045 0.05 0.055 0.06 0.065 0.07 0.075 0.08
Time (s)
Voltage (V)
200
0
-200
0.04 0.045 0.05 0.055 0.06 0.065 0.07 0.075 0.08
Time (s)
Voltage (V)
200
0
-200
0.04 0.045 0.05 0.055 0.06 0.065 0.07 0.075 0.08
Time (s)

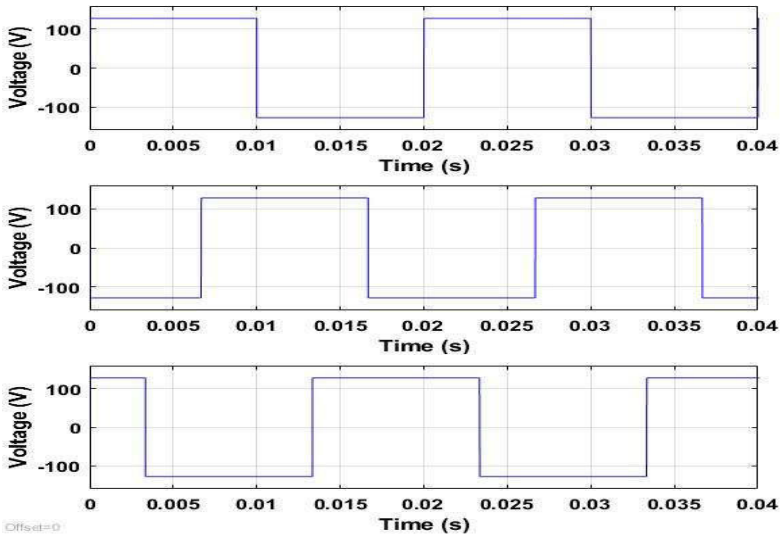
(b)


Voltage (V)
150
100
50
0
-50
-100
-150
0.1 0.105 0.11 0.115 0.12 0.125 0.13 0.135 0.14
Time (s)

(c)


Current (A)
4
3
2
1
0
-1
-2
-3
-4
0.1 0.105 0.11 0.115 0.12 0.125 0.13 0.135 0.14
Time (s)

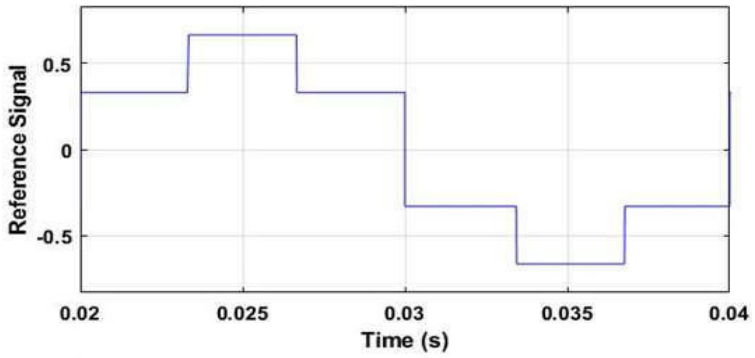
(d)



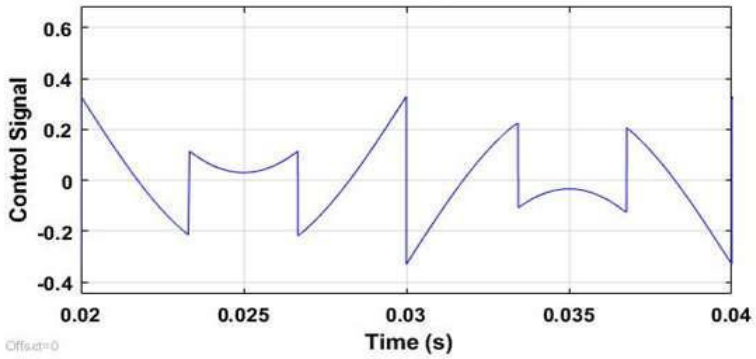
(e)

Figure 4.13 Waveforms at different points of the power circuit of the proposed inverter: a) Line to Neutral voltage of the main inverter; b) Line to Neutral voltage after the compensator; c) Three phase Line to Neutral voltage after LC filter (across R-L load); d) Three phase Line current through R-L load; e) Voltage across dc bus midpoint and inverter output

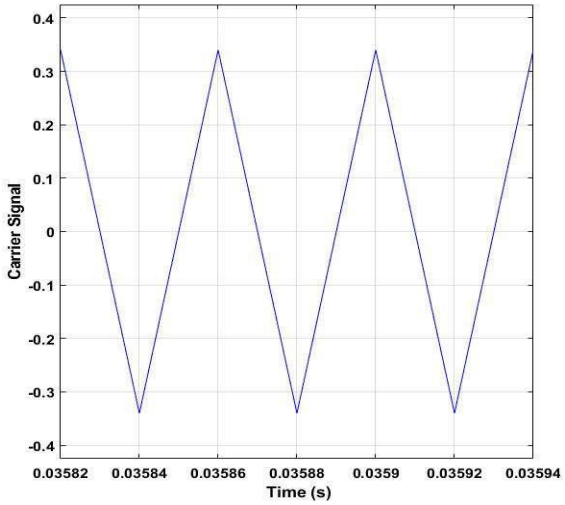
Fig. 4.14 presents the waveforms generated by the control circuit, namely, the reference signal from which the compensating waveform is derived after extraction of fundamental, the modulating signal for the high frequency PWM and the high frequency carrier for generating the switching pulses for the active compensator.



(a)



(b)

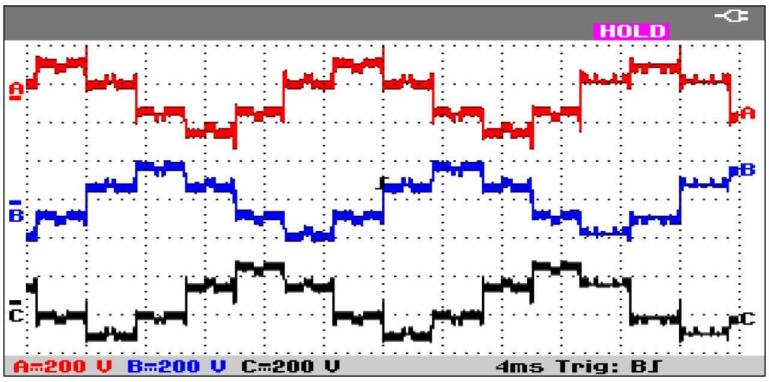


(c)

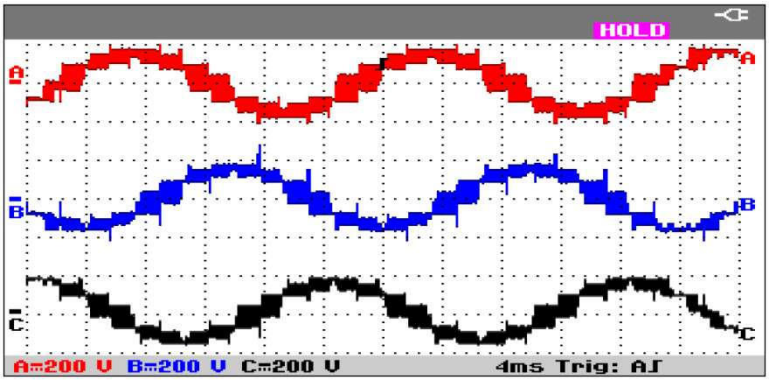
Fig. 4.14 Control circuit waveforms of active compensator: a) Reference signal for the active compensator; b) Modulating waveform for the high frequency PWM; c) Carrier signal for the high frequency PWM

4.5.2 Experimental Results

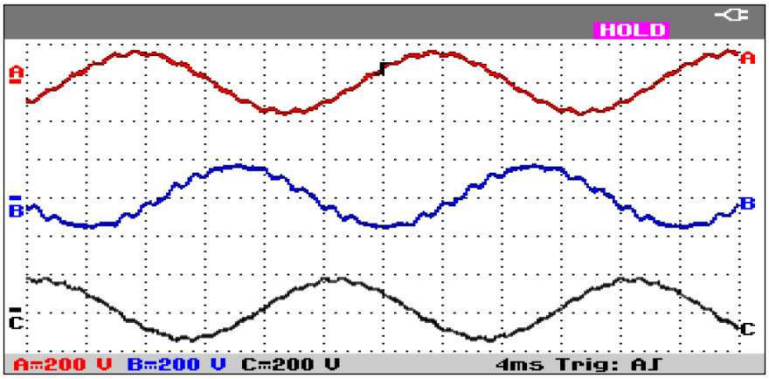
For the experimental verification, a prototype was built in the laboratory with parameters as close as possible to those under simulation as in Table 4.1. The major power circuit waveforms taken at different points during the time of experimentation are shown in below Fig 4.15.


HOLD
A
B
C
A=200 V B=200 V C=200 V
4ms Trig: BƒA

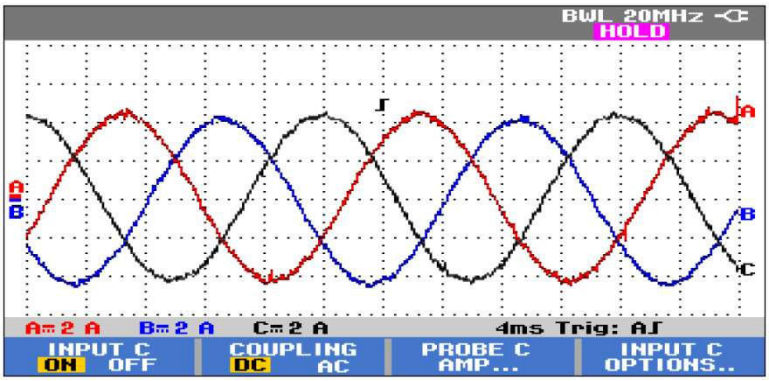
(a)


HOLD
A
B
C
A=200 V B=200 V C=200 V
4ms Trig: AƒA

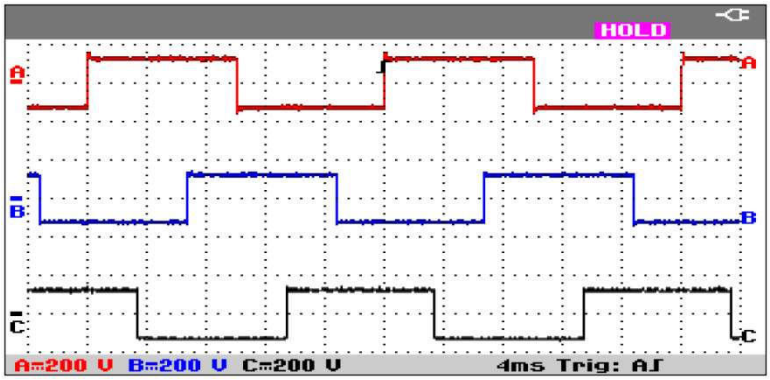
(b)


HOLD
A
B
C
A=200 V B=200 V C=200 V
4ms Trig: AƒA

(c)


BWL 20MHz
HOLD
A
B
A=2 A B=2 A C=2 A
4ms Trig: AƒA
INPUT C ON OFF
COUPLING DC AC
PROBE C AMP...
INPUT C OPTIONS..

(d)



(e)

Fig. 4.15 Experimental waveforms: (a) voltage across inverter output and load neutral; (b) voltage across load without the filter; (c) voltage across load; (d) load current; (e) voltage across terminals inverter output and dc bus midpoint

4.6 Efficiency Calculation

The efficiency (η) of the 3-phase inverter is given by

$$\eta = \frac{P_0}{Pin} \quad 4.18$$

Where, P_o is the output power of the inverter; Pi is the input to the inverter.

Also, $P_{in} = P_o + P_{loss}$ 4.19

Where, P_o= p.f. x RMS value of fundamental load voltage x RMS value of fundamental load current

Considering the parameter values as shown in Table 4.1 and 4.3, a conventional three-phase 2-level SPWM inverter is simulated in PSIM software to evaluate the loss and the efficiency of the overall system. For a 1000 VA, three phase inverter at 0.8 p.f., the RMS output voltage is 77.4 volts if the input dc voltage is 255 volts. Assume that the switching frequency is 25 kHz and all the IGBTs used in the inverter circuit will be supported by 255 volts.

Considering load current 3.03 A and p.f. 0.8, the load resistance and load inductance are calculated as 29.04 Ω and 69.3 mH using the following equations 4.20 and 4.21.

$$\text{Impedance(Z)} = \frac{\text{Fundamental RMS load voltage}}{\text{Fundamental RMS load current}} \quad 4.20$$

$$p.f. = \frac{R}{Z} \quad 4.21$$

Therefore, P_0= 0.8 x √3 x √3 x 77.4 x 3.03 = 562.85 watt

Loss= 8.97watt (see Appendix A)

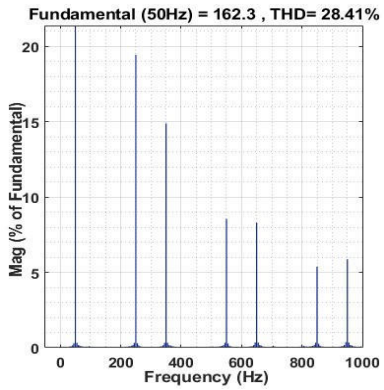
Hence, from equation 4.19, P_{in} can be calculated as 571.82 watt and efficiency is 98.4% using equation 4.18.

Similarly, for the three phase proposed inverter with a natural Compensator, using the same load current, the output RMS ac voltage is obtained as 110.76 volts. Here, six IGBTs of the main inverter are supported by 255 volts at the switching frequency of 50 Hz. The MOSFETs used in the active compensator will be supported by reduced voltage of 85 volts each at the switching frequency of 25 kHz. The output power can be calculated as

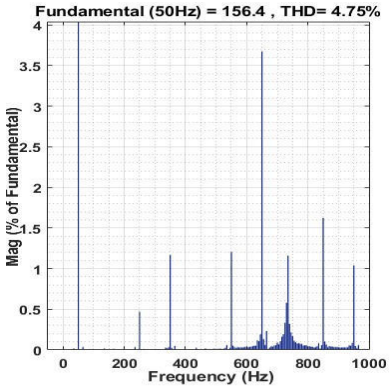
P_0=0.8x√3x√3x110.76x3.03=805.44 watt and loss=26.97 watt (see Appendix A). Thus the input power by equation 4.19 can be determined as P_{in}=805.44+26.97=832.41 watt.
Therefore, Efficiency by equation 4.18 can be obtained as P_o/P_{in}=96.7 %.
Appendix A shows the loss calculations for the conventional three phase inverter and the proposed three phase inverter with a natural harmonic compensator using PSIM simulation.

4.7 THD Analysis

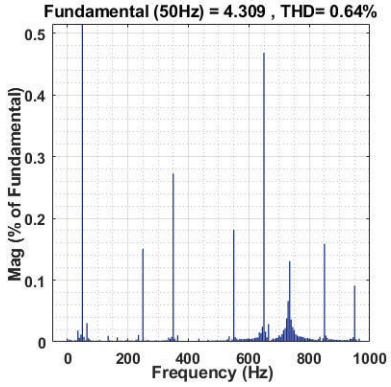
Fig. 4.14 shows the voltage waveforms at output of main inverter, after the compensatorand after the LC filter, along with load current waveform. Fig. 4.16 depicts the voltage harmonic spectrum at output of main inverter, after the compensator and after the L filter, along with load current harmonic spectrum.
The three phase inverter system comprising of the main inverter in series with the harmonic compensator is simulated using MATLAB software for the analysis of harmonic contents. It is seen that the L-N voltage of main inverter contains THD of 28.41% which is reduced to 4.75% across the load after the natural compensations using active compensator. Also it can be stated that the RMS fundamental output of the proposed inverter system is 110.76 V which implies the maximum DC bus utilization for a three phase inverter with the input DC voltage of 255 V and with a less THD count.
Fig. 4.16 depicts the harmonic spectrums at different points of the power circuit of the proposed inverter respectively (voltage harmonic spectrum at output of main inverter, after the compensator and after the LC filter).



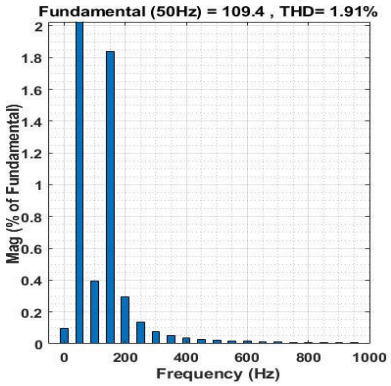
(a)



(b)



(c)



(d)

Fig. 4.16 Harmonic spectrum at different points of the power circuit of the proposed inverter: a) Harmonic spectrum of L-N voltage of main inverter; b) Harmonic spectrum of L-N voltage after LC filter (across load); c) Harmonic spectrum of line current through R-L load; d) Harmonic spectrum of L-N voltage after LC filter (across load) of three phase SPWM inverter

4.8 Comparative Study

To evaluate the performance of the proposed inverter, its parameters and components were fixed as given in Table 4.1.

Table 4.1 Values of Parameters and Component Ratings of System Studied

Parameter	Value	Component	Rating
Input DC voltage (V_{dc})	255 V	DC bus capacitors Ce & Cf (each)	2200 µF
Main inverter fundamental frequency	50 Hz	DC bus capacitors across Compensator	2200 µF
Main inverter switching frequency	50 Hz	Filter inductor L	7.5 mH
DC bus voltage of compensator (Vc)	85 V	Filter capacitor C	7 µF
Compensator switching frequency	25 kHz	Load resistance	29.04 Ω
Load VA	1000	Load inductance	69.3 mH
Load power factor	0.8		

The simulated results of the proposed inverter system are summarized in Table 4.2.

Table 4.2 Summary of simulation results

Parameter	Simulation Results
Input DC voltage (V_{dc})	255 V
Main inverter fundamental voltage (RMS) per phase	114.9 V
DC bus voltage of active compensator (V'_{dc}) per phase	85 V
Load voltage (RMS) per phase	110.76 V
Load current per phase	3.03 A
Output voltage THD	4.75%

A conventional three phase 2-level SPWM voltage source inverter is also simulated with the same parameters shown in the above Table 4.1 in MATLAB and the line to neutral voltage of one phase along with its harmonic spectrum with and without filter are shown in Fig. 4.14. It is seen that in spite of having almost same THD across the load, the DC bus utilization is more as compared to the three phase inverter without the compensator but with the same simulation parameters as given in Table 4.1.

The performance of the proposed inverter is compared with that of a conventional three phase inverter under simulation. The results are tabulated in Table 4.3. It will be observed that the proposed inverter is giving maximum fundamental RMS ac voltage and providing a improved THD than the three phase inverter without the compensator from the same DC supply while maintaining almost the same efficiency.

Table 4.3 Comparison with Conventional Three-Phase Inverter

Parameter	Three-Phase Inverter	Proposed Inverter
Input DC voltage	255 V	255 V
Number of switches	4 IGBTs to support 255V	6IGBTs to support 255V + 12 MOSFETs in compensator to support 85V
Switching frequency	All switches at 25 kHz	6 switches at 50Hz, 12 switches at 25kHz
Output AC RMS voltage (after the filter) per phase	77.4 V at m=0.9	110.76 V
Output voltage THD (after the filter) per phase	1.91%	4.75%
Load Current per phase	3.03 A	3.03 A
Efficiency	98.4%	96.7 %

Even though the proposed inverter has a higher number of switches that increases the total conduction losses, overall total losses are comparable to the three phase inverter. This is because of all the switches in the proposed inverter scheme, several of them switch at a low frequency only, while several face only an approximate 34% blocking voltage when compared to all the switches in the three phase inverter without the compensator, thereby creating lower switching losses.

4.9 Proposed Topology for Open End Winding Transformer Coupled Load

This proposed three phase inverter system can be modified for Open End Winding Transformer coupled load. Fig 4.17 depicts the power circuit diagram of an open end winding (OEW) transformer connection connected with the proposed three phase inverter system. The system is simulated in MATLAB using the parameters as shown in Table 4.4.

In this topology, the inverter comprises of a 3-phase, 2-level three limb voltage source inverter while the compensator has a similar configuration. The transformer coupled load per phase is connected between the mid-point of one limb of the inverter and the mid-point of one leg of the compensator. The advantage of this topology is the reduction of the number of switches, resulting in reduced losses. However, the load has to couple through a full power rated transformer winding per phase.

Since the compensator now behaves as an effective half-bridge inverter per phase instead of a full bridge as in the earlier topology of Fig. 4.8, it is expected that the dc bus voltage will be double that of the earlier value, ie., $2/3^{rd}$ of the input dc bus voltage instead of $1/3^{rd}$ value. This does increase the voltage stress on the compensator devices and switching losses, but the total path conduction losses are reduced due to less number of switches in series, along with the use of a single capacitor bank on the compensator dc bus. The ripple current through the

capacitors are also reduced due to proper 3-phase operation of the compensator compared to the 1-phase nature of operation in the earlier 3-phase version of Fig. 4.8.

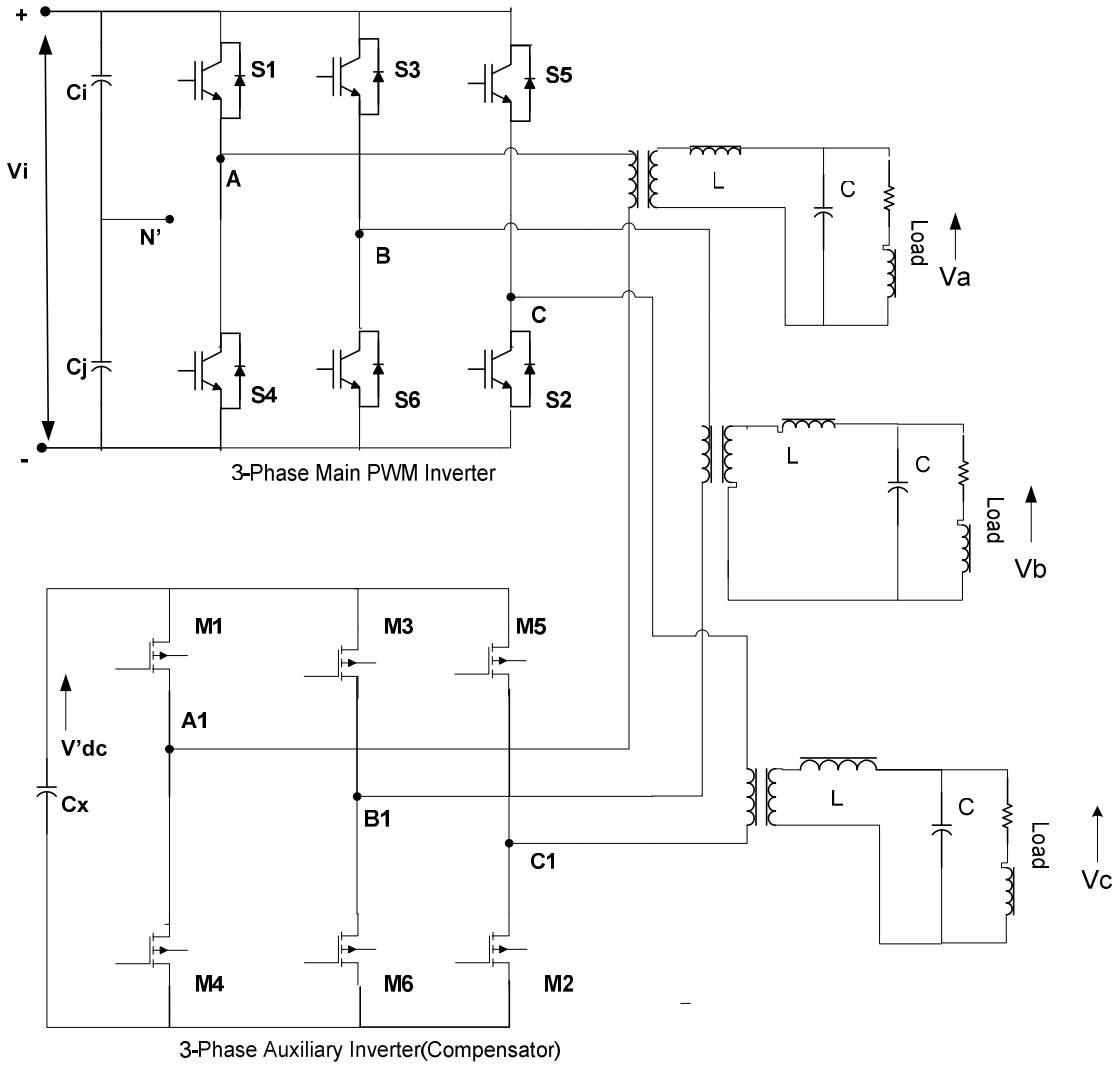


Fig. 4.17 Proposed topology for open end winding transformer coupled load

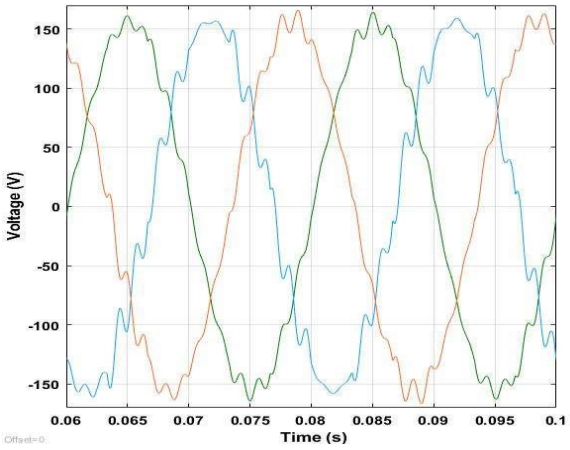
Table 4.4 Values of Parameters and Component Ratings of System Studied

Parameter	Value	Component	Rating
Input DC voltage (V_{dc})	255 V	DC bus capacitors Ci & Cj (each)	2200 µF
Main inverter fundamental frequency	50 Hz	DC bus capacitors across Compensator	2200 µF
Main inverter switching frequency	50 Hz	Filter inductor L	7.5 mH
DC bus voltage of compensator (V'_{dc})	170.085 V	Filter capacitor C	7 µF
Compensator switching frequency	25 kHz	Load resistance	29.04 Ω
		Load inductance	69.3 mH

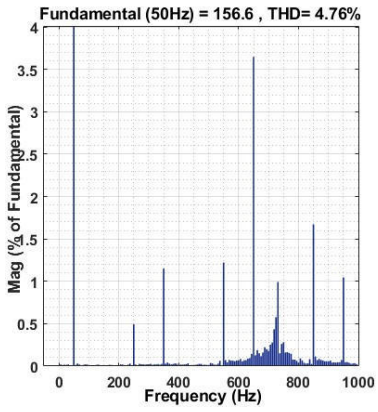
The simulated results of the proposed inverter system at over-modulation are summarized in Table 4.5. Fig. 4.18 depicts the waveforms at different terminals of the proposed system and the THD count is obtained as 4.76 % across the load voltage.

Table 4.5 Summary of simulation results

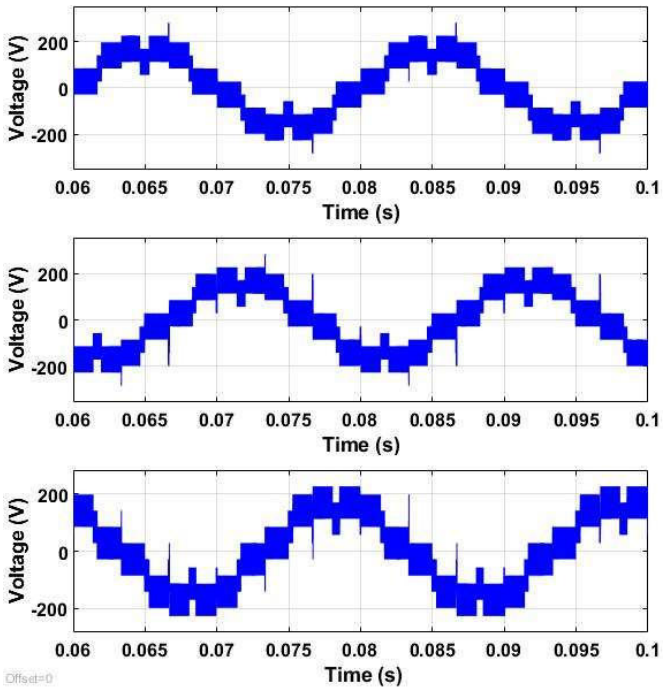
Parameter	Simulation Results
Input DC voltage (V_{dc})	255 V
DC bus voltage of active compensator (V'_{dc})	170.085 V
Load voltage(RMS) per phase	110.9 V
Load current per phase	3.03 A
Output voltage THD	4.76 %



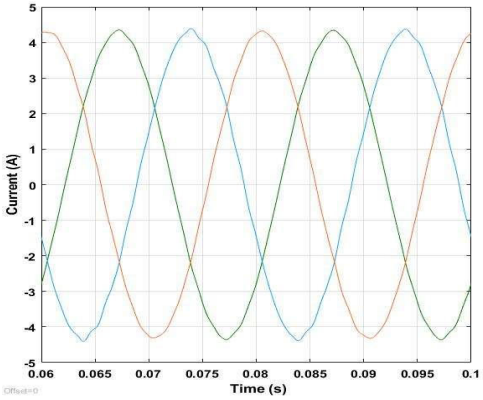
(a)



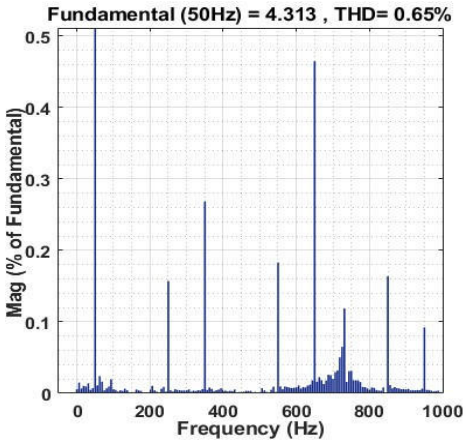
(b)


Voltage (V)
200
0
-200
0.06 0.065 0.07 0.075 0.08 0.085 0.09 0.095 0.1
Time (s)
Voltage (V)
200
0
-200
0.06 0.065 0.07 0.075 0.08 0.085 0.09 0.095 0.1
Time (s)
Voltage (V)
200
0
-200
0.06 0.065 0.07 0.075 0.08 0.085 0.09 0.095 0.1
Time (s)
Offset=0

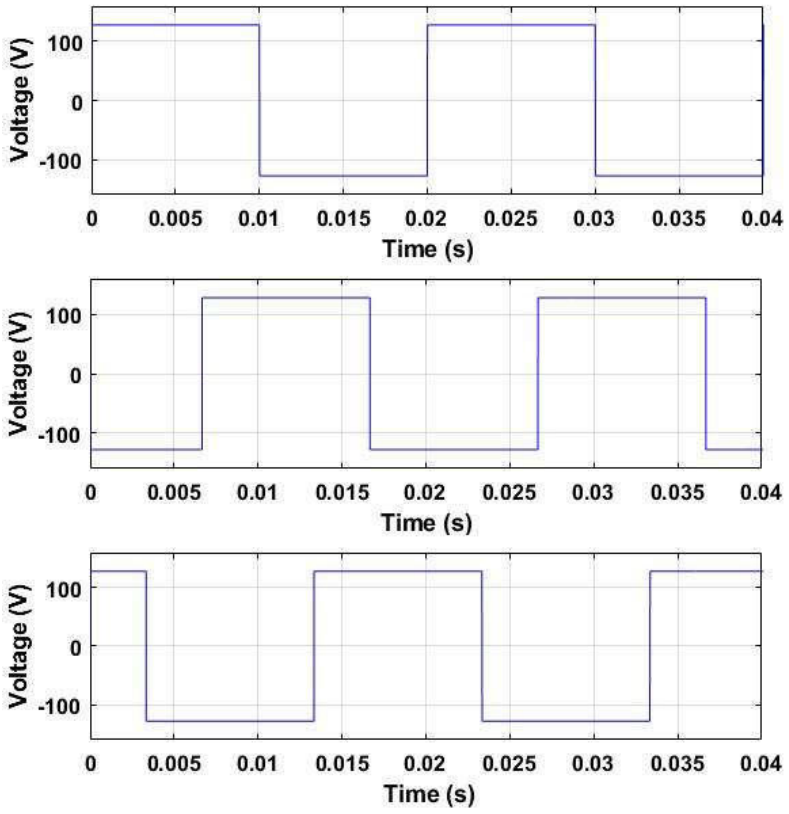
(c)


Current (A)
5 4 3 2 1 0 -1 -2 -3 -4 -5
0.06 0.065 0.07 0.075 0.08 0.085 0.09 0.095 0.1
Time (s)
Offset=0

(d)


Fundamental (50Hz) = 4.313 , THD= 0.65%
Mag (% of Fundamental)
0.5 0.4 0.3 0.2 0.1 0
0 200 400 600 800 1000
Frequency (Hz)

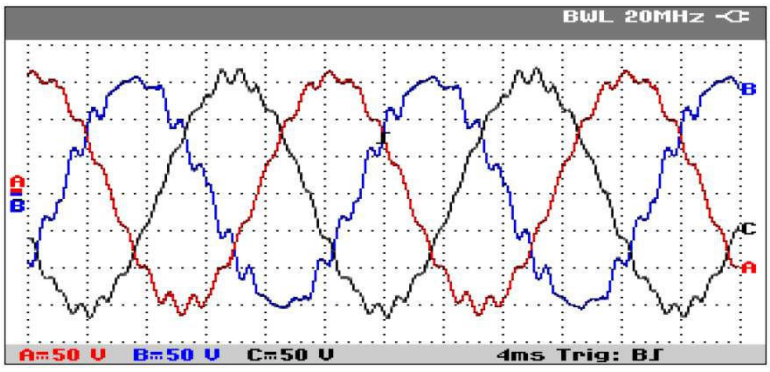
(e)



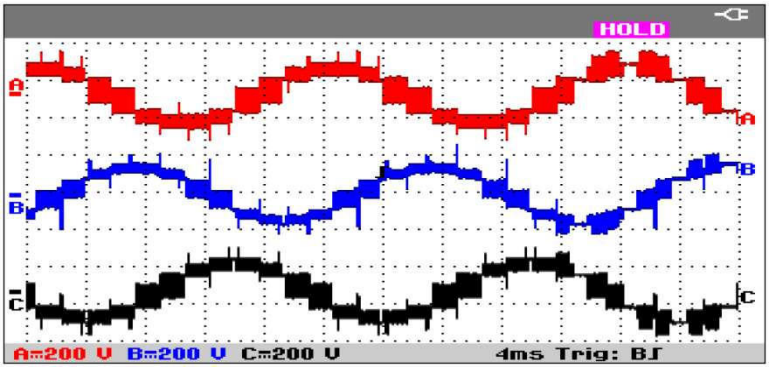
(f)

Fig. 4.18 Open End Winding Transformer in Proposed Converter: (a) Load voltage (after filter); (b) THD spectrum of load voltage (after filter); (c) Load voltage (before filter); (d) Load current; (e) THD spectrum of load current; f) Voltage across inverter and dc bus midpoint

For the experimental verification, a prototype was built in the laboratory with parameters as close as possible to those under simulation as in Table 4.4. The major control circuit waveforms taken at different points during the time of experimentation are shown below in Fig. 4.19



(a)



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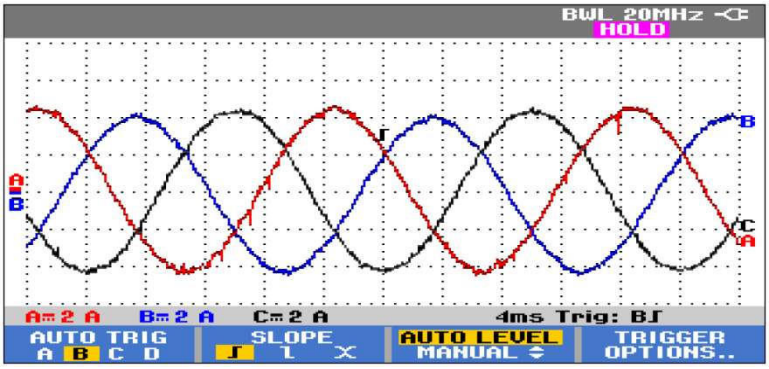

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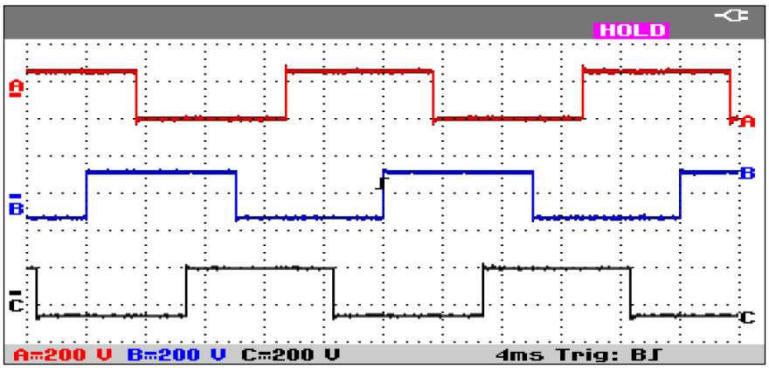


(d)

Fig. 4.19 Open End Winding Transformer in Proposed Converter: (a) Load voltage (after filter); (b) Load voltage (before filter); (c) Load current; (d) Voltage across dc bus midpoint and inverter output

4.10 Conclusion

This chapter presents a new three phase inverter topology consisting of three numbers of single phase half bridge inverter in series with three 2-level single phase active compensators, operating in the natural compensation mode. There is no requirement of any dc source to be provided across the compensators and the capacitors used in each bus of the compensators will get charged naturally due to the principle of natural harmonic compensation. These capacitors are charged to about 1/3rd of the input DC excitation due to the 2-level inverter

operation in feed-forward control methodology rather than a complex feedback mechanism. The main three phase PWM inverter will be switched at low frequency SPWM which is done by a 150 Hz carrier signal. The series active compensator operated at a very high switching frequency of 25 kHz. The compensated load voltage has reduced harmonic content, compared to the main inverter output. Thus a small low-pass filter is used at the final output to remove the dominant switching frequency components of the compensator. The advantages of the proposed scheme include high dc bus utilization, low overall switching loss, small size filter, low THD voltage output.

The proposed inverter system produces a near sinusoidal three phase voltage output at fixed fundamental frequency with low switching loss. The output of main inverter system can be controlled by low frequency Pulse Width Modulation. At the over-modulation, the fundamental of the output voltage is high with low THD which improves the dc bus utilization as compared to conventional PWM technique. The proposed system at over-modulation can be used as an open end winding transformer connection in which the capacitor across the three phase compensator will be charged naturally with only $2/3^{rd}$ of DC bus input voltage. Hence MOSFETs can be used in the compensator circuit with a low voltage rating and high switching frequency.

CHAPTER – FIVE

Three Phase Sine PWM Inverter using Natural Harmonic Compensation

5.1 Introduction

AC motor drives and uninterruptible ac power supplies require inverter systems with sinusoidal voltage signal whose magnitude and frequency have to be controlled. In square wave inverters the output voltage has a square wave-shape whose magnitude can be controlled by varying the dc input voltage. In square wave switching scheme each switch of the inverter limb will be active for half time period i.e. 180˚ of the desired output frequency. From the Fourier series, the maximum values of the fundamental frequency component and harmonic contents of the output voltage waveform of the inverter can be given by

$$V_{A0} = \frac{4}{\pi}\frac{V_d}{2} = 1.273\frac{V_d}{2} \quad 5.1$$

And $$V_{A0h} = \frac{V_{A01}}{h} \quad 5.2$$

Where the harmonic order h takes only odd values and V_d is the input dc voltage as given in Fig. 5.1.

The major usefulness of the square wave switching operation is that each switch of the inverter changes its state only twice per cycle, that is useful at very high power levels where the semiconductor switches usually have larger turn on and turn off times. The problem in square wave inverter is that the output voltage amplitude cannot be controlled. Thus, in order to have the provision of controlling the ac output voltage of the inverter, the PWM switching scheme should be adopted.

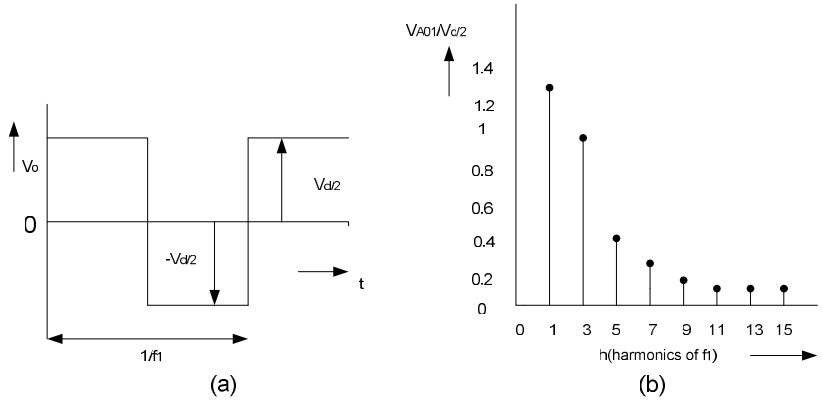


Fig 5.1 Square wave switching: (a) Fundamental output signal of the inverter; (b) harmonic spectrum

Most of the three phase Voltage Source Inverters (VSI) produce a voltage at the output whose

fundamental RMS value is lower than the DC bus input voltage. This implies ineffective DC bus utilization. Further, harmonics generated by the inverter are attenuated at the final output by the use of low-pass LC filters to create near-sinusoidal voltage. In order to reduce the size of the filter, the switches are operated at higher switching frequency, causing higher switching losses. On the other hand, low switching frequency stepped wave inverters produce higher DC bus utilization with lower switching loss at the cost of higher amount of lower order harmonics. Harmonics can be eliminated using Multi-level inverters, but at the expense of more number of switches and separate dc bus voltages [4]. Selective Harmonic Elimination (SHE) techniques can be used for high dc bus utilization and low switching losses but only selected lower order voltage harmonics are eliminated while output voltage control is not possible.

A square wave inverter has the lowest switching frequency with highest DC bus utilization, but has high harmonic content and output voltage control is not possible. The concept of using a high switching frequency inverter in series with the main inverter was introduced to eliminate the harmonics of a square wave inverter [4, 43-46]. This resulted in high dc bus utilization with moderate overall switching loss. However, the dc bus of the additional inverter needs an isolated supply. The principle of mitigation of harmonics using the natural process of maintaining the DC bus of the series connected high switching frequency inverter introduced a new method for generation of sinusoidal voltages without use of separate floating dc supply for the series compensator.

The proposed new three phase inverter system presented here is based on the principle of natural compensation of a Sinusoidal PWM stepped waveform, operating with modulation index less than unity, resulting in reasonable dc bus utilization and a small filter to achieve a low THD voltage waveform output. Due to the use of stepped waveform, the DC bus voltage of the compensator is required to be less than that of the inverter DC bus, permitting the use of lower voltage, higher switching frequency devices in the compensator in order to achieve low switching loss.

5.2 The Proposed Inverter

The circuit detail of the proposed 3-phase inverter system is shown in Fig. 5.2. The proposed inverter uses a 3-phase, three-limb two-level inverter, each phase output being connected in series with a two level compensator providing natural compensation of the major harmonics generated by the former.

The R-L load is star (or Y) connected and the inverter control is designed to produce a Sinusoidal PWM stepped voltage waveform across each phase of the load. This ensures adequate DC bus utilization and low switching frequency of inverter IGBT switches, as explained later.

The application of Sinusoidal PWM in the proposed system of inverter with series compensator allows voltage control flexibility at the sacrifice of very high DC bus utilization.

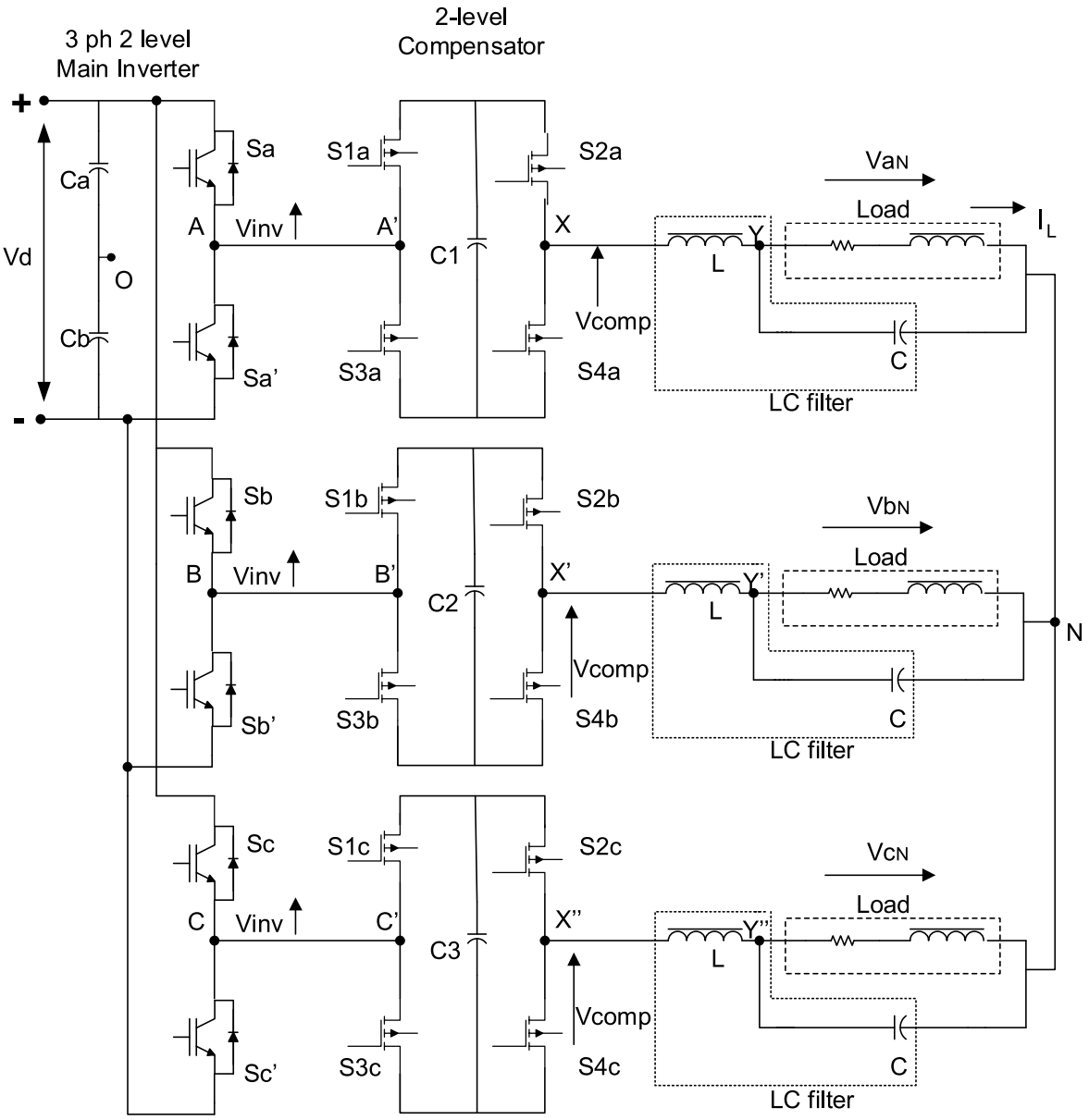


Fig. 5.2 Circuit connection of proposed SPWM three phase inverter

The series connected compensators uses a single phase H-bridge using four MOSFETs with a dc bus capacitor. The devices in the compensator circuit must switch at a frequency higher than that of the main inverter in order to achieve compensation of the main inverter output.

A small L-C low pass filter is connected across each phase of the final compensated output, in order to smoothen the voltage waveform by removing the compensator switching frequency component. Hence the filter size is quite small compared to what would have been needed to extract a sine wave from the basic stepped waveform of the inverter.

5.3 The Operating Principle of Proposed Inverter

Consider the three phase main inverter to be made up of three numbers of single phase half bridges, using two switches and output of each limb is connected to a series compensator followed by a small low-pass filter as shown in Fig. 5.3.

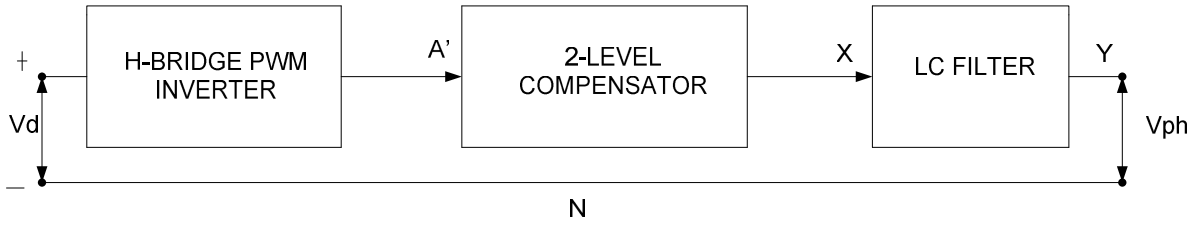


Fig. 5.3 Block schematic of one phase of proposed inverter

The voltage created by switches of one phase of main inverter, with respect to load neutral, can be given in terms of its fundamental and harmonics as:

$$V_i = V_{1m}\sin\omega t + V_{3m}\sin 3\omega t + V_{5m}\sin 5\omega t + \ldots \quad 5.3$$

The voltage generated by switches of the harmonic compensator, can similarly be given in terms of its harmonics as:

$$V_c = V'_{3m}\sin 3\omega t + V'_{5m}\sin 5\omega t + \ldots \quad 5.4$$

When the magnitude of the harmonics present in the two waveforms are equal and opposite to each other, the final output can be given as:

$$V_o = V_i - V_c = V_{1m}\sin\omega t \quad 5.5$$

The harmonics generated by main three phase inverter will thus be compensated through the presented technique without the need for a large low-pass filter at the output, creating a final voltage which is the sinusoidal fundamental generated by the low frequency switching of the main three phase inverter. This waveform can be fed to a three phase induction motor, with resulting near-sinusoidal current waveforms. However the use of an added small size low-pass filter to remove the switching frequency components, creates a good quality sine-wave for other three phase applications.

The principle of natural compensation [43-46] permits the use of only a charged dc bus capacitor Ca to maintain the output waveform of the compensator, without the use of separate dc supply. This can be explained by assuming that if only fundamental current is now flowing through the load due to complete compensation, then at the compensator output, no active power is contributed by the harmonic voltages only that are created by the compensator.

Since the voltage harmonics of inverter are compensated before reaching the load, it is possible to create fundamental of large amplitude than what can be generated by conventional PWM control from the same DC bus. Hence, a SPWM waveform per phase is chosen in this work to achieve reasonably high DC bus utilization with minimum switching loss. For three phase operation, line to neutral voltage is stepped in nature.

Since the line to neutral voltage is stepped in nature, it permits the dc bus capacitor of the compensator to maintain lower input dc bus voltage across it [4]. This permits the use of lower voltage, higher frequency switching devices than what is needed in the main inverter. Further, due to the lower operating voltage of the compensator, its switching loss will not be very high.

A square wave-shape of the voltage of magnitude $\pm V_d/2$ is created at the midpoint of each half-bridge inverter with respect to the input dc bus mid-point. All three units are connected with the same input dc bus to develop similar square outputs at the midpoint of the limbs but shifted by $2\pi/3$ radians in order to achieve a three phase balanced output voltage across the output.

When the top switch S_a of the first half bridge limb is turned on, the bottom switch $S_{a'}$ must be turned off as shown in Fig. 5.4. The logic is same for the other two units. A small dead band is provided between the switching to prevent unwanted shoot-through fault due to simultaneous on-condition of both the switches.

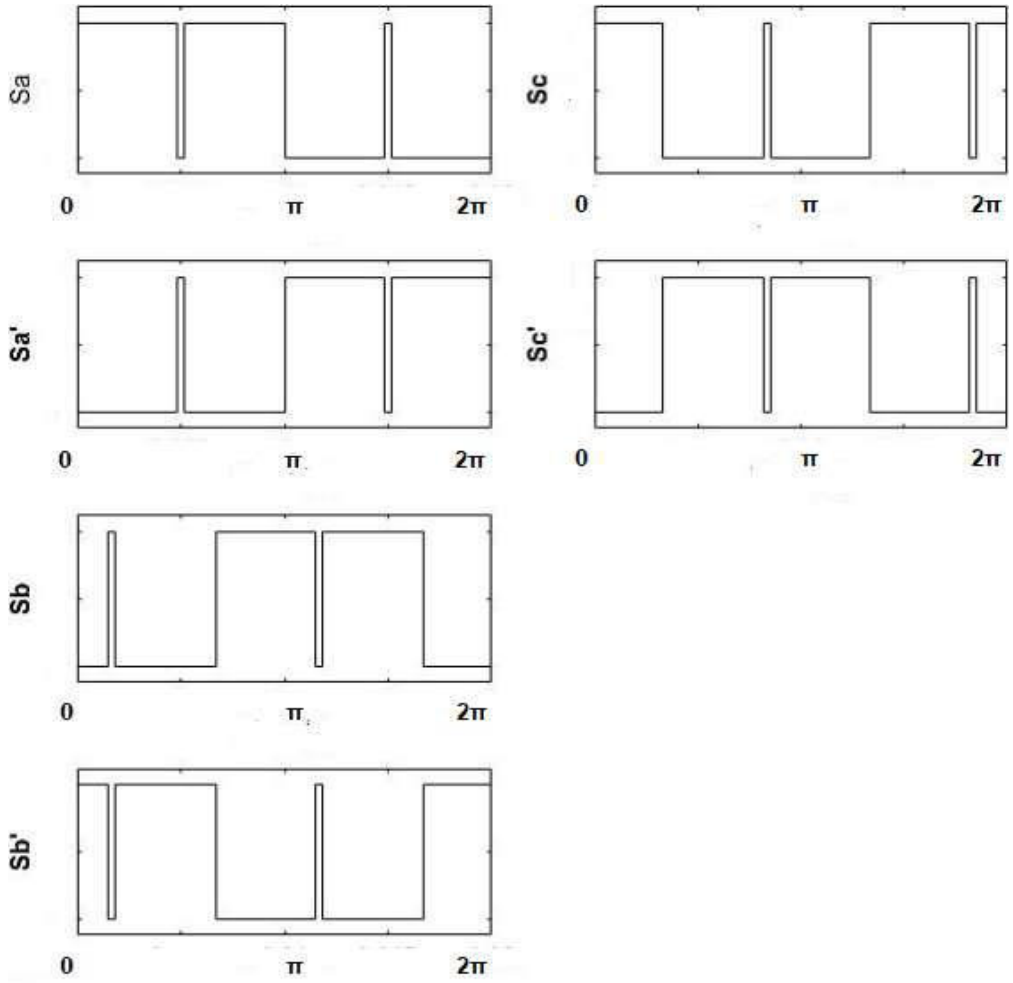


Fig. 5.4 Switching pulses for the three phase inverter

Since the load is balanced and star connected, the voltage at the output of each inverter phase with respect to the load neutral (across the terminals A′& N of Fig. 5.2) appears as a stepped waveform as shown in Fig. 5.5. The step heights are $V_d/3$ and $2V_d/3$.

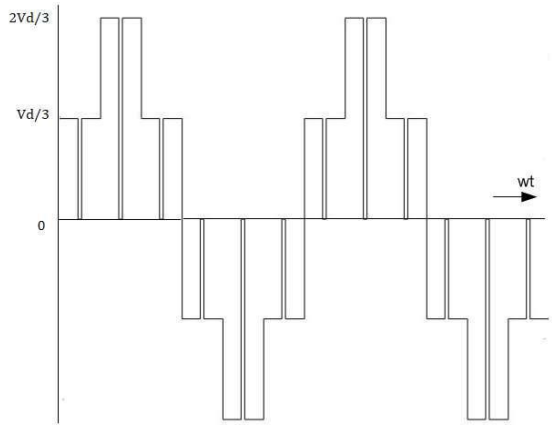


Fig. 5.5 PWM Stepped voltage waveform across terminals A′ & N

The phase voltage thus created at the output of main inverter comprises of fundamental as well as harmonics. The harmonics are removed by using a series connected active compensator at the output of each phase. The active compensator comprises of switches S1a to S4a, that creates a two level waveform (which is pulse width modulated at a frequency higher than that of inverter) between points A′ & X, consisting of identical order and magnitude of harmonics that was generated between A′ & N, other than being opposite in phase. This cancels the voltage harmonics in series opposition, leaving the fundamental voltage and the added switching frequency component between the terminals X & N.

The high PWM switching frequency component of the switches S1a to S4c of compensator will be however also present across the load and a small filter is needed to attenuate it in order to obtain a cleaner waveform.

As the load current is almost sinusoidal, due to the fundamental component, active power is drawn only from the dc source through the output of three phase main inverter comprising of switches Sa, Sa′, Sb, Sb′, Sc and Sc′ as it contains fundamental voltage. The active compensator comprising of switches S1a, S2a, S3a and S4a, operating from an energy storage dc bus capacitors Ce and Cf, does not generate any fundamental voltage and hence cannot provide active power. Thus, the average charge on both the capacitors Ce and Cf remains constant at a value depending on the modulation of compensator, amount of harmonic and the input dc supply. Charging and maintenance of charge is naturally obtained [46].

5.4 Control Pulse Generation Scheme

The two cascaded switching circuits are used for different objectives and hence switch in different modes. Switches of the main three phase inverter are operated at low frequency to

create a desired fundamental content. Switches of the series compensator are operated at higher frequency PWM so as to nullify the lower order harmonics generated by the main 3-phase inverter.

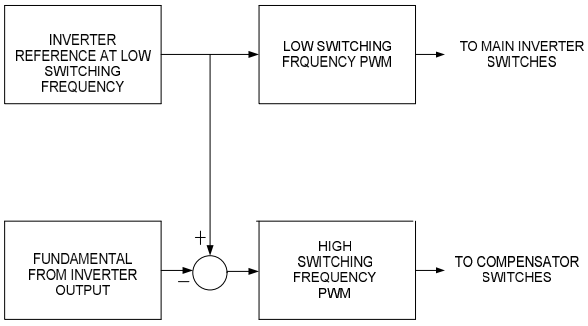


Fig. 5.6 Block diagram of control scheme for generation of gate pulse

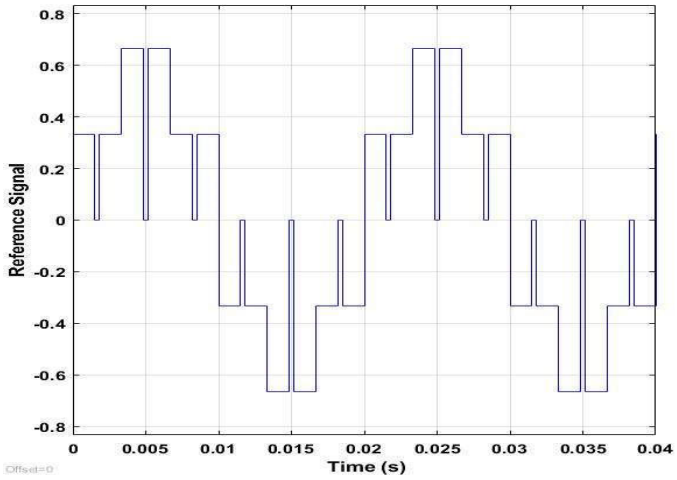
Fig. 5.6 presents the block schematic of the control scheme for generation of gate pulses for one phase. A reference waveform for the low switching frequency inverter is first generated. Hence, the actual wave-shape which will be developed at the mid-point of Sa and Sa′ (with respect to the dc mid-point) is determined and the switching pulses for Sa & Sa′ are generated.

From the reference waveform for the main inverter, the output line to load neutral voltage waveform is synthesized within the control circuit. Then, the fundamental component of the synthesized waveform as drawn in Fig. 5.5 is extracted and further subtracted from the reference (synthesized wave) signal, thereby leaving only the harmonics. This resulting waveform is used as the reference to create the power waveform that will be created across the terminals A & X of the active compensator. This is now compared with a triangular carrier to generate the switching pulses for the switches S1a, S2a, S3a and S4a. The control pulses of the other two phases are generated in a similar way.

5.5 Simulation Results

The proposed three phase inverter system comprising of the main inverter in series with the harmonic compensator is simulated using MATLAB software. Each limb of the half-bridge inverter is operated with the square pulses. The fundamental frequency considered in this simulation is 50 Hz. The harmonic compensator is operated with the high frequency switching at 25 kHz. The dc input voltage is 290 V, whereas the star (Y) connected load consists of a resistance of 29.04 Ω and inductance of 69.3 mH for each phase as shown in Table 5.1.

Fig. 5.7 presents the waveforms generated by the control circuit, namely, the reference signal from which the compensating waveform is derived after extraction of fundamental, the modulating signal for the high frequency PWM and the high frequency carrier for generating the switching pulses for the active compensator.



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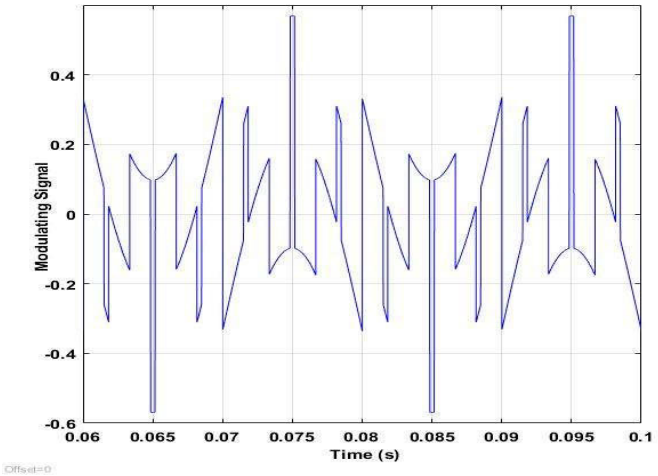

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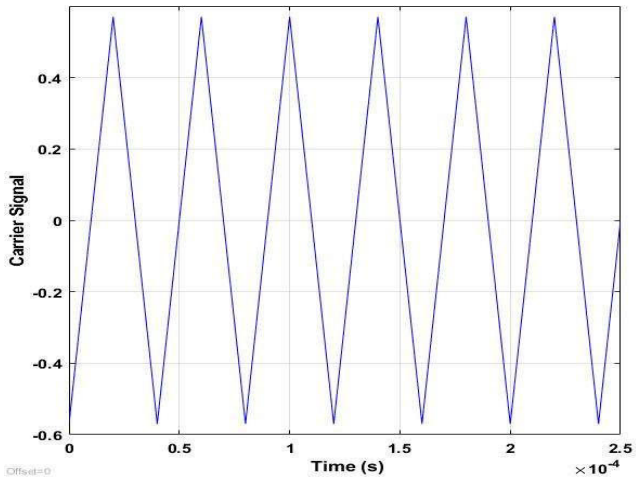
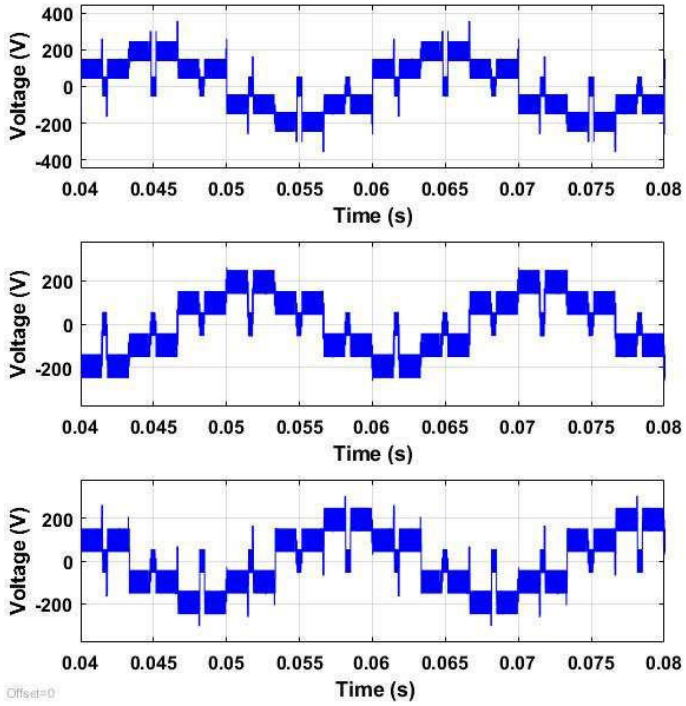


(c)

Fig. 5.7 Control circuit waveforms of active compensator: (a) Reference signal for the active compensator, (b) Modulating waveform for the high frequency PWM; (c) Carrier signal for the high frequency PWM

Fig. 5.8 shows the voltage waveforms at output of main inverter, after the compensator and after the LC filter, along with load current waveform.



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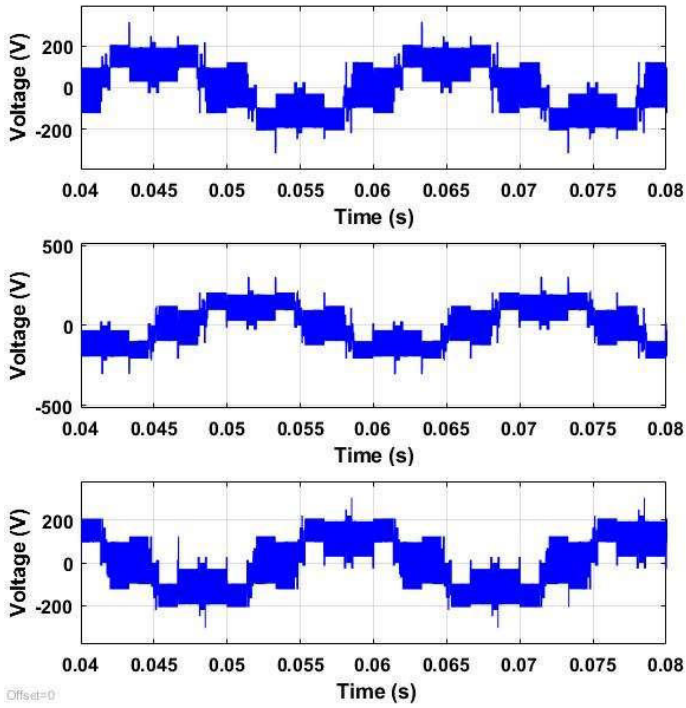

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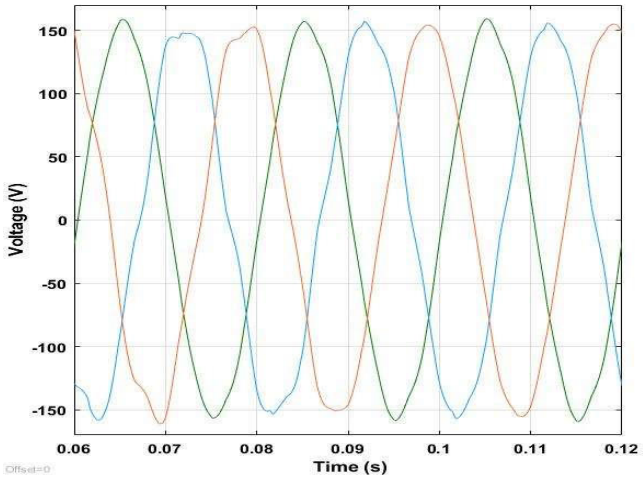

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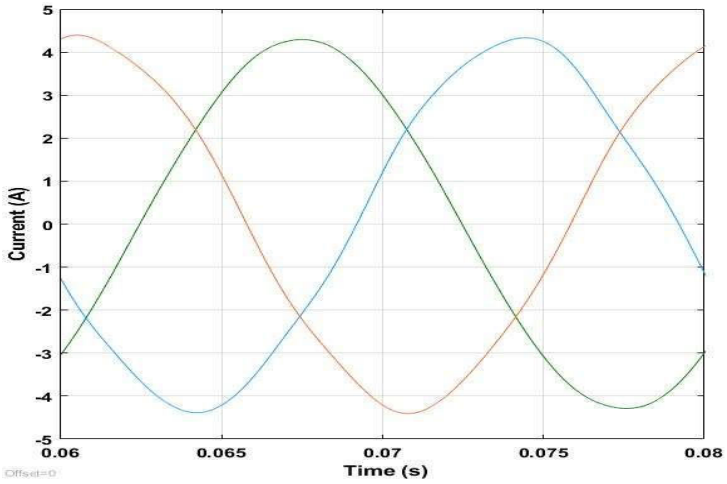

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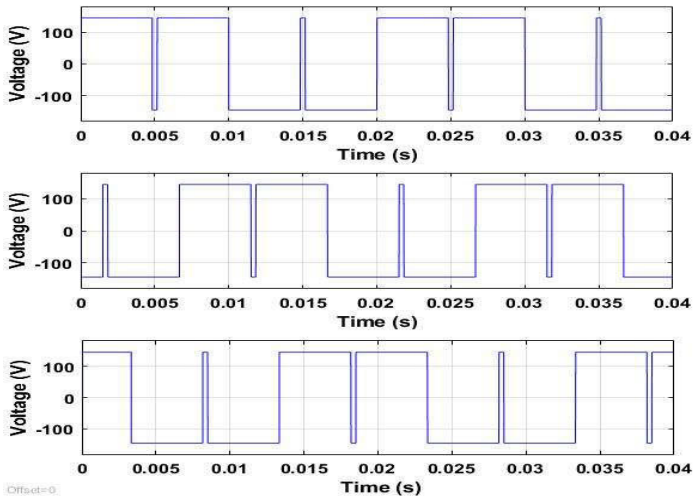


(e)

Fig. 5.8 Waveforms at different points of the power circuit of the proposed inverter: (a) three phase main inverter voltages; (b) three phase voltages after the compensator; (c) three phase voltages after LC filter (across R-L load); (d) three phase load current; (e) three phase main inverter voltages w.r.t. dc bus midpoint O

To evaluate the performance of the proposed inverter, its parameters and components were fixed as given in Table 5.1.

A conventional three phase voltage source inverter is also simulated with the same parameters shown in the above Table 5.1 using MATLAB and the line to neutral voltage of one phase along with its harmonic spectrum with and without filter are shown in Fig. 5.9. It is seen that in spite of having same maximum value of the fundamental voltage across the load, the THD content is less as compared to the three phase inverter without the compensator but with the same simulation parameters as given in Table 5.1.

Table 5.1 Values of Parameters and Component Ratings of System Studied

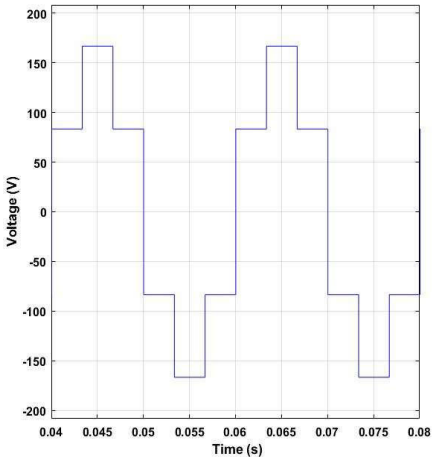
Parameter	Value	Component	Rating
Input DC voltage (V_{dc})	290 V	DC bus capacitors C1 & C2 (each)	2200 µF
Main inverter fundamental frequency	50 Hz	DC bus capacitors across Compensator	2200 µF
DC bus voltage of compensator (V'_{dc})	165 V	Filter inductor L	20 mH
Compensator switching frequency	25 kHz	Filter capacitor C	30 µF
Load VA	1000	Per Phase Load resistance	29.04 Ω
Load power factor	0.8	Per Phase Load inductance	69.3 mH

The simulated results of the proposed inverter system are summarized in Table 5.2.

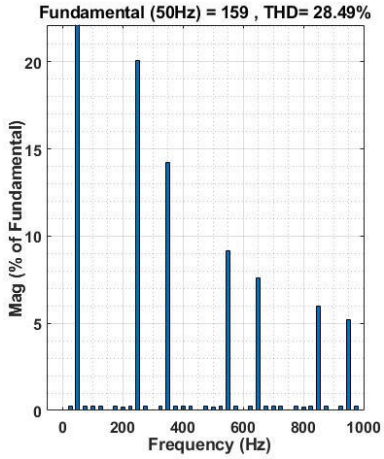
Table 5.2 Summary of simulation results

Parameter	Simulation Results
Input DC voltage (V_{dc})	290 V
Main inverter fundamental voltage(RMS)	116.8 V
DC bus voltage of active compensator (V'_{dc})	165 V
Load voltage(RMS)	110.5 V
Load current	3.03 A
Output voltage THD	1.83 %

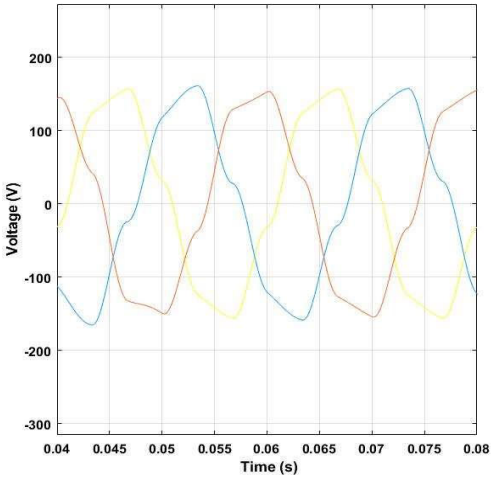
Table 5.2 shows that the input DC voltage is 290V whereas the RMS value of line to neutral of the Main inverter fundamental voltage (V_{LN}) is 116.8V in under-modulation scheme. Hence the RMS value of line to line of the main inverter fundamental voltage (V_{LL}) is $116.8x\sqrt{3}=202.30V$ and so the DC bus utilization is (202.3/290) or 69.75%.


Voltage (V)
Time (s)

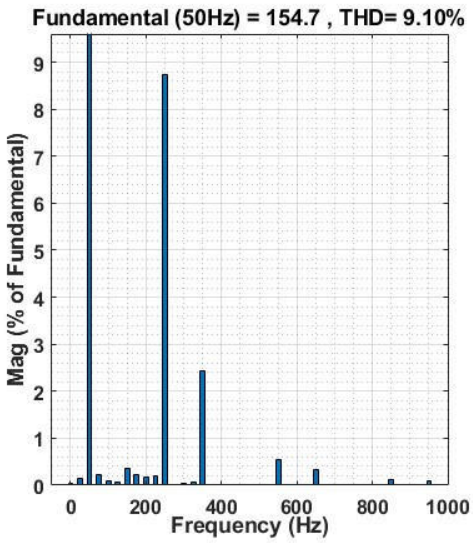
(a)


Fundamental (50Hz) = 159 , THD= 28.49%
Mag (% of Fundamental)
Frequency (Hz)

(b)


Voltage (V)
Time (s)

(c)



(d)

Fig. 5.9 (a) V_{LN} of one phase of the conventional three-phase inverter without filter; (b) harmonic spectrum of the inverter output without filter; (c) conventional three-phase inverter with filter; (d) harmonic spectrum of the inverter output with filter

The performance of the proposed inverter is compared with that of a conventional three phase inverter under simulation. The results are tabulated in Table 5.3. It will be observed that the proposed inverter is giving same output in terms of DC bus utilization, providing a improved THD than the three phase inverter without the compensator from the same DC supply while maintaining almost the same efficiency.

Table 5.3 Comparison with Conventional Three-Phase Inverter

Parameter	Three-Phase Inverter	Proposed Three-Phase Inverter
Input DC voltage	245V	290V
Number of switches	6 IGBTs to support 255V	6 IGBTs to support 290V + 12 MOSFETs in compensator to support 165V
Switching frequency	All switches at 50 Hz	6 switches at 50Hz 12 switches at 25kHz
Output AC RMS voltage (after the filter)	109.5 V	110.5 V
Output voltage THD (after the filter)	9.1 %	1.83 %
Load Current	3.03 A	3.03 A

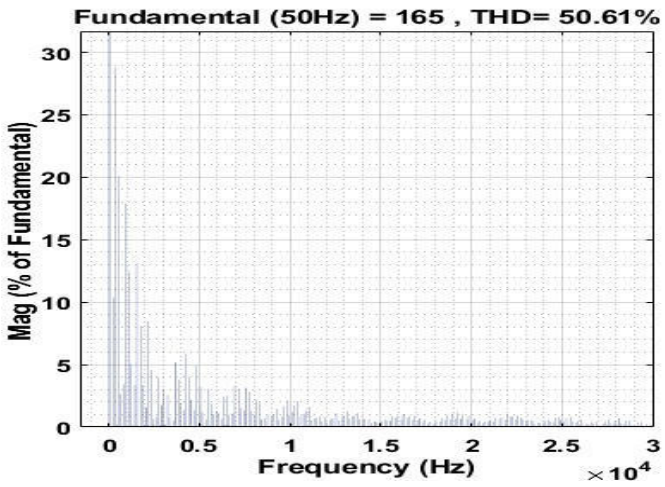
Even though the proposed inverter has a higher number of switches that increases the total conduction losses, overall total losses are comparable to the three phase inverter. This is

because of all the switches in the proposed inverter scheme, several of them switch at a low frequency only, while several face only an approximate 57% blocking voltage when compared to all the switches in the three phase inverter without the compensator, thereby creating lower switching losses.

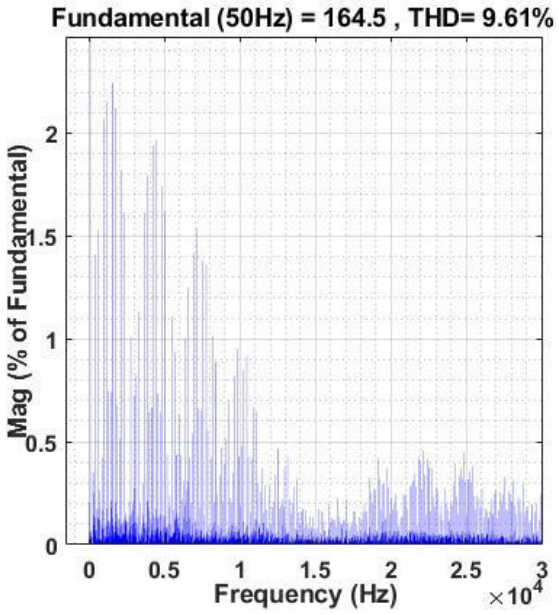
5.6 THD Analysis

The three phase inverter system comprising of the main inverter in series with the harmonic compensator is simulated using MATLAB software for the analysis of harmonic contents. It is seen that the L-N voltage of main inverter contains THD of 50.61% which is reduced to 1.83% after the natural compensations using active compensator. Hence a small LC filter is required to eliminate the high frequency PWM switching components. Also it can be stated that the RMS fundamental output of the proposed inverter system is 110.5 V which implies the maximum DC bus utilization for a three phase inverter with the input DC voltage of 290 V and with a less THD count.

Fig. 5.10 depicts the harmonic spectrums at different points of the power circuit of the proposed inverter respectively (voltage harmonic spectrum at output of main inverter, after the compensator and after the LC filter).



(a)



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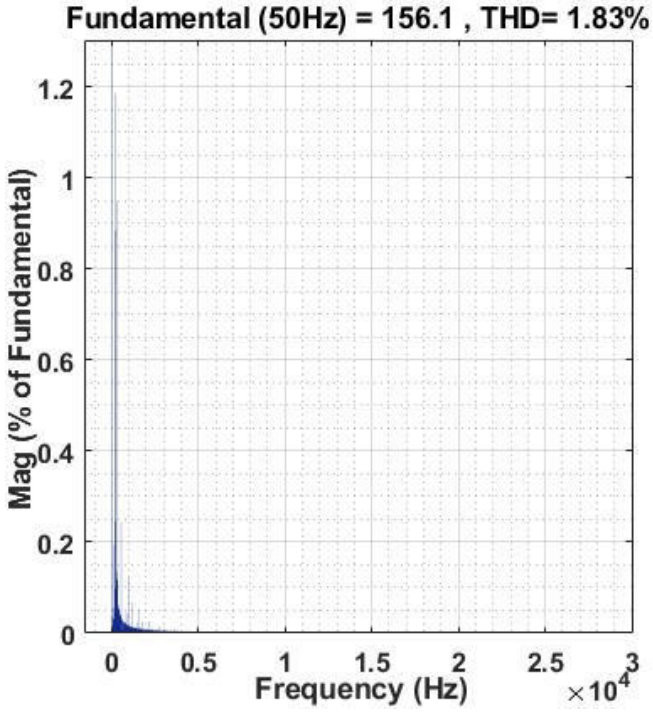

(c)

Fig. 5.10 Harmonic spectrum at different points of the power circuit of the proposed inverter: a) Harmonic spectrum of L-N voltage of main inverter; b) Harmonic spectrum of L-N voltage after the compensator; c) Harmonic spectrum of L-N voltage after LC filter (across load)

5.7 Conclusion

The application of Sinusoidal PWM in the proposed system of inverter with series compensator allows voltage control flexibility at the sacrifice of very high DC bus utilization. This work presents a new three phase inverter topology comprising of a three phase three limb 2-level inverter operated at modulation less than unity in series with three 2-level single phase active compensators, operating in the natural compensation mode. There is only one dc supply provided and the compensators use only charged capacitors on their respective dc bus, which are charged at around 0.57 times of the incoming supply due to the 2-level inverter operation. The compensated load voltage has reduced harmonic content, compared to the main inverter output. A small low-pass filter is used at the final output to remove the dominant switching frequency components of the compensator. The advantages of the proposed scheme include high dc bus utilization, low overall switching loss, small size filter, low THD voltage output.
The proposed inverter system produces a near sinusoidal three phase voltage output at fixed fundamental frequency with low switching loss. In this work, the low frequency Pulse Width Modulation will permit output voltage adjustment within the inverter. Since the value of the carrier frequency is less, the switching losses will be also less in the main three phase inverter. Also, it is found from the results that the naturally generated charging voltage across the compensator capacitor is reduced. Thus, the voltage rating of the switches used in the compensator circuit gets reduced and therefore the switches with high switching frequency can be selected for the compensator design.

CHAPTER – SIX

Conclusion and Future Scope

6.1 Conclusion

A new topology of single phase five-stepped inverter in series with two level harmonic compensator system is developed. This system is examined with three different modulation index, (1) under-modulation, (2) unity modulation index and (3) Over-modulation. Four level shifted carrier signals are used to generate gate pulses using SPWM scheme for the switches used in the first leg of the main inverter. The switches of the second leg of the same will be triggered by square pulses to create the multi-stepped output. All the switches in the main inverter are switched at low frequency. Whereas all four switches used in the compensator are switched at high frequency of 25 kHz. The principle of natural harmonic compensation is used here to mitigate the lower order harmonics. In order to create the maximum dc bus utilization this proposed model is investigated at over-modulation scheme. The proposed system is simulated in MATLAB/SIMULINK and all the results are compared with respect to a conventional SPWM inverter and also verified the same with a prototype hardware model. This new single phase inverter system produces a sinusoidal output with a very less number of higher order PWM switching frequencies that can be eliminated using a small size LC filter. Also no extra dc bus voltage source is required for the compensator. The capacitor used across the compensator output will be charged naturally due to the configuration of the proposed inverter system as discussed in chapter three.

In chapter four a three phase square wave inverter with natural compensation technique is examined. The advantages of the proposed scheme include high dc bus utilization, low overall switching loss, small size filter, low THD voltage output. The proposed inverter system produces a near sinusoidal three phase voltage output at fixed fundamental frequency with low switching loss. Since the inverter system comprises of fixed waveform, it is not possible to control the output voltage other than by adjusting the DC bus voltage of main inverter. However, introduction of low frequency Pulse Width Modulation will permit output voltage adjustment within the inverter which is described further in the chapter five in detail.
Three phase inverter with special PWM switching method for voltage control using Natural Harmonic Compensation is a new topic which causes reduction in the filter requirement with the improved DC bus utilization. The proposed three phase inverter is compared with respect to a conventional three phase PWM inverter. It is found that the proposed control scheme generates low THD output and also improves the DC bus utilization as compared to the standard one. Three phase balanced ac system voltages are compared with a low frequency triangular wave at over-modulation to create the suitable gating signals for the main three phase inverter. The phase to load neutral voltage contains large number of harmonics because of the stepped wave-shape at the main inverter output. But as the main three phase inverter is connected in series with the three single phase two level harmonic compensator, using the principle of natural compensation of harmonics, all lower order harmonics will be mitigated

naturally without any extra dc voltage source across each compensator output. Also, the three phase inverter along with the auxiliary inverter configuration can be further utilized to an open end winding transformer coupled load. At over-modulation scheme, the aforementioned topology is simulated in MATLAB with a switching frequency of 25 kHz and a resistive-inductive load.

6.2 Future Scope

The following points can be incorporated in further study to enhance the results of the inverter system:

1. In single phase five-stepped inverter with series active power filter system has been investigated with equal rating of the capacitors across the main dc bus input voltage. Hence with unequal capacitor voltage the overall system can be further analyzed in order to have the self balancing feature of the capacitor voltages across the main dc bus.
2. It is found that there are few notches in the output voltage waveforms of the proposed topology during the zero crossing instants of the ac output signal. The cause of these unavoidable spikes in the load voltage waveform is undefined in this work. This can be further investigated to have a pure sinusoidal voltage signal at the output of the inverter with almost negligible Total Harmonic Distortion (THD) factor.
3. In single phase five stepped inverter in series with the compensator, the ac output voltage is controlled by changing the modulation index at low switching frequency. In order to vary the output voltage in the wide range, the proposed inverter system can be further studied with a closed loop control system.
4. The proposed three-phase VSI with natural compensator system fed DVR can be designed to resolve any voltage sag/swell problem in the utility grid.
5. The proposed three phase PWM inverter using natural compensation technique can be further analyzed with an open-delta induction motor application and to study the motor stability problems.

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Appendix A

A1.1 Determination of Optimum Value of the Modulation Index for the Main Inverter

Parametric Values of the MATLAB Simulation Circuit of single Phase 5-Level Inverter with SAPF

Input DC voltage=100 V; Switching frequency of the Compensator=25 kHz; Modulation Index =unity

Case Study-1:

Table-A1.1

Carrier Signal Amplitude		Vsine		
v_{t1}	v_{t2}	2V	4V	9V
1.8	0.2	112.6	121.3	125.8
1.6	0.4	110.5	120.6	125.6
1.5	0.5	109.3	120.3	125.6
1.4	0.6	107.9	120	125.5
1.2	0.8	104.9	119.4	125.4
1	1	101.5	118.5	125.3

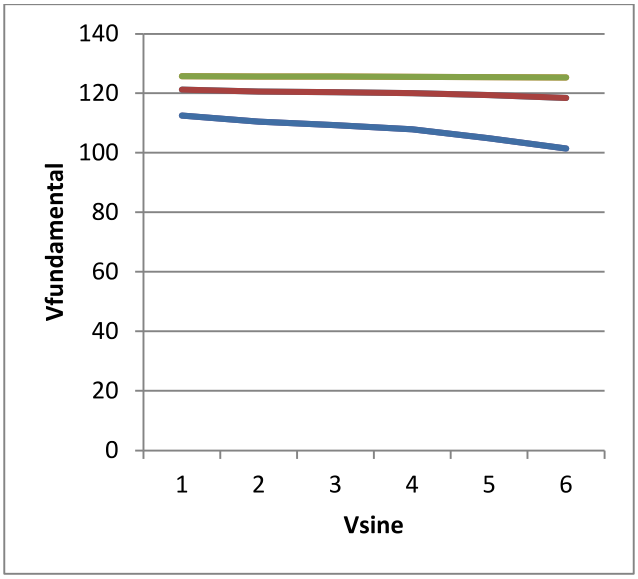

Fig.A1.1 Modulating Signal vs Fundamental Peak Voltage across Load

Case Study-2:

Table-A1.2

Vsine =2 V		
V_{t2}	V_{t1}	Fundamental(peak) voltage across $V_{AB'}$
0.1	0.9	121.2
0.2	0.8	120.7
0.3	0.7	120.1
0.4	0.6	119.3
0.5	0.5	118.5
0.6	0.4	117.6
0.7	0.3	116.6
0.8	0.2	115.5
0.9	0.1	114.4

Case Study-3:

Table-A1.3

Vsine =3 V		
V_{t2}	V_{t1}	Fundamental(peak) voltage across $V_{AB'}$
0.1	0.9	123.8
0.2	0.8	123.7
0.3	0.7	123.5
0.4	0.6	123.1
0.5	0.5	122.8
0.6	0.4	122.3
0.7	0.3	121.9
0.8	0.2	121.4
0.9	0.1	120.9

Case Study-4:

Table-A1.4

Vsine =4 V		
V_{t2}	V_{t1}	Fundamental(peak) voltage across $V_{AB'}$
0.1	0.9	125.3
0.2	0.8	125.2
0.3	0.7	125
0.4	0.6	124.8
0.5	0.5	124.6
0.6	0.4	124.4
0.7	0.3	124.2
0.8	0.2	124
0.9	0.1	123.6

Case Study-5:

Table-A1.5

V_{t1}=0.5,V_{t2}=0.5	
Vsine	Fundamental(peak) voltage across $V_{AB'}$
0	0
1	101.5
2	118.5
3	122.8
4	124.6
5	125.7
6	126.2
7	126.8
8	127
9	127.1
10	127.2

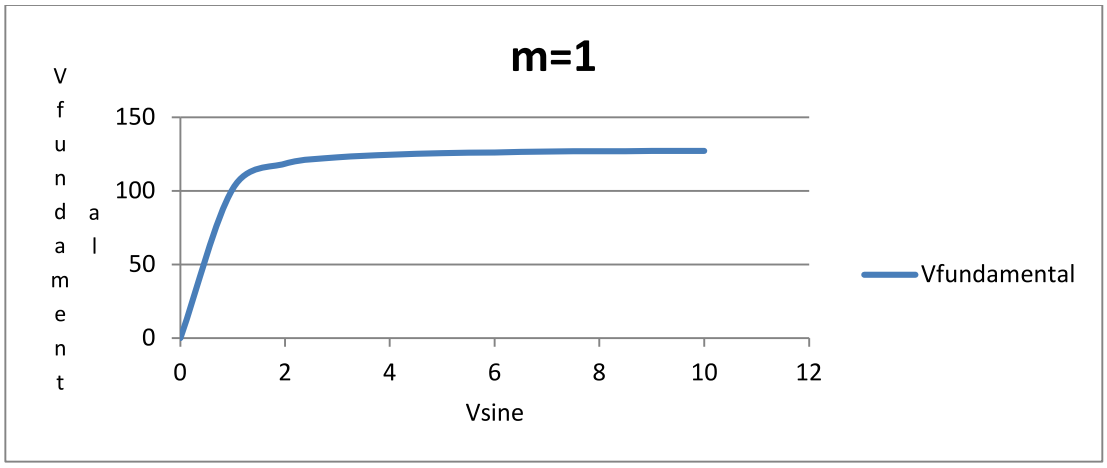

Fig.A1.2 Modulating Signal vs Fundamental Peak Voltage across Load at m=1

Case Study-6:

Table-A1.6

V_{t1}=0.5,V_{t2}=0.5	
Vsine	Fundamental(peak) voltage across VAB'
0	0
0.25	36.9
0.5	50.07
0.75	86.12
1	101.5
1.25	109.1
1.5	113.7
1.75	116.5
2	118.5
2.25	120
2.5	121.1
2.75	122
3	122.8

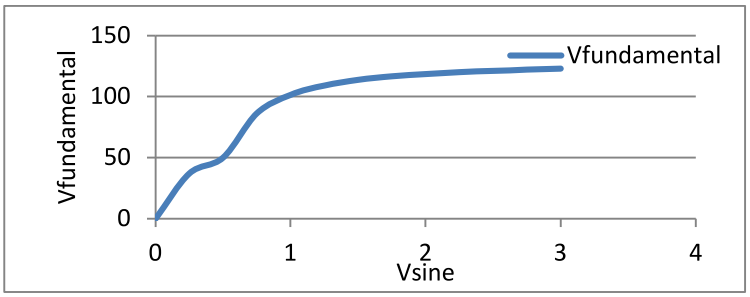

Fig.A1.3 Modulating Signal vs Fundamental Peak Voltage across Load at Over-modulation

A1.2 Design of a LC Passive Filter

Assuming, MOSFET switching frequency (f_{sw}) for the SAPF=25 kHz, cut off frequency (f) of the filter can be selected as half the switching frequency.

To determine the value of inductance L, let us assume C=2 μF

We know that, cut off frequency is given by

$$f = \frac{1}{2\pi\sqrt{LC}} \quad \text{A1}$$

or, $$L = \frac{1}{4C\pi^2 f^2} \quad \text{A2}$$

Now, by equation A2, the value of L can be calculated.

A1.3 Loss Calculation using PSIM Software of Different Configurations of Inverters

Table: A1.7 Summary of switching loss of conventional SPWM inverter and the proposed inverter

1-phase conventional SPWM inverter	
S_1	4.24 W
S_2	4.24 W
S_3	4.24 W
S_4	4.24 W
TOTAL	16.96 W

1-phase proposed inverter with a SAPF	
G1	2.87 W
G1a	2.11 W
G4a	2.13 W
G4	2.09 W
G3	2.84 W
G2	2.11 W
D1	0.194 W
D2	0.187 W
M1	3.46 W

M2	3.47 W
M3	3.50 W
M4	3.50 W
TOTAL	32.46W

Table: A1.8 Summary of switching loss of three-phase conventional inverter

3-phase conventional inverter	
S_1	1.72 W
S_2	1.89 W
S_3	1.65 W
S_4	1.89 W
S_5	1.51 W
S_6	1.37 W
TOTAL	10.03 W

Table: A1.9 Summary of switching loss of three-phase proposed inverter with a SAPF

3-phase proposed inverter with a SAPF	
Sa	1.66 W
Sa’	1.84 W
Sb	1.61 W
Sb’	1.86 W
Sc	1.47 W
Sc’	1.33 W
M1a	1.30 W
M2a	1.29 W
M3a	1.41 W
M4a	1.40 W
M1b	1.31 W
M2b	1.30 W
M3b	1.43 W
M4b	1.42 W
M1c	1.30 W
M2c	1.31 W
M3c	1.22 W
M4c	1.23 W
TOTAL	25.69 W

Table: A1.10 Summary of switching loss of three-phase conventional SPWM inverter

3-phase conventional SPWM inverter	
S_1	1.5W
S_2	1.49 W
S_3	1.5W
S_4	1.49 W
S_5	1.5W
S_6	1.49 W
TOTAL	8.97W

Table: A1.11 Summary of switching loss of three-phase proposed PWM inverter with a SAPF

3-phase proposed inverter with a SAPF	
Sa	1.57 W
Sa’	1.57 W
Sb	1.57 W
Sb’	1.57 W
Sc	1.57 W
Sc’	1.57 W
M1a	1.26 W
M2a	1.24 W
M3a	1.26 W
M4a	1.24 W
M1b	1.28 W
M2b	1.28 W
M3b	1.28 W
M4b	1.29 W
M1c	1.91 W
M2c	1.84 W
M3c	1.87 W
M4c	1.80 W
TOTAL	26.97 W

Table: A1.12 Part Number of the Devices used for Loss Calculation using PSIM

Product	Manufacturer	Part No	Package	Vce max	Ic max	Tj max
IGBT Transistors	Fairchild Semiconductor	HGTG20N60A4D	Discrete	600V	40A	150° C

Product	Manufacturer	Part No	Package	Vce max	Ic max	Tj max
N-Channel MOSFET	Fairchild Semiconductor	FCD7N60	Discrete	600V	7A	150° C

Appendix B

MATLAB Circuits of Different Inverter Configurations & Control Circuits

B1.1 Single phase 5-Level Inverter with Natural Compensator

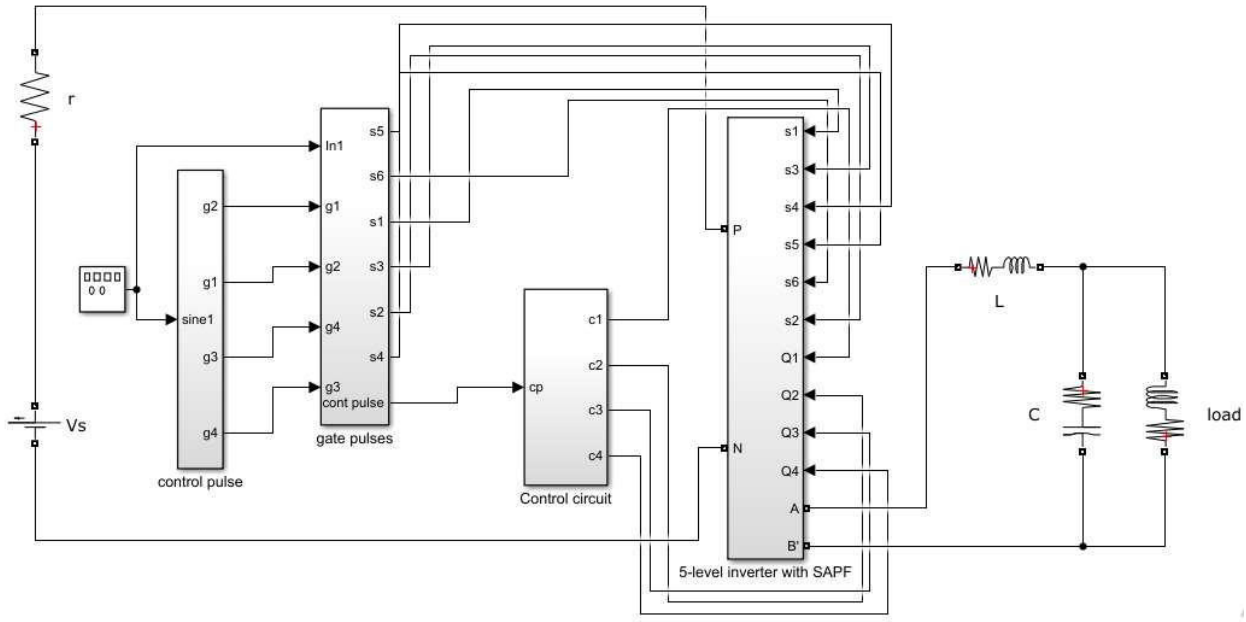

Fig. B1.1 Circuit diagram for single phase main inverter with natural harmonic compensator

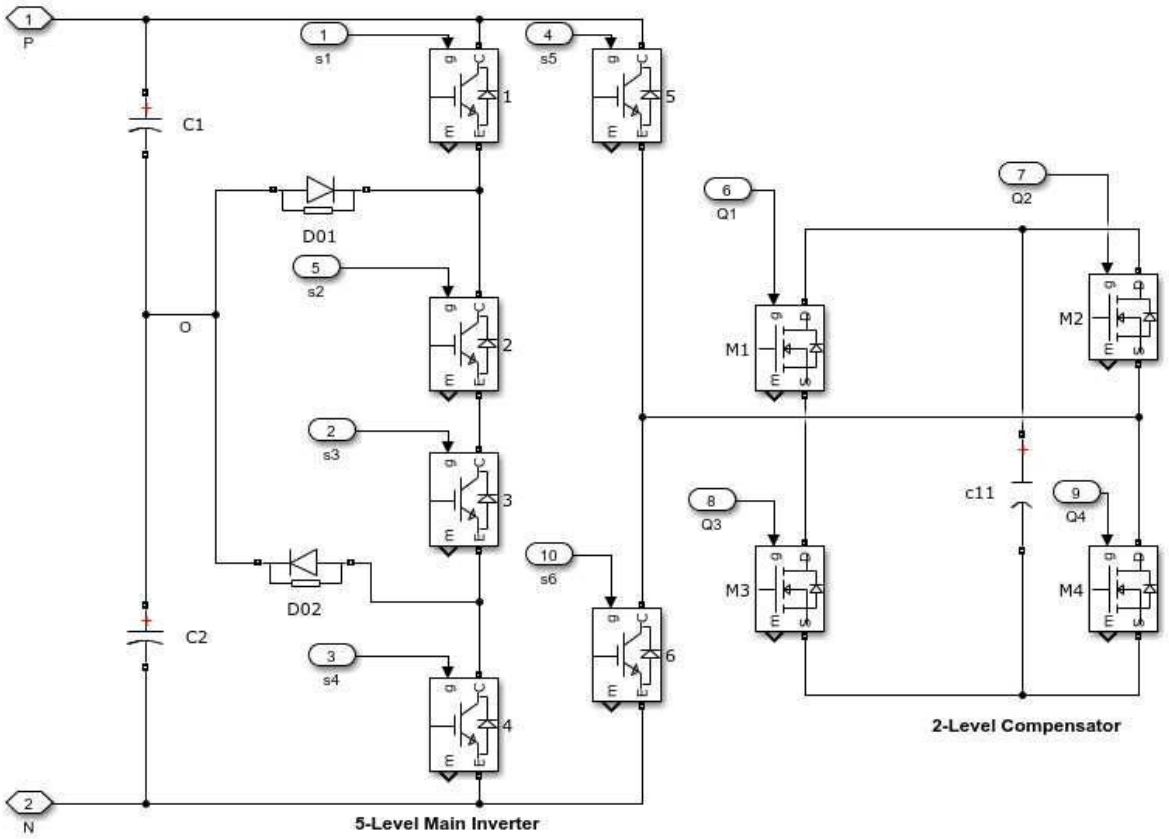

Fig. B1.2 Power circuit diagram for single phase main inverter with natural harmonic compensator

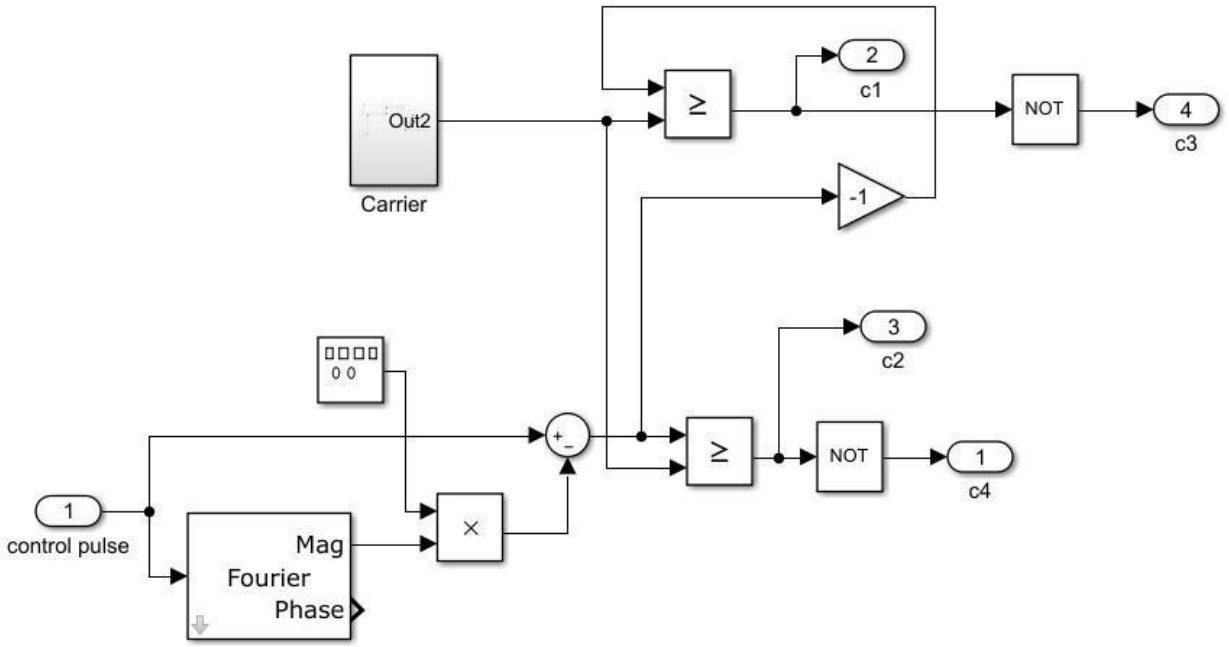

Fig. B1.3 Control circuit diagram for single phase natural harmonic compensator

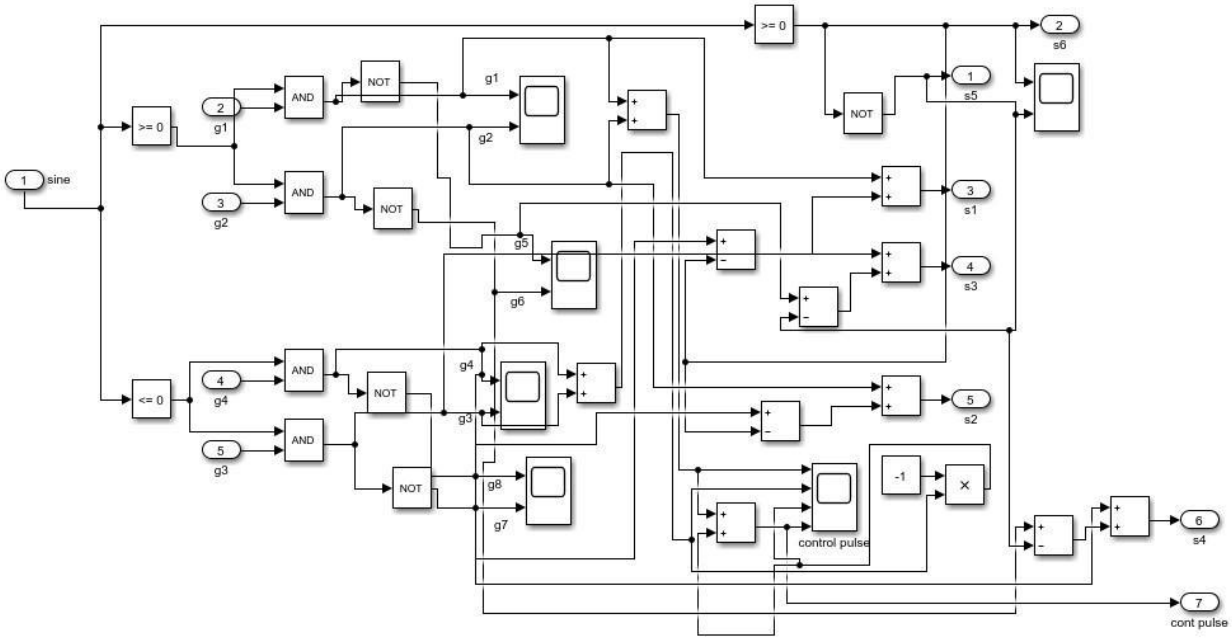

Fig. B1.4 Control circuit diagram for single phase main inverter

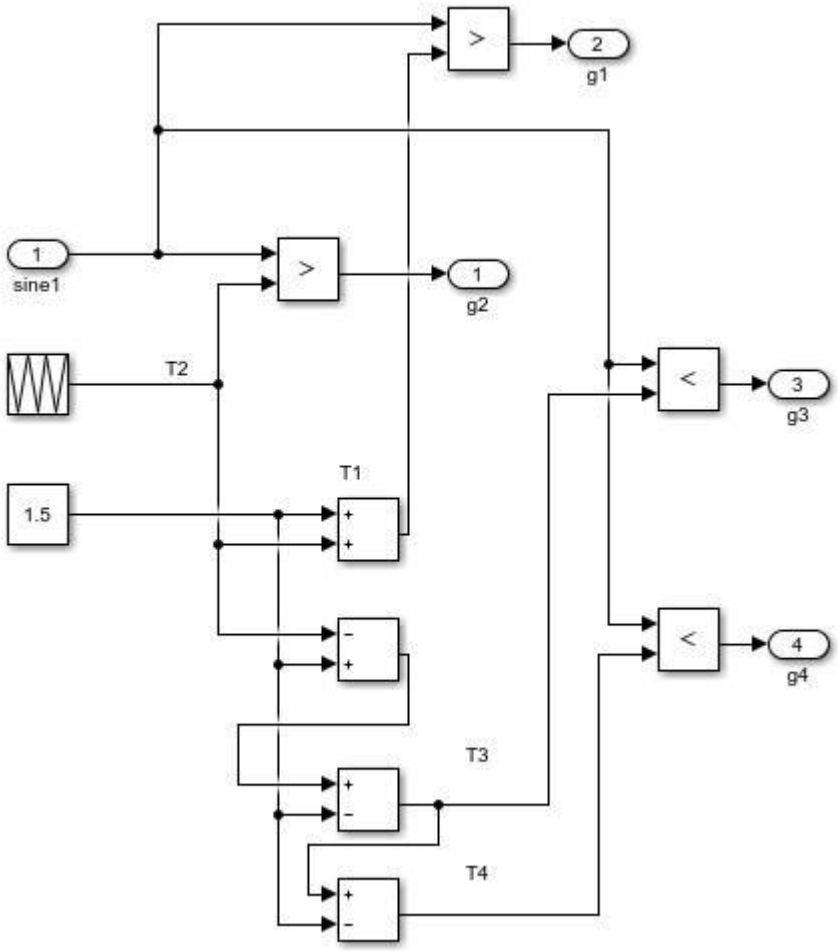

Fig. B1.5 Control circuit diagram for single phase main inverter

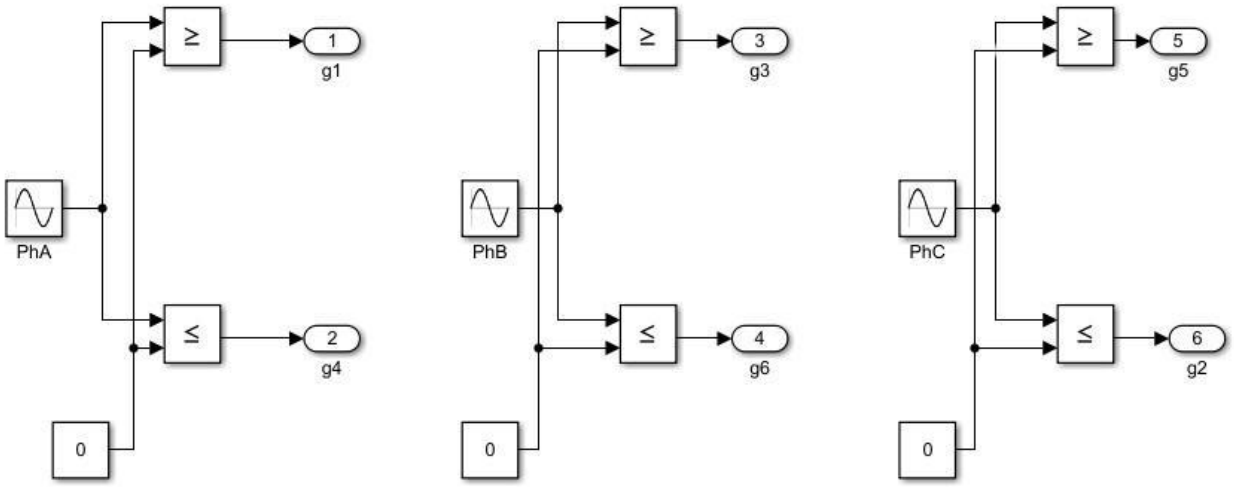

Fig. B1.6 Control circuit diagram for three phase main inverter

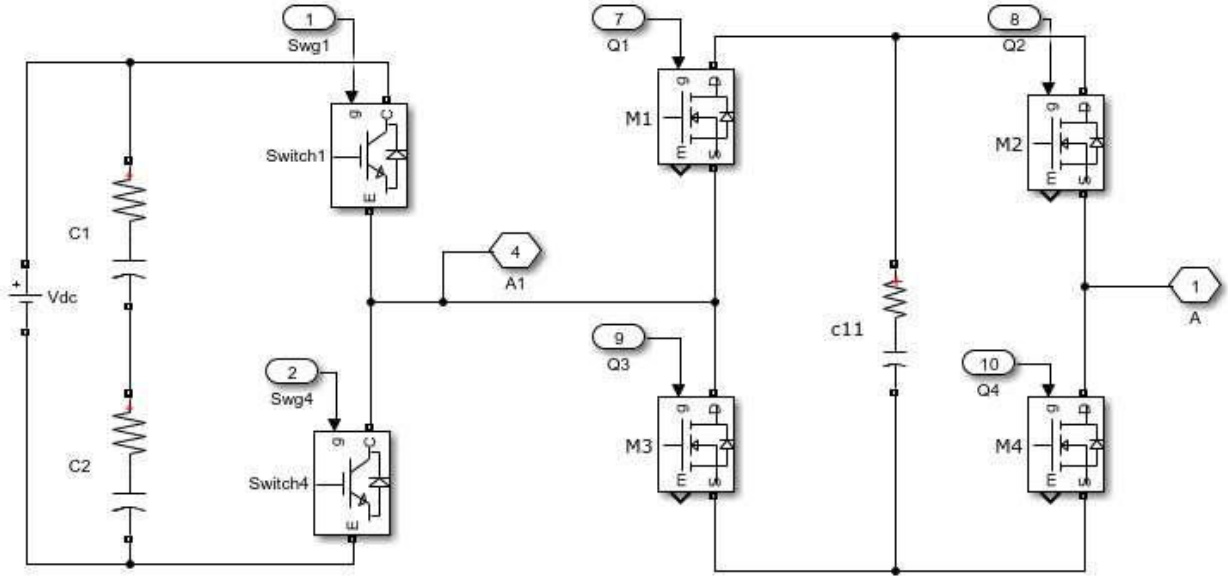

Fig. B1.7 One phase of power circuit diagram for three phase main inverter with a SAPF

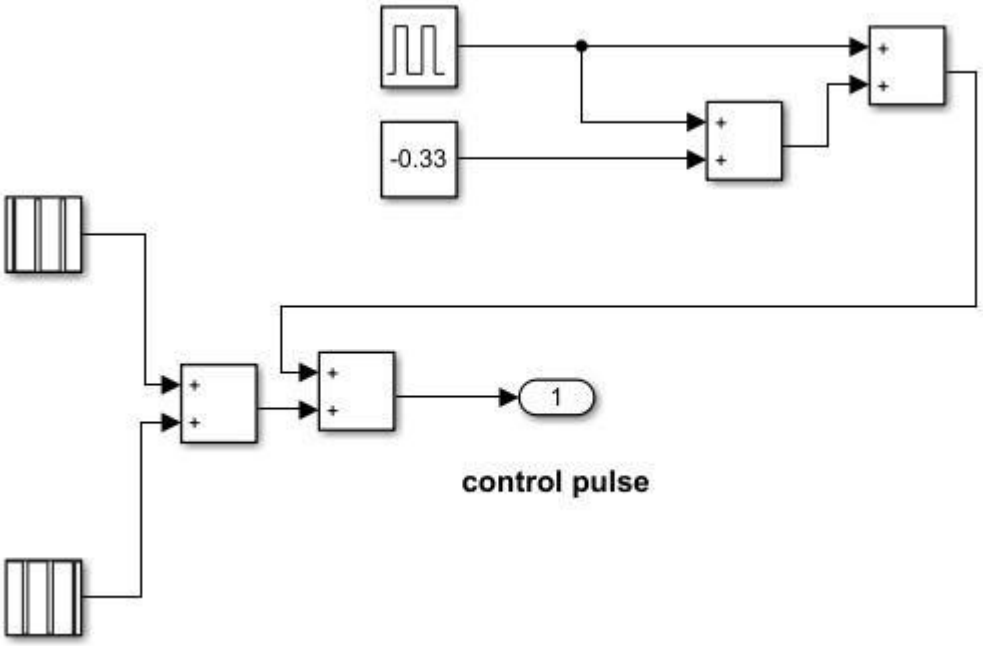

Fig. B1.8 Generation of stepped signal for SAPF

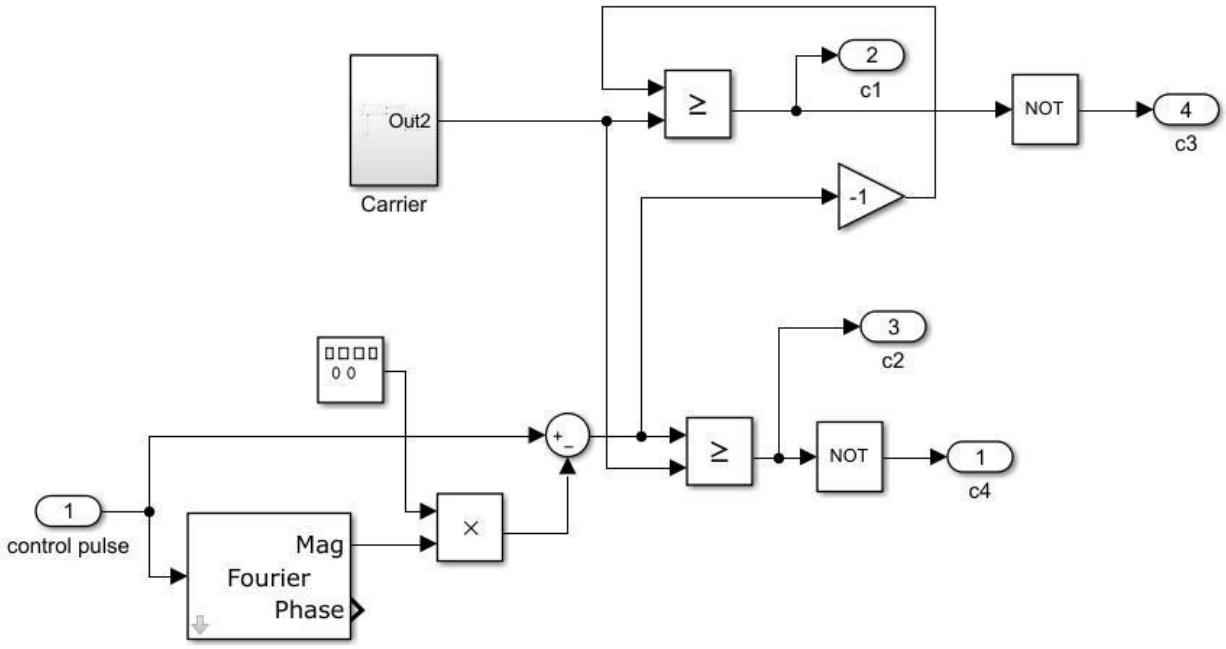

Fig. B1.9 Gate pulse generation for one phase of the compensator

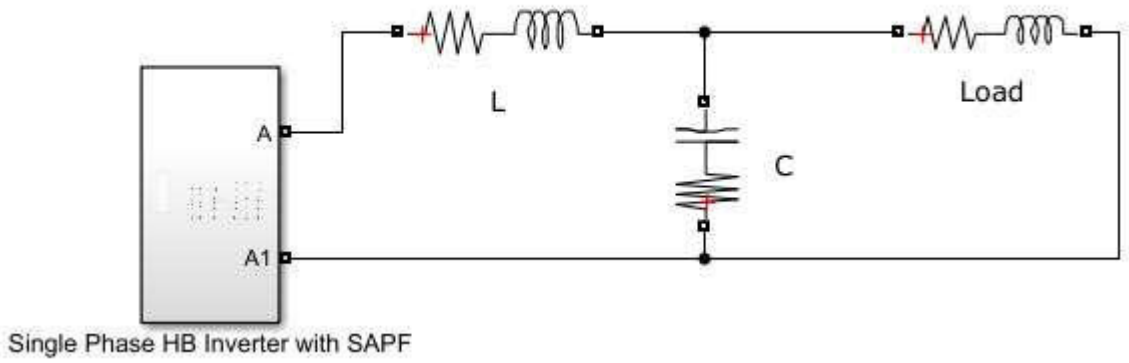

Fig. B1.10 Power circuit diagram of overall inverter system

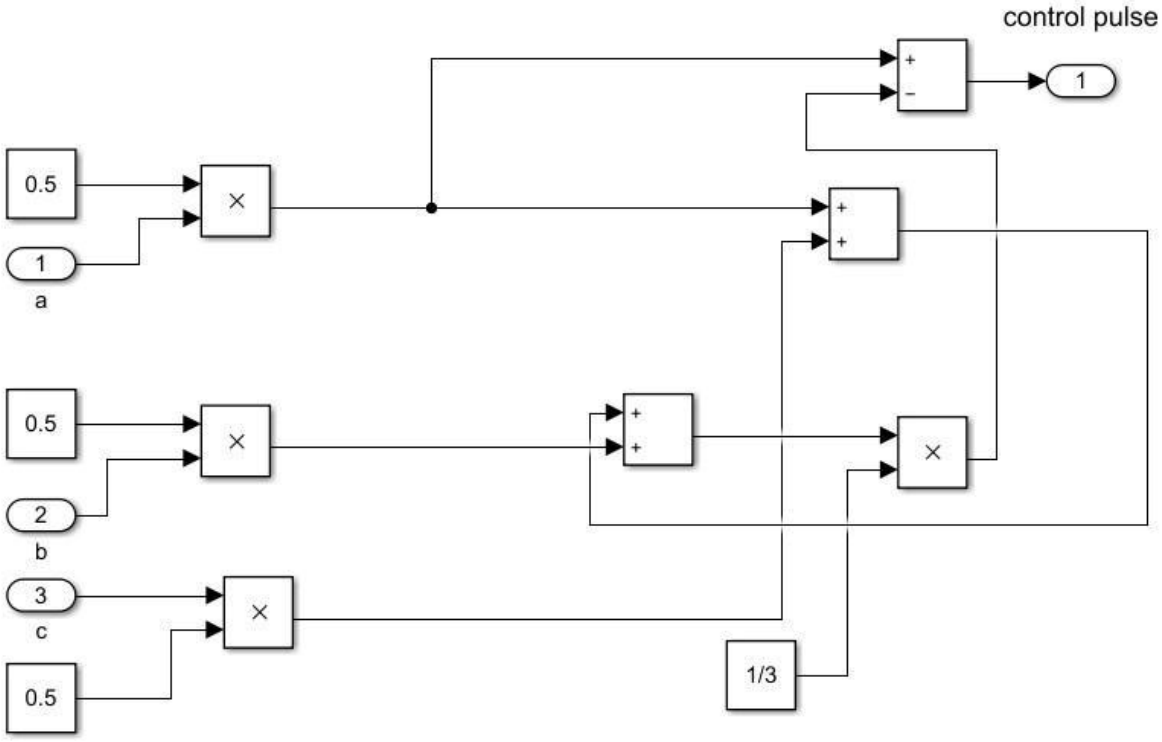

Fig. B1.11 Generation of stepped signal for SAPF

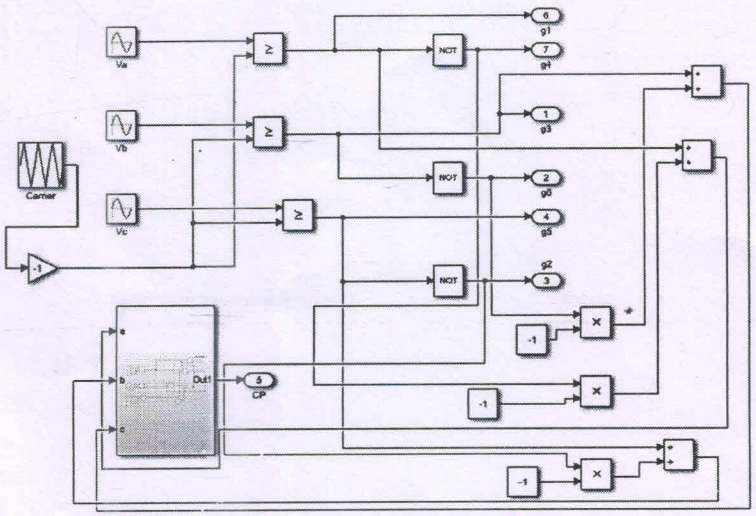

Fig. B1.12 Gate pulse generation for Main Inverter

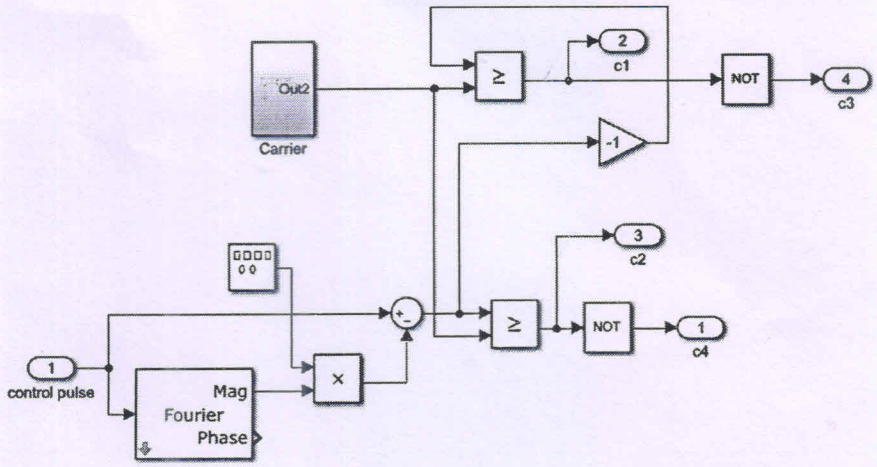

Fig. B1.13 Control Circuit for SAPF

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