ANALYSIS OF THREE LEVEL BI-DIRECTIONAL DC –DC CONVERTER AND ITS APPLICATION IN ELECTRIC VEHICLE

This thesis is submitted in the partial fulfilment of the requirements of the degree

MASTER OF ELECTRICAL ENGINEERING
(CONTROL SYSTEM)

Submitted by

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Certificate of Recommendation

This is to certify that **Mr. Rahul Kumar (002010802012)** has completed his dissertation entitled, "**Analysis of Three Level Bi-directional DC– DC Converter and its Application in Electric Vehicle**", under the direct supervision and guidance of **Dr. Sayantan Chakraborty**, Department of Electrical Engineering, Jadavpur University. We are satisfied with his work, which is being presentedfor the partial fulfilment of the degree of **Master of Electrical Engineering(Control System)** of Jadavpur University, Kolkata-700032.

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Certificate of Approval

The foregoing thesis entitled "**Analysis of Three Level Bi-directional DC – DC Converter and its Application in Electric Vehicle**" is hereby approved as a creditable study of an Engineering subject carried out and presented in a manner satisfactory to warrant its acceptance as a pre-requisite to the degree of Master of Electrical Engineering(Control System) for which it has been submitted. It is understood that, by this approval the undersigned does not necessarily endorse or approve any statement made, opinion expressed, or conclusion therein but approve this thesis only for the purpose for which it is submitted.

Final Examination for Evaluation of the Thesis

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I hereby declare that this thesis contains a literature survey and original research work by the undersigned candidate, as part of his Master of Electrical Engineering(Control System) curriculum. All information in this document has been obtained and presented in accordance with academic rules and ethical conduct. I also declare that, as required by these rules and conduct, I have fully cited and referenced all material and results that are not original to this work.

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ABSTRACT

Ultra-capacitors, are widely employed in power conversion systems such as controlled electric drives, active filters, power conditioners, and uninterruptible power supplies. The ultracapacitor is used as a form of energy storage since it has a short charge/discharge time. The ultracapacitor is connected to the power conversion system via an interface dc-dc power converter to improve flexibility and efficiency. The dc-dc power converter employs a variety of topologies, including isolated soft-switched dc-dc converters and non isolated two-level single-phase or multiphase interleaved converters.

The significant challenges faced by the engineers in the design and implementation of advanced electric drives are the recovery of the braking energy and the drive system's ability to ride over obstacles. In some applications, such as traction and lift drives, an approach based on the standard diode front-end-drive converter fitted with an energy-storage component is utilized in addition to the conventional alternatives, such as back-to-back and matrix converters. With the rapid development of electrochemical double layer capacitors, often known as ultra-capacitors, this strategy has recently gained attention.

The drive is connected to the ultracapacitor through a dc-dc converter to increase system flexibility and efficiency. The converter is managed in a fashion that satisfies the three control goals of peak-power filtering, ultracapacitor state of charge management, and dc-bus voltage management. Using an ultracapacitor as an energy storage and backup power source, we have covered the modelling and control components of the regenerative controlled electric motor in this study.

Contents

List of Abbreviations

BDC	: Bidirectional DC- DC Converter
UC	: Ultra-capacitor
EV	: Electric Vehicle
TLC	: Three Level Converter
CBC	: Conventional Two Level Converter
BIC	: Bidirectional Interleaved Converter
CCM	: Continuous Conduction Mode
SOC	: State of Charge
PWM	: Pulse Width Modulation
UDDS	: Urban Dynamometer Driving Schedule
UPS	: Uninterrupted Power Supply
MM	: Motoring Mode
STB	: Standby Mode
MC	: Motoring Energy Recovery Mode
RT	: Ride Through Mode
MM-CH	: Ultra-capacitor Charging Mode
DAB	: Dual Active Bridge
HESS	: Hybrid Energy Storage System
HEV	: Hybrid Electric Vehicle
IPSPM	: Interior Permanent Magnet Synchronous Motor

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CHAPTER 1

BIDIRECTIONAL DC-DC CONVERTER

1. Introduction:

Bi-directional dc-dc converters (BDC) have recently attracted a lot of interest due to the growing demand for systems that can transfer energy bi-directionally between two dc buses. Besides its usual use in dc motor drives, novel BDC applications include energy storage in renewable energy systems, fuel cell energy systems, hybrid electric vehicles (HEV), and uninterruptible power supply (UPS)[1].

The fluctuating nature of most renewable energy supplies, such as wind and sun, makes them unsuitable for use as a sole source of power. To compensate for these oscillations and ensure a smooth and continuous power supply to the load, one typical approach is to deploy an energy storage device in addition to the renewable energy resource. Batteries and supercapacitors are the most widely used and cost-effective energy storage devices in the medium-power range, so a dc-dc converter is always needed to enable energy transfer between storage devices and the rest of the system. A bidirectional power flow converter with flexible control in all working modes is required.

BDCs are used in HEV applications to connect different dc voltage buses and transmit energy between them. A BDC, for example, is used to interchange energy between the main batteries (200-300V) and the drive motor via a 500V direct current link. Some significant requirements for the BDC employed in this application include high efficiency, lightweight, compact size, and high reliability[2].

BDCs are also used in line-interactive UPS systems, which do not employ double conversion technology and hence achieve superior efficiency. During normal mode, energy can be sent back to the inverter's dc bus and used to charge the batteries via a BDC because the line-interactive UPS's output terminals are linked to the grid. In backup mode, the battery supplies the inverter dc bus again via BDC, but in the opposite power flow direction[3].

1.1 Conversion of Unidirectional DC-DC Converter Bidirectional DC-DC Converter:

Basic dc-dc converters like buck and boost converters are unable to transfer power in both directions. The presence of diodes in their structure prohibits reverse current flow. In general, a unidirectional dc-dc converter can be converted to a bidirectional converter by replacing the diodes with a controllable switch in its structure. An elementary buck and boost converter's structure is depicted in Fig. 1.1, as is the process by which the diodes in the converter can be changed to create a bidirectional converter. It is significant that the converter that is produced has the same structure in both situations.

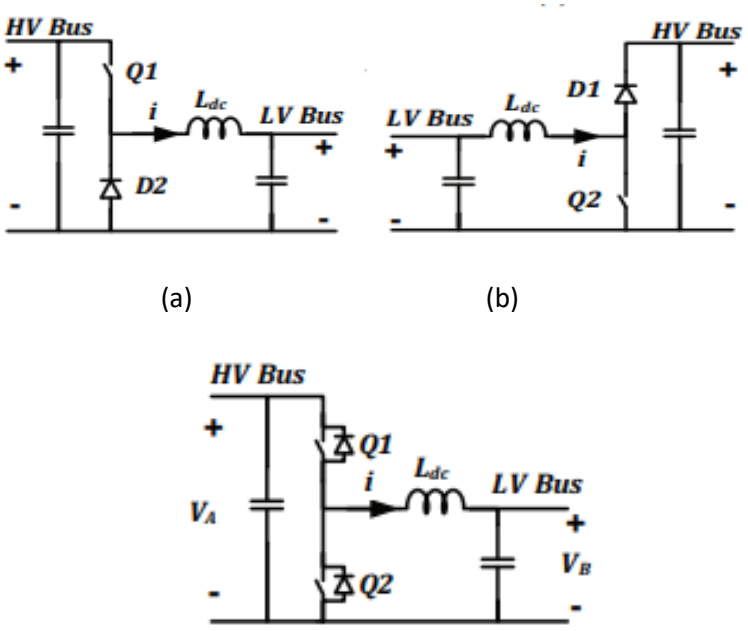


Fig. 1.1 (a) Unidirectional buck converter, (b) Unidirectional boost converter and (c) transformation to bidirectional converter by substituting diodes with a controllable switch [3]

1.2 Types of Bidirectional DC-DC Converter:

The bidirectional dc-dc converter is classified into two types (see in fig.1.2). 1) Non-isolated bidirectional DC-DC converter. 2) Isolated bidirectional DC-DC converter. Non-isolated bidirectional DC-DC converter is an impedance network composed of inductor, capacitor and used to realize direct DC-DC conversion.

1.3. Non-isolated Bidirectional DC-DC Topologies:

1.3.1 Construction of Impedance Networks of Novel Non-isolated Bidirectional DC-DC Converters:

The unique non-isolated bidirectional DC-DC converters, which are based on the fundamental bidirectional DC-DC converters, are intended to enhance the functionality of bidirectional DC-DC converters by impedance transformation from the view points of improving the voltage conversion ratio and efficiency, lowering the current ripple on the power source side, lowering the voltage/current stresses of the devices, and enhancing the input and output characteristics. The unique non-isolated DC-DC converter topologies that are now in use are categorized in this research based on various combinations of energy storage components. There are four categories of the unique non-isolated bidirectional DC-DC impedance networks: hybrid/cascaded, inductor + inductor, capacitor + inductor, and inductor + capacitor.

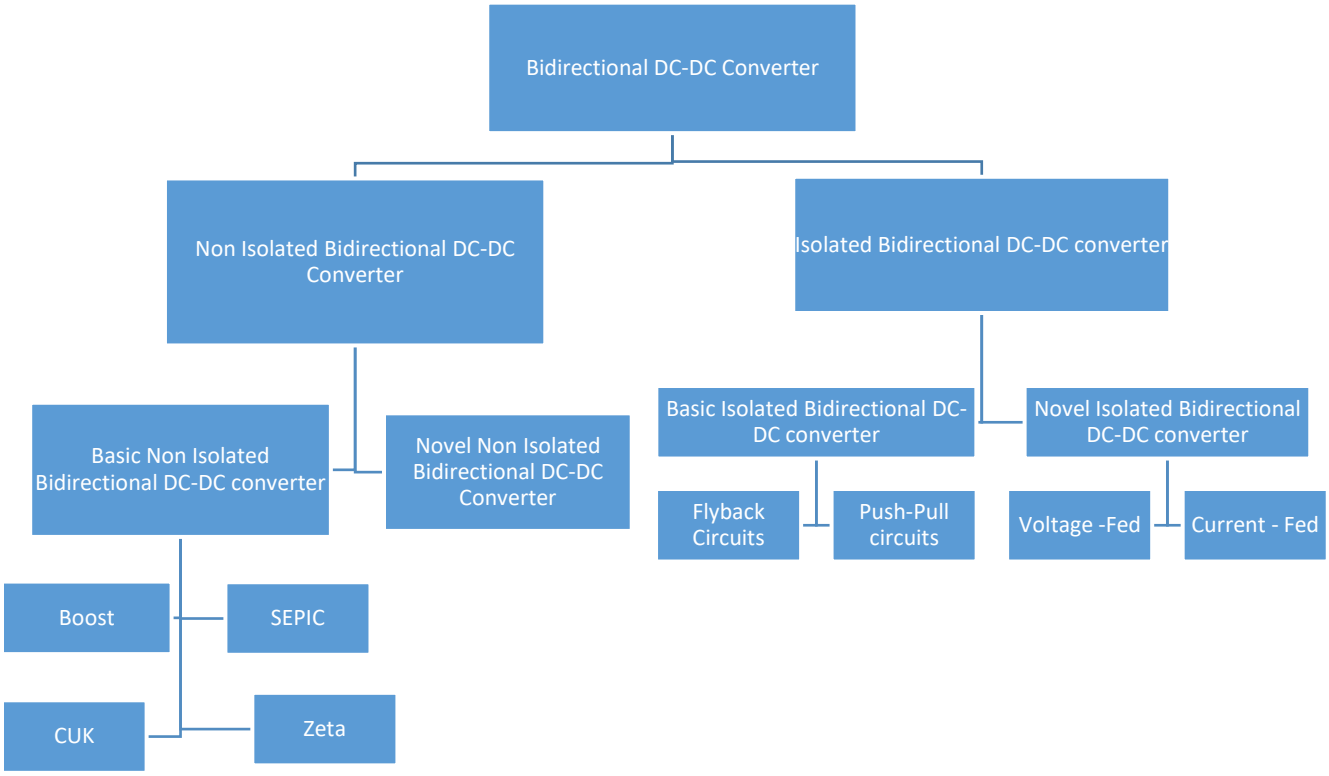


Fig.1.2 Classification of Bidirectional DC-DC Converter [4]

1.3.1.1 Inductor + Inductor type:

Two inductors are charged in parallel and discharged in series to create a switched inductor impedance network, which increases the voltage conversion ratio. An interleaved impedance network is created by turning on each inductor sequentially with the same trigger phase difference in order to eliminate the current ripple on the power source side. In order to achieve parallel charging and series discharging of inductors and obtain the quadratic Boost impedance network, the power source and one capacitor are employed as energy sources, respectively. Fig. 1.3 depicts the approach used to derive inductor + inductor impedance networks.

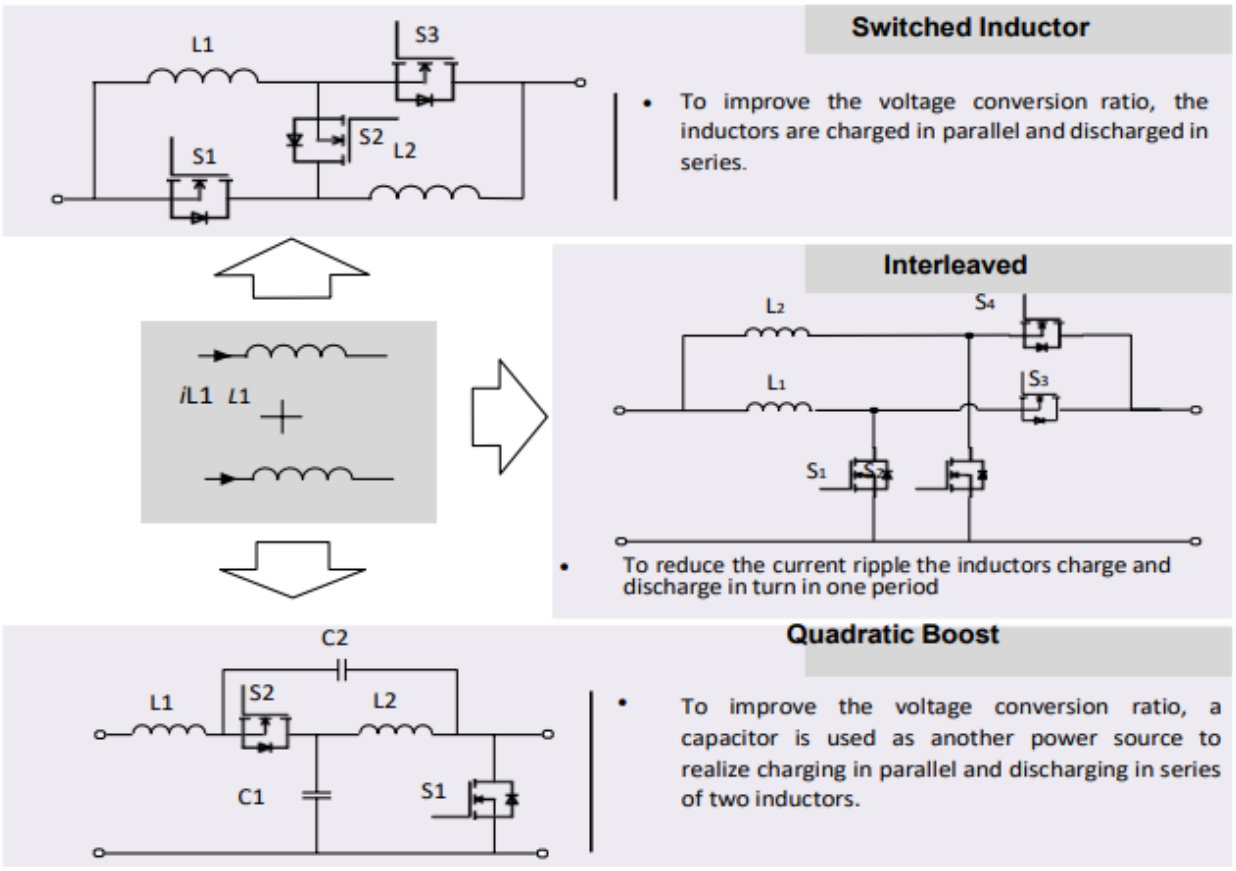


Fig.1.3 The derivation of inductor + inductor impedance network [5]

1.3.1.2 Capacitor + Capacitor type:

Two capacitors are charged in parallel and discharged in series to create a switched capacitor impedance network, which increases the voltage conversion ratio. The voltage multiplier (VM) impedance network can be obtained by first transferring energy between the two capacitors, followed by the capacitor and the power source supplying energy to the load at the same time. Inductor and switch only allow current to flow in one direction when the converter is operating steadily. The Z source impedance network can be created by switching the switch in the switched capacitor with an inductor without breaking the circuit rules.

The quasi-Z source impedance network can be created by impedance transforming the Z source in order to fix the defects of discontinuous current at the power source side and non-common ground of the input and output of Z sources. Two capacitors made to tolerate high voltages are combined to create a three level impedance network, which lowers the voltage stress.

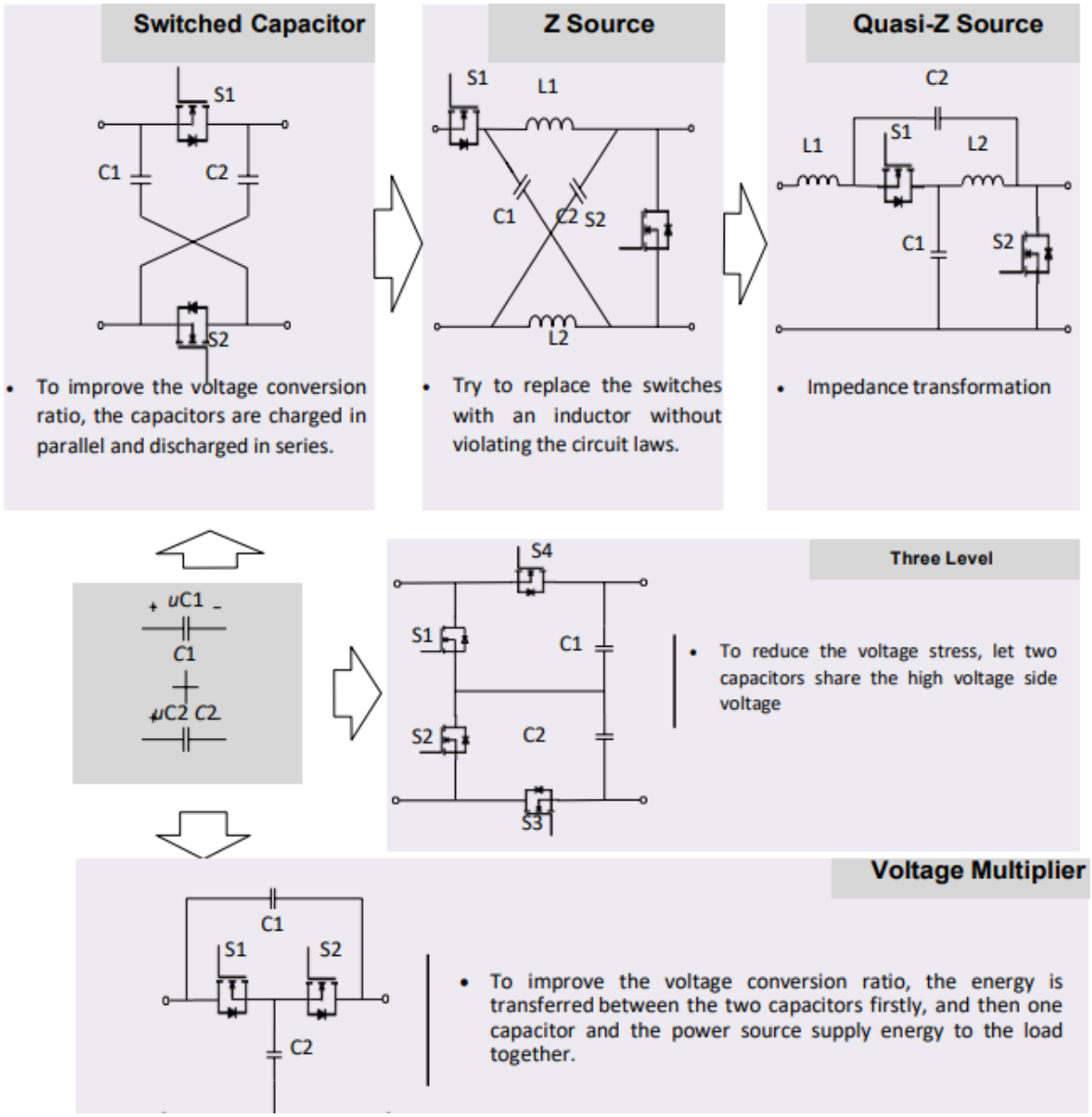


Fig.1.4 The derivation of capacitor + capacitor impedance network [4]

1.3.1.3 Inductor + Capacitor type:

The voltage lifting circuit is created by charging a capacitor and an inductor in parallel and discharging them in series to increase the voltage conversion ratio. Capacitors (or inductors) are connected between the two bridge arms made of four switches to increase the voltage conversion ratio. To achieve filtering, components (such as capacitors) are put on the power source side, generating an H-bridge impedance network. Fig. 1.5 depicts the approach used to derive inductor + capacitor impedance networks.

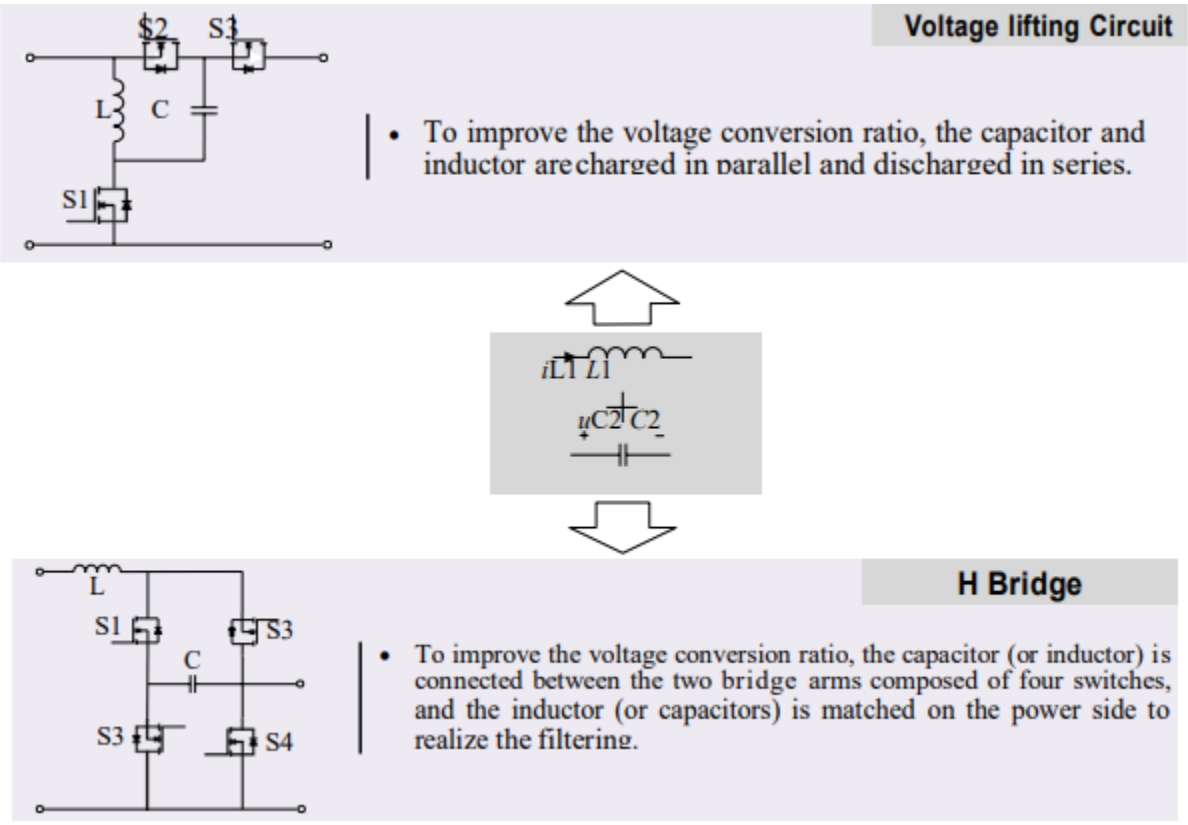


Fig.1.5 The derivation of inductor + capacitor impedance network [4]

1.3.1.4 Hybrid/Cascaded:

Bidirectional DC-DC converter performance can be improved and new topologies can be created by integrating and cascading the three types of impedance networks mentioned above. The purpose of a cascaded impedance network is to share some devices without breaking the circuit law, connect more than two impedance networks sequentially, and enhance topological performance. In order to achieve topology optimization, functional units of the existing topology can be swapped out for topologies (or impedance networks), yielding a hybrid impedance network. There are numerous publications [3] – [4] on cascaded structure and comparatively few on hybrid structure in the bidirectional DC-DC references that are currently available. The cascaded topologies are the main topic of this work.

1.3.2. Current Status of Non-isolated Bidirectional DC-DC Converter Topologies:

The derivation techniques of the impedance networks of the novel bidirectional DC-DC converters are similar to those of the unidirectional DC-DC converters. When the diode in the unidirectional DC-DC converter is swapped out for the switch, the equivalent bidirectional DC-DC converter architecture is produced.

There are only a few topologies based on switched inductor, switched capacitor, Z source, and voltage raising circuit because Novel Electric Vehicle have high requirements for the input and output common ground, as well as power source side current ripple of bidirectional DC-DC converters. In addition, it is also rare to find references to bidirectional DC-DC converters based on quadratic Boost and hybrid.

There are a number of non-isolated bidirectional DC-DC converter topologies now available, including bidirectional Boost, Cuk, SEPIC topologies, interleaved bidirectional DC-DC topologies, three level bidirectional DC-DC topologies, bidirectional DC-DC topologies based on VM, bidirectional DC-DC topologies based on quasi-Z sources, bidirectional DC-DC topologies based on H bridges, and cascaded.

Table 1.1 Advantages and disadvantages of typical non-isolated bidirectional DC-DC impedance networks

Classification	**Impedance Network**	**Advantages**	**Disadvantages**
Basic	Boost/SEPIC/ Cuk	• Simple Structure • Easy to control • Easy to generate new topologies • Low number of devices	• Narrow voltage conversion range
Inductor + Inductor	Switched Inductor	• Wide voltage conversion range • Easy to control • Easy to generate new topologies	• Pulsating current of power sources side
	Interleaved	• Low current ripple of power side • Input-Output common ground	• Requiring high control precision • Large number of switches
	Quadratic Boost	• Wide voltage conversion range • Continuous power source side current • Easy to control • Input-Output common ground	• High voltage stress at high voltage side
Capacitor + Capacitor	Switched Capacitor	• Wide voltage conversion range	• Input- Output non common ground • Pulsating current of power source side
	VM	• Wide voltage conversion range • Input- Output common ground	• High voltage stress at high voltage side
	Z Source	• High voltage conversion ratio in non extreme duty cycle	• Discontinuous power source side current • Input- Output non common ground • Steep slope of voltage conversion ratio • Requiring high control precision

	Quasi-Z Source	• High voltage conversion ratio in non extreme duty cycle • Continuous power source side current • Input- Output common ground	• Requiring high control precision • Steep slope of voltage conversion ratio • High voltage stress at high voltage side
Inductor + Capacitor	Voltage lifting circuit	• Easy to generate new topologies • Input- output common ground	• No obvious increase in voltage • Pulsating current of power source side
	H bridge	• Easy to generate new topologies • Less number of energy storage devices • Input- output common ground	• Large no of switches • Requiring high control precision
Hybrid/ cascaded	Cascaded	• Wide voltage conversion range • Easy to generate new topologies	• Large number of devices • Low conversion efficiency • Low power density
	Hybrid	• Wide voltage conversion range • Easy to generate new topologies	• Large number of devices • Low conversion efficiency • Low power density

1.3.3 Comparison and Evaluation of Typical Non-isolated Bidirectional DC-DC Converter:

The technology, power source side current, step-up ratio, step-down ratio, duty cycle range, voltage stress of switches, current stress of switches, number of devices, and presence of common ground are the ten comparison criteria used to rank non-isolated bidirectional DC-DC converters in this section. Table 1.2 summarizes the index distribution for nine common non-isolated bidirectional DC-DC topologies.

Table 1.2 Indexes of typical non-isolated bidirectional DC-DC topologies

Topo Logies	**Technology used**	**Power Source Side Current**	**Step-up ratio U_{high}/U_{low}**	**Step down ratio U_{low}/U_{high}**	**Duty-cycle range**	**Voltage stress of switches**	**Current stress of switches**	**Number of devices**			**Common ground**
Ref. [8]	Boost	Non Pulsating	$\frac{1}{1-d}$	d	0<d<1	u_{high}	$\frac{I_{high}}{1-d}$	1	1	2	Yes
Ref. [9]	Interleaved	Low Ripple	$\frac{3}{1-d}$	$\frac{d}{3}$	0.67<d<1	$\frac{2}{3}u_{high}$	$\frac{2I_{high}}{1-d}$	3	3	6	No
Ref. [10]	Interleaved + Three level	Low Ripple	$\frac{2}{1-d}$	$\frac{d}{2}$	0<d<0.5 0.5<d<1	$\frac{u_{high}}{2}$	$\frac{2I_{high}}{1-d}$	2	4	5	No
Ref. [11]	Three level	Non Pulsating	$\frac{2}{1-d}$	$\frac{d}{2}$	0<d<1	$\frac{u_{high}}{2}$	$\frac{2I_{high}}{1-d}$	1	3	4	No
Ref. [12]	VM	Non Pulsating	$\frac{2}{1-d}$	$\frac{d}{2}$	0<d<1	$\frac{u_{high}}{2}$	$\frac{(1+d)I_{high}}{d(1-d)}$)	1	4	4	Yes

Ref. [13]	Quasi Z-Quartz	Non Pulsating	$\frac{1+d}{1-d}$	$\frac{d}{2-d}$	0<d<1	$\frac{u_{high}}{1+d}$	$\frac{2I_{high}}{1-d}$	2	4	3	Yes
Ref. [14]	H Bridge	Non Pulsating	$\frac{1}{1-2d}$	$2d-1$	Up: 0<d<0.5 Down: 0.5<d<1	u_{high}	$\frac{dI_{high}}{(1-d)(1-2d}$	1	3	5	Yes
Ref. [15]	Cascaded	Non Pulsating	$\frac{2+d}{1-d}$	$\frac{d}{3-d}$	0<d<1	$\frac{u_{high}}{2+d}$	$\frac{(1+2d)I_{high}}{d(1-d)}$	2	6	5	No
Ref. [16]	Cascaded	Pulsating	$\frac{1+d+d^2}{(1-d)^2}$	$\frac{d^2}{1+d-d^2}$	0<d<1	$\frac{u_{high}}{1+d-d^2}$	$\frac{(1-d)^2I_{high}}{1+d-d^2}$	2	4	5	No

1.4 Isolated Bidirectional DC-DC topologies:

In comparison to a non-isolated bidirectional DC-DC converter, a high-frequency transformer can ensure galvanic isolation of the input and output in a bidirectional topology for HESS, which can alter the voltage conversion range by varying the turns ratio. Because of their better voltage conversion ratio and ability to accommodate various voltage levels for HESS, isolated bidirectional DC-DC topologies are advantageous. According to various DC power sources, the isolated bidirectional DC-DC converters can be separated into voltage-fed and current-fed types.

Rectifier and inverter units make up the voltage-fed bidirectional DC–DC converter. The current-fed and voltage-fed converters have a similar structural design. The primary distinction is the requirement for an inductor on the DC current source side of current-fed converters and DC source types to reduce current ripple. Considering that current-fed converters are less commonly employed in automotive applications, the current source can be replaced with a voltage source and an inductor.

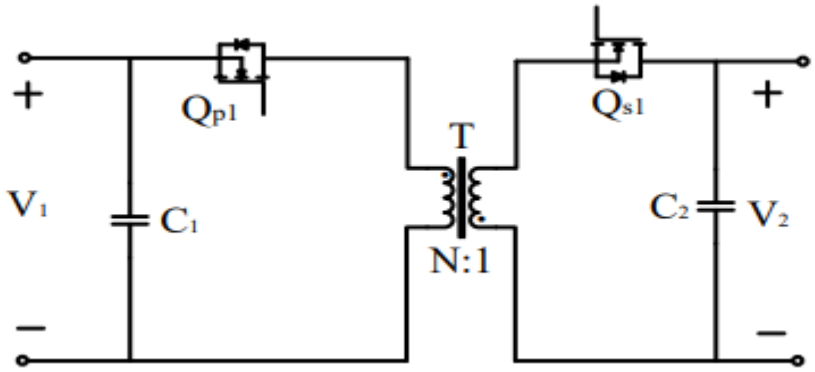
1.4.1 Voltage-fed Bidirectional DC-DC Converter:

- Basic Isolated Bidirectional DC-DC Converter
- Dual Active Bridge DC-DC Converters
- Z Source and Quasi-Z Source Full-bridge Bidirectional DC-DC Converters
- Interleaved Isolated Bidirectional DC-DC Converter

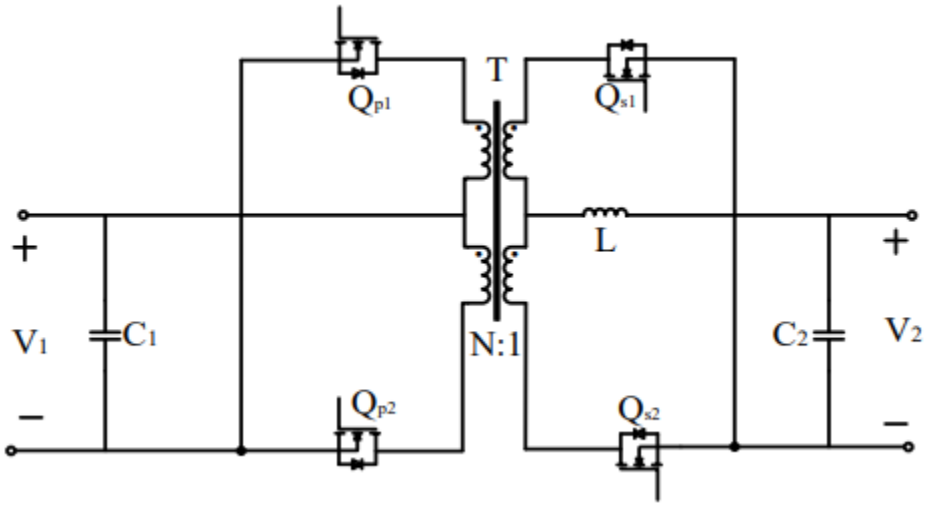
1.4.1.1 Basic Voltage-fed Isolated Bidirectional DC-DC Converter:

Bidirectional flyback and push-pull converters are two common fundamental voltage-fed bidirectional DC-DC converters. Due to their simple designs, small number of components, and quick dynamic response, bidirectional flyback converters are frequently utilized in low-power applications needing galvanic isolation [5]. Because the flyback converter's transformer must accomplish galvanic isolation while also storing energy, the switches must be able to tolerate high voltage and current strains. Both the conversion efficiency and the switching losses are significant. A significant voltage spike will be produced because the high-frequency transformer of push-pull converters has leakage inductance.

Additionally, the converter's reliability is decreased and design complexity is increased by the transformer's Centre tap. With the exception of HESS and Novel Electric Vehicle(NEV), the fundamental voltage-fed isolated converters are acceptable for low-power applications.



(a) Bidirectional flyback converter



(b) Bidirectional push-pull converter

Fig.1.6 Basic bidirectional DC-DC converters [5]

1.4.1.2 DAB Bidirectional DC-DC Topologies:

DAB converters can be divided into resonant and non-resonant variants based on the different arrangements of the primary and secondary sides of the high-frequency transformer. For DAB of

the resonant type, the high-frequency transformer is coupled in series with a soft switching resonant circuit.

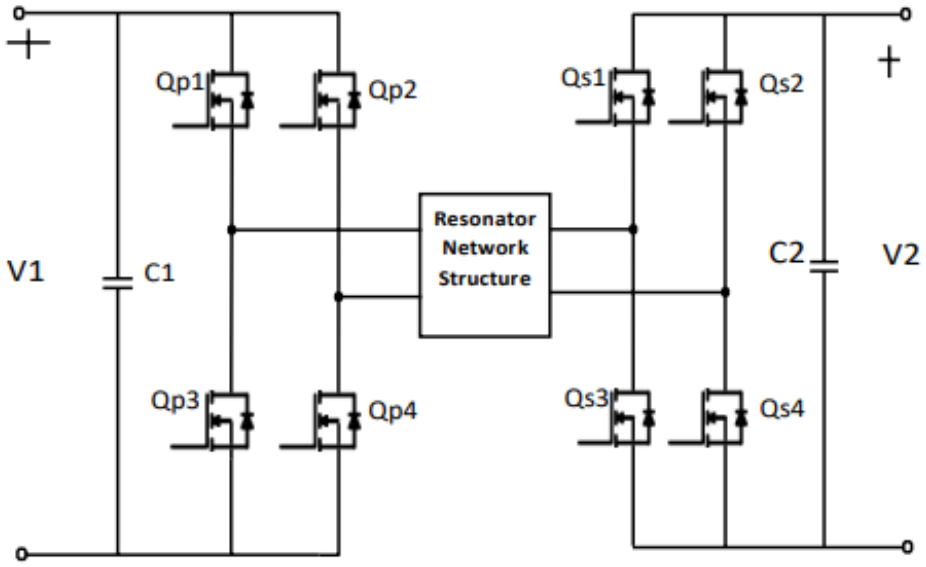


Fig.1.7 Resonant DAB converter [5]

The high-frequency transformer for non-resonant DAB converters only has one inductor connected in series. DAB converters, in general, refers to non-resonant DAB converters. Types of the structure include half bridges and full bridges.The advantages of fewer devices and a smaller volume make half bridge structures popular in battery chargers and UPS systems [5]. The dual active full-bridge converter has twice as many switches as a half-bridge converter.

The non-resonant DAB converter's intermediate stage is simply an inductor, which not only allows for bidirectional energy transmission but also offers the advantages of low voltage stress and flexible control. The resonant DAB DC-DC converter can increase the soft switching capabilities and efficiency by inheriting the benefits of the DAB converter. The resonant structure can also be chosen based on the needs of the various applications. However, as the number of resonant parts increases, so does the complexity of the converter and the difficulty of controller design. The bidirectional full-bridge converters are appropriate for HESS of NEV and other high voltage and power situations.

1.4.1.3 Z Source and Quasi-Z Source Full-bridge Bidirectional DC-DC Converters:

Two capacitors and two inductors make up the Z source and quasi-Z source impedance network. Between the power source and the inverter bridge arms of the conventional full-bridge DC-DC converter, the Z source full-bridge DC-DC converter will add a Z source impedance network. Based on this, thyristors are inserted between the power source and the Z source structure to limit the flow of current in one direction [5].

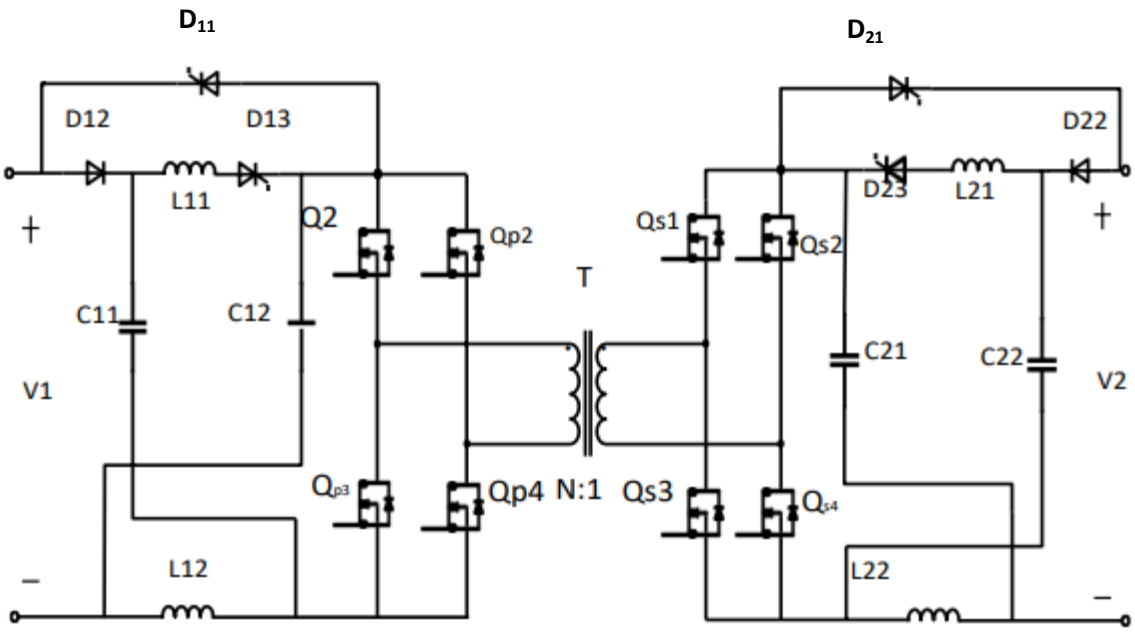


Fig.1.8 Z source bidirectional full-bridge DC-DC converter [5]

Four thyristor D_{11}, D_{13}, D_{21}, and D_{23} are added to the Z source structure in order to adapt it to the needs of bidirectional energy transfer. In order to provide reverse current, the thyristor D_{11} is switched on in the reverse power flow and off in the forward power flow. To separate the Z source network into LC filters, the thyristor D_{13} is turned on in the forward power flow and off in the reverse power flow. Thyristors D_{21} and D_{23} perform comparable tasks to those performed by thyristors D_{11} and D_{13}. The switching frequency is low because the states of D_{11}, D_{13}, D_{21}, and D_{23} only change when the current flow direction changes, and using thyristors can lower the cost and boost reliability.

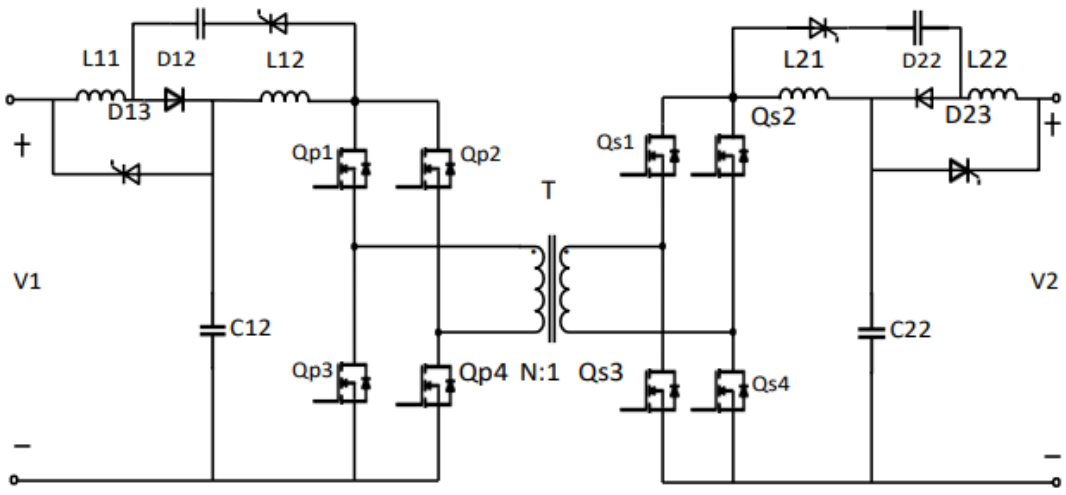


Fig.1.9 Quasi-Z source bidirectional full-bridge DC-DC converter [5]

The Z source network is added to the usual DAB structure, thus eliminating the possibility of shoot-through of the same bridge arm and improving conversion efficiency. Since the startup current will decrease system stability and device service life. The starting current and the problem of current discontinuity in the Z-source full bridge structure can both be improved by the quasi-Z source full bridge construction. Therefore mentioned updated converters, however, increase the number of components and the level of design complexity, which lowers system reliability and makes them unsuitable for HESS of NEV.

1.4.1.4 Interleaved Isolated Bidirectional DC-DC Converter:

The interleaved construction can increase the voltage conversion ratio and power transmission level while sharing the voltage and current strains and reducing current ripple [6]. The resonator structure of interleaved converters is similar to the DAB resonant structure, and they are classified as Y-Y and $\Delta - \Delta$ types of interleaved isolated converters.

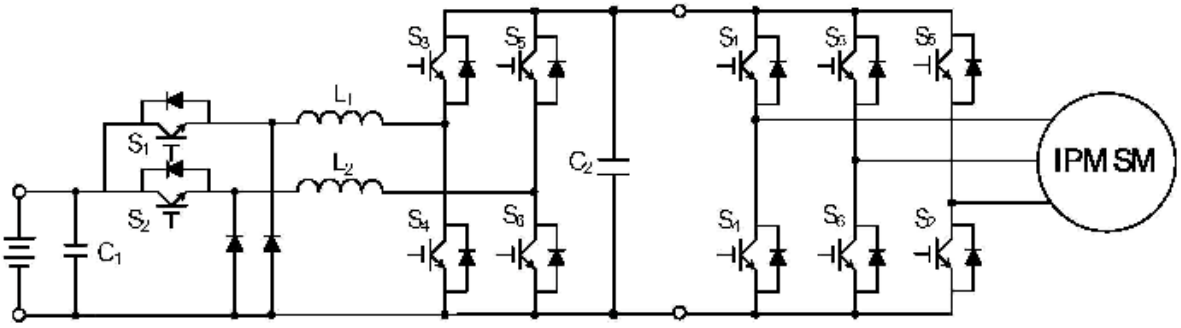


Fig.1.10 Two phase interleaved bidirectional DC-DC converter [6]

Low input and output current ripples are advantages of the two phase dual active full-bridge structure.

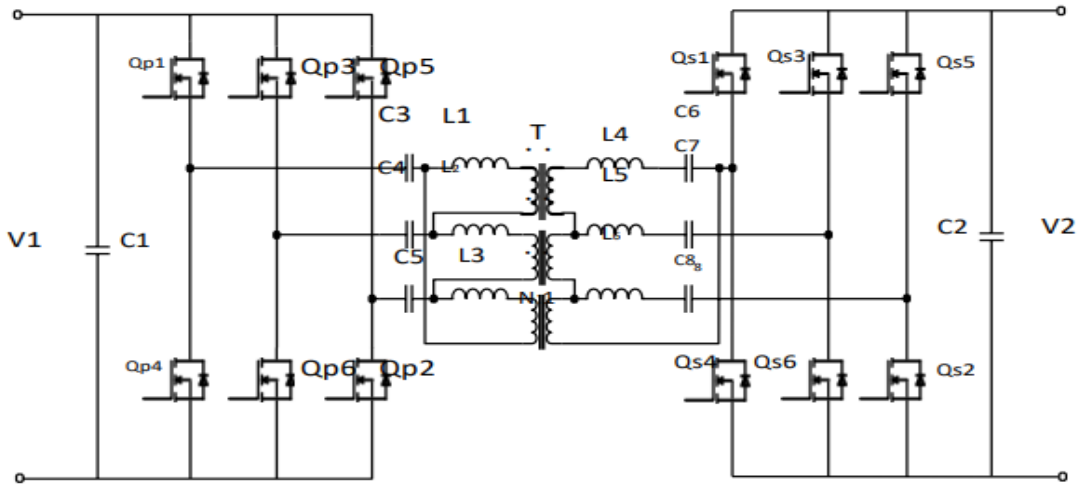


Fig.1.11 Three phase Δ–Δ interleaved LLC resonant bidirectional DC-DC converter [7]

Additionally, they can lessen the turn ratio of the transformer as well as the voltage and current stresses placed on the primary and secondary side devices, respectively.

The need for current balance and the issue of a high number of devices, however, make the design more challenging. Current self-balancing and power source side current ripple might both be reduced by the Y-Y type connection topology.

The three phase interleaved LLC resonant full-bridge structure, which is appropriate for applications needing a significant voltage differential between the input and output voltages, can modify the voltage conversion ratio through phase shift and frequency modulation control schemes. Among them, the Y-Y structure is of particular interest because to its exceptional present self-balancing ability.

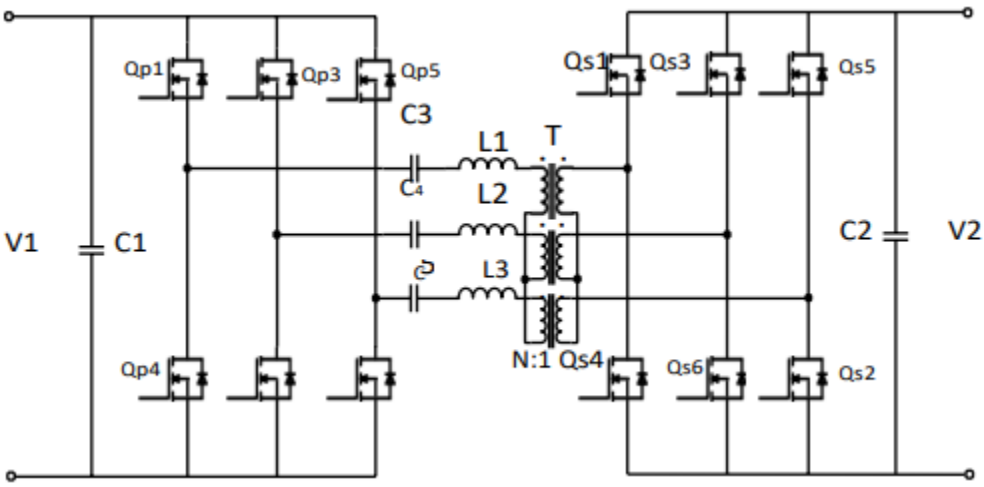


Fig.1.12 Three phase Y-Y interleaved LLC resonant bidirectional DC-DC converter [7]

1.5 Comparison of Common Isolated Bi-directional DC-DC Converter

Table 1.3 Advantages and disadvantages of isolated bidirectional DC-DC converters

Classification	Advantages	Disadvantages
Basic	• Simple structure • Easy to control • Easy to generate new topologies • Low number of devices	• Large switching loss • Low conversion efficiency • Low power application
DAB	• Wide voltage conversion range • Low stress of switches • Flexible control method • High power density	• Complex structure • Difficult to control • Large volume and cost
Z Source/ Quasi-Z Source	• High conversion efficiency • Small startup current	• Complex structure • Large number of devices • Difficulty to design
Interleaved	• Wide voltage conversion range • Low current ripple • High power density	• Large number of switches • Complex structure

Typical isolated bidirectional DC-DC topologies are compared in this section from six perspectives: power source side current ripple, voltage and current stresses, power density, number of devices, and transformer winding design. Table 1.4 provides an overview of the index distribution for seven common isolated bidirectional DC-DC topologies.

Table 1.4 Indexes of typical isolated bidirectional DC-DC topologies

Topologies	Technology Used	Power Source Side Current	Voltage stress of switches	Transformer design	Current stress of switches	Number of devices L	T	C	Common ground
Ref. [17]	Flyback	Pulsating	u_{high}	Difficulty	$\frac{I_{high}}{1-d}$	1	1	2	Yes
Ref. [18]	Resonant DAB	Pulsating	$\frac{u_{high}}{2}$	Medium	I_{high}	3	3	6	No
Ref. [19]	Non-resonant DAB	Non Pulsating	$\frac{u_{high}}{2}$	Easy	I_{high}	2	4	5	No
Ref. [20]	Z Source Full Bridge	Pulsating	u_{high}	Easy	$\frac{2I_{high}}{1-2d}$	1	3	4	No

Ref. [21]	Quasi-Z Source Full Bridge	Non Pulsating	u_{high}	Easy	$\frac{2I_{high}}{1-2d}$	1	4	4	Yes
Ref. [22]	Two-Phase Interleaved	Low Ripple	$\frac{u_{high}}{2}$	Medium	$\frac{I_{high}}{4}$	2	4	3	Yes
Ref. [23]	Three Phase Y-Y Interleaved	Low Ripple	$\frac{u_{high}}{2}$	Difficulty	$\frac{I_{high}}{3}$	1	3	5	Yes

1.6 Limitations and Prospects of Bidirectional DC-DC Converters

The bidirectional DC-DC demand voltage and power will fluctuate in a wide range because the instantaneous power needed by the NEV will alter in real time with changes in driving conditions. As a result, the bidirectional DC-DC converter reduces the ripple in the current flowing from the power source while producing steady voltage under all operating situations. The topological design, correct modelling, and optimal management of the bidirectional converters for HESS are key concerns that require immediate attention[12]-[14].

An essential element that has a significant impact on the development of the NEV industry is the dependability of a bidirectional DC-DC converter for the vehicle powertrain. An important study area for bidirectional converters for HESS would be to fully integrate the studies of system detection, modelling, control strategy, and fault diagnosis techniques to accomplish the safe and dependable operation of bidirectional DC-DC conversion systems[16]-[18].

A bidirectional DC-DC converter is a highly nonlinear system. There would be several kinds of bifurcation, chaos, and other nonlinear phenomena under certain circumstances. These are reflected in the converter's increased harmonic content, increased harmonic voltage and current ripples, decreased conversion efficiency, noise, oscillations, and even system collapse. Important study areas in relation to bidirectional DC-DC converters include the method for doing nonlinear modelling of DC-DC converters, examining converter stability, and applying chaos control. Given the difficulties encountered during research on bidirectional DC-DC converters for NEV, the following works can be evaluated.

Bidirectional DC-DC converters for HESS can operate efficiently and with a high voltage conversion ratio by taking advantage of wideband gaps' high frequency and low loss characteristics. The optimization calculation approach can be utilised to enhance and optimise existing interleaved, quasi-Z source, cascaded, and other topologies for bidirectional DC-DC converters[20]. To do this, it is possible to reduce switching loss, device stress, and energy storage element volume.

The bidirectional DC-DC converter for HESS has the challenge of stable operation under all operating situations and a low power side current ripple[22]. To address this issue, the converter's dynamic response and anti-interference ability can be artificially enhanced based on existing topology optimization, such as by applying an interleaved parallel technology, in conjunction with research on accurate modelling and the adaptive control method.

In order to address the problem of nonlinear modelling and control of the bidirectional DC-DC converter for HESS, the nonlinear behaviour brought on by changes in the bidirectional DC-DC converter parameter can be revealed by qualitative and quantitative methods based on the study of nonlinear dynamics and combined synthetical modelling techniques, such as state variable equation and discrete mapping[23]. In order to apply chaos control to the converter and get the desired periodicity, this is done.

1.7 THESIS OUTLINE

In this thesis, chapter 1 includes a review of bidirectional dc-dc converters (IBDC). The basic structure of these converters along with the terminology used in the literature was described. The advantages and disadvantages of each configuration were briefly stated.

In chapter 2, the three-level converter is reviewed and comprehensively compared with CBC and interleaved bidirectional converter in terms of magnetic component size and efficiency.

Chapter 3 discusses the macro model of ultra-capacitor. Depending on the application, a simplified first order or higher order RC model is proposed. The model can be used to estimate the ultra-capacitor losses and temperature.

Chapter 4 explores the State-of-the-art interface dc-dc converter topologies, and a new three-level dc-dc converter is presented. In addition to providing design principles, the suggested topology is analysed. A control strategy is suggested together with the development of the model of the full conversion system. Controlling the ultra-capacitor current and dc bus midpoint voltage is the aim of the proposed control technique. Depending on the operating mode, the second control goal is to asymptotically regulate the dc bus voltage to the specified reference. The third control objective is to regulate the state of charge (SOC) of ultra-capacitors.

Chapter 5 concludes the contributions of the thesis and points out the scope of future work.

CHAPTER 2

COMPARATIVE STUDY OF BIDIRECTIONAL THREE-LEVEL DC–DC CONVERTER FOR AUTOMOTIVE APPLICATIONS

2.1 Three-Level Interface DC-DC Converter:

In applications requiring a high input voltage and high switching frequency, three-level converters are a popular choice. One-half of the total dc bus voltage is used to stress the switches[29].

This enables us to employ switches with lower voltage ratings that perform better in terms of switching and conduction than switches rated for the full dc bus voltage. Therefore, compared to two-level converters, the converter's overall performance, including cost and efficiency, can be noticeably improved, especially when switching frequency is above 20 kHz or MOSFETs are utilized as switches.

The input filter capacitors work as a capacitive voltage divider to divide the dc bus voltage V_{BUS} into two equal voltages, V_{C1} and V_{C2}. They are connected in series. The switching cell midpoint is connected to the midpoint of the capacitor.

2.1.1. Working Principle:

Switching function S_1 and the complimentary function determine the states of the switches SW_{1A} and SW_{1B}, whereas switching function S_2 and the complementary function determine the states of the switches SW_{2A} and SW_{2B}. The S_1 and S_2 switching operations are produced by the PWM_1 and PWM_2 pulse width modulators. The S_1 and S_2 switching operations are

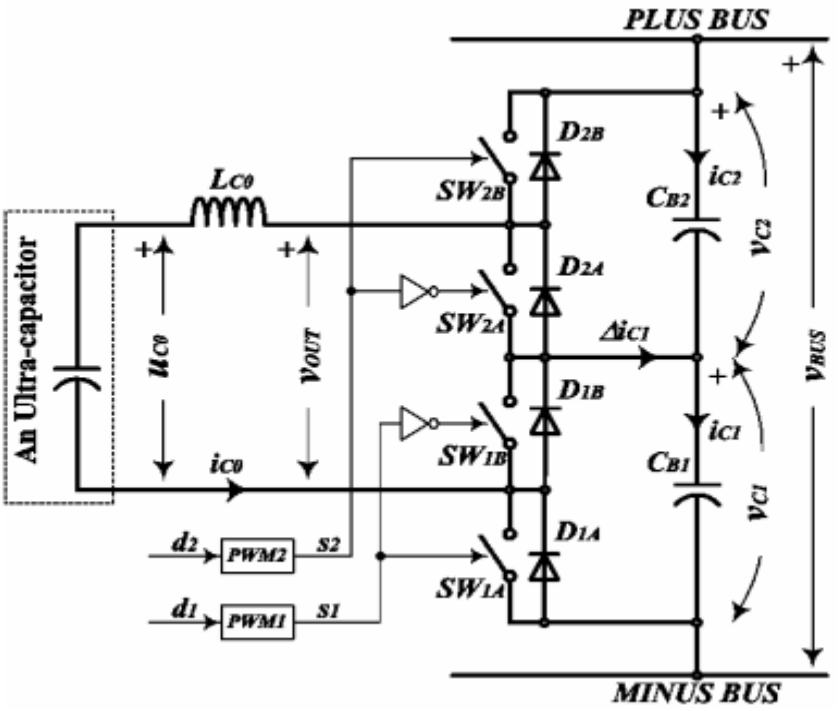


Fig. 2.1. Circuit diagram for a three-level bidirectional dc-dc converter interface [24].

$$S_1(t) = \begin{cases} 1, KT_{SW} < t \le T_{SW}\left(K+1-\frac{d_1}{2}\right) \quad AND\ T_{SW}\left(K+1-\frac{d_1}{2}\right) < t \le (K+1)T_{SW} \\ 0, T_{SW}\left(K+\frac{d_1}{2}\right) < t \le T_{SW}\left(K+1-\frac{d_1}{2}\right) \end{cases} \quad (2.1)$$

$$S_2(t) = \begin{cases} 1, KT_{SW} < t-\frac{T_{SW}}{2} \le T_{SW}\left(K+\frac{d_2}{2}\right) AND\ T_{SW}\left(K+1-\frac{d_2}{2}\right) < t-\frac{T_{SW}}{2} \le (K+1)T_{SW} \\ 0, T_{SW}\left(K+\frac{d_2}{2}\right) < t-\frac{T_{SW}}{2} \le T_{SW}\left(K+1-\frac{d_1}{2}\right) \end{cases} \quad (2.2)$$

where T_{SW} is the switching period and k is an integer between 0 and 1. The signals of modulation Duty cycles d_1 and d_2 are produced by the control circuit. The control circuit balances the voltages V_{C1} and V_{C2} and regulates the ultra-capacitor current i_{C0}. They are the modulation carriers. Triangle signals V_{T1} and V_{T2} running at the same frequency f_{SW} but with a shift of radians. When $d_1 = d_2 < 1/2$, the converter waveforms are shown in Fig. 2.3 (a), while Fig (b) when $d_1 = d_2 > 1/2$, displays the waveforms. The switches' states determine four different there are four topological stages that can be identified: A, B, C, and D. Diagrams of equivalent circuits Fig. 2.2 provides an illustration of these steps (c). Idealized models of the input filter capacitors are used. V_{C1} and V_{C2} are voltage sources.

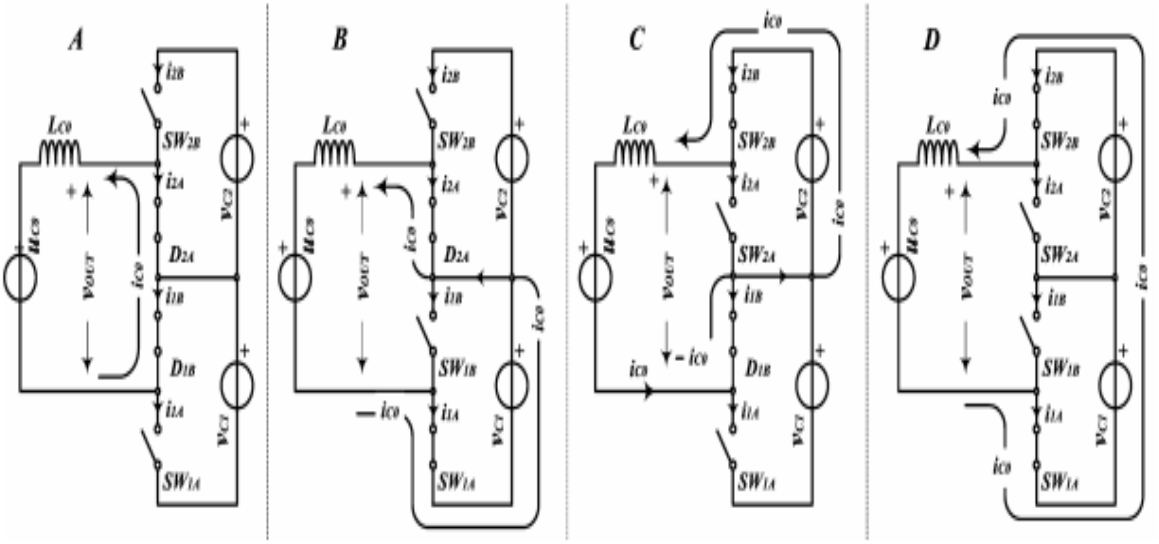


Fig.2.2. equivalent circuits for steps A, B, C, and D [24].

Stage A): The converter can only be at this stage if the duty cycle is less than 1/2. SW_{1B} and SW_{2A} switches are closed, whereas SW_{1B} and SW_{2B} switches are open. Because the current i_{C0} is believed to be positive in the circuit design, the currents i_{1B} and i_{2A} is negative. The freewheeling diodes D_{1B} and D_{2A} are conducting. Input voltage is Since $V_{OUT} = 0$, the current i_{C0} declines.

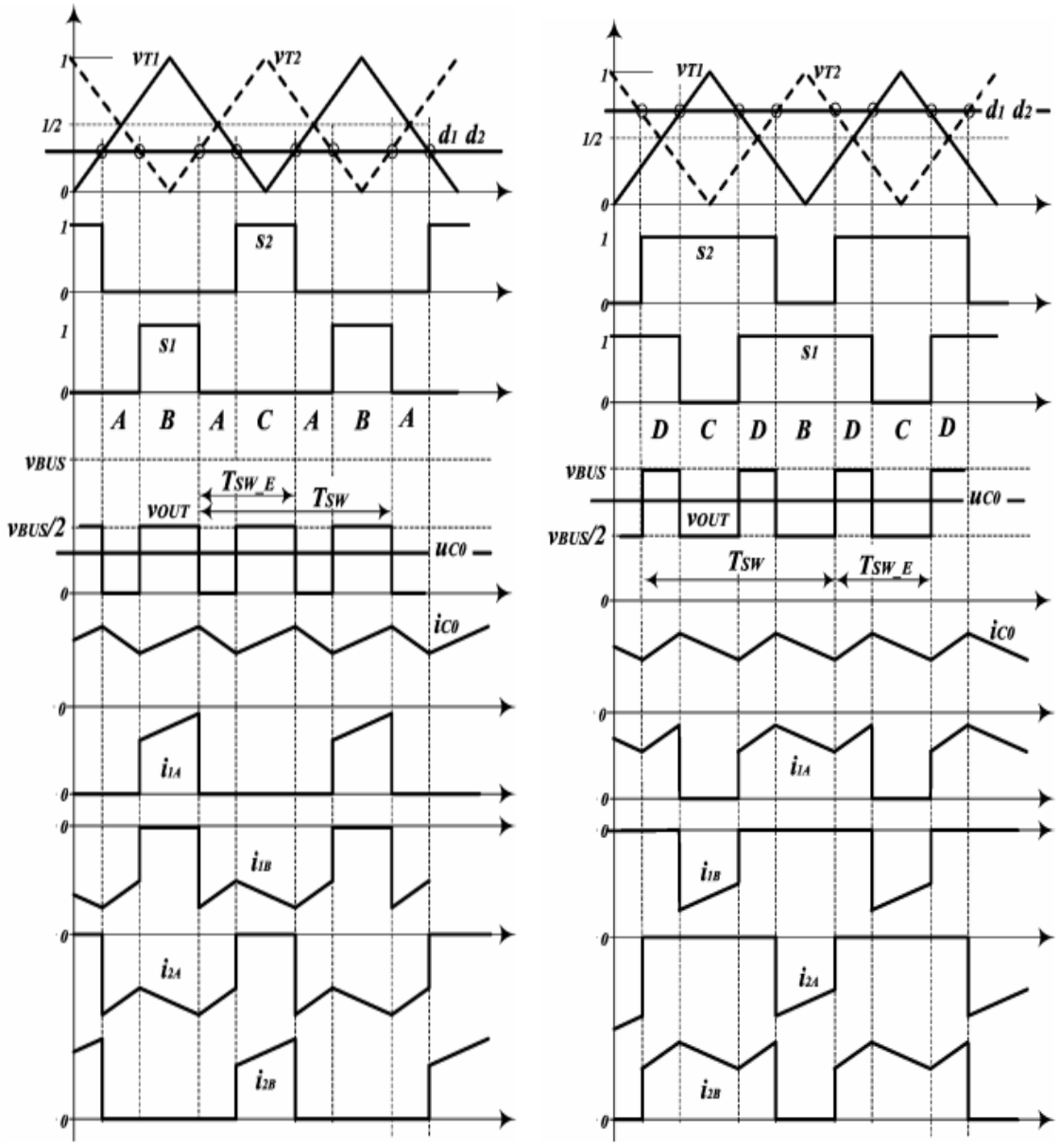
$$\frac{di_{c0}}{dt} = \left(-\frac{u_{c0}}{L_{c0}}\right) < 0 \qquad (2.3)$$

Stage B): The switches SW_{1A} and SW_{2A} are closed, whereas the switches SW_{1B} and SW_{2B} are open. The freewheeling diode D_{2A} is conducting, and the currents i_{1A} and i_{2A} are both positive. The current i_{1A} discharges the filter capacitor C_{B1}. The voltage at the output is $V_{OUT} = V_{C1}$. There is a change in the current i_{C0} depending on the voltage of the ultra-capacitors (duty cycle consequently).

$$\frac{di_{c0}}{dt} = \frac{1}{L_{C0}}(V_{C1} - u_{C0}) \begin{cases} > 0, u_{C0} < V_{C1} \\ < 0, u_{C0} > V_{C1} \end{cases} \qquad (2.4)$$

In stage C), the switches SW_{1A} and SW_{1B} are open while SW_{1B} and SW_{2B} are both closed. The freewheeling diode D_{1B} is conducting, and the currents i_{2B} and i_{1B} are both positive. The current i_{2B} discharges the filter capacitor C_{B2}. The voltage at the output is $V_{OUT} = V_{C2}$. The duty cycle determines whether the current i_{C0} grows or drops.

$$\frac{di_{c0}}{dt} = \frac{1}{L_{C0}}(V_{C2} - u_{C0}) \begin{cases} > 0, u_{C0} < V_{C2} \\ < 0, u_{C0} > V_{C2} \end{cases} \qquad (2.5)$$



(a) (b)

Figure 2.3 (a) and (b) shows the several topological stages of the three-level dc-dc converter. Ideal waveforms for d < 1/2 and d > 1/2, respectively [24]

Stage D): Only if the duty cycles are more than 1/2 can the converter be at this stage. When compared to the switches SW_{1B} and SW_{2A}, SW_{1A} and SW_{2B} are closed. Positive currents flow through the switches, i_{1A} and i_{2B}. Because the output voltage is $V_{OUT} = V_{BUS}$, the current i_{CO} rises.

$$\frac{di_{c0}}{dt} = \frac{1}{L_{C0}}(V_{BUS} - u_{C0}) > 0 \qquad (2.6)$$

The expression for instantaneous output voltage V_{OUT} is :

$$V_{OUT}(t) = V_{BUS}S_1(t) + V_{C1}\big(S_1(t) - S_2(t)\big) \quad (2.7)$$

where the switching functions are $S_1(t)$ and $S_2(t)$ (2.1) and (2.2).

Assuming that $d_1 = d_2 = d$ and $V_{C1}=V_{C2}=V_{BUS}/2$ (as in a well-designed and controlled converter), it follows from (4.9)-(4.14)

$$V_{OUT}\left(t + \frac{T_{SW}}{2}\right) = V_{OUT}(t) \quad (2.8)$$

$$u_{C0} = \frac{1}{T_{SW}}\int_0^{T_{SW}} V_{OUT}(t)\,dt = V_{BUS}d \quad (2.9)$$

The output voltage is a periodic function with a period of $T_{SW}/2$, as shown by (2.8) and (2.9). As a result, the output current iC0 and its effective fundamental frequency, $f_{SW\text{-}E}=2f_{SW}$, are twice that of the switching frequency.

2.2 Comparison of Three-Level Converter with the state-of-the-art Converters:

In comparison to the most advanced two-level bidirectional dc-dc converter and interleaved bidirectional buck/boost converters, three level dc-dc converter offers a number of benefits. The voltage put across the switch plays a significant role in switching losses. In particular, when the switches are exposed to half the output voltage compared to CBC, the switching loss of the parasitic capacitance can be greatly decreased even without soft switching.

As low-voltage switches are employed, parasitic capacitance losses are anticipated to be even lower. Due to the fact that the reverse voltage is only half as high as the output voltage and low-voltage diodes often recover more quickly, the diode reverse recovery losses are smaller for passive components. This section compares the topologies of bidirectional buck/boost dc-dc converters shown in terms of the size and efficiency of magnetic components over the entire drive cycle range, taking into account the dynamic variations of the battery and UC voltages as well as the power processed by the converter.

2.2.1. Drive Cycle Characteristic:

The load power and dynamic voltage changes of the energy sources have a significant impact on the efficiency of the bidirectional converter.

In this theis, we discuss the three-level wavelet decomposition battery and UC reference power results [27]. Fig. 2.4 displays the converter power and battery voltage fluctuations for four successive UDDS cycles. In this particular instance, it is assumed that the battery has an initial state of charge (SOC) of 80% and that the UC has a SOC of 91.6%. During the driving cycle, the converter power fluctuates between 10.78 and 45.32 kW, the battery voltage varies between 381 and 357 V, the UC voltage varies between 575 and 384 V, and the battery voltage varies between 381 and 357 V.

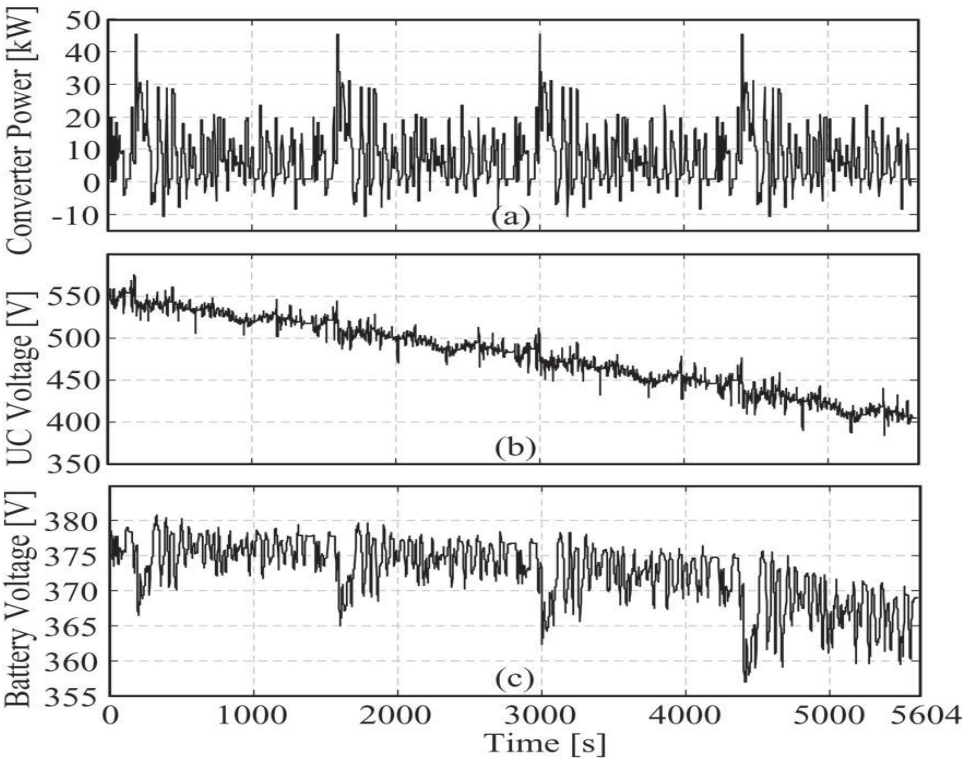


Fig.2.4. Dynamic variations of state variables [27](a) Converter power.(b) UC voltage. (c) Battery voltage.

2.2.2. Magnetic Component Size:

Peak flux density and peak current flowing through the core are both correlated with the size of the magnetic component. The battery's current ripple can be represented in CBC as

$$\Delta i_{batt-boost}(d) = \frac{v_0}{Lf_s} d(1-d) \quad (2.10)$$

The battery current ripple for TLC is

$$\Delta i_{batt-TL}(d) = \frac{v_0}{2Lf_s} d_{eff}(1-d_{eff}) \quad (2.11)$$

Two inductor currents are added to create the BIC converter's input current. The input current ripple increases when the switches' duty cycles are lower than 50% the current ripple as

$$\Delta i_{batt-Interleaved}(d) = \frac{2v_{in}-v_0}{Lf_s}\left(1-\frac{v_{in}}{v_0}\right) \quad (2.12)$$

The core geometry approach is used to determine the approximate size of the magnetic component. Many factors, including peak current (I_{peak}), rms current (I_{rms}), maximum flux density (B_{max}), regulation (α), maximum output power (P_{omax}), necessary inductance (L), and window utilisation factor (Ku), should be evaluated in order to estimate the core size.

Table 2.1: Converter Currents During Four UDDs (F_S = 20 kHz) [26]

	CBC(200µH)	TLC(100µH)	BIC(200µH)
Max bat. Current[A]	138.64	130	123.2
Ripple current[A]	30.86	4.28	15.43
Max. Inductor cur[A]	138.64	130	77.03
Ind. Ripple cur[A]	30.86	4.28	30.86
Max bat. Ripple cur[A]	32.94	11.5	15.8
Max ind. Ripple cur[A]	32.94	11.5	31.6
Max ind. RMS cur[A]	126.89	126.86	63.49

The necessary inductance and peak inductor current must be calculated in order to estimate the magnetic core size. In this regard, the drive cycle has been assessed using an intermediate buck/boost converter with a switching frequency of 20 kHz, where the effective frequency of the input current ripple is 40 kHz in BIC and TLC. The maximum discharge rate limits the battery current ripple to 20% of the discharging current, which translates to a 40% inductor current ripple for BIC. The inductances for CBC, BIC, and TLC are computed as 400µH, 200 µH(×2), and 100 µH, respectively, based on the expected ripple current, switching frequency, and operational maximum voltage across the inductor with corresponding duty cycle.

2.2.3. Semiconductor Selection Guidelines:

The voltage and current stress on the switches should be examined before choosing any power switches. The switches in CBC and BIC are exposed to the output voltage, but the switches in TLC are exposed to half the output voltage.

TABLE 2.2: Analyzed Converter Specifications [26]

	CBC	TLC	BIC
Input voltage[V]	357-381	357-381	357-381
Output voltage[V]	384-575	384-575	384-575
Peak prop. Power[KW]	45.32	45.32	45.32
Power switch	1XFB30 N120P	1XFX80 N60P3	1XFB30 N120P
Switch rating	1200V/30A	600V/80A	1200V/30A
No. of switches	12	8	12
Switch freq.[KHZ]	20	20	20
Input ripple freq.[KHZ]	20	40	40
Inductance[µH]	200	100	200
No. of cores	2	1	6
Cores weight[kg]	2.6	1.3	1.6

2.3 Loss Mechanism and Efficiency Analysis:

To determine the energy loss and efficiency of the converters during the full driving cycle, efficiency models reflecting various losses, such as conduction, switching, inductor core, and winding losses, are given and evaluated.

2.3.1. Switching Losses:

There are four main loss components that make up the switching losses:

1) MOSFET power losses from the overlap of current and voltage at the moment of switching;

2) gate charge losses;

3) parasitic capacitance losses; and

4) reverse recovery losses of the body diode of the MOSFET.

The switching losses contribute significantly to power dissipation at frequencies higher than 20 kHz. The area under the waveforms of the drain-source voltage V_{DS} and drain current I_D provides information about the switching losses of the MOSFET.

The gate charge loss, or Q, is a type of switching loss because it results from the gate capacitance being charged by the gate voltage V_G and then being discharged to the ground during each switching cycle. Additionally, power is lost due to the charge that is held in the parasitic output capacitor COSS during the MOSFET's turn-off period.

Reverse recovery losses of the MOSFET's body diode, which are correlated with the reverse recovery period t_{rr}, are an additional source of switching losses. The excess charge Q_{rr} held in the drift zone is released at the diode's turn-off transition before the junction starts to become reverse biased. The unwanted reverse recovery voltage, or V_{rr}, is caused by this excess $Q_{rr.}$

The switching losses in CBC, BIC, and TLC are expressed by the following expression:

$$P_{sw} = f_s \times N_{PS} \times N_{PC} \times \left(0.5 \times V_{DS}(t) I_D(t)\left(t_r + t_f\right) + 0.5 \times {V_{DS}}^2(t) C_{LOSS} + Q_t V_G + V_{rr}(t) Q_{rr}\right) \quad (2.13)$$

where f_s is the switching frequency and N_{PS} and N_{PC} are the number of paralleled switches and paralleled converters, which are 6 for CBC, 3 for BIC, and 2 for TLC, respectively. The MOSFET rise-time and fall-time transitions are also indicated by the t_r and t_f.

2.3.2. Conduction Losses:

Conduction loss is prevalent at low switching frequencies, and it is affected by the ON-state resistance R_{DS}(on) and drain RMS current I_S RMS of MOSFETs. The following equation can be used to estimate the conduction loss for CBC and BIC:

$$P_{CD(CBC-BIC)} = N_{PC} \times \left(R_{DS(ON)} I^2{}_{SRMS}(t)/N_{PS} V_F I_{Davg}(t)\right) \quad (2.14)$$

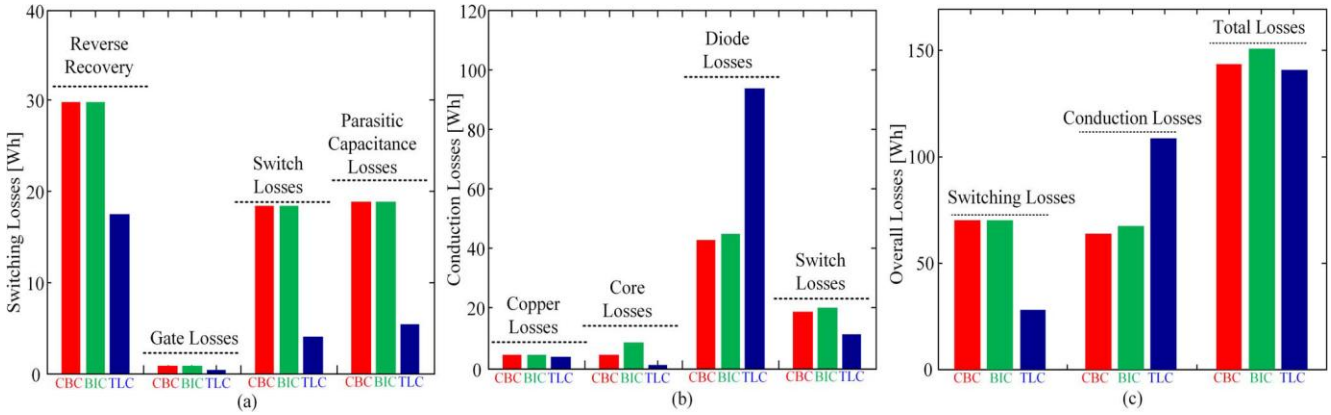


Fig.2.5 Energy losses at the switching frequency of 20 kHz[27] (a) Switching losses. (b) Conduction and core losses. (c) Overall loss

where V_F and I_D avg represent the forward bias voltage drop and the average diode current, respectively.

2.3.3. Inductor Losses :

The inductor's copper loss is estimated using winding ohmic resistance, which can be calculated as

$$P_{cu} = MLT \frac{\rho_{cu}}{A_W} N I^2{}_{LRMS} \quad (2.15)$$

Where P_{Cu} is the copper resistivity constant.

In addition to copper losses, core losses should be considered, which are mostly caused by hysteresis losses.

2.3.4. Efficiency Analysis:

The reverse recovery losses are larger in CBC and BIC converters, owing to the increased drain-source voltage across the diodes during the turn-off instants. In TLC, however, the voltage across the diodes is half that of the output voltage, resulting in lesser power dissipation. The losses connected with the MOSFETs with parasitic capacitance are also considerably reduced. At the specified switching frequency, gate losses are negligible.

When considering the entire drive cycle, the converters' overall efficiencies can be calculated by

$$\eta = \frac{P_O}{P_O + P_{SW} + P_{CD} + P_{CU} + P_C} \quad (2.16)$$

For CBC, BIC, and TLC, respectively, the efficiencies are 98.7%, 98.5%, and 98.8%, according to (25). The efficiencies decrease to 96.4%, 96.3%, and 98%, respectively, with switching frequencies of 100 kHz.

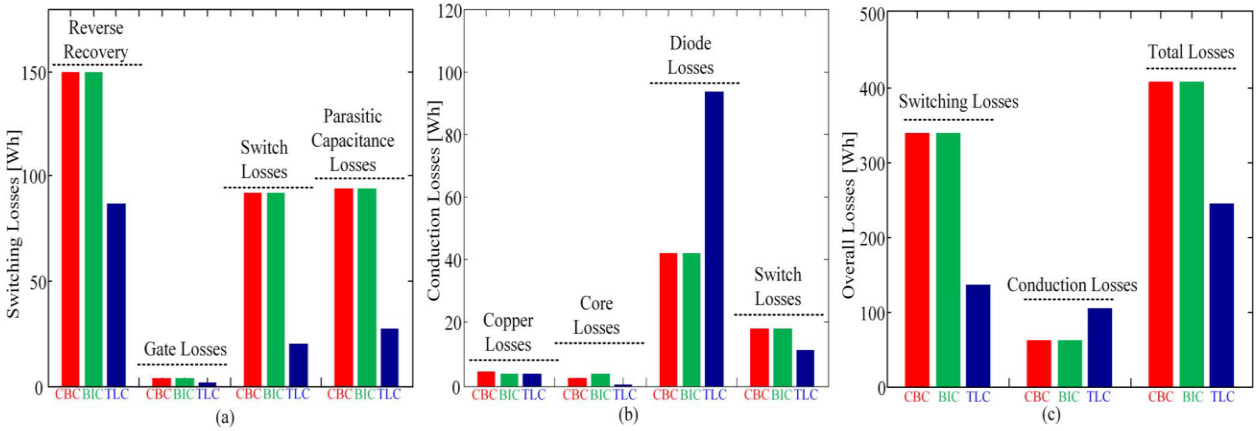


Fig. 2.6. Energy losses at the switching frequency of 100 kHz [27] (a) Switching losses. (b) Conduction and core losses. (c) Overall loss

As a result of the investigation, TLC is found to be the most efficient converter when compared to CBC and BIC, both in terms of magnetic component size and efficiency under certain driving cycle parameters. With an increase in switching frequency, the efficiency gap becomes more apparent.

2.3.5. Control Complexity:

Compared to BIC and TLC converters, which only require one carrier signal to produce two PWM pulses, CBC has a lower switch count, making management of the device relatively easier. The two carrier signals needed for CBC and TLC, however, must be 180 degrees phase-shifted from one another. Thus, TLC control and BIC control are equivalent from the perspective of PWM generation. However, because of the floating ground, three of the switches require isolated gate drivers. Both the cost and the circuitry increase as a result.

2.4 Conclusion:

In battery/UC hybrid EVs, choosing the bidirectional dc/dc converter architecture, which manages the battery power, is crucial because it is one of the key elements affecting the size and efficiency of the system. This converter's efficiency declines when switching losses rise, especially at higher switching frequencies.

The power electronics interface between the battery and the UC has been suggested in this paper to be a three-level nonisolated bidirectional dc/dc converter (TLC), as opposed to a conventional two-quadrant buck/boost converter (CBC), to improve conversion efficiency and minimize the size of the magnetic components.

In this regard, the three-level converter was examined and thoroughly compared with CBC and interleaved bidirectional converter in terms of magnetic component size and efficiency taking into account a UDDS drive cycle where the battery and UC power are separated using three-level wavelet decomposition. The outcomes show that the TLC converter, especially at high switching frequencies, has the smallest size magnetic component while yet offering a significant boost in efficiency.

CHAPTER 3

AN ULTRA-CAPACITOR AS ENERGY STORAGE DEVICE FOR POWER CONVERSION APPLICATIONS

3.1. The Ultra-capacitor:

A passive dynamic two-terminal electric device is an electric capacitor. Dynamic here refers to a device's terminal voltage to current ratio that isn't continuous and linear. A differential equation, which is in the general case a, connects the voltage and current nonlinear equations. An electric capacitor has the ability to store electric energy as electric charge, charge is the electric field that exists between the capacitor plates [28]. There are three different kinds of capacitors: electrostatic, electrolytic, and electrochemical. In this dissertation, only electrochemical capacitors, also known as ultra-capacitors, are taken into account.

The fundamental distinction between ultra-capacitors and other types of capacitors is that they have specific capacitances [F/dm3] and energy densities [kJ/dm3] that are many orders of magnitude greater than those of electrolytic capacitors. The power density is greater than that of ordinary batteries yet the energy density is lower when compared to electrochemical batteries. Additionally, the cycling capacity is noticeably better than that of batteries.

3.1.1. Short History of the Ultra-capacitors:

Helmholtz discovered and described the double-layer capacitor effect in 1879 [28]–[29]. A first ultra-capacitor was patented by Standard Oil Company in 1966, nearly a century later. Approximately ten years after NEC created and marketed this device in 1978 [28]–[29]. The Pinnacle Research Institute created the first high power ultra-capacitor for military purposes in 1982 [28]- [29]. The Maxwell Laboratory began working on DOE ultra-capacitors for hybrid electric vehicles ten years later, in 1992.

These days, ultra-capacitors are made up of two electrodes separated by a separator, a porous membrane. A solvent electrolyte is used to impregnate the separator and the electrodes. The electrodes are constructed from porous materials like carbon nanotubes or activated carbon. The decomposition voltage of the electrolyte determines the ultra-capacitor cell's rated voltage. Depending on the electrolyte technology, the typical cell voltage ranges from 1 to 2.8V [28]–[29]. A number of cells must be series-connected into one capacitor module in order to get a higher operating voltage, which is specified by the application.

Due to their advantages over ordinary capacitors and electro-chemical batteries, including their high energy and power density, high efficiency, high cycle capability, and long life, ultra-capacitors have found a very wide range of applications in power conversion.

3.1.2. Overview of Different Technologies:

The classification of the many electrochemical capacitor types is shown in Fig. 3.1. Electric double layer capacitors (EDLC) and pseudo-capacitors make up the entire family of ultra-capacitors. Pseudo-capacitors and the EDLC are a combination of a hybrid capacitor group. Three subgroups make up the EDLC group: activated carbon, Carbon aerogels and carbon nanotubes. In this chapter application of Electric double layer capacitors (EDLC) is discussed.

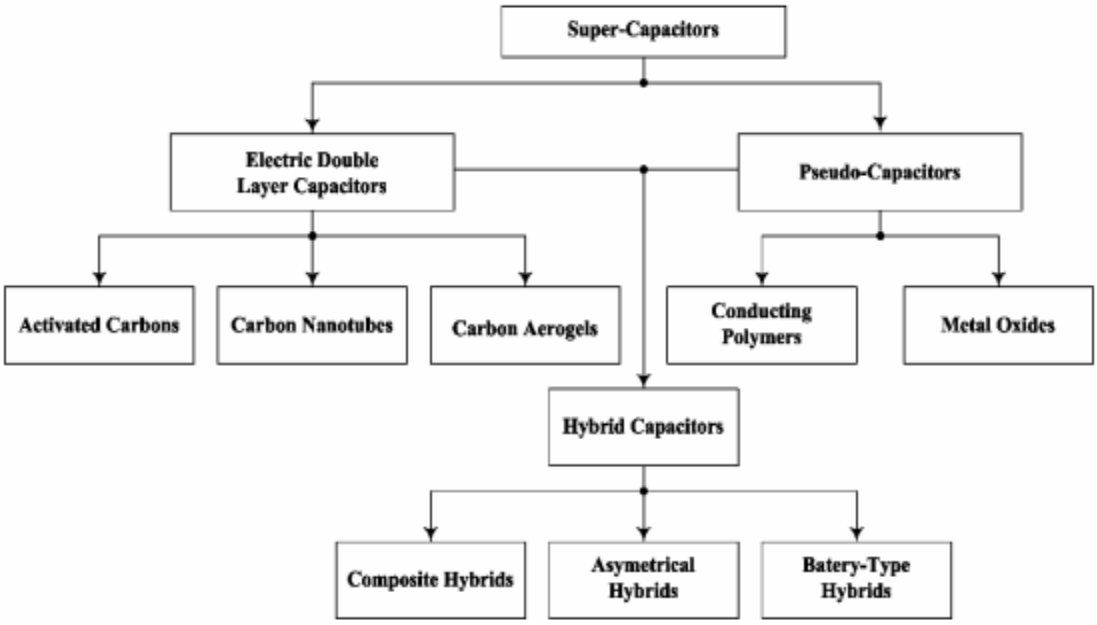


Fig. 3.1 Taxonomy of the ultra-capacitors [28]

3.1.3. Electric Double Layer Capacitors –EDLC:

3.1.3.1 The Ultra-capacitor Structure:

Maximizing the contact surface area is important to increase the capacitance of an ultra-capacitor. One needs to employ a particular material for the electrode in order to accomplish this without increasing the volume of the capacitor. This substance must be porous, and as a result, have an extremely high specific surface. Activated carbon or carbon nanotubes are the materials that are employed the most commonly. The specific surface in both situations might reach 1000 m^2/g to 3000 m^2/g.

Fig. 3.2 shows the super-capacitor cell's simplified construction. The components of the basic capacitor cell are a separator between the porous electrodes, positive and negative current collectors, positive and negative porous electrodes composed of activated carbon that are attached to the current collectors. The separator is made of an insulating substance that prevents direct contact between the porous electrodes and is transparent to ions.

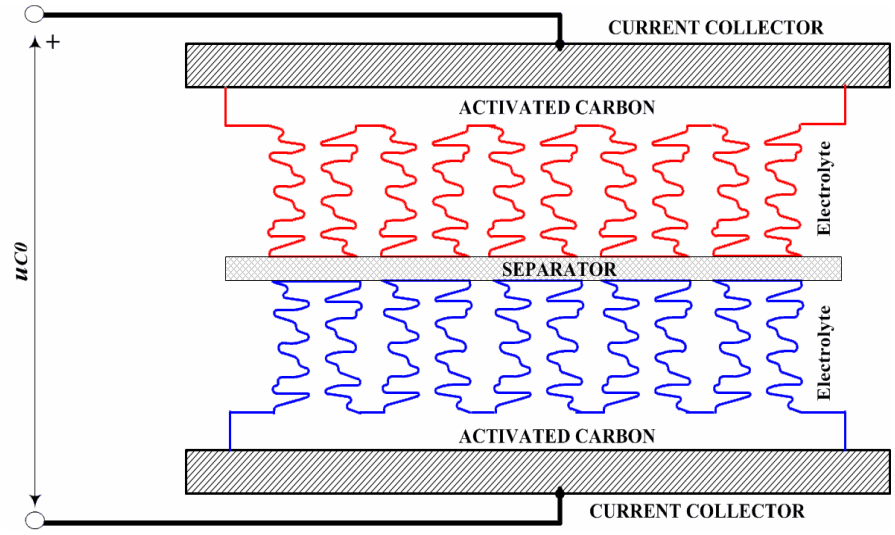


Fig. 3.2 Construction of an electrochemical double layer capacitor with porous electrodes (activated carbon) [30]

3.2. The Ultra-capacitors Macro (Electric Circuit) Model:

The ultra-capacitor macro model is analyzed and explained in this section. The ultra-capacitor macro model is used for conversion system control analysis and design, as well as evaluating ultra-capacitor losses and temperature in various operating modes.

3.2.1 Full Theoretical Model:

In the conventional model, an ideal linear capacitor and an equivalent series resistance are used (ESR). Due to two phenomena, (1) the capacitance is voltage dependent, and (2) the time/space redistribution of the charge caused by the porosity of the activated carbon electrodes, this straightforward model cannot be used in a super-capacitor model. The porous electrode structure exhibits nonlinear transmission line behavior [30]-[31].

Serial connection of two RC leader networks of N_{th} order, the separator resistance R_{SP}, and the current collector resistances R_{CP} and R_{CN}, represents an approximation of an ultra-capacitor with porous electrodes. Here is a schematic representation of the rough model as seen in Fig. 3.3.

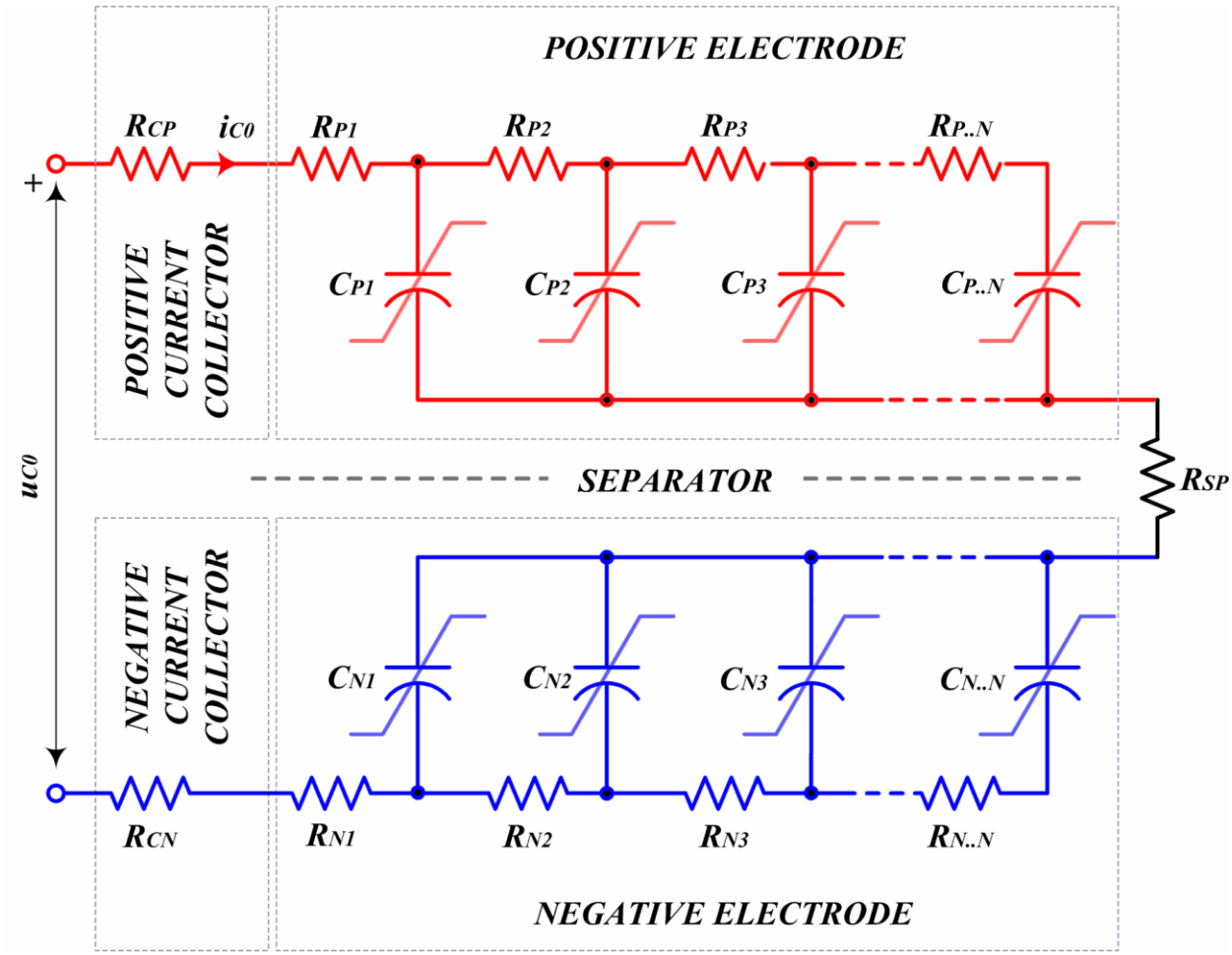


Fig. 3.3 An approximation of the electrochemical double layer capacitor that takes the electrodes' porosity into consideration [31]

The positive and negative porous electrode resistances are represented by the resistors R_{P1}.....$R_{P...N}$ and R_{N1}.....$R_{N...N}$, respectively. The nonlinearity and dependence of these resistances on the capacitor voltage must be taken into consideration for more precise modelling of the ultra-capacitor. Nonlinear capacitances the positive and negative capacitances of porous electrodes are denoted by C_{P1}.....$C_{P...N}$ and C_{N1}.....$C_{N...N}$, respectively.

The first order functions of the voltage across each cell can be used to estimate the voltage-dependent capacitances C_{P1}.....$C_{P...N}$ and C_{N1}.....$C_{N...N}$, respectively.

$$\begin{bmatrix} C_{P1} \\ C_{P2} \\ \vdots \\ C_{P..N} \end{bmatrix} = \begin{bmatrix} C_{0P1} \\ C_{0P2} \\ \vdots \\ C_{0P..N} \end{bmatrix} + \begin{bmatrix} K_{CP1} & 0 & 0 & 0 \\ 0 & K_{CP2} & 0 & 0 \\ 0 & 0 & \dots & 0 \\ 0 & 0 & 0 & K_{CP..N} \end{bmatrix} \begin{vmatrix} u_{CP1} \\ u_{CP2} \\ \vdots \\ u_{CP..N} \end{vmatrix}, \tag{3.1}$$

$$\begin{bmatrix} C_{N1} \\ C_{N2} \\ \vdots \\ C_{N..N} \end{bmatrix} = \begin{bmatrix} C_{0N1} \\ C_{0N2} \\ \vdots \\ C_{0N..N} \end{bmatrix} + \begin{bmatrix} K_{CN1} & 0 & 0 & 0 \\ 0 & K_{CN2} & 0 & 0 \\ 0 & 0 & ... & 0 \\ 0 & 0 & 0 & K_{CN..N} \end{bmatrix} \begin{vmatrix} u_{CN1} \\ u_{CN2} \\ \vdots \\ u_{CN..N} \end{vmatrix}, \quad (3.2)$$

The voltage dependence of the capacitance caused by the diffused layer is modelled as coefficients $K_{CN1}..K_{CP...N}$. The voltage across each elementary capacitor cell is measured as coefficients $u_{CN1}...u_{CP...N}$.

Considering that the positive and negative electrodes are symmetric, the circuit in Fig.3.3 can be reduced to a simple Nt_h order RC ladder network, depicted in Fig.3.4.

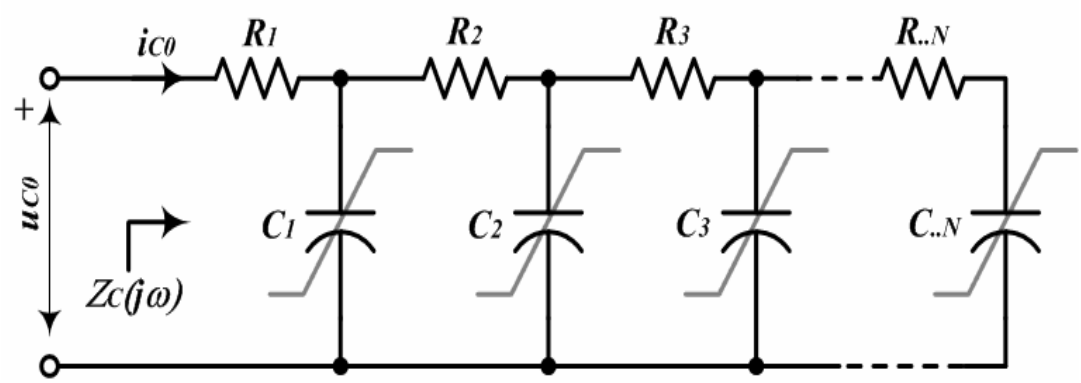


Fig. 3.4 Nth order equivalent model of an electrochemical double layer capacitor [32]

The comparable circuit in Fig. 3.4 has resistances that are

$$\begin{bmatrix} R_1 \\ R_2 \\ \vdots \\ R_N \end{bmatrix} = \begin{bmatrix} R_{CP} + R_{SP} + R_{CN} \\ 0 \\ \vdots \\ 0 \end{bmatrix} + \begin{bmatrix} R_{P1} \\ R_{P2} \\ \vdots \\ R_{P...N} \end{bmatrix} + \begin{bmatrix} R_{N1} \\ R_{N2} \\ \vdots \\ R_{N...N} \end{bmatrix} \quad (3.3)$$

To determine the capacitances of the equivalent model, we will use electrical elastance as the inverse variable of capacitance,

$$\begin{bmatrix} \frac{1}{C_1} \\ \frac{1}{C_2} \\ \vdots \\ \frac{1}{C_{..N}} \end{bmatrix} = \begin{bmatrix} \frac{1}{C_{P1}} \\ \frac{1}{C_{P2}} \\ \vdots \\ \frac{1}{C_{P...N}} \end{bmatrix} + \begin{bmatrix} \frac{1}{C_{N1}} \\ \frac{1}{C_{N2}} \\ \vdots \\ \frac{1}{C_{N...N}} \end{bmatrix} \quad (3.4)$$

3.2.2. Simplified Model:

An ultra-capacitor is modelled using a first order nonlinear equation for the sake of simplicity in the analysis. The total capacitance as a function of the capacitor voltage is considered in the model along with the linear (voltage independent) internal resistance R_{C0}. The transmission line's effects are disregarded. Modeled as a constant and frequency-independent resistance is the internal equivalent resistance, or R_{C0}. A simplified version of the ultra-capacitor model utilized in the analysis is shown in Fig. 3.5. A linear capacitor C_0 and a parallel-connected voltage-dependent capacitor $C(u_C)$ make up the equivalent capacitor.

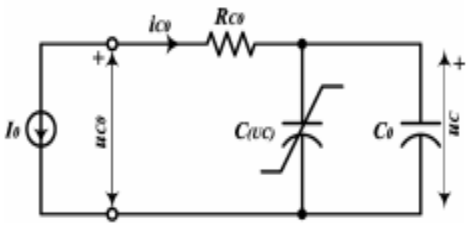


Fig. 3.5 Ultra-capacitor simple RC model [32]

The voltage-controlled capacitance used to determine an ultra-capacitor's total capacitance is$C\,(\mathrm{uc}) = C_0 + K_C\ .u_c$ (3.5)

Where C_0 is the initial linear capacitance, which represents the capacitor's electrostatic capacitance, and k_C is a coefficient, which shows the impacts of the supercapacitor's diffused layer. The coefficient models the Faradic effect and electrochemical reactions on one side of a hybrid supercapacitor [32].

The specified capacitor current is

$$i_c = \frac{\partial Q}{\partial t} = \left(c(u_c) + u_c \frac{dC(u_c)}{du_c}\right)\frac{du_c}{dt} = C_I(u_c)\frac{du_c}{dt} \quad (3.6)$$

The virtual capacitance represented by the symbol $C_I(u_C)$ is the so-called current capacitance. In putting (3.5) into (3.6)

$$C_I(u_c) = C_0 + 2K_C.u_c \qquad \text{And} \quad i_c = (C_0 + 2K_C.u_c)\frac{du_c}{dt} \quad (3.7)$$

3.2.3 The Ultra-capacitor Energy Capacity:

When an ultra capacitor is charged to a voltage of Uc, the energy it contains

$$E_C(u_c) = \frac{1}{2}\left(C_0 + \frac{4}{3}K_C u_C\right){u_C}^2 = \frac{1}{2}C_E(u_C){u_C}^2 \quad (3.8)$$

The so-called energetic capacitance is represented by the symbol CE (u_C).

When an ultracapacitor discharges from its maximum initial voltage UC0max to its minimum final voltage UC0min , the energy available is

$$\Delta E_C = \frac{C_0}{2}(U^2{}_{C0MAX} - U^2{}_{C0MIN}) + \frac{2}{3}K_C(U^3{}_{C0MAX} - U^3{}_{C0MIN}) \quad (3.9)$$

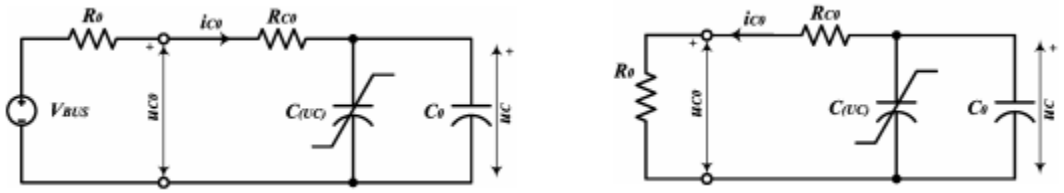
In practical applications, this equation will be utilized to determine how much energy the ultra-capacitor can store and release.

3.3. The Ultra-capacitor Charge/Discharge Method:

Constant voltage, constant resistance, constant current, and constant power conversion mode are theoretically the four different power conversion modes that are feasible. Since the ultra-capacitor is a voltage source with an internal resistance, the first one is not applicable. The following section provides a brief overview of the three other conversion methods' most significant traits.

3.3.1. Constant Resistive Load:

The simplest charge/discharge technique uses a constant resistive load. Through a charge resistor R0 and a load resistor R0, the capacitor is charged from voltage source VBUS and discharged. This approach will not be explored, though, due to its low conversion efficiency, which is rarely employed in power applications.



(a) (b)

Fig 3.6 the power conversion using ultra-capacitors and resistors. A charging and a discharging process [33]

3.3.2. Constant Current:

A steady current load or source can charge or discharge the ultra-capacitor. Constant torque driven electric motors and controlled chargers are two examples of regulated power converters that frequently use constant current loads and sources.

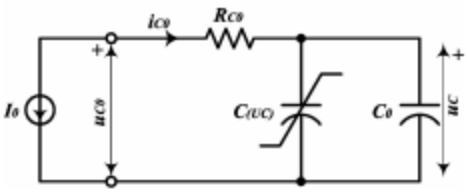


Fig 3.7 using a continuous current source to charge and discharge the ultra-capacitor [34]

3.3.2.1 Discharging:

Assuming the ultra-capacitor is being discharged by constant current I0, let's say the ultra-initial capacitor's voltage is UC0. The internal voltage of the capacitor drops as

$$u_c(t) = \sqrt{\frac{{C_0}^2}{4{K_C}^2} + \frac{1}{K_C}}\left(U_{C0}C_0 + {U_{C0}}^2K_C - I_0t\right) - \frac{C_0}{2K_C} \text{ …….0<t<} T_{DIS} \quad (3.10)$$

where the discharge time is

$$T_{DIS} = \frac{1}{I_0}\left(C_0U_{C0} + K_C{U_{C0}}^2\right) \quad (3.11)$$

3.3.2.2 Maximum Discharge Power

The internal resistance of the capacitor R_{C0}, limits and defines the maximum power provided to the load.

$$P_{0MAX} = \frac{{u^2}_c}{4R_{C0}} \quad (3.12)$$

The capacitor voltage uC and internal resistance RC0 determine how much current I0 is allowed to flow.

$$0 < I_0 < I_{0MAX} \text{ where } I_{0MAX} = \frac{u_c}{R_{C0}} \quad (3.13)$$

The capacitor terminal voltage u_{C0} turns negative and the load changes state to become a source if the current exceeds the limit. The capacitor is nevertheless still discharging. The capacitor's intrinsic series resistance, R_{C0}, dissipates all of the energy given from the current source and energy recovered from the capacitor.

3.3.3. Charging:

When charging an ultracapacitor, the voltage is

$$u_c(t) = \sqrt{\frac{{C_0}^2}{4{K_C}^2} + \frac{1}{K_C}}\left(U_{C0}C_0 + {U_{C0}}^2K_C + I_0t\right) - \frac{C_0}{2K_C} \quad 0<t<T_{CH} \quad (3.14)$$

And charging time is

$$T_{CH} = \frac{1}{I_0}\left(\frac{{C_0}^2}{4} - K_C\left(U_{0MAX} - R_{C0}I_0 + \frac{C_0}{2K_C}\right)^2 - C_0U_{C0} - K_C{U_{C0}}^2\right) \quad (3.15)$$

where U_{0MAX} is the capacitor terminal voltage.

3.3.3.1 Maximum Charging Power:

The current I_0 is negative when charging. The capacitor terminal voltage U_{0MAX} limits the amount of current that may be injected into an ultracapacitor,

$$I_{0MAX} = \frac{U_{0MAX} - u_c}{R_{C0}} \qquad (3.16)$$

Maximum charging power can be defined from (3.16) as a function of capacitor voltage and resistance.

$$P_{0MAX} = \frac{U_{0MAX}(U_{0MAX} - u_c)}{R_{C0}} \qquad (3.17)$$

3.3.4 Constant Power:

Most loads and sources in power conversion applications behave as constant power, either positive or negative. Power converters with regulated output voltage, such as pulse width modulated (PWM) variable speed drives and dc-dc converters, are typical instances of such continuous power loads. Power of the load is defined as $P_{C0} = -u_{C0} i_{C0}$ in accordance with Fig. 3.8's convention, where power is positive in sink (load) mode and negative in source mode.

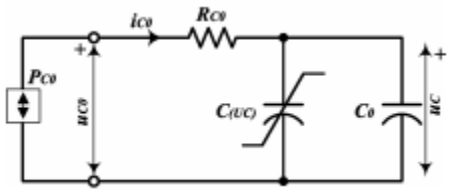


Fig. 3.8. Using a constant power supply to charge and discharge an ultra-capacitor [34]

3.3.4.1 Discharging:

The differential equation shown below describes the circuit in Fig. 3.8

$$P_{C0} = -C_0 \frac{P^2_{C0}}{i^3_{C0}} \frac{di_{C0}}{dt} + R_{C0} C^2_0 \frac{P^2_{C0}}{i^4_{C0}} \left(\frac{di_{C0}}{dt}\right)^2 \qquad (3.18)$$

Where k_C=0 and the ultra-capacitor is assumed to be a linear capacitor. The ultra-capacitor resistance R_{C0} can be disregarded in the analysis if the ultra-capacitor is chosen properly since the power P_{C0} will be substantially lower than the matching maximum power, $P_{C0} \ll P_{0MAX} = \frac{u^2_c}{4R_{C0}}$ One can determine the ultra-capacitor discharge current from those two approximations.

$$i_{C0} = -\frac{|P_{C0}|^2}{U_C} \sqrt{\frac{C_O U^2_C}{C_0 U^2_C - 2P_{C0} t}} \qquad (3.19)$$

The initial voltage of an ultracapacitor is U_{C0}. The maximum discharge period is

$$t \leq \frac{C_O U^2{}_{C0}}{2|P_{C0}|} \quad (3.20)$$

3.3.4.2 Maximum Discharge Power:

The internal series resistance R_{C0} limits the capacitor's maximum power, just as it does in the case of current or resistive discharge. The greatest amount of power that may be applied to a load with a constant power characteristic is

$$P_{0MAX} = \frac{u^2{}_c}{4R_{C0}} \quad (3.21)$$

Please be aware that, just like in the two situations before it, the maximum power is determined by the capacitor voltage and R_{C0} (constant resistance and constant current load). But there is a crucial distinction. The system becomes unstable and the voltage collapses if the load exceeds the maximum power at the specified ultra-capacitor voltage.

3.3.4.3 Charging:

According to the notation in Fig. 3.8, the power of the power source P_{C0} is negative when an ultra-capacitor is in the charging mode. We acquire the ultra-capacitor charging current by applying only negative power using the same technique as before.

$$i_{C0} = \frac{P_{C0min}}{U_{C0min}}{}^2 \sqrt{\frac{C_O U^2{}_{C0min}}{C_0 U^2{}_{C0min} + 2P_{C0}t}} \quad (3.22)$$

Where U_{C0min} is the starting ultracapacitor voltage.

3.3.4.4 Maximum Charging Power:

Power P_{C0} is negative when the device is charging. As a result, in this instance, the maximum power stability constraints are not relevant. In other words, regardless of the power P_{C0}, the system shown in Fig. 3.8 is stable in the charging mode. But in a genuine application, there is Maximum power that can be transferred into the ultra-capacitor bank is also constrained by this factor. It is due to the maximum voltage of the power source, U_{0MAX}.

$$P_{0MAX} = \frac{U_{0MAX}\,(U_{0MAX} - u_c)}{R_{ESR}} \quad (3.23)$$

3.4 Trends in the Development of Ultra-capacitors:

Energy density and the internal equivalent series resistance, which essentially defines the power density, are two important characteristics that are significant for the creation of a new generation of ultracapacitors. The majority of commercially available ultra-capacitors at this time have a power density of up to 20kW/kg and an energy density of roughly 5Wh/kg [36]-[39].

The energy density of currently available ultra-capacitors is only about 5% that of commonly used lithium-ion batteries. This is insufficient for the majority of applications. Energy densities of at least 20Wh/kg are required.

The development of ultra-capacitors is currently divided into four major mainstreams: 1) carbon nano tube technology, 2) nano - gate technology, 3) EeStore technology, and 4) mega farad super-capacitor technology.

The creation of a novel ultra-capacitor based on carbon nanotube technology has begun at the Massachusetts Institute of Technology (MIT), under the direction of Professor Joel Schindall [33 -34]. Based on such an approach, an ultra-capacitor might have an energy density as high as 25% or even 50% of that of the current chemical batteries.

In September 2007, Okamura Laboratory and Power Systems released the first key development findings for a new generation of ultra-capacitors based on the highly promising Nano-gate technology [35]. The anticipated energy density is in the range of 50 to 80 Wh/kg, which is similar to the range of current electrochemical batteries.

The so-called EE-Store technology, which claims to boost energy density up to 280Wh/kg and operating voltage up to 3000V, is the third and most distinctive ultra-capacitor technology [36].

The double layer capacitor, which has an activated carbon electrode on top of a thin layer of high permittivity material, is a recently introduced technology [37]. The anticipated energy density is 500 [Wh/kg], which is two orders of magnitude more than what is now possible.

3.5 Conclusion:

This chapter has covered the ultra-capacitor as a device for storing energy specifically for power conversion purposes. Modern electrochemical batteries can't compete with the ultra-capacitors' higher power density, higher efficiency, longer lifespan, and larger cycling capacity. The energy density of ultra-capacitors is higher than that of modern electrolytic capacitors. With all these benefits, ultra-capacitors are an excellent choice for many power conversion applications that require short-term, 0.1 to 15s, energy storage. Industrial, building, and IT centre applications are only a few examples of the applications.

We've discussed the ultra-capacitor macro model. A first order or higher order RC model that has been simplified is suggested depending on the application's requirements. The temperature and ultracapacitor losses can be calculated using the model. If the ultracapacitor current frequency is much below or above the transition frequency, the first order model is adequate. A second or perhaps third order model is required in the absence of this. For the analysis and synthesis of the interface power converter controllers, the first order model is precise enough.

CHAPTER 4

REGENERATIVE ELECTRIC DRIVES BASED ON ULTRA-CAPCITORS

4.1 Introduction:

Induction or permanent magnet (PM) synchronous motors are the only kind of three-phase motors used in modern regulated electric drives. A pulse width modulated (PWM) converter powers the motor, and the converter receives power from the industrial or distributive mains at 230 V to 690 V and 50 to 60 Hz. The use of such devices still presents a number of technological challenges. In this chapter, two of these problems - recovery of braking energy and drive ride-through capability - are reviewed and a solution is suggested [38].

The majority of drive applications, including those found in lifts, cranes, tooling machines, and other equipment, are characterized by poor balance between average and peak power. Furthermore, many applications require brakes at rated power. The mechanical energy of the spinning mass of the motor load and the motor shaft is typically absorbed in a braking resistor in conventional variable speed drives. In these applications, energy losses might range from 20 to 50 percent of the energy used.

4.2. Operational Modes:

A basic concept of the regenerative controlled electric drive system using an ultracapacitor as an energy storage device is depicted in fig 4.1. An conventional variable speed drive converter (input diode rectifier, voltage dc link, and output inverter) plus an energy storage device coupled in parallel make up the drive system. The inverter feeds a three-phase motor (the induction or synchronies PM motor), whereas the rectifier is connected to the three-phase distribution network. A bi-directional dc-dc power converter and an ultra-capacitor C_{C0} make up the energy storage device. Another sort of storage mechanism, such as a flywheel or battery, could be used as the energy storage. The flywheel is a system that is more complex than the ultracapacitor system, but the battery is not a suitable solution due to its low power density.

For the purposes of the analysis, the dc-dc power converter will be referred to in the first portion of this subsection as a controlled bi-directional dc-dc power converter with one input (the dc bus voltage V_{BUS}) and one output (the ultra-capacitor voltage u_{C0}). The dc-dc converter could be a multiphase interleaved converter, a non-isolated two - or three-level converter, or an isolated dc-dc converter. Depending on the converter topology, the control variable may affect the duty cycle, phase shift, or switching frequency of the dc-dc converter.

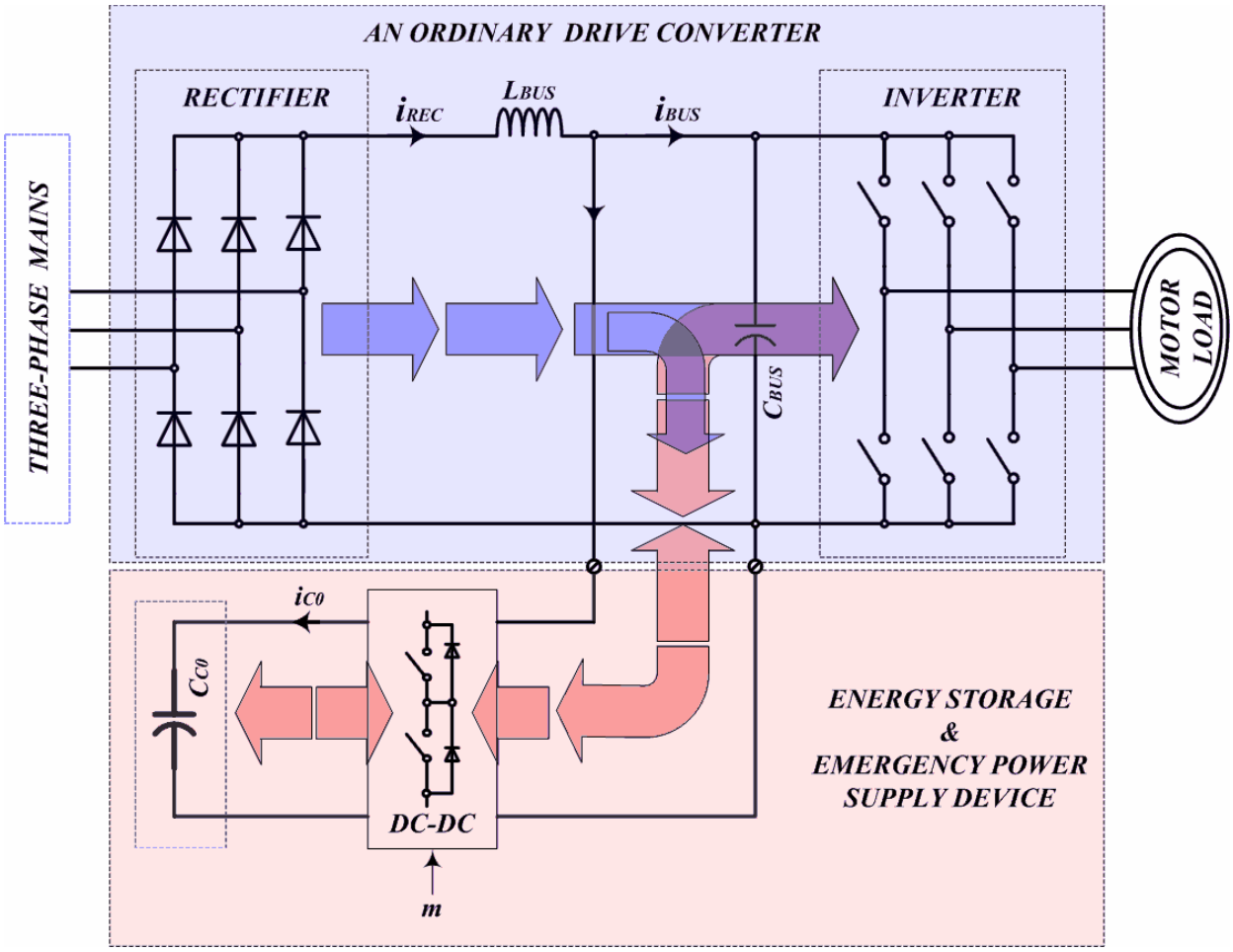


Fig. 4.1 Concept of a regenerative regulated electric drive based on a dc-dc converter and auxiliary energy storage device[38]

The drive system shown in Fig. 4.1's block circuit design is capable of six different modes of operation. The modes are shown in Figures 4.2 and 4.3. The rectifier, inverter, dc bus capacitor CBUS, dc-dc converter, and ultracapacitor all serve as symbols for the driving system. It is just noted in the circuit as an inductance between the rectifier and inverter because the dc bus inductor L_{BUS} is not important for this analysis.

Figure 4.2, MM) "Motoring from the Mains," provides an illustration (a). The drive is powered by the mains and runs in driving mode. The input phase to phase peak voltage is slightly higher than the dc bus voltage (V_{BUS}). In order to stop energy from flowing between the ultra-capacitor and the drive dc bus, the dc-dc converter regulates the ultra-capacitor voltage to $U_{C0inM.}$The mains voltage and the conduction state of the rectifier diodes, which is defined by the dc bus filter capacitor, inductor, and load, respectively, in this mode, determine the rectifier voltage V_{rec}[38].

B) In Fig. 4.2, the braking and energy-storing mode is depicted (b). The drive is in braking mode when in use. The dc bus capacitor charges as the dc bus load becomes negative (the motor becomes a generator), which raises the dc bus voltage V_{BUS}. The dc-dc converter begins to

control the ultra-capacitor current i_{C0} once the dc bus voltage reaches V_{BUSmax} in order to control the dc bus voltage to V_{BUSmax}. The ultra-capacitor voltage rises as the ultra-capacitor current is positive. The ultra-capacitor holds the braking energy.The drive rectifier is blocked because the dc-dc converter controller is built to keep the dc bus voltage V_{BUSmax} higher than the input phase to phase peak voltage. As a result, the rectifier voltage V_{REC} is equal to the dc bus voltage V_{BUS} and the drive input current is zero. The ultra-capacitor is designed to hold a specific amount of energy while braking. Therefore, the ultra-capacitor voltage must be lower than the maximum rated voltage, $U_{C0Max.}$, at the end of a braking phase.

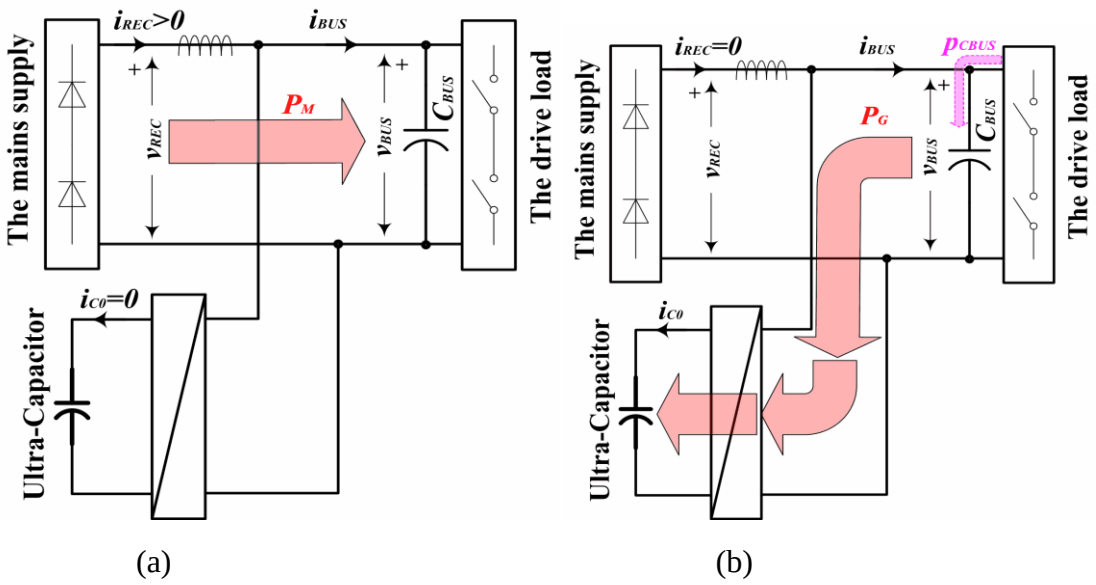


Fig. 4.2 The power flow for various operation modes are following a) The mains motoring mode (MM) and b) the braking mode (B) [38]

STB) Standby mode: The drive, mains, and ultracapacitor do not exchange energy. The ultra-capacitor voltage can be any value between U_{C0max} and U_{C0inM} and is constant. Every time the ultra-capacitor voltage exceeds U_{C0inM}, the control mechanism is built to keep the dc bus voltage at V_{BUSmax}. As a result, in standby mode, if this is the case, the dc bus voltage will remain constant at V_{BUSmax}.

Fig. 4.3 shows the motoring and energy recovery mode for the M_{C0} (a). The drive is fueled by an ultra-capacitor and runs in motoring mode. The voltage of the ultracapacitor is higher than U_{C0inM}. To keep the dc bus voltage constant, the dc bus voltage controller interacts with the dc-dc converter (V_{BUSmax}). In order to reach the intermediate level $U_{C0inM.}$, the ultracapacitor is depleted. The ultra-capacitor provides the energy back. The dc bus voltage drops to the nominal voltage as soon as the ultra-capacitor is depleted to the intermediate level $U_{C0inM.}$, at which point the drive rectifier diodes begin to conduct. Once more, the drive is powered by the mains.

Fig. 4.3 provides an illustration of the ride-through mode (b). The dc bus voltage begins to rapidly drop when the mains power is cut off. The dc-dc converter begins to discharge the ultra-capacitor once it reaches the minimum voltage V_{BUSmin} and keeps the dc bus voltage there. The

ultra-capacitor powers the drive. Deeper discharges of the ultracapacitor occur below the intermediate level $U_{C0inM.}$ and toward $U_{C0Min.}$, the lowest level.

MM-CH) Fig. 3.3 shows the ultra-capacitor charging mode (b). After recovering the mains supply, the ultra-capacitor is refilled to the mid-level $U_{C0inM.}$.

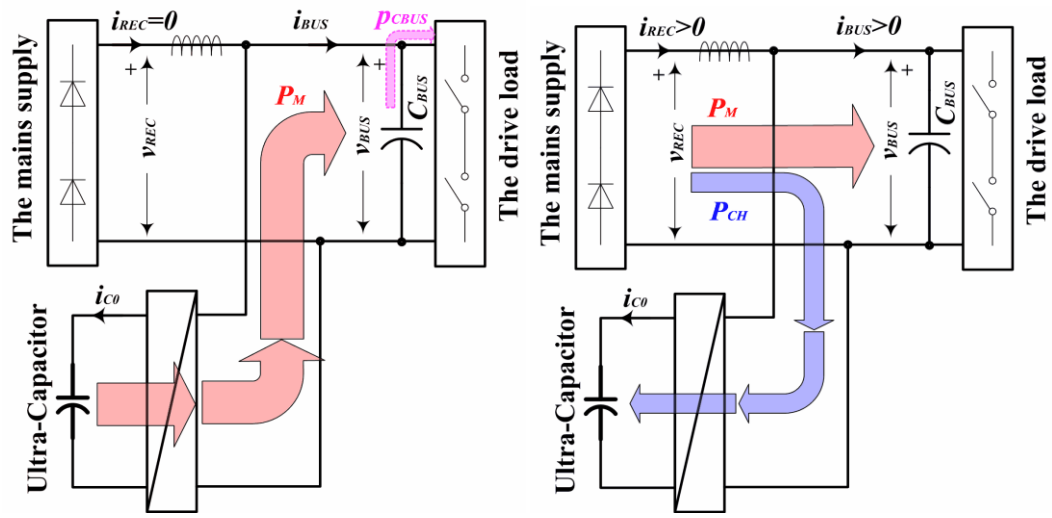
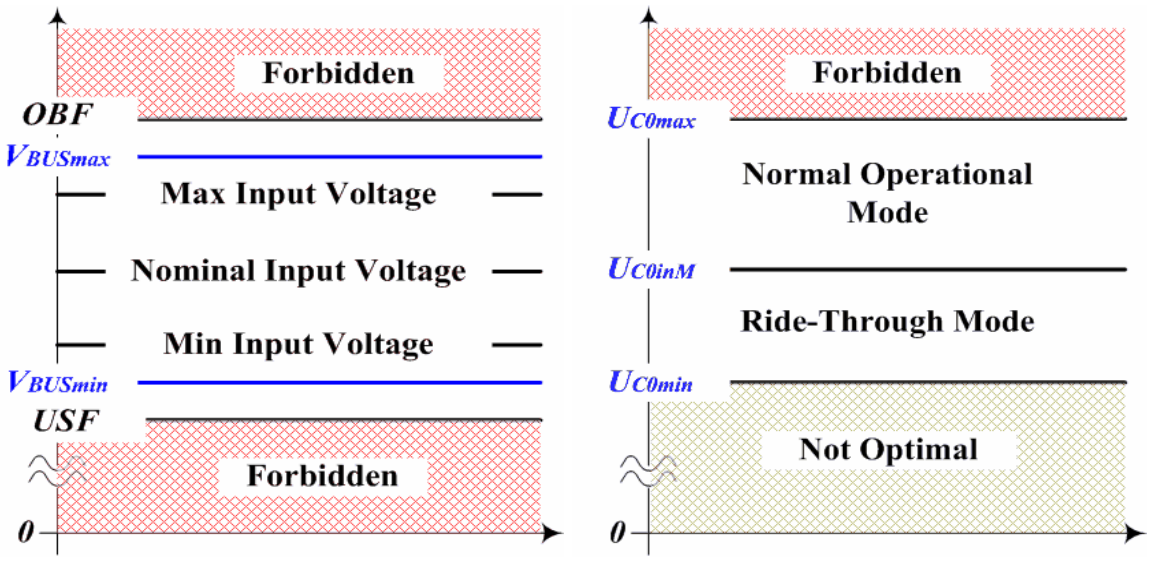


Fig. 4.3 The power flow for each of the following operating modes: a) energy recovery mode (MC0) and ride-through mode (RT); b) the ultra-capacitor charging mode (MM-CH) [38].

4.2.1. Definition of the Reference Voltages

The meanings of the reference voltages V_{BUSmax}, V_{BUSmin}, $U_{C0max.}$, $U_{C0inM.}$, and $U_{C0Min.}$ will now be discussed. The significance of the reference voltages V_{BUSmax} is shown in Fig. 3.5 (a) V_{BUSmin}, too. USF stands for the Under Supply Fault, while OBF stands for Over-Braking Fault.The dc bus voltage changes while the system is in the mains driving mode between the lowest and highest input voltage. To avoid paying unwanted fees and discharge of the ultracapacitor, references to the dc bus voltage V_{BUSmin} and V_{BUSmax} have to remain beyond the typical operating range, as depicted in Fig. 4.4 (a). On the other hand, to stop the dc bus voltage references must not be in the prohibited range during a system fault, either OBF or USF regions. The reference V_{BUSmax} is thus positioned inside an interval [Max Input Voltage, OBF] while the reference V_{BUSmin} is located within an interval [USF, Min Input Voltage].



(a) (b)

Fig. 4.4 The reference voltages are defined in as (a)V_{BUSmax}, (b) V_{BUSmin} and (c) U_{C0Min}, U_{C0inM}, and U_{C0Max} [38].

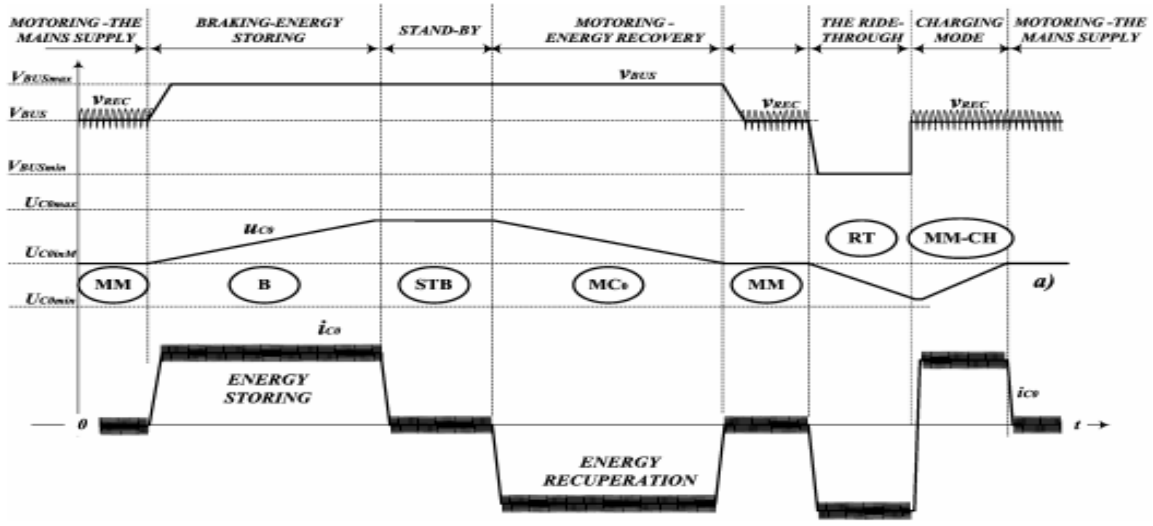


Fig 4.5 the waveforms for the various operating modes, including the mains motoring mode (MM), the braking mode (B), the stand-by mode (STB), the energy recovery mode (MC0), the ride-through mode (RT), the ultra-capacitor charging mode (MM-CH), and the mains peak power filtering mode (MPFM)[38].

4.3. Ultra-capacitor Selection and Design:

The three factors serve as the foundation for the ultra-capacitor design and selection criteria. 1) The ultra-capacitor module's rated voltage, 2) the capacitance of the ultra-capacitor, and 3) the losses and efficiency of the ultra-capacitor.

4.3.1. Voltage Rating:

The rated voltage of an ultra-capacitor module is determined by the interface dc-dc converter topology. For the purposes of this analysis, we've presummated that the dc-dc converter is a non-isolated direct converter with a voltage gain of no more than unity $u_{c0}/V_{BUS} \leq 1$. As a result, the dc bus voltage cannot be higher than the ultra-capacitor voltage. The ultra-rated capacitor's voltage, U_{C0max}, is when the drive's dc bus voltage is at its highest (the drive is braking).

$$U_{C0MAX} \leq V_{BUSMAX} \quad (4.1)$$

The maximum current capability of the dc-dc converter, I_{C0max}, and the conversion power, P_0 determine the ultra-capacitor's minimal working voltage.

$$U_{C0MIN} \geq \frac{P_0}{I_{0MAX}} \quad (4.2)$$

4.3.2. The Capacitance:

The voltage-controlled capacitance is defined as the overall capacitance of an ultra-capacitor as

$$C_{C0}(u_C) = C_0 + K_C * u_c \quad (4.3)$$

where C_0 is the initial capacitance, which represents the electrostatic capacitance of the capacitor, and k_C is a coefficient, which indicates the effects of the diffused layer of the supercapacitor[46].

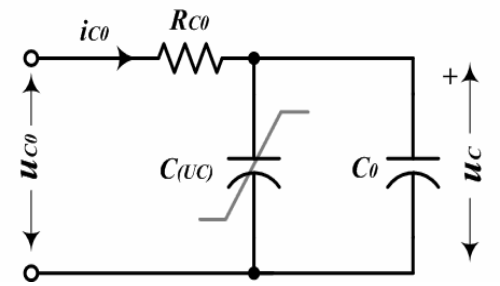


Figure 4.6.Ultracapacitor's first order RC model [34]

Energy storage capacity of the ultra-capacitor as

$$E_C = \frac{C_0}{2}\left({U_{C0MAX}}^2 - {U_{C0}}^2\right) + \frac{2}{3}K_C({U^3}_{C0MAX} - {U^3}_{C0}) \quad (4.4)$$

Where U_{C0} is the ultra-capacitor initial voltage and U_{C0max} is the ultra-capacitor maximum voltage, as specified in (4.1). From (4.4), it is possible to calculate the starting capacitance C_0 for the given braking energy EB and coefficient k_C.

4.3.3. Current Stress and Losses:

In most cases, the ultra-capacitor current has two basically distinct frequency components: 1) Extremely low frequency, and 2) current at high switching frequency.

Energy is transferred from the driving dc bus to the ultra-capacitor through a very low frequency current (braking and motoring from the ultra-capacitor). Taking into account that the ultra-capacitor is a linear capacitor (k_{C0}), one can calculate the ultra-capacitor charging current as

$$i_{c0} = P_{C0}{}^{2}\sqrt{\frac{C_0}{C_0 U^2{}_{C0min} + 2P_{C0}t}} \tag{4.5}$$

where U_{C0min} is the starting ultra-capacitor voltage.

Discharging current has similar form

$$i_{C0} = -|P_{C0}|^{2}\sqrt{\frac{C_O}{C_0 U^2{}_{C0} - 2P_{C0}t}} \tag{4.6}$$

in which the voltage The ultracapacitor's starting voltage is U_{C0}. The charging/discharging power P_{C0} of an ultra-capacitor is constant.

The ultra-capacitor losses are calculated using (4.5) and (4.6), respectively.

$$P_C(t) = R_{C0}P^2{}_{CO}\begin{cases}\frac{C_0}{C_0 U^2{}_{C0}+2P_{C0}t} & Charging \\ \frac{C_0}{C_0 U^2{}_{C0}+2P_{C0}t} & Discharging\end{cases} \tag{4.7}$$

Only when the charging/discharging current frequency is lower than the ultra-capacitor cut-off frequency is the losses model (4.7) accurate. Due to its typical size being far smaller than the average current, high frequency ripple i_{C0} can be disregarded. The additional high frequency losses must be considered if this is not the case.

$$P_{C(HF)} = P_{C0(HF)}\Delta i^2{}_{C0(RMS)} \tag{4.8}$$

R_{C0}(HF) denotes the ultra-capacitor resistance at high frequency.

4.3.3. Conversion Efficiency:

The losses of an ultra-capacitor are determined by a few parameters: the series resistance, capacitance, and the initial voltage of the ultra-capacitor.

4.4 Modeling Aspects and Control Scheme:

4.4.1 Modelling Techniques:

Two models are discussed in this chapter DC-DC converter model and DC Bus circuit model. DC-DC converter model is discussed with two different model Large Signal model and small signal model.

4.4.2 The DC-DC Converter Model:

The converter equivalent circuit schematic is shown in Fig. 4.7, Ideal capacitors C_{B1}, C_{B2} are used to simulate the input filter capacitors. The leakage current of the capacitor is represented by

the current sources i_{B1} and i_{B2}. R_{LC0} is the constant (frequency independent) resistance of the inductor.

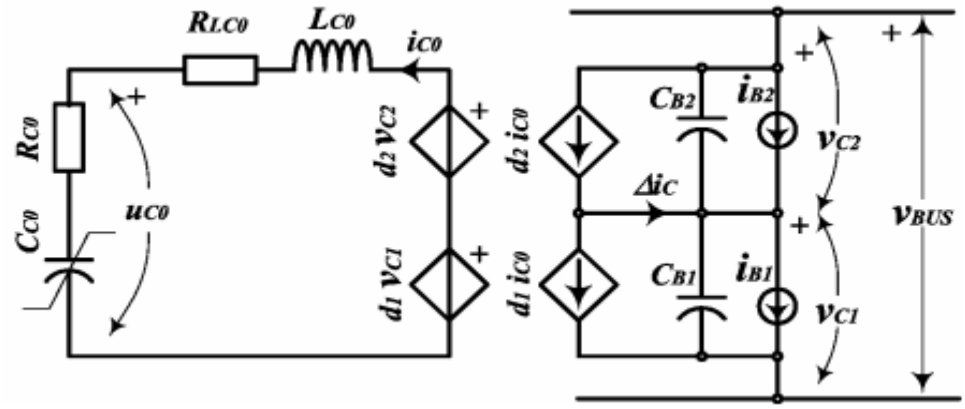


Fig. 4.7 Large signal (average) dc-dc converter model [39].

4.4.2.1 Large Signal Model:

The circuit shown in Fig. 5.1 can be explained by the following set of equations, presuming that V_{BUS}= constant:

$$L_{C0}\frac{d\langle i_{C0}\rangle}{dt} = \langle V_{C1}\rangle d_1 + \langle V_{C2}\rangle d_2 - u_{C0} - R_{LC0}\langle i_{C0}\rangle \quad (4.9)$$

$$\frac{d\Delta\langle V_C\rangle}{dt} = \frac{2}{C_{B1}+C_{B2}}\left(\langle i_{C0}\rangle(d_2-d_1) + (i_{B2}-i_{B1})\right) \quad (4.10)$$

When C_{B1}=C_{B2}=C

$$\frac{d\Delta\langle V_C\rangle}{dt} = \frac{1}{C}\left(\langle i_{C0}\rangle(d_2-d_1) + (i_{B2}-i_{B1})\right) \quad (4.11)$$

$$\langle V_{C1}\rangle = \frac{1}{2}(\langle \Delta V_C\rangle + \langle V_{BUS}\rangle) \quad (4.12)$$

Where $\Delta\langle V_C\rangle = \langle V_{C1}\rangle - \langle V_{C2}\rangle$ And i_{b1} and i_{b2} are the filter capacitors leakage current.

The modulation signals (PWM1 and PWM2) for duty cycles d1 and d2 are produced by a non-linear controller, and the control law is

$$d_1 = \frac{u_0+u_{c0}}{V_{BUS}} + \Delta d \quad (4.13)$$

$$d_1 = \frac{u_0+u_{c0}}{V_{BUS}} - \Delta d \quad (4.14)$$

The main control variable is u_0, while the balancing duty cycle is an auxiliary control variable. The voltage of an ultra-capacitor is u_{C0}, whereas the voltage of a dc bus is V_{BUS}. The voltage error controller (Δvc) generates the control variable Δd, while the current controller (generates) u_0.

Substitute (4.13) and (4.14) into the (4.9)-(4.11)

$$L_{C0}\frac{d\langle i_{C0}\rangle}{dt} = u_0 + \Delta\langle V_C\rangle\Delta d - R_{LC0}\langle i_{C0}\rangle \qquad (4.15)$$

$$\frac{d\Delta\langle V_C\rangle}{dt} = \frac{-2}{C}\langle i_{c0}\rangle\Delta d - \frac{1}{C}\Delta i_B \qquad (4.16)$$

Where $\Delta i_B = \langle i_{B1}\rangle - \langle i_{B2}\rangle$

4.4.2.2 Linearization and Small Signal:

The first order perturbation model can be used to estimate the state and control variables of the system (4.15) and (4.16)

$$\langle i_{C0}\rangle = I_{C0} + \hat{\imath}_{C0}\,\langle\Delta V_C\rangle = \Delta V_C + \Delta\hat{v}_C \qquad (4.17)$$

$$\Delta d = \Delta D + \Delta\hat{d}\Delta i_B = \Delta I_B + \Delta\hat{\imath}_B \qquad (4.18)$$

$$\begin{bmatrix} u_{c0}(s) \\ V_{Bus}(s) \end{bmatrix} = \begin{bmatrix} G_{c0}(s) \\ G_{Bus}(s) \end{bmatrix} i_{c0}(s) + \begin{bmatrix} 0 \\ G_p(s) \end{bmatrix} P_{Load}(s)$$

$$\overleftarrow{control} \qquad \overleftarrow{Disturbance}$$

The ultra-capacitor current to voltage transfer function is

$$G_{C0}(S) = R_{C0}\frac{s + \frac{c_0 - 2kI_{c0}R_{c0} + 2k(U_{c0} + I_{c0}R_{c0})}{R_{C0}(c_0 + 2k(U_{c0} - I_{c0}R_{c0}))^2}}{s + \frac{2kI_{c0}R_{c0}}{c_0 + 2k(U_{c0} - I_{c0}R_{c0}))^2}}$$

$$= R_{C0}\frac{s + w_z}{s + w_p} \qquad (4.19)$$

where w_z and w_p are zero and pole values that are determined by the steady-state variables U_{c0}, I_{c0}, and the ultra-capacitor parameters.

The dc bus voltage transfer activities are under control and disturbed by

$$G_{BUS}(S) = \frac{-(I_{C0}G_{C0}(S) + U_{C0})(1 + SC_{BUS}\,R_{ESR})V_{BUS}}{SC_{BUS}\,(V^2{}_{BUS} - R_{ESR}\,(U_{C0}I_{C0} + P_{LOAD}\,)) - (U_{C0}I_{C0} + P_{LOAD}\,)} \qquad (4.20)$$

$$G_P(S) = \frac{-V_{BUS}\,(1 + SC_{BUS}\,R_{ESR}\,)}{SC_{BUS}\,(V^2{}_{BUS} - R_{ESR}\,(U_{C0}I_{C0} + P_{LOAD}\,)) - (U_{C0}I_{C0} + P_{LOAD}\,)} \qquad (4.21)$$

where V_{BUS} and P_{LOAD} are the steady-state dc bus voltage and load power, and G_{C0} is the ultra-capacitor voltage transfer function (4.19). When the electric drive is powered by an ultra-capacitor and is operating in steady state, the load and power of the ultra-capacitor are equal, or $U_{C0}I_{C0} + P_{LOAD} = 0$. This condition is substituted into (4.20) to produce

$$G_{BUS}(S) = \frac{-(I_{C0}G_{C0}(S) + U_{C0})(1 + SC_{BUS}\,R_{ESR}\,)}{SC_{BUS}\,V_{BUS}} \qquad (4.22)$$

$$G_P(S) = \frac{-(1+SC_{BUS}\,R_{ESR}\,)}{SC_{BUS}\,V_{BUS}} \quad (4.23)$$

As is the case in the majority of cases, the transfer function G_{BUS} changes if the ultra-capacitor is large enough to be regarded as having infinite capacitance in comparison to the dc bus capacitor C_{BUS}.

$$\lim_{c_{c0}\to\infty} G_{BUS}\,(S) = \frac{-(I_{C0}G_{C0}(S) + U_{C0})(1 + SC_{BUS}R_{ESR})}{SC_{BUS}V_{BUS}}$$

Further simplification of the transfer function is possible. Because of the sufficient ultra-capacitor voltage, $U_{C0}>>I_{c0}R_{c0}$, it is possible to ignore the voltage drop on the series resistance. The voltage transfer function for the dc bus is

$$G_{BUS}(S) = \frac{-U_{C0}(1+SC_{BUS}\,R_{ESR}\,)}{SC_{BUS}\,V_{BUS}} \quad (4.24)$$

4.5. Control Scheme:

The primary control goal is to reduce the ultra-capacitor current i_{C0} and the voltage balancing error ΔV_C [40]. The secondary control goal is to asymptotically regulate the desired reference, which relies on the system operation mode, at the desired dc bus voltage, or ΔV_{BUS} [41]. The ultimate goal of control is to manage the ultracapacitor's state of charge, where the state of charge reference varies depending on the mode of operation [41].

4.5.1 The Ultra-capacitor and the DC Bus Voltage Control:

Three operational modes from the control scheme that are significant are

1) the mains motoring mode,

2) the braking and ultra-capacitor motoring, and

3) ride-through mode [41].

4.5.1.1 The mains motoring mode:

The dc bus voltage is V_{BUS} = 1.41V_{MAINS}, where V_{MAINS} is the phase-to-phase RMS voltage on the mains. The dc bus voltage is more than the V_{BUSmin} and less than the V_{BUSmax} of the reference. As a result, the controller for dc bus voltage $G_{VBUSmax}$ is saturated to U_{C0inM} whereas the controller for dc bus voltage $G_{VBUSmin}$ is saturated to zero. Consequently, the ultra-capacitor voltage reference

$$u_{coref} = U_{COiNM} + 0 = U_{COiNM} \quad (4.25)$$

To stop energy from flowing between the ultra-capacitor and the drive, the controller G_{uC0} keeps the ultra-capacitor voltage constant up to the intermediate level U_{COiNM}.

4.5.1.2 The Drive Braking Mode and Motoring Mode from the Ultra-capacitor:

The dc bus capacitor C_{BUS} is charged since the driving load is inverted (the motor acts as a generator). The reference V_{BUSmax} is reached when the dc bus voltage V_{BUS} reaches that level. While the controller $G_{vBUSmin}$ remains saturated to zero, the dc bus voltage controller $G_{vBUSmax}$ exits saturation. The ultra-capacitor current increases when the ultra-capacitor reference voltage starts to rise from U_{C0inM} towards U_{C0max}. The cascaded controllers $G_{vBUSmax}$ and G_{uC0} change the current's magnitude to a specific level in order to keep the dc bus voltage constant. The voltage u_{C0} will reach the maximum U_{C0max} if the braking energy is larger than the ultra-capacity. capacitor's At U_{C0max}, the dc bus voltage controller $G_{vBUSmax}$ will then become saturated.The voltage of the ultracapacitor is controlled to U_{C0max}, and the current i_{C0} decreases to zero. The ultra-capacitor is no longer being charged. The dc bus voltage starts to rise up until the brake resistor or drive over-voltage (over-braking) protection is activated.

The ultra-capacitor must be discharged to the intermediate value U_{C0inM} when the drive is in driving mode in order to be prepared for the subsequent braking phase. The dc bus voltage is maintained for V_{BUSmax} by the dc bus voltage controller $G_{vBUSmax}$. The ultra-capacitor voltage reference lowers towards U_{C0inM} as the controller $G_{vBUSmax}$ output decreases.

$$U_{coinM} \leq u_{coref} \leq U_{comax} \tag{4.26}$$

The drive is being powered by the discharge of the ultra-capacitor. The dc bus voltage controller $G_{vBUSmax}$ will become saturated at the reference U_{C0inM} once the ultra-capacitor voltage hits the intermediate value U_{C0inM}. Since the ultra-capacitor voltage is controlled to U_{C0inM}, the ultra-capacitor current zeroes out. The ultra-capacitor has finished being discharged. The dc bus voltage drops as the dc bus capacitor is depleted, and this process continues until the drive input rectifier begins to conduct. The drive is now again receiving power from the mains.

4.5.1.3 The Ride-Through Mode:

The dc bus voltage starts to drop when the mains are cut off and continues to drop until it reaches the lower reference V_{BUSmin} . As the controller $G_{vBUSmin}$ exits saturation, its output begins to fall below zero in the direction of $\Delta U_{COmin} = U_{COmin} - U_{COiNM.}$ $G_{vBUSmax}$ on the controller is saturated.The ultracapacitor reference voltage begins to fall below U_{COiNM} and approaching U_{COmin}.

$$U_{coinM} \leq u_{coref} \leq U_{coinM} - U_{coinM} + U_{comin} = U_{comin} \tag{4.27}$$

It enables a deeper ultracapacitor discharge as well as the control of the dc bus voltage to the V_{BUSmin} minimum level. The ultracapacitor will discharge to its lowest level, U_{C0min}, if the power outage lasts longer than what is set. The dc bus voltage will drop until it reaches the under-voltage supply fault (USF) threshold as the ultra-capacitor current reaches zero.

4.6 The Controller(s) Synthesis:

4.6.1. The Ultra-capacitor Voltage Controller:

The ultra-capacitor voltage control loop is depicted in Fig. 5.14, where G_F is the feedback filter, G_{uC0} is the voltage controller, and G_{C0} is the ultra-capacitor current to voltage transfer function (4.19).

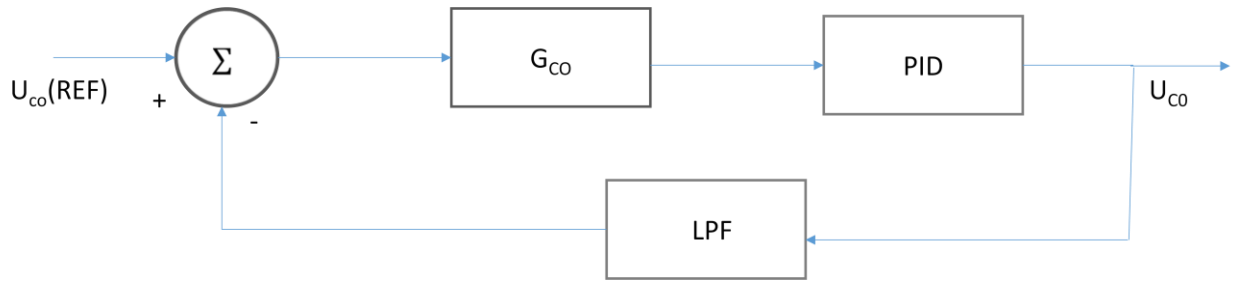


Fig 4.8.The ultra-capacitor voltage closed loop.

Here, low pass filter transfer function is

$$G_F(S) = \frac{1}{ST_F+1} \tag{4.28}$$

And PID controller transfer function is G_{uco}.

The ultra-capacitor voltage closed loop transfer function is

$$\frac{U_{co}(s)}{U_{co\,(REF)}(s)} = \frac{G_{co}(s)G_{uco}(s)}{1+G_{co}(s)G_{uco}(s)G_F(S)} \tag{4.29}$$

The ultra-capacitor voltage controller is a proportional (P) controller.

$$G_{uco}(s) = K_{PC0} \tag{4.30}$$

The ultra-capacitor current to voltage transfer functions from (4.19) is

$$G_{co}(s) = R_{C0}\frac{s+w_z}{s+w_p}$$

where w_z and w_p are the zero and pole of the ultra-capacitor voltage transfer function (4.19).

The ultra-capacitor voltage closed loop transfer function is

$$\frac{U_{co}(s)}{U_{co(REF)}(s)} = \frac{G_{co}(s)G_{uco}(s)}{1+G_{co}(s)G_{uco}(s)G_F(S)}$$

$$\frac{U_{co}(s)}{U_{co\,(REF)}(s)} = \frac{R_{C0}K_{PC0}(s+w_z)}{s^2T_F+s(1+T_Fw_p+R_{C0}K_{PC0})+(w_p+w_zR_{C0}K_{PC0})} \tag{4.31}$$

Characteristic equation of (5.21) is

$$D_{uco}(s) = s^2 + s\frac{(1+T_F w_p + R_{C0}K_{PC0})}{T_F} + \frac{(w_p + w_z R_{C0}K_{PC0})}{T_F} \quad (4.32)$$

where ζ_{C0} is damping factor and ω_{C0} is the closed loop natural frequency. Proportional gain of the controller and time constant of the filter can be computed from (4.20) and (4.32) using the binomial criterion (ζ_{C0}=1).

The current capacity of the converter determines the maximum bandwidth. The ultra-capacitor voltage controller will produce a current reference that is bigger than the maximum current of the dc-dc converter if the bandwidth is high. The present controller G_{iC0} will therefore as a result, the ultra-capacitor voltage controller will not be able to control the voltage because the feedback loop is full.

From (5.22) follows relation between proportional and integral gain

$$\frac{(1+T_F w_p + R_{C0}K_{PC0})^2}{4\zeta_{co}{}^2 T_F} - w_p - w_z R_{C0}K_{PC0} = 0 \quad (4.33)$$

The ultra-capacitor voltage error is

$$\Delta U_{co}(s) = U_{co(REF)}(s) - U_{co}(s) = i_{co}(s)\frac{1}{K_{PCO}} \quad (4.34)$$

Assume that the time taken to charge and discharge the ultra-capacitor is T_0 and that the current is constant at i_{C0max}. One may calculate

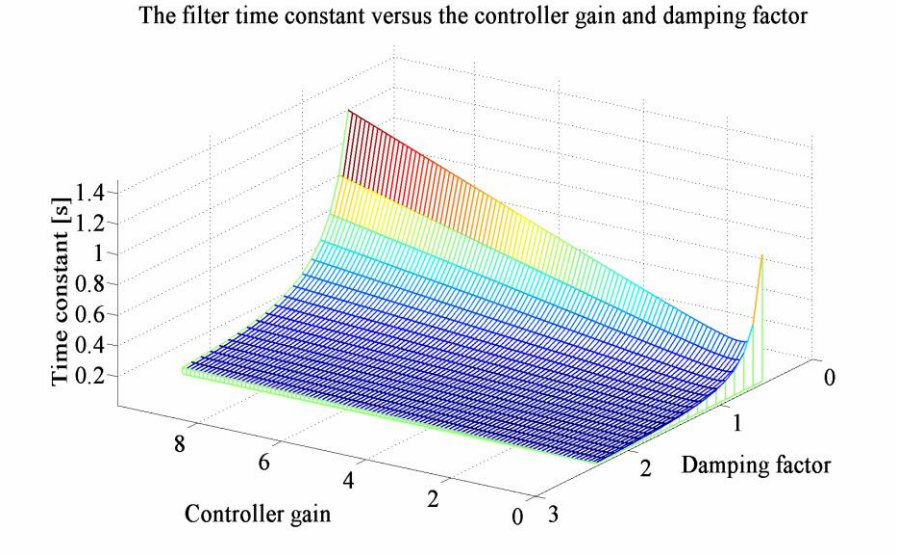
$$\Delta U_{co} = \frac{i_{coMAX}}{K_{PCO}} \quad (4.35)$$

The controller proportional gain K_{PCO} is computed from (4.34) as

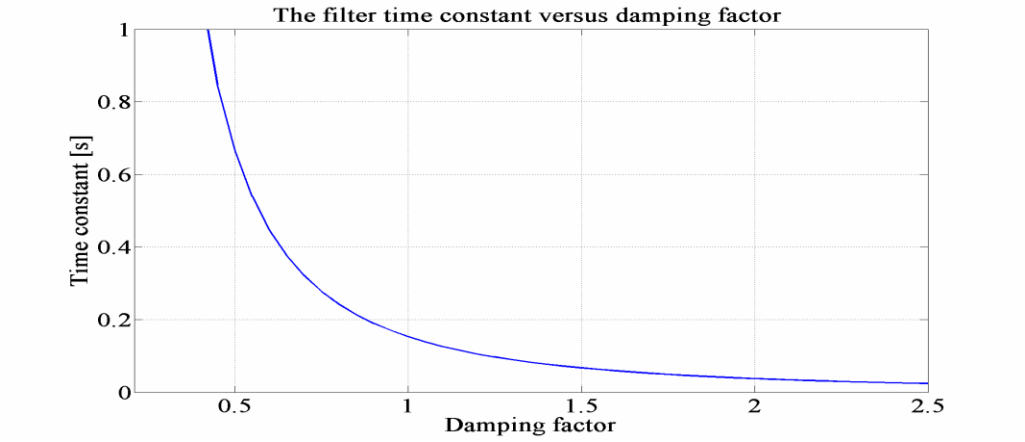
$$K_{PCO} \geq \frac{i_{coMAX}}{\Delta U_{co}} \quad (4.36)$$

The filter time constant is then produced as a function of the ultra-capacitor parameters and the closed loop damping factor by putting (4.36) into (4.33).

$$T_F = \frac{1}{2w_p{}^2}\left(\left(w_p + w_z R_{C0}K_{PC0}\right)4\zeta_{co}{}^2 - 2(1 + R_{C0}K_{PC0}) \pm \sqrt[2]{\left(\left(w_p + w_z R_{C0}K_{PC0}\right)4\zeta_{co}{}^2 - 2(1 + R_{C0}K_{PC0})\right)^2 - 4(1 + R_{C0}K_{PC0})^2 w_p{}^2}\right) \quad (4.37)$$



(a)



(b)

Fig.4.9 (a) The filter time constant (TF) vs the controller gain and damping factor is shown. RC0 = 2, CC0 = 3, and kC = 0.1/700 F/V. (b) TF vs damping factor for a controller with fixed gain, kPC0 = 5.

Table 5.1.Specification of the Control System

ULTRA-CAPACITOR		DC BUS	
U_{coMAX}	780V	V_{BUSMAX}	700V
U_{coinM}	350V	V_{BUSMIN}	450V
U_{coMIN}	250V	C_{BUS}	820µF
C_{co}	0.4F	R_{ESR}	190mΩ
R_{co}	2Ω	BANDWIDTH	50HZ

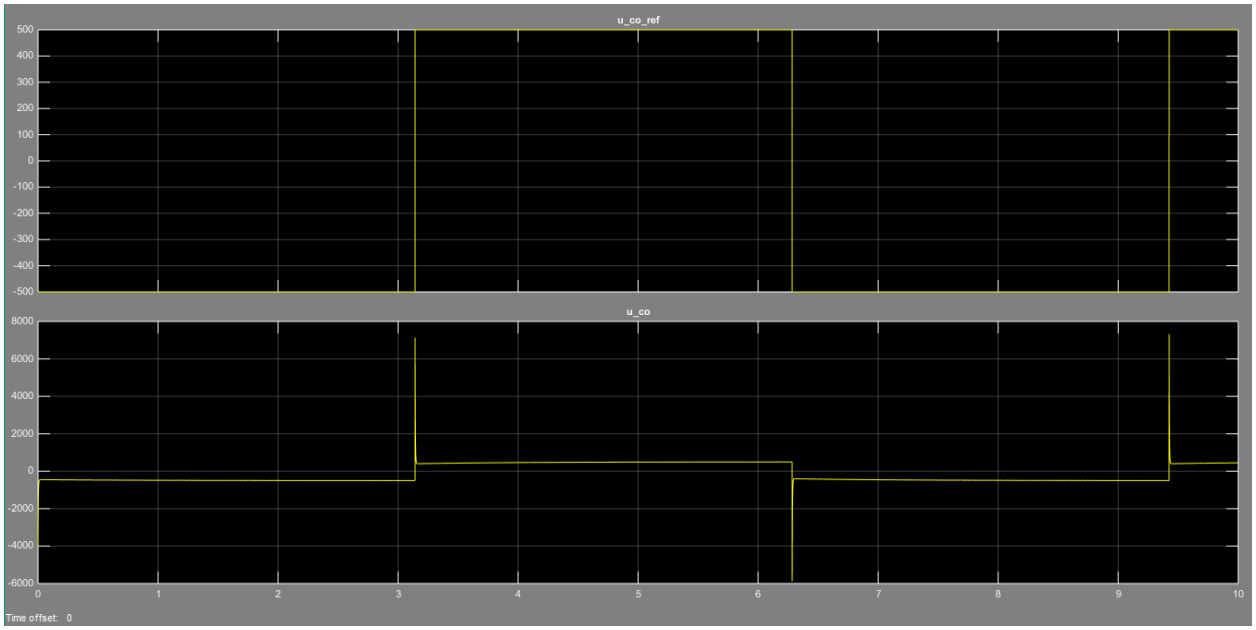


Fig 4.10 Simulated result of ultra-capacitor reference voltage and ultra-capacitor voltage

4.6.2 The DC Bus Voltage Controller:

The dc bus voltage control and the ultra-capacitor voltage control are cascaded. The ultra-capacitor voltage control loop is an order of magnitude slower than the dc bus voltage control loop, which could provide a difficulty for the controller synthesis. Let's look at how the analysis can be made simpler and the dc bus voltage controller created.

The dc bus voltage close loop transfer function is define as from fig.(4.28)

$$\frac{V_{BUS}(S)}{V_{BUS\,(REF)}(S)} = \frac{G_{VBUS}(S)G_{UC}(S)G_{CONTROLLER}(S)}{1+G_{VBUS}(S)G_{UC}(S)G_{CONTROLLER}(S)} \tag{4.38}$$

Here, $G_{UC}(S)$ is the overall transfer function is ultra-capacitor loop.

$G_{CONTROLLER}(S)$ is the transfer function of PID controller.

The dc bus voltage controller is the classical PI controller

$$G_{CONTROLLER}(S) = \frac{K_P S + K_I}{S} \tag{4.39}$$

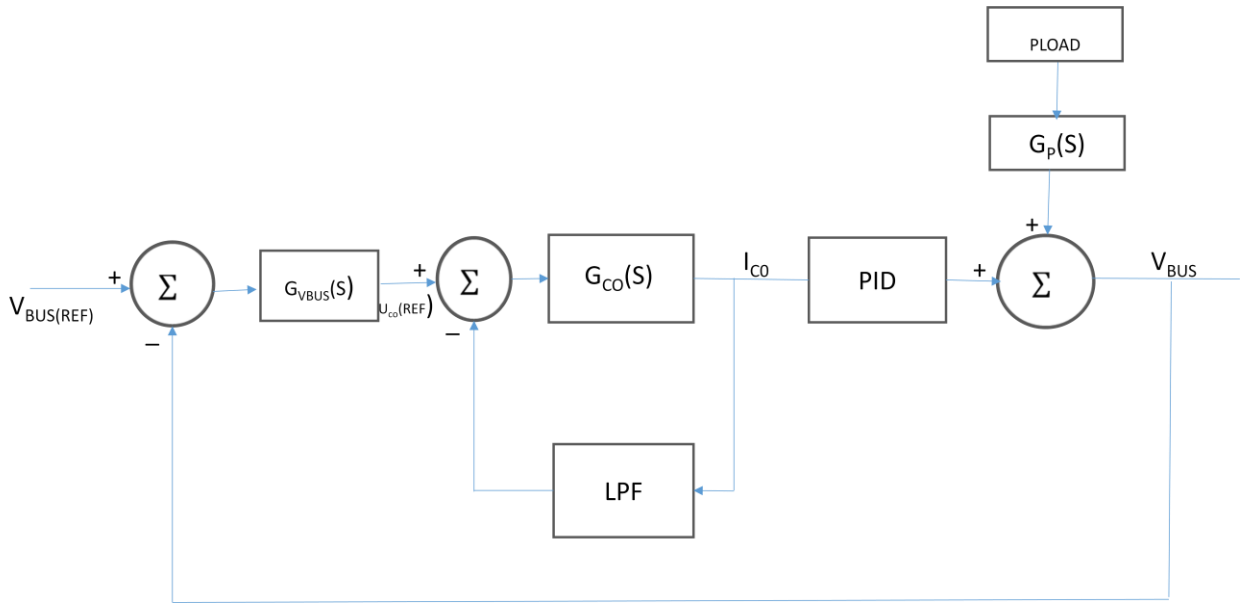


Fig 4.11 Block diagram of DC bus voltage controller

The characteristic equation of the closed loop transfer function (4.38) is

$$D_{VBUS\,(S)} = S^2 - S\frac{(K_P + K_I R_{ESR}\, C_{BUS}\,) K_{PC\,0} U_{C0}}{C_{BUS}\,(V_{BUS} - K_P R_{ESR}\, C_{BUS}\, U_{C0})} - \frac{K_I K_{PC\,0} U_{C0}}{C_{BUS}\,(V_{BUS} - K_P R_{ESR}\, C_{BUS}\, U_{C0})} \quad (4.40)$$

$$= S^2 + 2\zeta_{BUS} W_{BUS} S + {W_{BUS}}^2$$

Here, where ζ_{BUS} is damping factor and W_{BUS} is the closed loop natural frequency.

The Butterworth criterion (ζ_{BUS}=0.7) are used to calculate proportional and integral gains.

$$K_P = -\frac{W_{BUS}\, C_{BUS}\, V_{BUS}\,(1.4 - W_{BUS}\, R_{ESR}\, C_{BUS}\,)}{K_{PC\,0} U_{C0}(1 - W_{BUS}\, R_{ESR}\, C_{BUS}\,(1.4 - W_{BUS}\, R_{ESR}\, C_{BUS}\,))} \quad (4.41)$$

$$K_I = -\frac{{W^2}_{BUS}\, C_{BUS}\, V_{BUS}}{K_{PC\,0} U_{C0}(1 - W_{BUS}\, R_{ESR}\, C_{BUS}\,(1.4 - W_{BUS}\, R_{ESR}\, C_{BUS}\,))} \quad (4.42)$$

If the dc bus capacitor series resistance can be neglected, $W_{BUS} R_{ESR} C_{BUS} \ll 1$ is simplified and the controller gains computed as

$$K_P = -\frac{W_{BUS}\, C_{BUS}\, V_{BUS}\, 1.4}{K_{PC\,0} U_{C0}} \quad (4.43)$$

$$K_I = -\frac{{W^2}_{BUS}\, C_{BUS}\, V_{BUS}}{K_{PC\,0} U_{C0}} \quad (4.44)$$

The gains of the controllers are dependent on the ultra-capacitor voltage, which in most cases is not constant over time, taking values between U_{C0min} and U_{C0max}. The ultra-capacitor voltage U_{C0}'s worst-case scenario must be adequately dampened by the dc bus voltage controller's design. One can plot the near loop root locus versus the ultra-capacitor voltage to establish the worst-case scenario. Fig. 4.12 illustrates the location of the root.

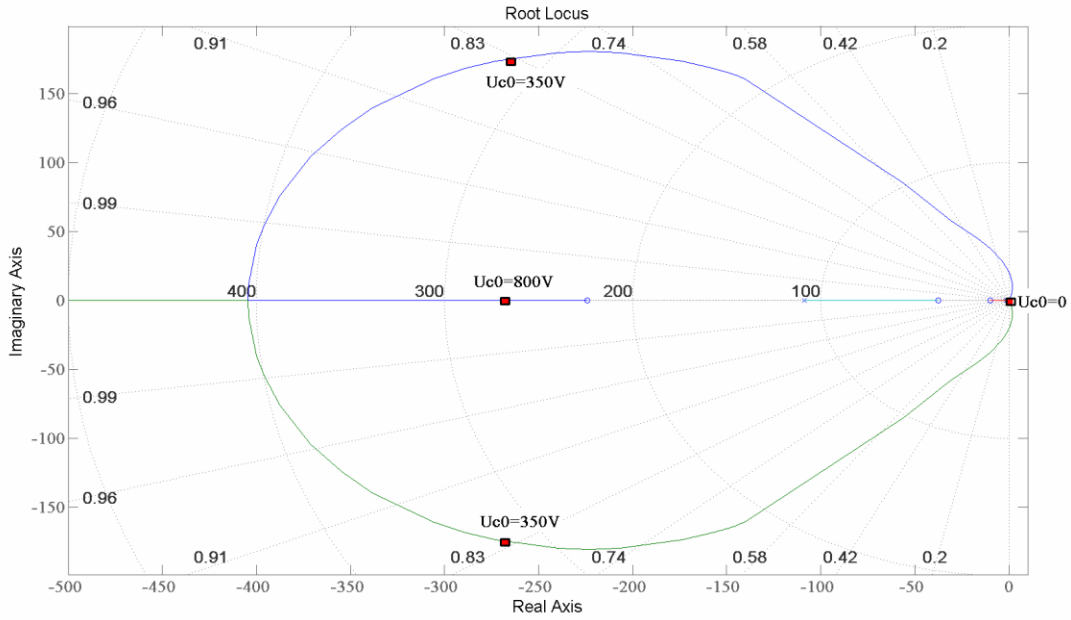


Fig.4.12. The ultra-capacitor voltage U_{C0} in relation to the closed loop root locus of the dc bus voltage. k_{PBUS}=0.08, k_{IBUS}=16, f_{BUS}=25Hz, and V_{BUS}=700V [38].

As can be observed, the damping factor rises as the voltage of the ultra-capacitor does. As a result, the controllers must be built to handle the UC0min minimum ultra-capacitor voltage. In that case, the damping factor will not be lower than the desired for any value of the ultracapacitor voltage.

$$K_{PMAX} = K_P(V_{BUSMAX}, U_{COINM})$$

$$K_{IMAX} = K_I(V_{BUSMAX}, U_{COINM})$$

$$K_{PMIN} = K_P(V_{BUSMIN}, U_{COMIN})$$

$$K_{IMIN} = K_I(V_{BUSMIN}, U_{COMIN})$$

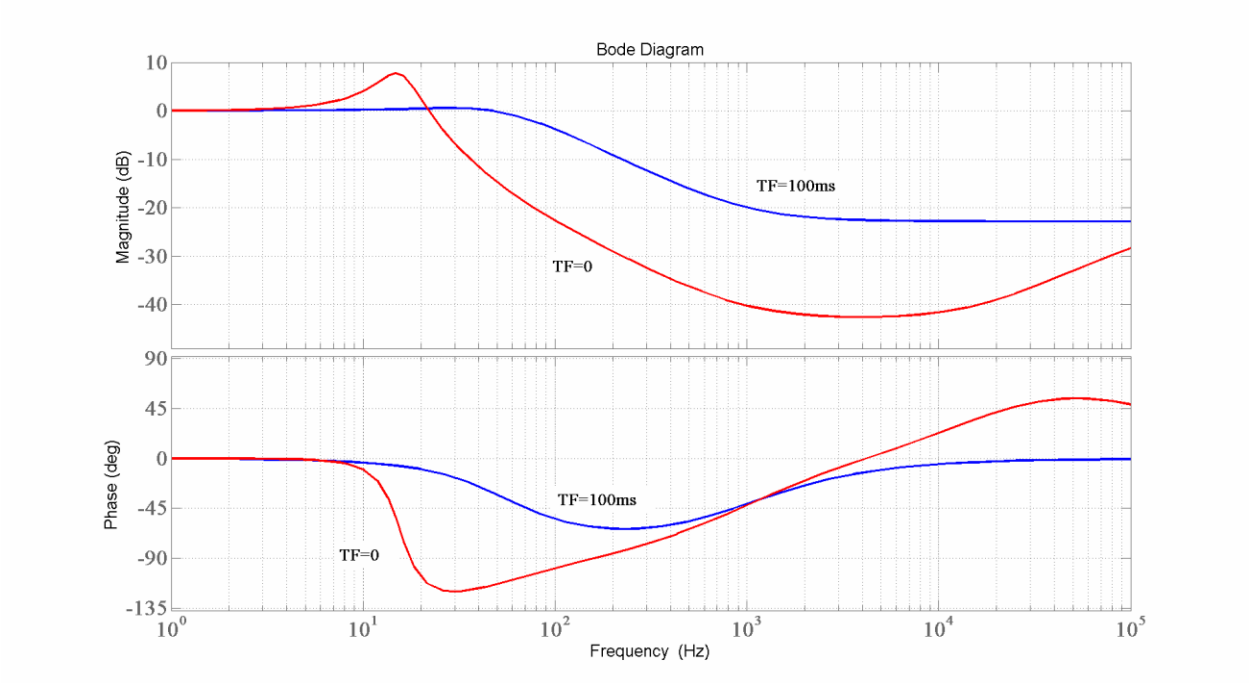


Fig 4.13 Bode diagram of the ultra-capacitor voltage feedback filter's dc bus voltage transfer function for various time constants, $V_{BUS}(s)/V_{BUS(REF)}(s)$ [38]

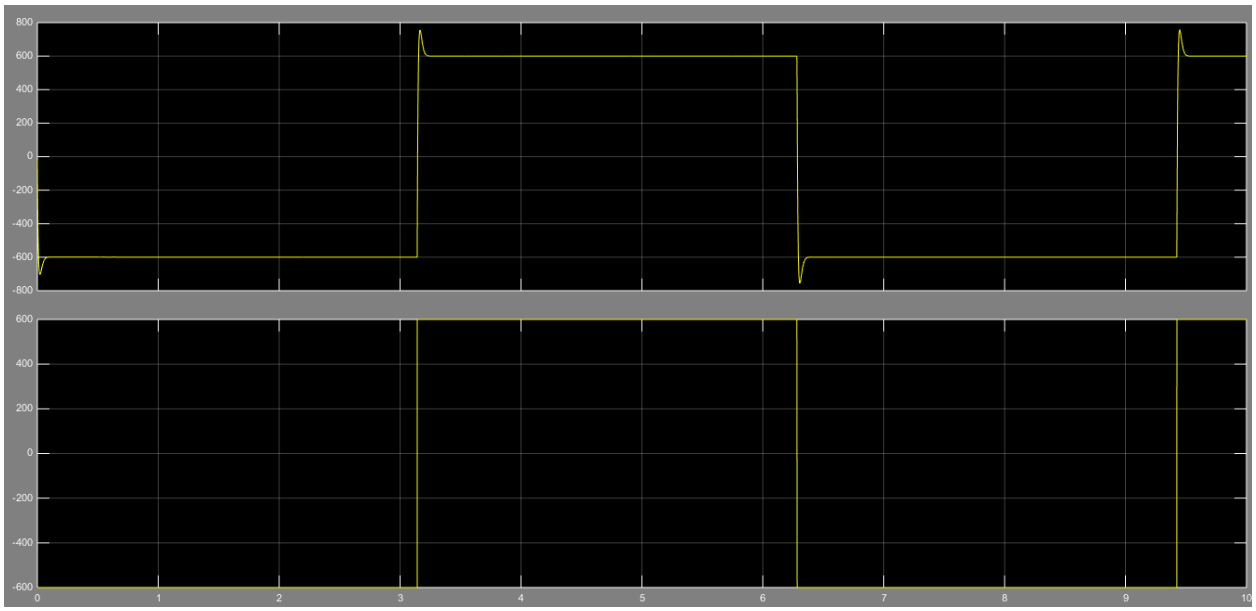


Fig 4.14. simulated result of DC bus voltage and reference DC bus voltage

4.7 Conclusion:

This section of the dissertation discusses the use of ultra-capacitor-based energy storage devices in controlled electric drives. When possible, the ultra-capacitor is employed to restore the energy

stored in the drive braking system. In addition, the ultra-capacitor can be used as backup energy in the event of a mains power outage.

An interface dc-dc converter is required since it is not practical to connect the ultra-capacitor directly to the regulated electric drive. Modern interface dc-dc converter topologies are explored, and a brand-new three-level converter is suggested. In addition to providing design principles, the suggested topology is analysed. A new control strategy is suggested together with the development of the model of the full conversion system. Controlling the ultra-capacitor current and dc bus midpoint voltage is the aim of the proposed control technique. Depending on the operating mode, the second control goal is to asymptotically regulate the dc bus voltage to the specified reference. The third control objective is to regulate the state of charge (SOC) of ultra-capacitors.

CHAPTER 5

CONCLUSION

5.1 Contribution of the Thesis:

- Bidirectional dc-dc Converters (BDC) are one of the key elements in electrical energy storage systems. Two main families of BDCs are non-isolated and isolated structures. A review of bidirectional dc-dc converters (IBDC) was presented. The basic structure of these converters along with the terminology used in the literature was described. The advantages and disadvantages of each configuration were briefly stated.
- A three-level non isolated bidirectional dc/dc converter (TLC) is used as the power electronics interface between the battery and the UC, instead of a conventional two-quadrant buck/ boost converter (CBC), which would increase the conversion efficiency and reduce the size of the magnetic components. The three-level converter was analyzed and comprehensively compared with CBC and interleaved bidirectional converter in terms of magnetic component size and efficiency.
- The ultra-capacitor as an energy storage device dedicated for power conversion applications has been discussed. In comparison to state of the art electrochemical batteries, the ultra-capacitors have higher power density, higher efficiency, longer lifetime and greater cycling capability. In comparison to the state of the art electrolytic capacitors, the ultra-capacitors have higher energy density. The ultra-capacitor macro model has been discussed. Depending on the application need, a simplified first order or higher order RC model is proposed. The model can be used to estimate the ultra-capacitor losses and temperature.
- State-of-the-art interface dc-dc converter topologies are explored, and a new three-level dc-dc converter is presented. In addition to providing design principles, the suggested topology is analysed. A new control strategy is suggested together with the development of the model of the full conversion system. Controlling the ultra-capacitor current and dc bus midpoint voltage is the aim of the proposed control technique. Depending on the operating mode, the second control goal is to asymptotically regulate the dc bus voltage to the specified reference. The third control objective is to regulate the state of charge (SOC) of ultra-capacitors.

5.2. Scope of Future Work:

- Analysis of ultra-capacitor based regenerative breaking model for electric vehicle in different operating modes (mains motoring mode,Drive Braking Mode and Motoring Mode from the Ultra-capacitor,Ride-Through Mode)
- The ultra-capacitor lifetime prediction is another aspect to be considered. In certain applications, such as critical industrial processes [10], unexpected interruptions of the system are not allowed. Hence, failures such as end of life of the ultra-capacitor must be predicted and preventive replacement done on time..

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