Ref. No.: Ex/ET/T/415A/2019

B. ETCE 4TH YEAR 1ST SEMESTER EXAMINATION 2019

ELECTRONIC DESIGN AUTOMATION

Time: 3 Hours

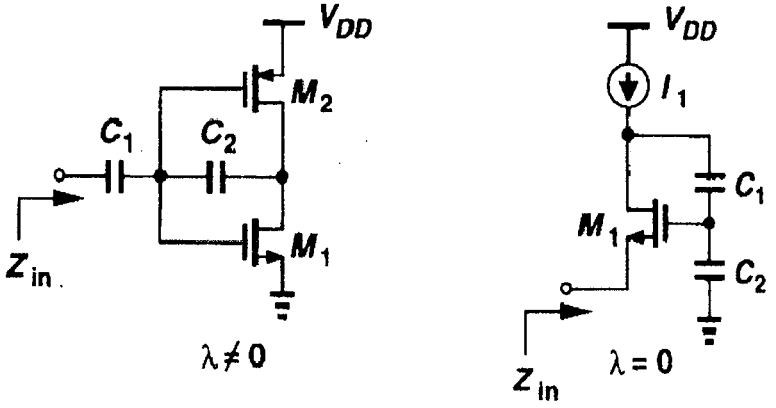
Full Marks: 100

(All parts of the same question must be answered at one place only)

1. **A)** What is different process variation and how it changes characteristics of an IC?
   B) What is parametric yield and variability?
   C) Compare rise time and fall time of two CMOS inverters INV_1 and INV_2 with process corner at snfp and fnsp respectively. [Marks: 10+5+5=20]

2. **A)** Why scaling is important? What is constant field scaling and constant voltage scaling?
   B) Describe the condition of C_{ox} , $I_{D(linear)}$ $I_{D(sat)}$, Power dissipation, Power density, gate delay for both types of scaling. [Marks: (4+6)+10=20]

3. **A)** Describe the operation of MOS capacitor and their behavior in different operating zones.
   B) Calculate the input impedance of the circuits shown in Figure 1. [Marks: 6+(7+7)=20]



4. Design a differential amplifier with active load for differential gain more than 100. Calculate maximum peak to peak differential output voltage swing and power dissipation. (consider 180nm technology and supply voltage 1.8V) [Marks: 20]

5. For the CS amplifier shown in Figure 2 find the high frequency poles due to parasitic capacitances. [Marks: 20]

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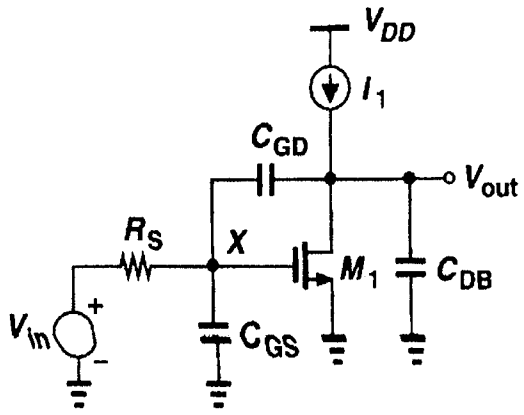
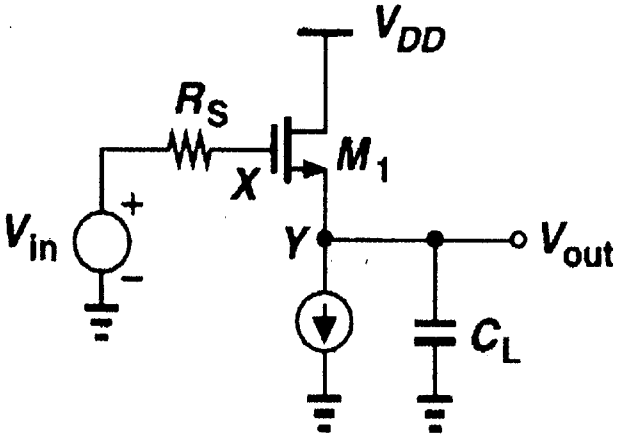


6. **A)** Determine the high frequency gain expression of the source follower shown in Figure 3.
   B) Show that the high frequency output resistance of the source follower amplifier reflects inductive nature if $R_S.g_m > 1$.
   (Consider parasitic capacitances C_{GD}, C_{DB}, C_{GS} along with load capacitance C_L)
   [Marks: 15+5=20]



7. A) What is delta delay in VHDL? How Transport and inertial delays are described?
   B) Write a program of serial adder using structural model. Design the memory using flip flop. [Marks: (4+6)+10=20]

8. A) What is test bench? Write test bench program to verify AND gate.
   B) Write a program of n input AND gate. [Marks: (2+10)+8=20]