Department of Electronics and Telecommunication Engineering, Jadavpur University
B.E. ETCE Fourth year 1st semester Examination 2019.
Attempt all questions and all question carry equal marks. Missing data may be assumed.
Time: Three Hours **Subject: VLSI Design** **Full marks: 100**
Ref.: Ex/ET/T/413/2019

Q1 (a) Explain MOS capacitance in detail. For inverter design, why depletion load n-MOS inverter is preferred?
(b) Prove that the charging of a capacitor C in *n* steps to a voltage Vdd instead of a conventional single-step charging reduces the power dissipation by a factor of *n*. (10+10)

OR

Write notes on the following: -
(i) Skewed logic gates. (ii) GDI logic (iii) Non-threshold logic (NTL) (iv) pseudo NMOS logic. 5x4=20

Q2. (a) In what situation pipelining can be implemented? Explain how pipelining can be used to achieve low power instead of high performance in realizing digital circuits.
(b). Distinguish between constant field and constant voltage feature size scaling? Compare their advantages and disadvantages. (08+12=20)

OR

(a) Describe with necessary diagram i) Basic BiCMOS circuits (ii) Static and switching characteristics of BiCMOS logic circuits (iii) One BiCMOS application
(b) Explain how *parallelism* can be used to achieve low power instead of high performance in realizing digital circuits. 15 + 5=20

Q3 (a) What is glitching power dissipation? How can it be minimized? Explain how the ordering of input signal does affect the dynamic power dissipation on a bus? Illustrate with an example.
(b) Give the justification with proper explanation and diagram if any (related to Low power VLSI) for the following comments:
i) "Dynamic Power Consumption is Data Dependent" ii) "Low Vth for speed critical circuits" 10+10=20

OR

(a) How can you combine sizing and supply voltage scaling to realize low power circuits?
(b) How gray coding helps to reduce power dissipation. Explain with an example
(c) How state encoding can be used to reduce power dissipation in an FSM? Explain with an example. (6+6+8)

Q4. (a) Define the symmetric and asymmetric logic gates with an example. Explain pseudo and Ganges CMOS logic.
(b) Draw the ideal characteristics of a CMOS inverter and compare it with the actual characteristics. What is noise margin? Find out the noise margin from the actual characteristics of the inverter. 10+10=20

OR

(a) Describe the constrains of CMOS logic. Draw and explain the operation of CMOS XOR logic circuit. What is body effect? Explain with one example. Explain why a CMOS Inverter is different from an Inverter when a NAND Gate is converted to that.?
(b) How is a CMOS inverter different from a resistive load inverter? 15+5=20

Q5 (a) Give the structures, impedance diagram along with advantages and disadvantages of pass transistor . Explain the operation of TG –based NOR and NAND Gates using pass transistor Logic with necessary diagrams.
(b) In what way the DRAMs differ from SRAMs? Justify the statement; "there is no short circuit power dissipation in a static CMOS circuit if Vdd< (Vtn+ | Vtp |)" 15+5=20

OR

(a) Define the symmetric and asymmetric logic gates with an example for each. Explain why the input ordering of a logic gate may affect propagation delays.
(b). Explain fan-in and fan-out of logic gates.
(c) Write notes on ESD Protection 10+5+5= 20