B.ETCE 3RD YEAR 2ND SEMESTER EXAMINATION 2019

Subject: IC DESIGN **Time: 3 hours** **Full Marks: 100**

Candidates are required to give their answers in their own words as far as practicable.

GROUP - A
(Multiple Choice Type Questions)

1. Answer any ten of the following questions: $10 \times 1 = 10$

i.) The distance between drain and source diffusion regions is called as
   a. Channel width.
   b. Channel length.
   c. Channel
   d. None of the above

ii.) What is the minimum poly width in layout design rule?
   a. 1λ b. 2λ c. 3λ d. 4λ

iii) What is meant by fan out of a logic gate?
   a. The same amount of cooling required by a gate.
   b. The physical distance between the output pins on device.
   c. Number of other gates that can be connected to gate output.
   d. Number of other gates that can be connected to one of gate output.

iv.)The threshold voltage is defined as
   a. The work function difference between gate and channel.
   b. Gate voltage component to change surface potential.
   c. Gate voltage to offset depletion region charge.
   d. All of above.

v.) CMOS technology is better than bipolar technology because
   a. High noise margin.
   b. Low packing density.
   c. Low input impedence.
   d. None of above.

vi). PLA and PAL are known as:

a) CPLD b) FPGA c) SPLD d) GPLD

vii.). In VHDL process statement is executed when:
a) sensitivity list varies b) sensitivity list remains unchanged
c) both a & b d) none of the above

viii). In VHDL sequential logic is defined in :

a) process b) library c)package d)none of the above

Ix.).Memory of SRAM based FPGA is:
a) Volatile type b) non-volatile type
c) Dynamic type d) none of the above

x.) To store the configuration bits of CPLD :
a) external PROM is required
b) no external PROM is required
c) FPGA is required
d)RAM is required

xi.) In PLA :
a) only AND array is programmable
b) only OR array is programmable
c) both a & b
d) LUT is building block

xii .) FPGA is :

a) full custom ASIC b) semi-custom ASIC
c) Programmable ASIC d) none of the above

GROUP – B

((Long Answer Type Questions)

Answer any six of the following questions **6×15=90**

2. Explain operation of enhancement type n-channel MOSFET and depletion type n-channel MOSFET. Explain about scaling of MOS transistor dimensions- constant field scaling and constant voltage scaling.(5+5+5)

3. Draw the ideal characteristics of a CMOS inverter and compare it with the actual characteristics. What is noise margin? Find out the noise margin from the actual characteristics of the inverter.(2+5+3+5)

4. How MOS can be used as voltage reference? What is switch Capacitor? How to emulate a resistance by using switch capacitor? Describe switch capacitor integrator circuit. (5+2+5+3)

5. What is differential amplifier? Describe CMOS differential amplifier. What are the characteristics of CMOS OPAMP? Describe the structure of CMOS OPAMP. (2+5+3+5)

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6. Draw and explain the FPGA chip architecture. Compare with CPLD. (10+5)

7. Draw the CMOS implementation of 2-to-1 MUX using transmission gates. Design logic circuit using CMOS Pull-up and Pull Down network of the Boolean function. Y= A (B+C)+DE. Explain about the Pass Transistor Logic with examples.(5+5+5)

8. Design HALF–ADDER Circuit and write the VHDL CODE for it in all four model.(5+10)

9. Explain the concept of Domino logic circuit. Design the following Boolean expression Y=ABC+DE by using Domino logic and CMOS PULL UP and PULL DOWN network. Compare the number of MOS used in both the design.(5+10)

10. Explain the concept of static and dynamic CMOS design. Explain with neat diagram the latches using transmission Gate. Explain with neat diagrams the edge triggered flip flop using transmission Gate. (5+5+5)

11. What are the differences between micron rule and MOSIS λ rule? Draw stick diagram of two input NAND gate using proper color code. Draw layout of CMOS Inverter using MOSIS design rule? (5+5+5)

12. What is ASIC? Explain the types of ASIC. Explain the VLSI design flow with a neat diagram. (2+8+5)