B.E. ELECTRONICS AND TELE-COMMUNICATION ENGINEERING
THIRD YEAR FIRST SEMESTER EXAM - 2019

COMPUTER ORGANIZATION AND ARCHITECTURE

Time: 3 hours **Full Marks: 100**

1. Give brief answers to the following questions: **10x2**
   a) State Amdahl's law.
   b) State one advantage and one disadvantage of using MIPS rating as a measure of CPU performance.
   c) Differentiate between *immediate addressing* and *register addressing* with example instructions.
   d) Use a 32-bit binary representation of 3 using a sign extension shortcut of its 16-bit binary representation.
   e) How multiplication is realized in MIPS?
   f) Obtain the single precision binary representation of -0.75.
   g) Why both instruction memory and data memory are used in processor design?
   h) Why single cycle processor design is not favored? Mention one solution for this problem.
   i) Why a memory hierarchy is necessary?
   j) What is a multilevel cache?

2. a) How CPU performance can be unambiguously measured? **2**
   b) Discuss how different factors can affect the CPU performance using the CPU performance equation. **4**
   c) Consider two different implementations P1 and P2 of the same instruction set architecture. The instructions can be divided into four classes according to their CPI (class A, B, C, and D). P1 has a clock rate of 2.5 GHz and CPIs of 1, 2, 3, and 3, and P2 with a clock rate of 3 GHz and CPIs of 2, 2, 2, and 2. Given a program with a dynamic instruction count of 1.0E6 instructions divided into classes as follows: 10% class A, 20% class B, 50% class C, and 20% class D, which implementation is faster? Also, find the global CPI of each implementation. **10**

3. a) Name any four R-type instructions in MIPS. State and explain different MIPS fields used to represent them. **2+4**
   b) Write the corresponding MIPS assembly code for the following C statement: **5**
   B[8] = A[i – j]
   Assume that the variables f, g, h, i, and j are assigned to registers $s0, $s1, $s2, $s3 and $s4, respectively. Assume that the base address of the arrays A and B are in registers $s6 and $s7 respectively.

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c) Write the corresponding MIPS assembly code for the following C function: **5**

```
int my_add (int x, int y, int z)
{
    int sum;
    sum = x + y + z;
    return sum;
}
```

Use appropriate number of argument register(s), return value register(s), saved register(s) and temporary register(s) for optimized performance.

4. Division of 74 by 21 needs to be realized using a simple hardware. Assume both inputs are unsigned 6-bit integers.
   a) Design a simple hardware to realize the above task. **4**
   b) Draw a flowchart to implement the above task using the hardware in a). **4**
   c) Show step-by-step calculation to achieve the above task using the hardware in a) and the flowchart in b). **8**

5. a) State the problem of a ripple carry adder. **2**
   b) Using a first level of abstraction, build a carry-lookahead adder. **4**
   c) Design a 32-bit MIPS ALU which can realize *AND*, *OR*, *add*, *sub* and *slt* operations. **6**
   d) Design the datapath for realizing the *beq* instruction in MIPS. Clearly explain the role of different components in your design. **4**

6. a) Discuss the design principles of a direct mapped cache and a set associative cache. **3 + 3**
   b) Find the miss rate for i) a direct mapped cache, ii) a 2-way set associative cache with least recently used block replacement policy, and iii) a 2-way set associative cache with most recently used block replacement policy for the following sequence of block addresses: 0, 8, 0, 6, 8, 6. **10**

OR

   a) What is a cache miss? **2**
   b) Discuss the impact of memory stalls (due to cache misses) on CPU performance. **4**
   c) For a computer, the cache miss penalty is 100 clock cycles, average miss rate is 2%, and average number of cache misses per 1000 instructions is 30. Assume all instructions ideally take 1.0 clock cycle for completion and there is an average of 1.5 memory references per instruction. Calculate the impacts on CPU time using i) misses per instruction and ii) miss rate and show they are same. Next compare the CPU times with and without a cache. **10**