Ref. No. : Ex/ET/T/315/2019

B.E. ELECTRONICS AND TELE-COMMUNICATION ENGINEERING
THIRD YEAR, FIRST SEMESTER-2019
Subject: IC Technology

Full Marks: 100 **Time: 3 hours**

Answer ALL the three Modules
(All Parts of the same question must be answered at one place only)

MODULE I
(Answer any two questions)

Q1. a. Calculate atomic packing factor for hexagonal closed packed structure. (5)
b. Sketch a cubic unit cell and show the following planes: (3)
(i) (112) (ii) (101) (iii) (123)
c. Describe various types of point defects with diagram in ionic crystals. (4)
d. Describe burger vector; write down the burger vector for face centred crystal (FCC) structure. (2+1)
e. Explain Interstitial and substitution solid solutions with suitable diagram. (5)

Q2. a. What is clean room and what is type of contaminations in clean room? (3)
b. Enlist the steps for obtaining Electronic Grade Silicon (EGS) from sand. (4)
c. Explain Czochralski (CZ) method for silicon crystal growth with suitable diagram. (6)
d. What is Zone refining; show that doping concentration in the crystal at the retreating end (C_s) for float zone process given as $C_s = C_0[1\text{-}1(1\text{-}k_e)^{-k_e x/L}]$, where C_0 is the initial uniform doping concentration in the rod, L is the length of molten zone at a distance x along the rod and k_e is the effective segregation coefficient. (2+5)

Q3. a. Define effective segregation coefficient (k_e) in terms of equilibrium segregation coefficient (k_0). (10)
b. A silicon ingots, which should have 10^{16} boron/cm^3, is to be grown by the CZ process, what concentration of boron atoms should be in the melt to give the required concentration in the ingot. If the initial load of Si in the crucible is 80 Kg, how many grams of boron (Atomic weight = 10.8) should be added. The density of molten Si is 2.53 g/cm^3 (k_0 = 0.8). (6)
c. What is wet chemical etching? Name the common wet chemical etchant used in integrated circuit fabrication with their composition for Si, SiO_2 and Si_3N_4 etching. (4)

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MODULE II
(Answer any two questions)

Q4.a Show the Deal-Grove kinetic equation for oxidation of silicon is $x^2+Ax= B(t+\tau)$ and show that it reduces to $x^2 = Bt$ for long times and to $x = B/A\ (t+ \tau)$ for short times duration. (12)

b. What is field aided diffusion? (4)

c. Draw the practical diffusion profile of phosphorus (P) in Si. (4)

Q5. a. Explain graphically predeposition and drive in steps in diffusion process. (8)

b. Give an example of (i) solid source (ii) liquid source (iii) gaseous source of Boron (B) diffusion in Si. (3)

c. Explain Ion channelling with an example. (4)

d. What are the pros and cons of ion implantation vs. diffusion? (5)

Q6. a. Describe e-beam lithography technique with the schematic diagram and what are its advantages over photolithography? (5+3+2)

b. Define "dose" in ion-implantation technique, explain how ions are selected in an ion implanter system. (1+3)

c. Explain the difference between contact, proximity and projection printing. (6)

Q7. a. Explain electromigration in relation to Al metallization. (5)

b. Describe DC sputtering technique with suitable diagram and explain why RF is needed to deposit insulators using sputtering? (6+4)

c. What are the typical reactions involved in depositing (i) SiO_2 and (ii) Si_3N_4 via plasma-enhanced chemical vapor deposition (PECVD) method. (3)

d. Why silicides preferred in multilevel interconnects? (2)

MODULE III

Q8. a. With the help of IC process flow diagram, show the process sequence for forming a deep and narrow trench isolation structure. (6)

b. Draw the doping profile for n-p-n transistor. (4)

c. Describe briefly, the IC processing steps for fabrication of the complementary metal-oxide-semiconductor (CMOS) using twin well process. (10)