BACHELOR OF ETCE EXAMINATION, 2019
(2^{nd} yr, 1^{st} Semester)

DIGITAL LOGIC CIRCUITS

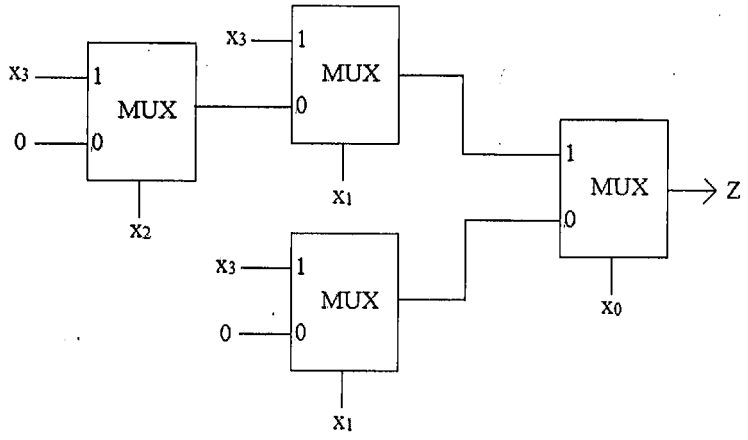
Time : Three Hours | Full Marks : 100

Answer any ***five*** questions.

1. a) A lift door control is to operate in the following manner. When the lift stops at a floor the door will open and a signal is generated that remains on until all the passengers are on or off the lift. An additional signal is also generated to ensure that the doors do not close on a passenger in the doorway. Doors will close if a call button has been pressed on another floor or if a lift passenger has pressed a button for another floor. Set up a truth table for the design of the lift control and derive the corresponding logic equation. 10

b) The majority function M(x, y, z) is equal to 1 when two or three of its arguments equal to 1, i.e.
$M(x, y, z) = xy + xz + yz = (x+y) . (x+z) . (y+z)$
Show that
$M[a, b, M(c, d, e)] = M[M(a, b, c), d, M(a, b, e)]$ 10

2. a) Analyze the MUX network shown below and find out the expression for Z



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b) Obtain the Reed-Muller representation of the following function.

$F(x1, x2, x3) = \Sigma (3, 5, 7)$ 4

c) Design a 4-bit parity checker/generator circuit with appropriate cascading facilities using gates. Your circuit should work like a 4-bit version of an 8-bit 74180 IC. 10

3. a) Design a priority encoder with four active high inputs p_0, p_1, p_2 and p_3 and three active outputs, A and B indicating the number of the highest priority device requesting service, and N, indicating no active requests. Input p_0 is the highest priority line and p_3 the lowest. 10

b) Construct the truth table of a Full Adder. Design a Full Adder using two Half Adders and other SSI gates. Further, design a circuit to add two 4-bit numbers using these Full Adder blocks. 3+4+3

4. a) Simplify the following function using Quine McCluskey procedure. 10

$f(A, B, C, D) = \Sigma (0, 2, 3, 5, 8, 10, 11, 13)$

b) Draw the circuit diagram of a 3-bit R-2R ladder type DAC and explain its operation. Mention advantages of the circuit. Assume that the input is provided by a 3-bit counter and hence draw the corresponding output waveform. 10

5. a) Draw the circuit diagram of a mod-6 switch tail ring counter using JK flip-flops. Obtain its decoding logic. Modify this circuit to obtain a modulus of 5 and validate it through the timing analysis of the circuit. 5+5

b) Design a circuit using 74164 ICs and SSI gates to produce a series of four pulses repetitively every 70 μs. The pulses are to be HIGH during the following times:

A: 0 - 20 μs, B: 15 - 45 μs, C: 35 - 60 μs, D: 55-70 μs 10

6. a) A set dominate flip-flop has a set and reset input. It differs from a conventional SR flip-flop in that an attempt to simultaneously set and reset results in setting the flip-flop. Obtain (a) the characteristic table, (b) the characteristic equation, (c) the excitation table and (d) the state diagram. 3+2+2+3

b) Design a 3-bit controlled register with LOAD and SHR control lines. Assume that the LOAD line has the higher priority. Explain the loading and shifting operations with the help of suitable examples. 10

7. a) Design a mod-6 synchronous up counter using JK flip-flops. Avoid lockout. Draw the timing waveform and hence the state diagram of the resulting counter. 10

b) Design mod-6 ripple counters using
i) JK flip-flops with active low CLR lines,
ii) JK flip-flops with active low PRESET lines,
iii) 7490 IC.
You may use additional SSI gates, if necessary. 3+4+3

8. a) Design a sequence detector to detect a sequence 0101. Assume overlapping sequence and use D flip-flops to implement the sequence detector. 10

b) Draw the block diagram of a successive approximation type of ADC and explain its operation. Compare its performance with that of a counter type ADC. Identify important signals for interfacing an ADC with a microprocessor. 10