B.E. ELECTRONICS AND TELE-COMMUNICATION ENGINEERING

2ND YEAR 1ST SEMESTER EXAM, 2019

ANALOG CIRCUITS- I **Time: Three hours** **Full Marks: 100**

Use a separate Answer-Script for each Part

PART-I (50 MARKS)

Answer ***Q.1***, any ***one*** from ***2 and 3*** and any ***one*** from ***4 and 5***

1. a) Explain the function of R_G, R_{S1} and R_{S2} in Fig. 1. Determine the Q-point and show it on load line. How will the Q point be changed if R_{S2} is replaced by 220 Ω. Given that V_S= 2 V. [4+4+2]

   b) Draw the small signal equivalent circuit of Fig. 1. Calculate maximum ac voltage gain, input resistance and output resistance. [10]

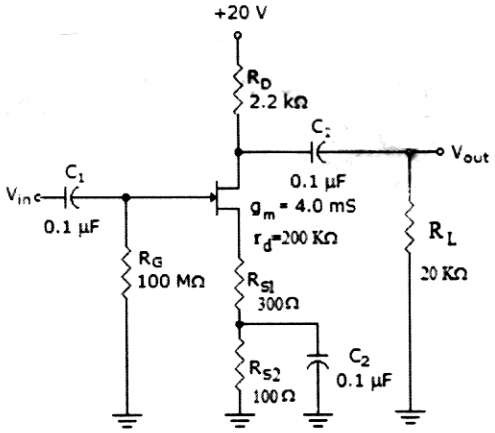


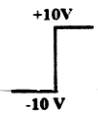
Figure 1

2. a) Explain the function of external capacitances in IC voltage regulators. Explain short circuit protection in series voltage regulator circuit. [2+3]

   b) Why negative feedback is important in wide range of OP-AMP applications. [3]

   c) Define input offset voltage and slew rate and explain their origin. [5]

   d) For a step input the output of op-amp appears after 1μs. calculate its slew rate. Vin= [2]



3. a) Design a voltage regulator using LM317 to obtain regulated voltage of 10 V. [5]

   b) Explain difference mode and common mode operation of differential amplifier using BJT. Find the expression for voltage gain, input resistance and output resistance for both cases. [5+5]

4. a) Explain the effect of noise in comparator circuits. [4]

   b) Calculate output voltage in Fig. 2. [6]

   c) Explain the temperature measurement using instrumentation amplifier [10]

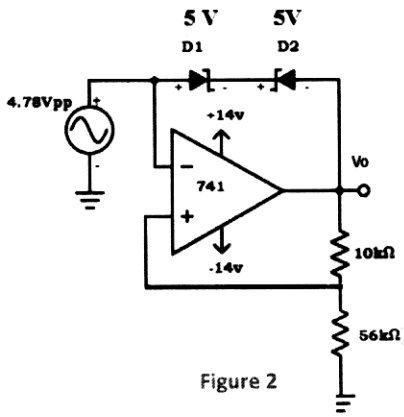


Figure 2

5. a) Explain the function of all pass filter with circuit diagram and mention its use. [6+2]

   b) Design a all pass filter to obtain a phase shift of 90° [4]

   c) Draw and explain frequency response of practical integrator circuit. [8]

PART- II

Section A : Answer any TWO

1. **Explain** the working principle of a Full Wave Voltage Multiplier with proper circuit diagram. **Plot** the initial voltage across both the capacitors and the overall output voltage for a sinusoidal input *(assume ideal diode and capacitors are uncharged initially).*

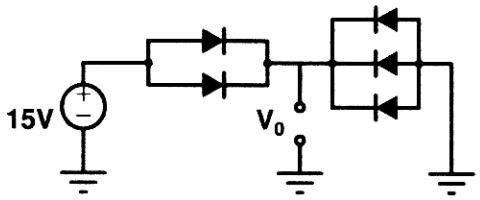
[Marks: 4+6=10]

2. A full wave transformer coupled rectifier with $R_L = 20k\Omega$ is implemented using ideal diodes. Find the value of $\mathbf{V_{dc}}$,$\mathbf{V_{rms}}$ and $\mathbf{V_{rrms}}$ (ripple rms). **Design** one capacitive filter (*find the value of the capacitor*) to reduce the peak to peak ripple voltage across load within 1% of DC output.

[Marks: 6+4=10]

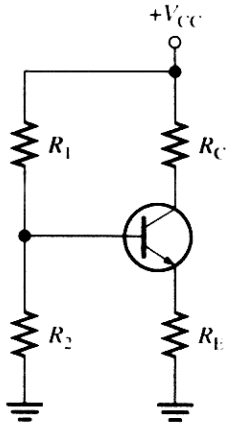
3. Find the output voltage $\mathbf{V_0}$ of the diode circuit shown in Figure 1 and **plot** the output voltage for a temperature range 0 to 100°C. [*All diodes are real and identical*]

[Marks: 6+4=10]



Section B : Compulsory

4. **Determine** the expression of stability factor **S(Ico)** for a BJT in Emitter Bias configuration. **Calculate** the value of **S(Ico)** of the voltage divider circuit shown in Figure 2. [$\beta = 100$, $R_1 = 60k\Omega$, $R_2 = 30k\Omega$, $R_E = 3k\Omega$, $R_C = 1k\Omega$, and $V_{CC} = 12V$] [Marks: 5+5=10]



Section C : Answer any TWO

5. **Explain** the working principle of a current mirror circuit. **Design** one current mirror with 1μA current in primary branch and 2μA and 2.5μA in two different secondary branches. *(Available transistors are identical with β=1000 and V_{BE} =0.7V. Supply voltage 3V)* [Marks: 4+6=10]

6. A CE amplifier with proper biasing arrangement is shown in Figure 3. [β= 100, $C_E = C_C = C_B = 1\,\mu F$ *and neglect* r_o]
   A) **Draw** the small signal model of the entire amplifier and **calculate** the midband gain.
   B) **Find** all the low frequency poles, zeros and lower cut-off frequency due to coupling capacitors.
   C) **Plot** the gain response with respect to frequency for very low to mid frequency range.
   [Marks: 5+3+2=10]

7. Using the high frequency model of BJT find the expression of **β(s)**, **ω_β** and **ω_T**.
   Calculate the value of ω_β and ω_T for the BJT shown in figure 3. [use β= 100, $C_\pi = 12pF$, $C_C = 2pF$]
   [Marks: 6+4=10]