SUBTHRESHOLD ANALYSIS OF NEGATIVE CAPACITANCE FIELD EFFECT TRANSISTORS FOR DIFFERENT FERROELECTRIC MATERIALS

Thesis Submitted to the Department of Electronics and Telecommunication Engineering in partial fulfilment of the requirements for the degree of

MASTER OF ENGINEERING ELECTRONICS AND TELE-COMMUNICATION ENGINEERING

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May, 2019

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Certificate of Recommendation

This is to certify that **Neha Kapoor (Exam Roll No M4ETC19012, Registration No 140696 of 2017-2018)** has satisfactorily completed the thesis entitled " **SUBTHRESHOLD ANALYSIS OF NEGATIVE CAPACITANCE FIELD EFFECT TRANSISTORS FOR DIFFERENT FERROELECTRIC MATERIALS"**, under the guidance of **Dr. Chandrima Mondal**, Department of Electronics and Telecommunication Engineering, Jadavpur University. We recommend that her dissertation is fully adequate in scope and quality for the partial fulfilment of the requirement for the degree of **MASTER OF ENGINEERING ELECTRONICS AND TELE-COMMUNICATION ENGINEERING** in the Department of Electronics and Telecommunication Engineering, Jadavpur University, Kolkata-700032.

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The foregoing thesis titled "**SUBTHRESHOLD ANALYSIS OF NEGATIVE CAPACITANCE FIELD EFFECT TRANSISTORS FOR DIFFERENT FERROELECTRIC MATERIALS"** is hereby approved as a creditable study of **MASTER OF ENGINEERING ELECTRONICS AND TELE-COMMUNICATION ENGINEERING** in Department of Electronics and Telecommunication Engineering and presented in a manner satisfactory to warrant its acceptance as a prerequisite to the degree for which it has been submitted. It is understood that by this approval the undersigned do not necessarily endorse or approve any statement made, opinion expressed or conclusion therein but approve this thesis only for the purpose for which it is submitted.

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ACKNOWLEDGEMENT

It is a pleasant task to express my gratitude to all those who have accompanied and helped me in my project work.
First and foremost, I really take this opportunity to express my deep sense of gratitude to my guide, ***Dr. Chandrima Mondal***, Department of Electronics and Telecommunication Engineering, Jadavpur University, Kolkata, for her invaluable guidance, suggestions and encouragement throughout the project, which helped me a lot to improve this project work. It has been very nice to be under her guidance. Her appreciation during the good times has been boosting my morals and confidence.
I am also indebted to ***Prof. Sheli Sinha Chaudhuri*****,** the Head, Department of Electronics and Telecommunication Engineering, Jadavpur University, for her kind help during this project work.
My heart-felt thanks also goes to all my family members for their love and encouragement, without which, the work would not have been possible.
Last, but not the least, I would like to thank my batch-mates who have directly or indirectly helped me in this work.

ABSTRACT

MOSFET current voltage characteristics is dependent on the potential barrier present between source and the channel. This barrier is controlled by the voltage applied at the gate. The number of carriers (governed by the Boltzmann statistics) that cross the barrier specifies that to rise the I by a decade, 60 mV of rise in voltage is minimum requirement. This has put an important block in downscaling of voltage. Hence, we are not able to optimize the power requirement.

S. Salahuddin and S. Dutta of *Purdue University* came out with the concept of adding a ferroelectric material in MOSFET. The material shall be added at the gate stack and this will help in amplification of the voltage applied at the gate. This allows us to operate at lower voltage and hence less power consumption as well. Moreover, the subthreshold swing is also found to improve.

In this thesis, a simple mathematical model-based study of NCFET devices has been made. Study is carried out to know how the device react to the changes in the ferroelectric material. At first, a compact mathematical model-based method to study device features is taken. In the results we will see that the developed model of NCFET, the subthreshold swing of such devices improves. Further properties like drain induced barrier rising are observed to improve as well.

Using the compact model developed, the NCFET has been analysed for two different ferroelectric materials and with its varying thickness.

Scaling has been performed to see the performance of NC devices in future technologies. This analysis demonstrations that NC devices are more advantageous in overpowering short channel effects like DIBL and thus helps in scaling down of devices.

CONTENTS

CHAPTER 1

INTRODUCTION

Before introducing negative capacitance Field Effect Transistor (NCFET), let us known a little about conventional Metal Oxide Semiconductor Field effect transistor, MOSFET and its limitation.

1.1. MOSFET

In 1926, a patent was filed by Julius Edgar Lilienfeld[1], "Method and Apparatus for Controlling Electric Currents," in which he anticipated a 3-electrode assemblyby means of copper-sulphide semiconductor material. Now this is well known as field-effect transistor, and also later he proposed the idea of the depletion-mode MOSFET [2]. The idea of the inversion-mode MOSFET was proposed, seven years later, by Reil [3]. In 1960 first MOSFET was fabricated by Kahng and Atalla [4]. We observe that there was a huge time gap between the emergence of the idea and the fabrication. This was due to the absence of a stable oxide and the lack of information on semiconductors. For example, the idea of a "hole," developed by Wilson in 1931 [5], was used in 1941 by Ohl [6]. Brattain [8] developed a good field effect device and first talked about transistor effect. Shockley defined in [9] discovery of transistor. They used Silicon instead of Ge. The reason for this was that Atalla had shown that a high-quality Si/SiO_2 interface could be obtained using his oxidation process. This high-quality Si/SiO_2 interface was extremely important, since it constitutes the heart of the MOSFET. In contrast, the oxide of germanium is soluble in water and its interface with germanium often contains plenty of defects. Due to the availability of stable oxide, Silicon became the leading semiconductor.

1.2. THE HAPPY DAYS OF SCALING (1960–2000)

In 1965, it was observed by Moore that the number of transistors increases by two times in every two year. This empirical law has indeed been the driving force behind the semiconductor industry for many decades. Throughout this period, the architecture and working principle of the MOSFET have essentially not been changed. The continuous scaling of its physical dimensions has delivered improved performance and lower cost at every single technology generation.
Until 2000, this evolution has driven the growing computing power of the PC and ever-increasing functionalities (more data storage, performing games, internet access, etc.).

1.3. MOTIVATION FOR NCFET

FETs at Room Temperature require the potential at the g to change by minimum of 60 mV to get the current at the drain to increase by ten times. This minimum sub-threshold slope forces

anessential lower boundary on the allowable voltage and also on the dissipation in the switching action using FET.

Due to the difficulty in removing this heat dissipated in the switching process, the scaling down of FET will be limited [15-18]. Thus, to enjoy the advantages of scaling, it is needed to come up with new ideas on the ways to reduce power dissipation.

As the power dissipation is proportional to the square of voltage, hence reduction in the voltage helps in reduction in the power dissipation. A limit to the operating voltage is posed by the sub-threshold swing *S*, which is given by the reverse of the change of current that we can get for a unit change in gate voltage, *V*g:

$$S = \frac{\partial Vg}{\partial(\log_{10} I)} = \frac{\partial Vg}{\partial \psi s}\frac{\partial \psi s}{\partial(log_{10} I)} \quad \text{.....(1)}$$

The variation in drain current to the variation in the surface potentialψ_s in the channel can be a minimum of 60mV at room temperature. In FET, gate voltage *V*g and surface potential ψscan be related by a capacitive voltage divider, thus the 1st term in eq(1) can be given as

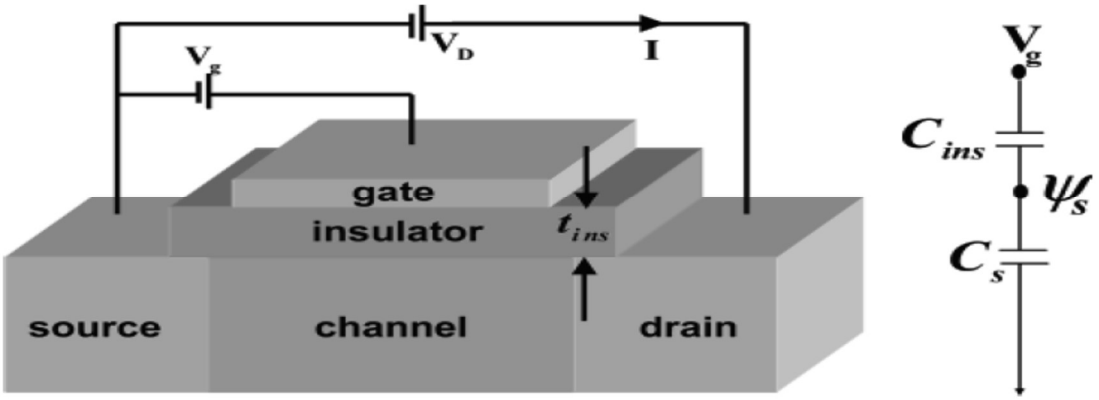


Figure 1: a simple n channel MOSFET and its capacitive model

$$\frac{\partial Vg}{\partial \psi s} = 1 + \frac{Cs}{Cins} \quad \text{.....(2)}$$

This is called body factor(m).

From the equation it is clear that m should begreater than one. This puts a limit of 60mV/decade(m=1 condition) on the S given in (1).This is true even for high k(dielctric constant) materials [19].Even large values of C_{ins} can only be used to make the body factor 1 but not lower than that.

1.4. NEGATIVE CAPACITANCE IN MOSFET

It has been studied that if we add a ferroelectric material in the gate stack of FET, we can obtain an amplification. Thus, $\frac{\partial Vg}{\partial \psi s} < 1$ can be obtainedand value of subthreshold swing lower than 60 mV/decade can be obtained. This unique feature is obtained due to the unique P vs E characteristics of FE, that shows a negative slope at the origin.

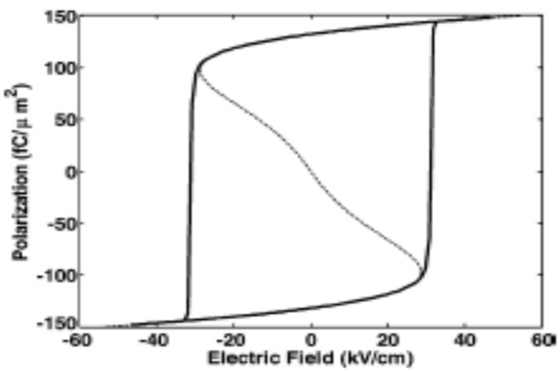


Figure 2: polarization vs electric field of any ferroelectric material

This FET is termed as Negative Capacitance FET. Due to the ability of internal voltage gain (Av) and getting a steep slope, it has gained substantial interest for ultra-low power applications. Very thin body structure is suggested for getting more internal amplification and steeper slope in the subthreshold region. 2D semiconductor TMD (transition-metal-dichalcogenides) is a suitable channel material. This is due to their atomically thin thickness, untouched surface, and acceptable bandgap. Thus, TMD materials like MoS_2 is a suitable channel material for NCFET.Sub-2.3 kT/q swing in a TMD NCFET has recently been experimentally demonstrated.

Experiments exhibiting hysteresis jumps in polarization are not stable at the negative capacitance region of the FE material. This unstable capacitance can be stabilized by introduction of a series positive capacitance. This further helps ingetting the channel potential Ψs to change more than the voltage Vg applied at the gate terminal. It thus provides a voltage amplifier or to be specific a step-up voltage transformer. The concept of negative capacitance arises from the positive feedback. This is shown in FE material. Similar features can be obtained also through other microscopic mechanism.

Positive feedback can be used to explain NCFET [20]as follows. Let us assume, we have a (positive) capacitor C_0 (per unit area) with a terminal voltage equal to the applied voltage V plus a feedback voltage $\alpha_f Q$that isproportional to charge Q (per unit area) on the capacitor,

$Q=C_0 (V + \alpha_f Q)$ ……………………………………………………………………………(3)

This yields Q=CinsV where

$$Cins = \frac{Co}{1-\alpha f}\dots\dots(4)$$

Certainly, with α_f Co >1 we have a negative capacitance that in general is unstablethus leading toincrease in charge tillcontrolled by the non-linear terms that had been avoided so far. If we stabilize the negative capacitor by putting an ordinary capacitor *C*s (semiconductor capacitor) in series such that the overall capacitance $[C_s^{-1} + C_{ins}^{-1}]^{-1}$ is positive, then it follows from equations that the body factor canbe made small showing that the NC can be applied as a step-up voltage transformer. This transformer canamplify the applied potential *V*g to channel/ surface potential of Ψs**.** As long as, $Ceq^{-1} = Cs^{-1} + Cins^{-1}$ remains positive, the composite ferroelectric- semiconductor system will behave like a normal positive capacitor and *C*eq (equivalent capacitance) will be larger than both *C*s and *C*ins(insulator capacitance). Thus, the dissipated energy in switching event for the equivalent capacitor will be much less than the individual capacitors.

Thus the linear capacitor can be replaced by capacitor $Q=C_0 (V + \alpha_f Q)$ with a nonlinear capacitance function $Q=F(V + \alpha_f Q)$, so that

$$V= F^{-1} (Q) - \alpha_f Q \dots\dots(5)$$

The function F^{-1} is odd, expanding it to the fifth power to write

$$V = \alpha_0 Q + \beta_0 Q^3 + \gamma_0 Q^5 + \rho_0 \frac{dQ}{dt}\dots\dots(6)$$

The first term being the inverse linear capacitance 1/*C*o.

A resistive drop *is* added which is proportional to the$\frac{dQ}{dt}$. Further the parameter α_0 equals $(1/C_0)$ - α_f and is negative provided we are operating in the negative capacitance region where $\alpha_f C_0 > 1$.

We illustrated the positive feedback approach of the NCFET. But same equations can also be derived from the dynamics of ferroelectric capacitors given by the Landau- Khalatnikov(LK) equations[21-23]

$$\rho \frac{dP}{dt} + \nabla_p U = 0\dots\dots(7)$$

Where,

$$U = \alpha P^2 + \beta P^3 + \gamma Q P^5 - E_{ext} P\dots\dots(8)$$

U is the Gibb's free energy which is given by the addition of the anisotropy energy and the external field energy E_{ext}, and the polarization charge per unit area is represented by P. From equations

$$E_{ext} = 2\alpha P + 4\beta P^3 + 6\gamma P^5 + \rho \frac{dP}{dt}\dots\dots(9)$$

If Q=P and V=E_{ext}*T_{ins} where T_{ins} is the thickness of the insulator, we get $\alpha_0=2\alpha T_{ins}$ and $\beta_0=4\beta T_{ins}$ and $\gamma_0=6\gamma T_{ins}$ and $p_0=pT_{ins}$ in our equations.

Now replacing the insulator with a FE one. The gate circuit can now be represented as a series combination of the FE capacitor and semiconductor capacitor*C*s, channel-to-source and channel-to-drain capacitors. A voltage *Ψs (surface potential)* appears across *semiconductor capacitor*, while *V*g - Ψs appears across the FE capacitor. As both capacitors are in series so they have same charge. Thus, we can write

$$\psi_s = \frac{Q}{C_s} \quad \text{.....(10)}$$

$$Vg - \psi_s \approx \alpha_0 Q + \beta_0 Q^3 + \gamma_0 Q^5 + \rho_0 \frac{dQ}{dt} \quad \text{.....(11)}$$

Thus, we get

$$\tau \frac{d\psi_s}{dt} + (1 + a_1)\psi_s + a_2 {\psi_s}^3 + a_3 {\psi_s}^5 = V_g \quad \text{.....(12)}$$

Where

$$\tau = \rho C_s t_{ins}, \quad a_1 = 2\alpha C_s t_{ins}, \qquad a_2 = 4\beta {C_s}^3 t_{ins}, \qquad a_3 = 6\gamma {C_s}^5 t_{ins}$$

By setting d*Ψ*s/d*t*= 0 we can obtain the steady state *Ψ*s versus *V*g.This relation depends on the material.If a1 is more than both a2 and a3 thanΨs and *V*g is essentially linear.

$$\frac{\partial V_g}{\partial \psi_s} \approx 1 + a_1 \quad \text{.....(13)}$$

This mimics the earlier obtained results. Even, when a2 and a3 are significant, (1 + *a*1) represents the slope close to the origin Ψs = 0, *V*g = 0. This slope must be greater than 0if origin is to be made a stable operating point. Thus, it puts a limit to the thickness of the insulator.

$$t_{ins} \leq \frac{1}{2\alpha C_s} \equiv t_c \quad \text{.....(14)}$$

Tc is the critical thickness.

1.5. SCOPE OF WORK

In this thesis, a simple mathematical model-based study of NCFET devices has been made. Study is carried out to know how the device react to the changes in the ferroelectric material. At first, a compact mathematical model-based method to study device features is taken. In the results we will see that the developed model of NCFET, the subthreshold swing of such devices improves. Further properties like drain induced barrier rising are observed to improve as well.

Using the compact model developed, the NCFET has been analysed for two different ferroelectric materials and with its varying thickness.

Scaling has been performed to see the performance of NC devices in future technologies. This analysis demonstrations that NC devices are more advantageous in overpowering short channel effects like DIBL and thus helps in scaling down of devices.

Next in chapter 2 literature survey is presented. In Chapter 3 the device structure and the model has been described. Chapter 4 involves the results and discussion of the simulation done in MATLAB for the described model. In Chapter 5, Conclusion and future work is presented. Finally, references are provided.

CHAPTER 2

LITERATURE SURVEY

In this chapter, the latest findings of negative capacitance FETs is presented. We begin with a review of development of the idea of the NCFETs, and their future prospects in a theoretical perspective. Then we look at various experimental realizations of negative capacitance MOSFETs. Finally, we discuss the latest developments made in modeling of NCFETs.

2.1. DEVELOPMENT AND PROSPECTS OF NCFETS

Datta and Salahuddin [24] proposed the idea of negative capacitance MOSFETs to achieve SS < 60 mV/dec, wherein a ferroelectric insulator is used as gate oxide and provides step up voltage transformation.

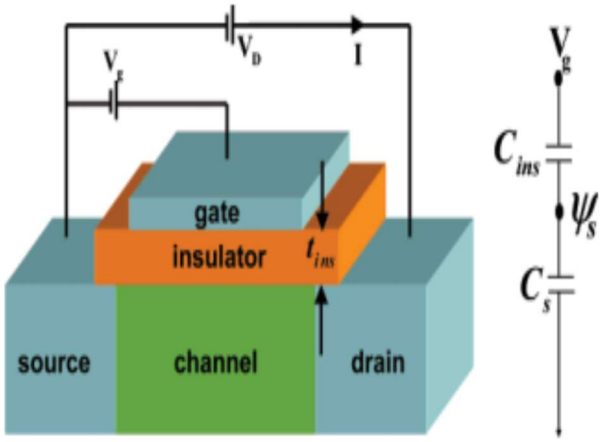


figure 3: a cross section area of a metal oxide semiconductor field effect transistor (MOSFET)

Further they argued that for the system to stable in its totality the capacitance of the system should be positive. This poses a fundamental limit on the maximum thickness of the ferroelectric for hysteresis free operation given by

$$t_{FE} = \frac{1}{2\alpha C_s} \quad \text{.....(15)}$$

where α is the material property of the ferroelectric and C_S is the semiconductor capacitance.

In [25] design guidelines for designing NCFETs are given. They showed that for stableoperation, the total capacitance of the system should be positive, and hence

$$C_S^{-1}(Q) > C_{ins}^{-1}(Q)$$ ……..(16)

throughout the region of operation of the device. Further for minimum coupling factor m, C_S and ferroelectric capacitance -Cins should be as close as possible.

For ferroelectric FET operating in stable region, they showed that the minimum subthreshold swing is given by

$$SS_{min} = \frac{2.3k_BT}{q}\left(1 + \frac{M}{y_0}\right)$$ ……(17)

where

$$M = (2\phi_t(\alpha Q_{C1} + \beta Q_{C1}^3 + \gamma Q_{C1}^5)/(2\alpha^2 Q_{C1}^2),$$

$$y_0 = \sqrt{\frac{4\phi_f\phi_t}{\alpha^2 Q_{C1}^2}}$$ and QC1 is the solution ofthe equation

$$5\gamma Q_C^4 + 3\beta Q_C^2 + \alpha = 0.$$

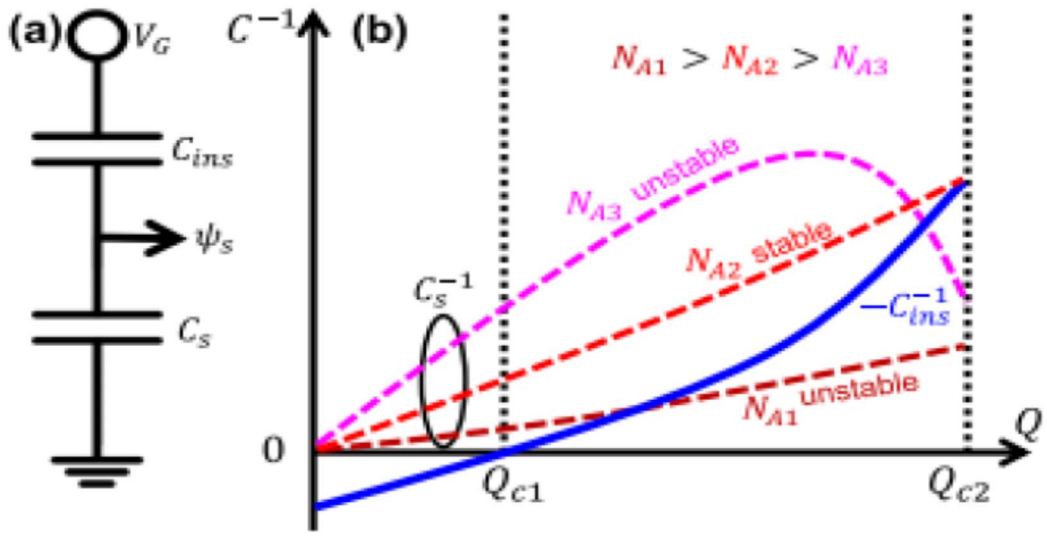


Figure 4(a) capacitive model of fet (b) stability analysis of fet for different doping concentration

Other implementations of NCFETs have been discussed in [26,27]. In particular the nano electromechanical switch (NEMS) with suspended gate can also provide the negative capacitance effect. Asthe suspended gate is charged, it is attracted towards the MOSFET and consequently the voltageacross it decreases. The NEMS

switch can be then used in series with the ferroelectric capacitor toprovide an ideal logic switch with SS = 0 mV/dec

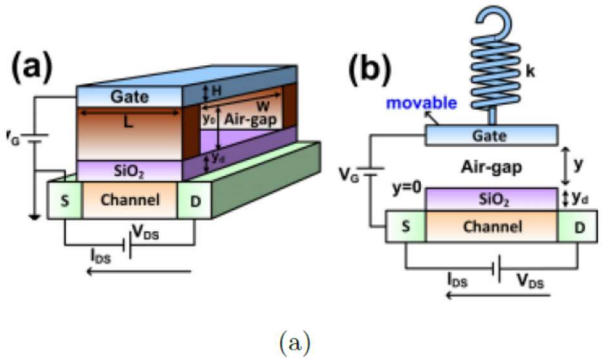


figure 5: suspended gate and ideal logic switch (a) a suspended gate ncmos with a nano mechanical spring (b) sg technology can be used in series with ferroelectric insulator to provide an ideal logic switch by providing a dual energy landscape [26,27]

2.2. EXPERIMENTAL EVIDENCE OF NCFETS

Experimental evidence of NC mechanism has been first provided by A.I.Khan and Salahuddin [28].In this experiment they connected a ferroelectric capacitor in series with a high resistor. The flow ofscreening charges from battery is then hindered by the resistance and a transient negative capacitanceis observed, where in the charge across the ferroelectric decreases even though the voltage across itincreases.

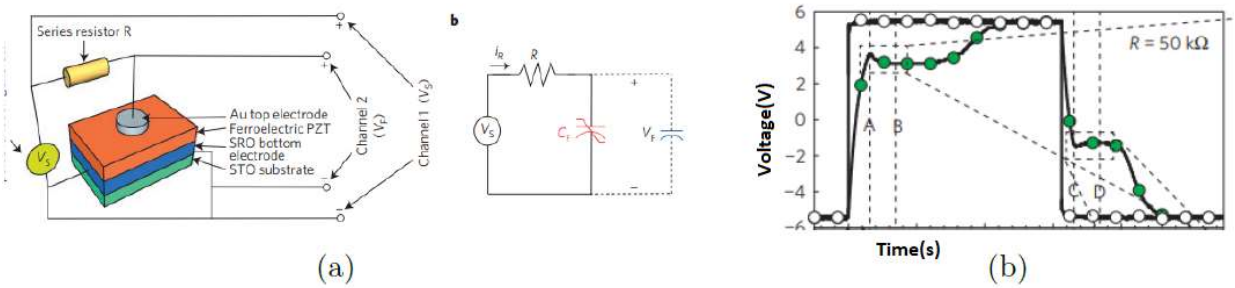


figure 6: experimental evidence of NCFETs (a) experimental setup (b) output obtained while switching

Experimental evidence of FE-FinFETs have been discussed in [29]. In particular in 1.5 nmthickness HZO (HalfniumZincronium Oxide) was used to achieve a subthreshold swing of about 52mV/dec.

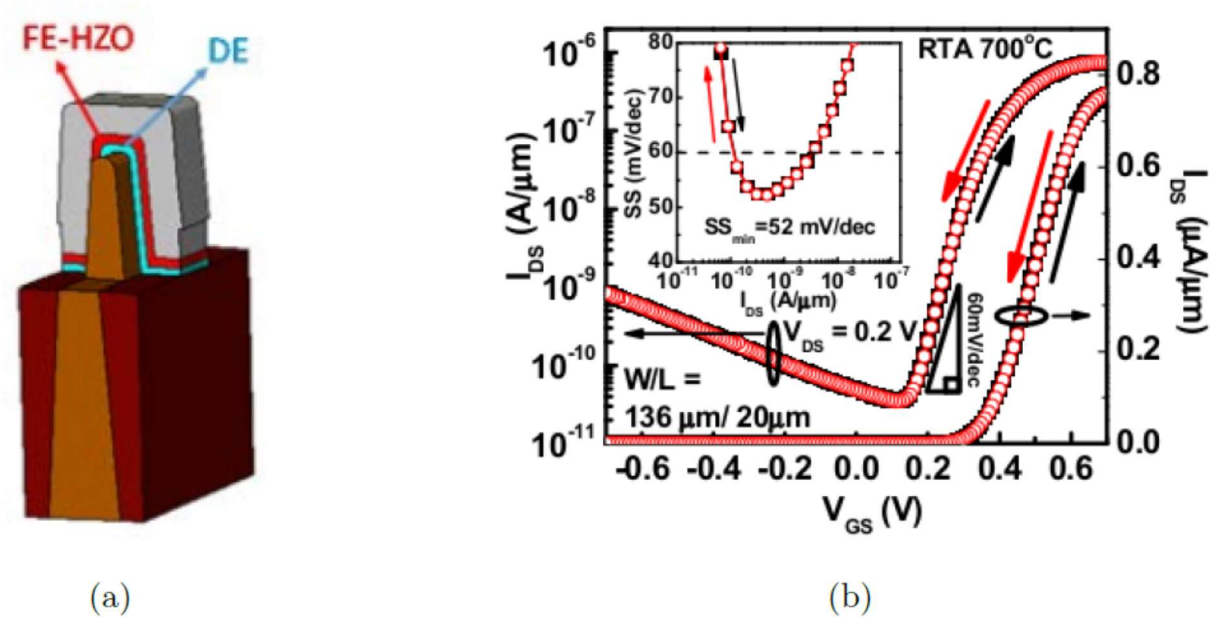


Figure 7: experimental evidence of fe-FinFET (a) structure of the device (b) current voltage characteristics

2.3. MODELING NCFETS

The basic methodology to model the performance of NCFETs has been including an additionalinsulating layer governed by Landau Khaltnikov equation,

$$V_{FE} = 2\alpha Q + 4\beta Q^3 + 6\gamma Q^5 \quad \text{……..(18)}$$

and then solve the MOS equation

$$V_G = V_{FE} + \psi_s + \psi_{ox} + V_{FB} \quad \text{……..(19)}$$

self consistently. If the ferroelectric is connected through a metal, Eq. 19 is homogeneous throughoutthe length of the ferroelectric and can be solved easily. However, if the ferroelectric is connecteddirectly to the dielectric insulator, Eq. 19 has to be solved at each point along the length of theferroelectric self consistently as is done in [30].

A compact model compatible with BSIM-CMG model has been proposed in [31]. In this workthe core BSIM-CMG model is extended by an additional term. This model can also be used without lumped metal by solving the equation selfconsistently at n points along the channel.

The non-ideal phenomena of leakage through the ferroelectric has been studied in [32]. Theleakage is modeled as resistor parallel to ferroelectric capacitor. The resistor provides an additionalpath to provide screening charges to ferroelectric degrading its performance. A solution is alsoprovided by changing the metal work functions

appropriately. With appropriate work functionselection, the point where ferroelectrics go into negative capacitance regime is decreased. This alsoreduces the leakage, as leakage has been modeled as a resistance (I = V/R).

Multidomain nature of ferroelectrics is taken into account in [33] where NEGF formalism hasbeen used to get the device characteristics. An additional term of

$$\kappa\left(\frac{dP_z}{dx}\right)^2 \quad \text{.....(20)}$$

has to be added to Eq. to account for variation in polarization in ferroelectric. This gives us an equation of state

$$E_Z = \alpha P + \beta P^3 + \gamma P^5 - k\frac{\partial^2 P_Z}{\partial x^2} \quad \text{.....(21)}$$

The k factor is shown to provide a coupling between the polarization in different regions of ferro-electric. Higher values of k are shown to make the ferroelectric polarization more uniform and even the MFIS structure tends to become MFMIS structure.

2.4. GETTING SS LOWER THAN 60 [40]

In this work, it has been experimentally demonstratedthat integrating a thin FE layer into the gate stack of a standard MOS transistor, we can get a SS lower than 60 mV/decade. It was obtained as low as 13mV/decade in Fe-FETs with 40nm P(VDFTrFE)/ SiO2 gate stack.

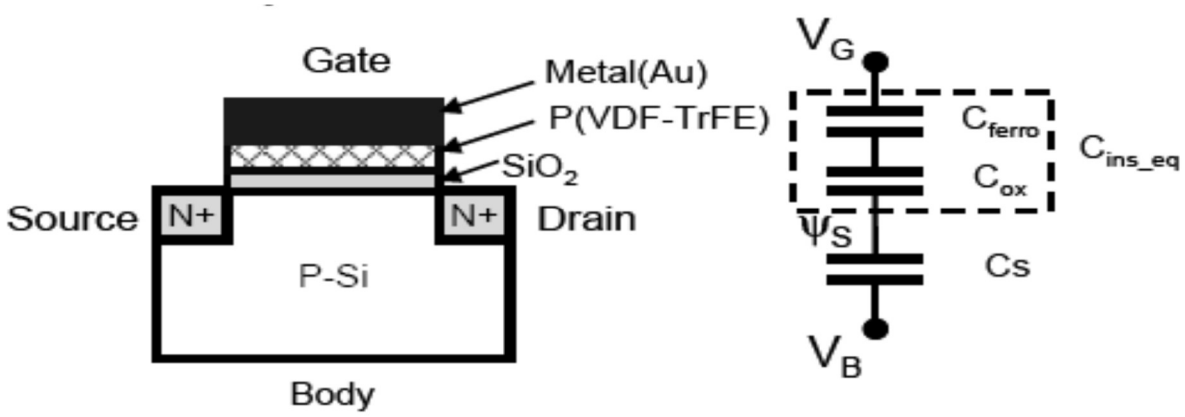


Figure 8: 40nm p(vdftrfe)/ sio2 gate stack with the capacitive representation

2.5. LOW POWER NCFETS FOR QW BODY TECHNOLOGY [41]

A new transistor concept is projected that synergistically syndicates two vital trends of future transistors: ultra-thin body to defeat the short-channel properties and sub-60mV/decade operation to radically reduce power dissipation.

NCFET do not change the carrier transport physics and thus benefited from all the permanent and future materials research meant for refining the MOSFET channel transport. On the other hand, NCFET 'amplify' the gate voltage electro-statically to obtain sub-60mV/decade sub-threshold swing (SS). The problem is hysteresis which is seen in the I-V characteristics and is not good for devices.

The structure of the device is shown in Fig.

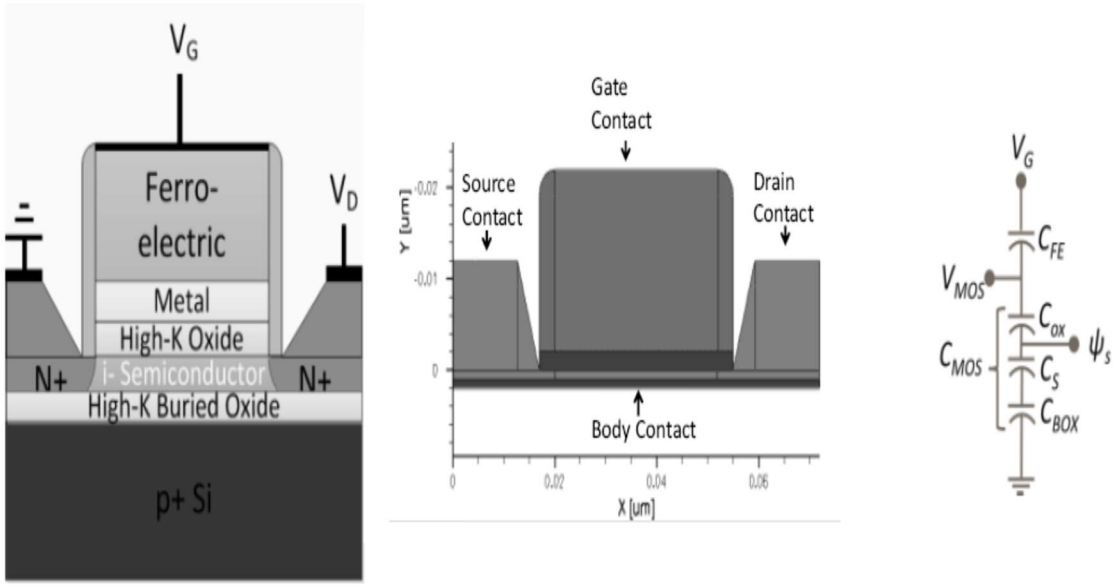


Figure 9: low power NCFETs for qw body technology (a) structure (b) dimension of the device (c) capacitive model

2.6. A Compact Sub-threshold Model for Short-Channel Monolayer Transition Metal Dichalcogenide Field-Effect Transistors [42]

Here fringe field effect of high k insulators is presented. Subthreshold analysis is done for NCFET after considering this effect.

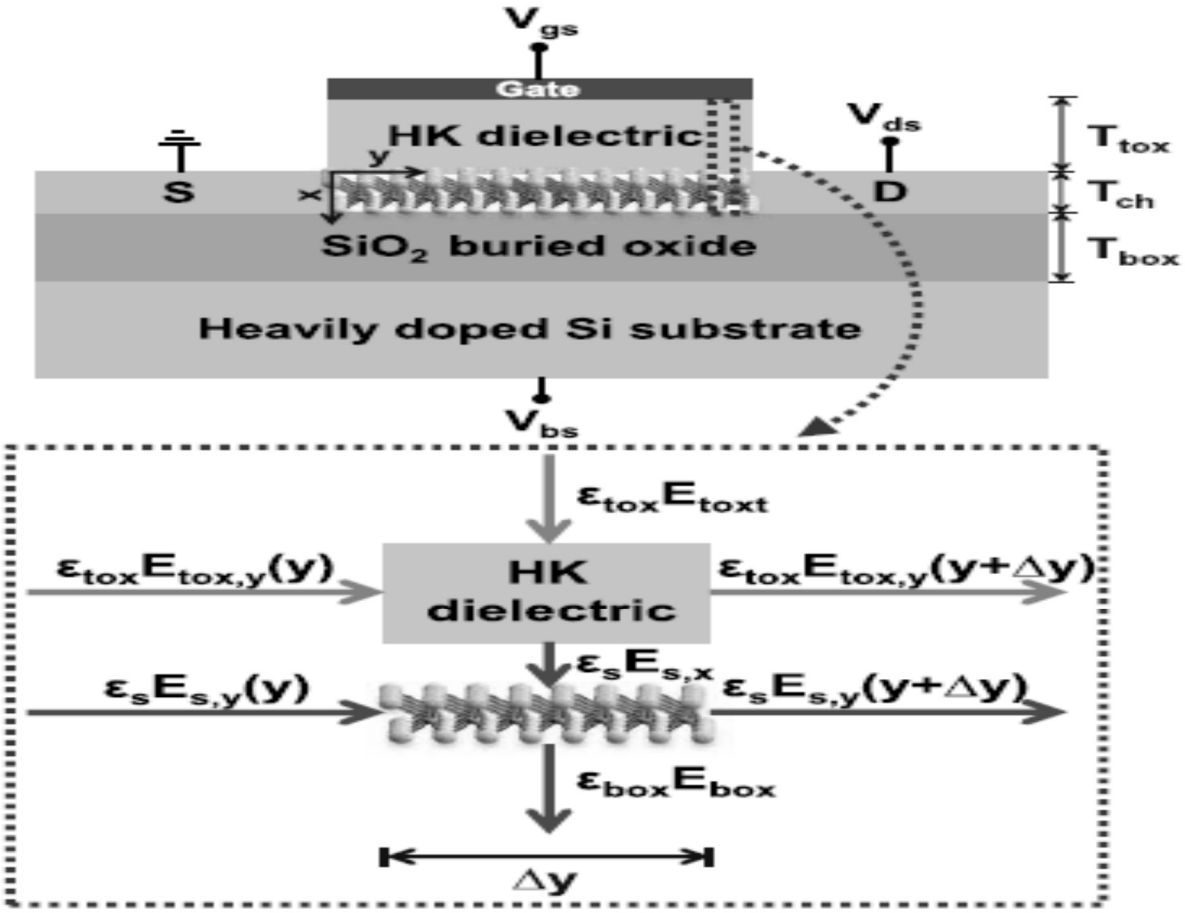


Figure 10: Compact sub-threshold model of box SiO_2

CHAPTER 3

DEVICE STRUCTURE AND MODEL

DEVICE STRUCTURE

A simple model for Negative Capacitance FET presented. Discussion on the ballistic to diffusive transport and the electrostatic effects is also made. Lowering of Drain-induced barrier (DIBL) and improvement of subthreshold swing as the Negative Capacitance FETs scale down is also studied. At low voltage operation the improvement of SS results in linear increase of RDIBL.

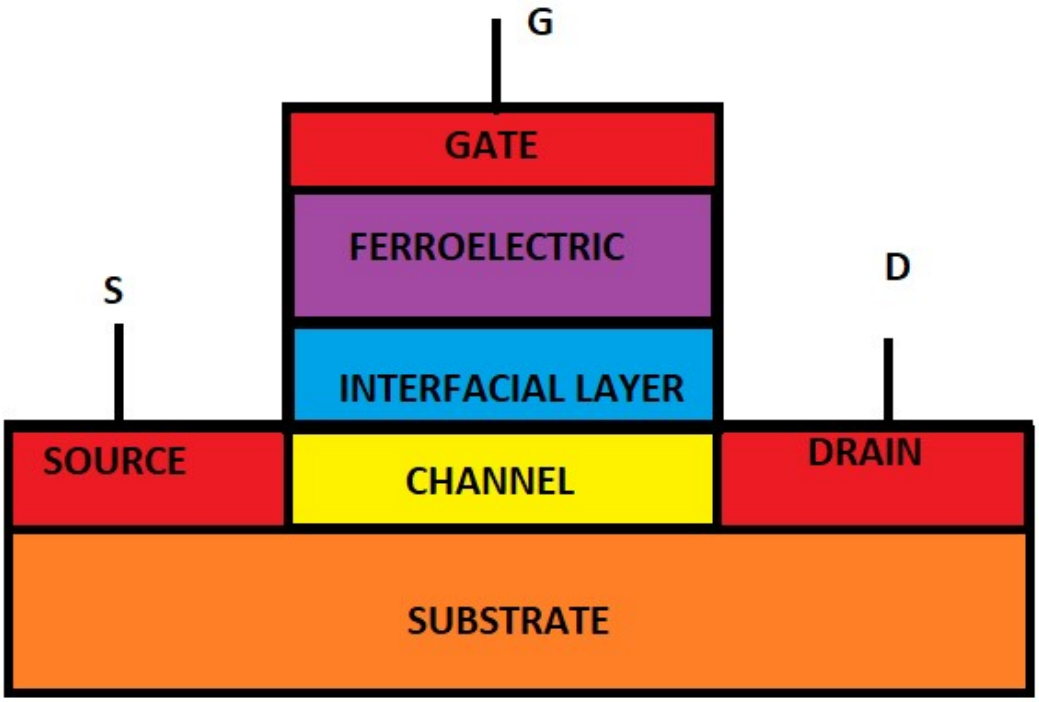


Figure 11: device structure of ncfet

Channel material used is Monolayer MoS2(2D semiconductor). To simulate the native oxide or intentionally induced dielectric a thin dielectric interfacial layer (IL) is included between the semiconductor channel and the FE oxide. Two ferroelectric materials are studied in this thesis.

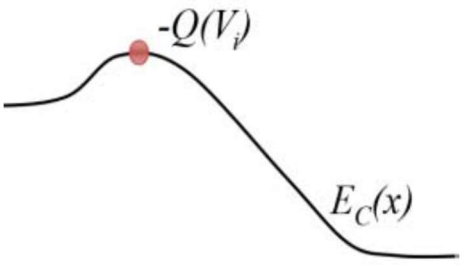
a. The FE oxide doped with Si having FE parameters of $\alpha = -6 \times 10^8$ m/F, $\beta = 5 \times 10^9$ $m^5/F/C^2$, and $\gamma = 4 \times 10^{10}$ $m^9/F/C^4$(FE1)

b. HfZrO(Hafnium Zirchonium Oxide) is used as the ferroelectric material with $\alpha = -14 \times 10^8$ m/F, $\beta = 4 \times 10^{12}$ $m^5/F/C^2$, and $\gamma = 0$ $m^9/F/C^4$(FE2)

The thickness of FE is considered to be 10nm and is varied to analyze its effect on the operation of NCFET.

Further the channel length is taken as 10nm and to analyze the scaling effect it has been lowered to 7nm.

MODEL DESCRIPTION



In "charge-sheet approximation," the drain current normalized by width (I_d/W) of a MOSFET can be given as the product of the charge density multiplied by the velocity of the carriers. This equation can be written at the position of the maximum energy barrier. This location is present between source and the channel and is called "virtual source"[38]

$I_D = Q_i v_{sat}$ ----------(i)

For devices having channel length in nano-meters or less, the velocity at the virtual source,v_{sat} is proportional to the thermal velocity [34], [35]. When the device is biased in saturation, weak dependence of velocity to the bias voltage is also observed. These bias voltages are V_{GS} or V_{DS}.These dependencies can therefore be neglected. Moreover, in [36] it has been proved that in saturation region, the velocity as well as the charge per unit area at the virtual source is independent of V_{DS}. Thus, the V_{DS} dependencies at the non-ballistic regions also negligible for charge density at the virtual source as well as the potential at that point. In contrast, with the increase in Vgsthe ballistic velocity increases as shown in [36]. In [34] with the help of Monte Carlo simulations it has been shown that the velocity at the virtual source is almost constant at high V_{GS}this is because of the increase in carrier scattering. Empirical function in [35] can be used to describe the virtual-source charge density approximated. This expression is valid for the low and high inversion regions and in between as well. The form of the expression was first projected by Wright [37] as follows:

Charge density $Q_i$at the top of the potential barrier is related to the potential V_i:

$$Q_i = C_i\left(nV_{kT} \ln\left[1 + \exp\left(\frac{V_i - (V_{T0} - \xi V_{kT} F_f)}{nV_{kT}}\right)\right]\right)$$

……...(22)

where V_i is the potential at the vertical position of the IL-FE layer interface and the top of the barrier, C_i is the effective capacitance (dielectric IL capacitance, C_{IL} and series semiconductor capacitance), V_{kT} is the thermal voltage, n is the subthreshold coefficient.

As the ferroelectric material used is very thin the subthreshold coefficient is taken as 1.

The threshold voltage is given by:

$$V_T = V_{T0} - \xi V_{kT} F_f \quad \text{.....(23)}$$

and

$$F_f = \left[\frac{1}{\left(1+exp\left(\frac{\left(V_i-\left(V_{T0}-\frac{\xi V_{kT}}{2}\right)\right)}{\xi V_{kT}}\right)\right)}\right] \quad \text{.....(24)}$$

with ξ is fitting constant and has no unit.

The device structure can be represented by a capacitance model shown below:

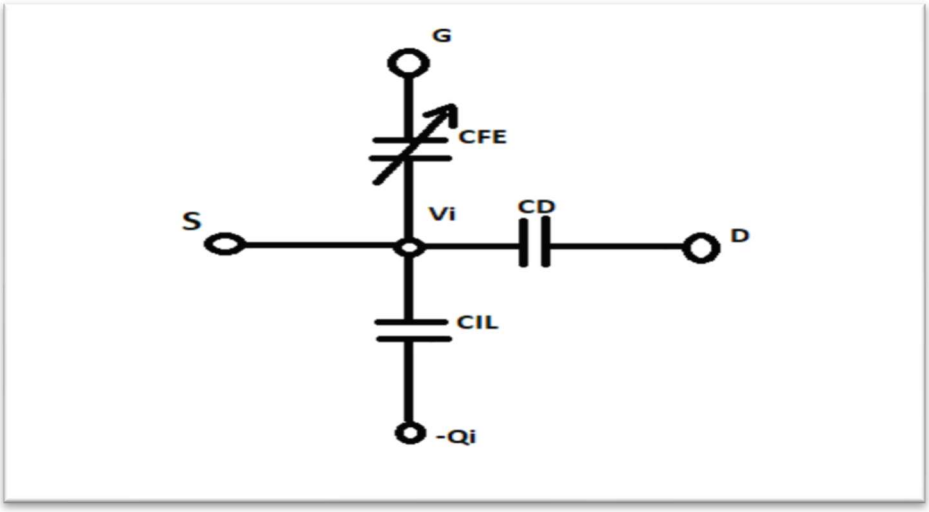


Figure 12: Capacitance model of the structure shown in fig 11

According to L-K Theory(Landau-Khalatnikov) the electric field and the polarization in any ferroelectric material is related as:

$$E = \alpha P + \beta P^3 + \gamma P^5 \quad \text{.....(25)}$$

As $P \approx Q$ so

$$E \approx \alpha Q + \beta Q^3 + \gamma Q^5 \quad \text{.....(26)}$$

where α, β, and γ are FE parameters of the L–K theory. From the above we can find the voltage drop across the FE oxide with a thickness t_{FE} as

$$V_{FE} = \alpha t_{FE} Q_{FE} + \beta t_{FE} {Q_{FE}}^3 + \gamma t_{FE} {Q_{FE}}^5 \text{.....(27)}$$

From the above equation we find that there is one term that shows the linear relation between charge and voltage. While the other terms show the non-linear relation. So, the FE capacitance can be viewed as the series combination of a linear and one non-linear capacitance

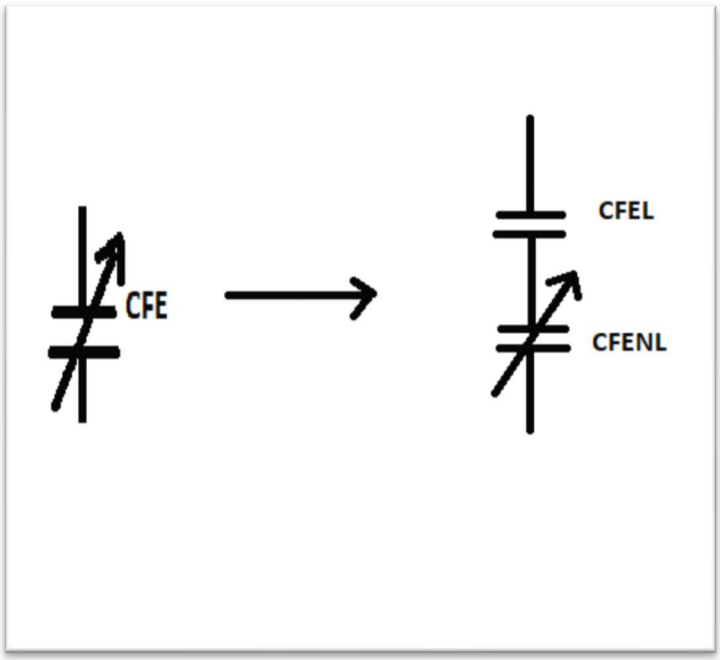


Figure 13: representation of fe capacitor as linear and non-linear capacitor in series

$$V_{FE} = \frac{Q_{FE}}{C_{FEl}} + V_{FEnl}(Q_{FE}) \text{.....(28)}$$

Where the linear capacitance is given by

$$C_{FEl} = \frac{1}{\alpha t_{FE}} \text{.....(29)}$$

And a non-linear capacitance with voltage drop given by:

$$V_{FEnl}(Q_{FE}) = \beta t_{FE} {Q_{FE}}^3 + \gamma t_{FE} {Q_{FE}}^5 \text{.....(30)}$$

Drain capacitance Cd is used to model 2D electrostatic effect as shown in Fig.

$$Q_i = Q_{FE}(V_{FE}) + C_d \cdot (V_D - V_i) \text{ .....(31)}$$

where the voltage drop over the FE layer is $V_{FE} = V'_G - V_i$, V'_G is the effective gate voltage, V_D is the applied drain voltage, and $Q_{FE}(V_{FE})$ is the charge of the FE capacitor. For a given bias point, the unknowns Q_{FE} and V_i can be solved. The charge Q_i can then be computed.

To take into accountthe non-saturation region operation, the velocity v_{sat} is multiplied by a "saturation function" *F*. After the charge is computed from the electrostatic model described above, the current can be expressed as

$I = Q\upsilon_{sat}F$ ……..……..(32)

where the unitless factor

$$F = \frac{\frac{V_D}{V_{Dsat}}}{((1+(\frac{V_D}{V_{Dsat}})^{\beta})^{1/\beta})} \quad \text{…….…….(33)}$$

$V_{Dsat}=(v_{sat}L_g)/\mu$ ……..…….(34)

V_{sat} is the saturation velocity, and μ is the carrier mobility. The above expression of the source–drain current can be applied to ballistic, quasi-ballistic, and diffusive transistors, if the saturation velocity and the mobility are expressed as

$$\frac{1}{v_{sat}} = \frac{1}{v_{satB}} + \frac{1}{v_s} \quad \text{……..(35)}$$

$$\frac{1}{\mu} = \frac{1}{\mu_{sB}} + \frac{1}{\mu_s} \quad \text{……..(36)}$$

where v_{satB} and μ_B are the "apparent" saturation velocity and mobility at the ballistic limit, respectively, μ_s is the effective mobility due to scattering, the velocity $v_s = D/l = (kT/q)\mu_s/l$, and l is the critical length of scattering at the top of the potential barrier.

The apparent carrier saturation velocity at the ballistic limit is

$$v_{satB} = \sqrt{\frac{2kT}{\pi m^*}} \frac{F_{\frac{1}{2}}(\eta'_F)}{F_0(\eta'_F)} \quad \text{…….(37)}$$

Where $\eta'_F = (\frac{E_{F1}-E_{c0}}{kT})$ is defined at high V_D bias condition, E_{F1} is the source Fermi energy level and E_{C0} is the conduction band edge at the top of the potential barrier, kT is the thermal energy, and m^* is the effective mass of the channel material. The apparent mobility at the ballistic limit is determined by

$$\mu_B(L_g) = \frac{\sqrt{2kT/\pi m^*}}{(2kT/q)} \frac{F_{\frac{-1}{2}}(\eta_F)}{F_0(\eta_F)} L_g \quad \text{……..…….(38)}$$

$$\eta_F = (\frac{E_F - E_{c0}}{kT}) \quad \text{…….(39)}$$

is defined at the equilibrium condition at which $V_D = 0$.

The definitions of apparent mobility and saturation velocity are based on the ballistic transistor theory and allow descriptions of the ballistic transport limit. Equation indicates that the smaller value of μ_B or μ_s plays a more dominant role in determining μ. Because μ_B is proportional to the channel length, the mobility μ approaches μ_s at the long channel diffusive limit, and it approaches μ_B at the short channel ballistic transport limit.

CHAPTER 4

RESULTS AND DISCUSSION

The model described in chapter 3 is validated in MATLAB. The results obtained is presented below:

The model is first validated with

1. **POLARIZATION VS ELECTRIC FIELD OF FE OXIDE:**

A. FE1: The FE oxide has a thickness of t_{FE} = 10 nm, and FE parameters of $\alpha = -6 \times 10^8$ m/F, $\beta = 5 \times 10^9$ $m^5/F/C^2$, and $\gamma = 4 \times 10^{10}$ $m^9/F/C^4$

For this material the polarization is plotted against electric field. The S type graph is obtained which shows a negative capacitance region.

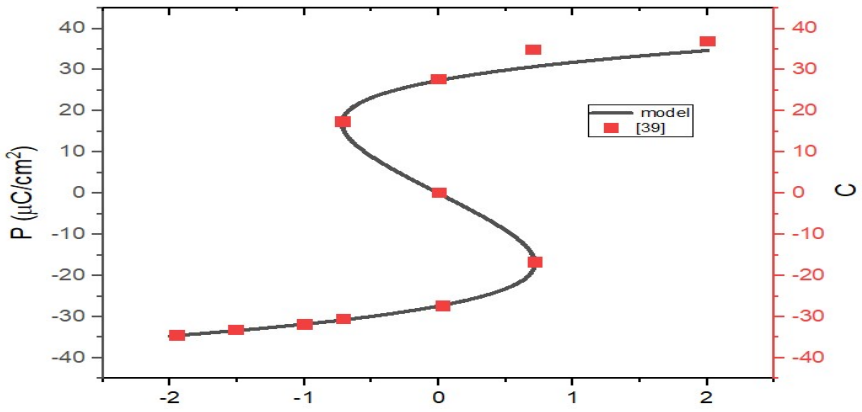


figure 14: polarization variation wrt electric field for FE1

B. FE2: HfZrO is used as the ferroelectric material with $\alpha = -14 \times 10^8$ m/F, $\beta = 4 \times 10^{12}$ $m^5/F/C^2$, and $\gamma = 0$ $m^9/F/C^4$

Similar graph is obtained for another Ferroelectric material. We find that for this ferroelectric material to operate as negative capacitance the voltage variation is very less.

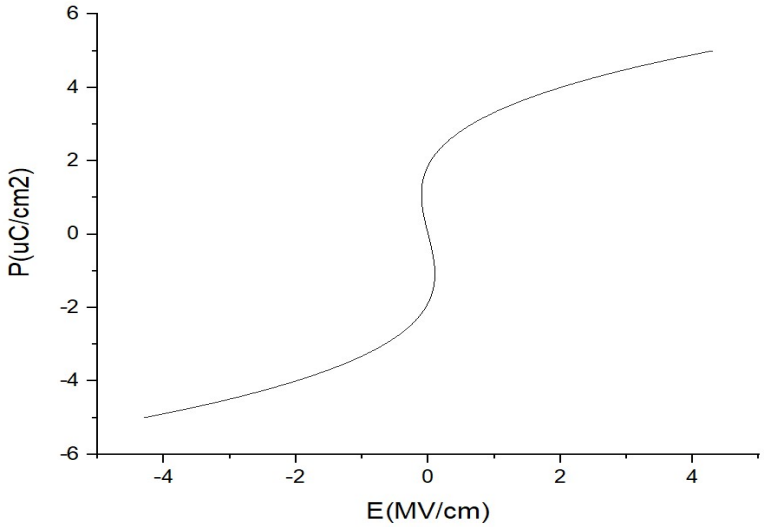


figure 15: polarization variation wrt electric field for FE2

C. Comparing both in one graph:
From the below graph, FE1 is a better material for NCFET than FE2.

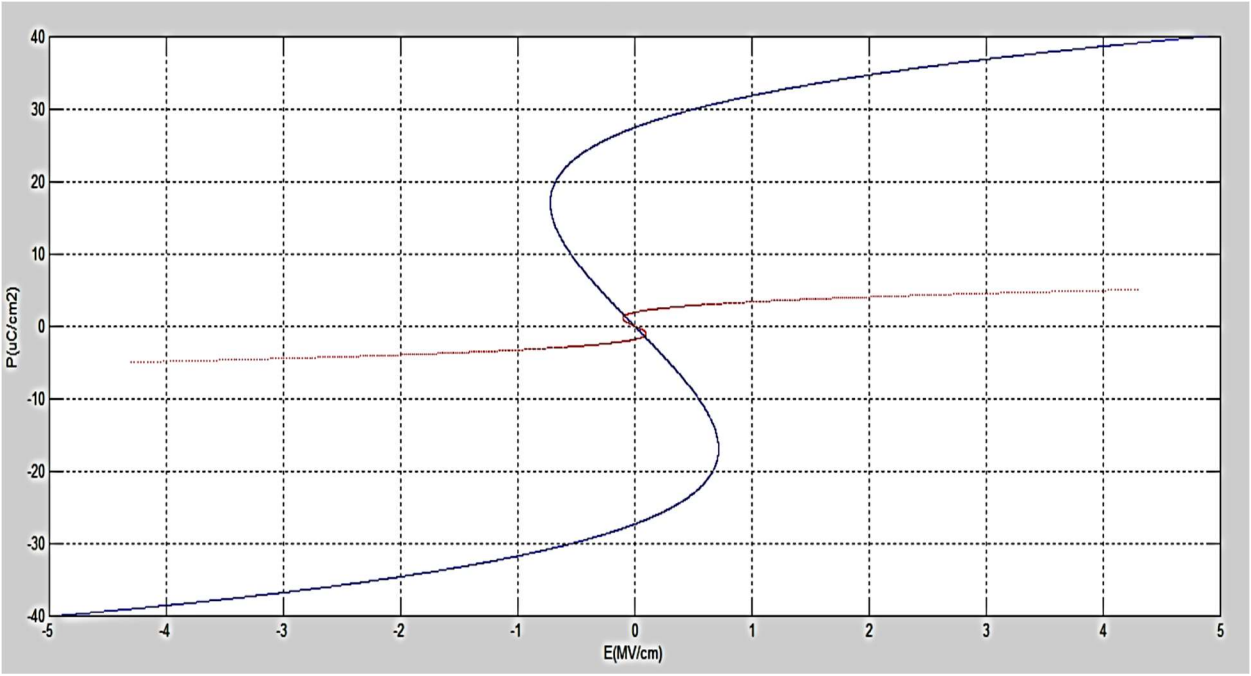


figure 16: comparing polarization variation wrt electric field of FE1(blue) and FE2(red)

2. CHARGE VERSUS GATE VOLTAGE:

The Charge is plotted against the gate voltage. It has been plotted for different ferroelectric materials with varying thickness of the ferroelectric as well. We find that as the thickness decreases the slope of the graph decreases.

a. <u>For FE1</u>

The charge vs gate voltage is plotted in the below figure and its compared with the results obtained in [39]

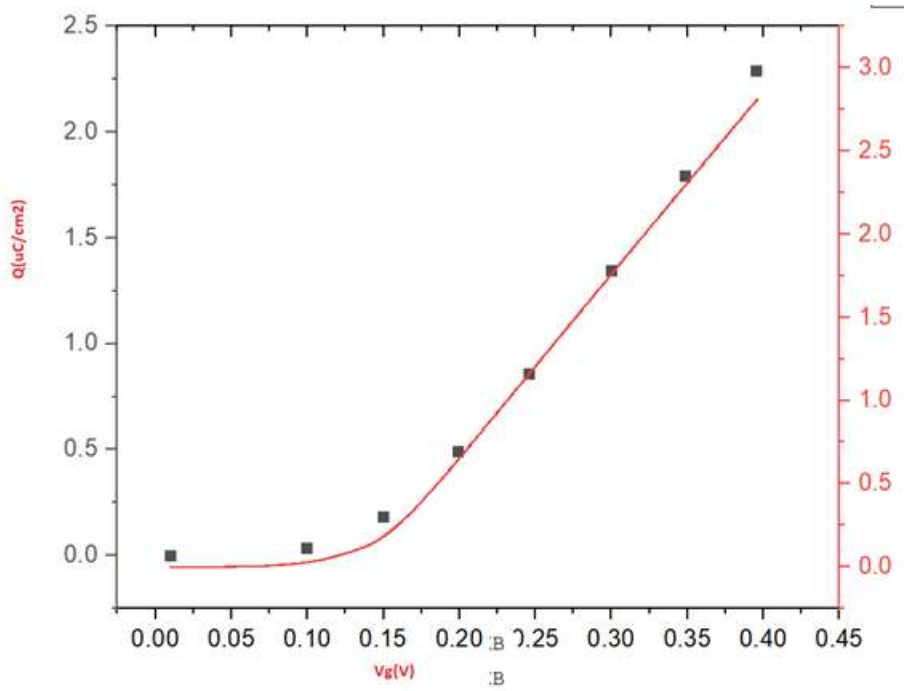


figure 17: charge variation wrt voltage comparing with [39] (symbol)

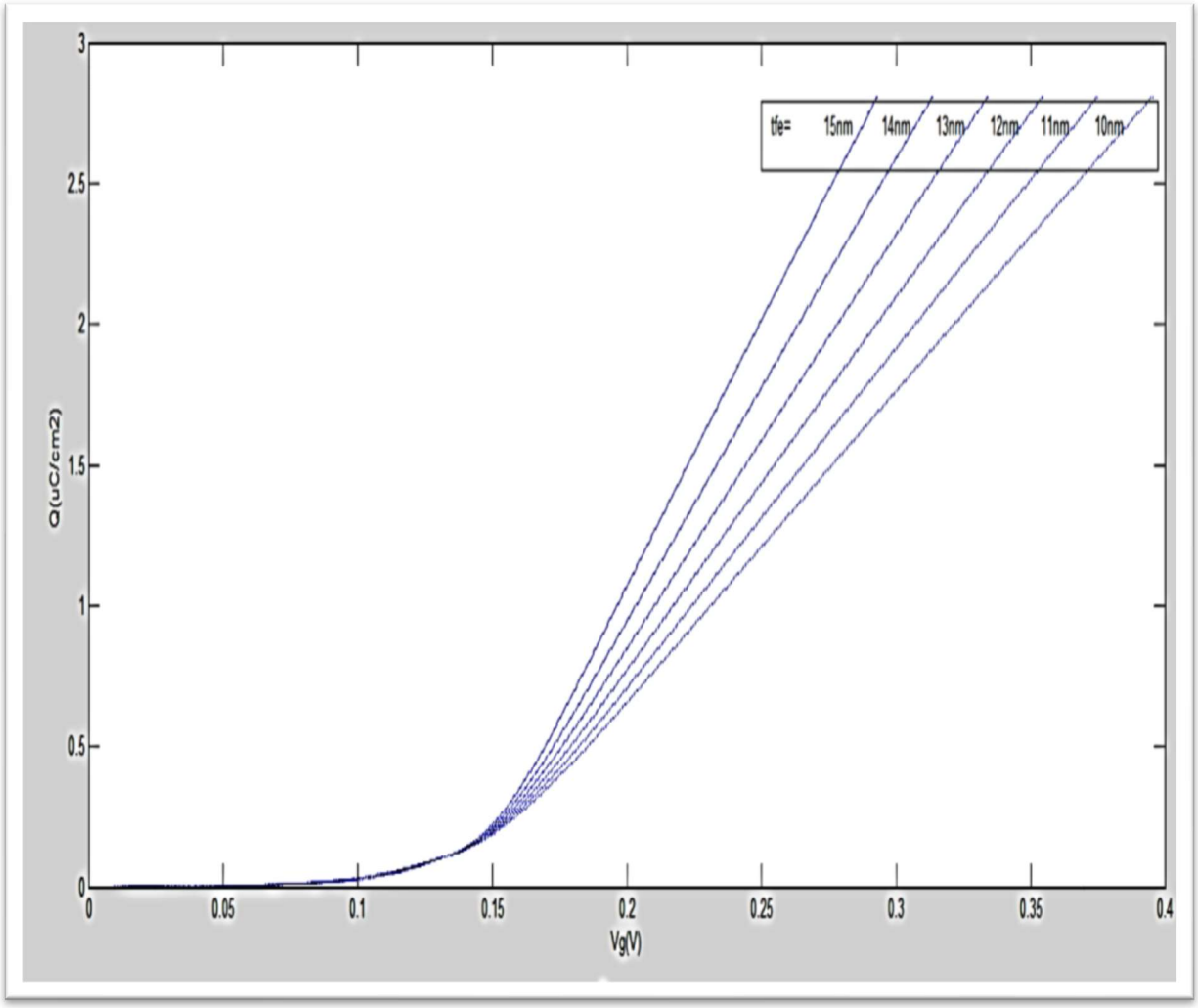


figure 18: charge variation wrt voltage at gate with varying tfe for FE1

From the above graph it is obtained that with decrease in the thickness of FE the rate at which the charge increases with voltage reduces.

b. For FE2

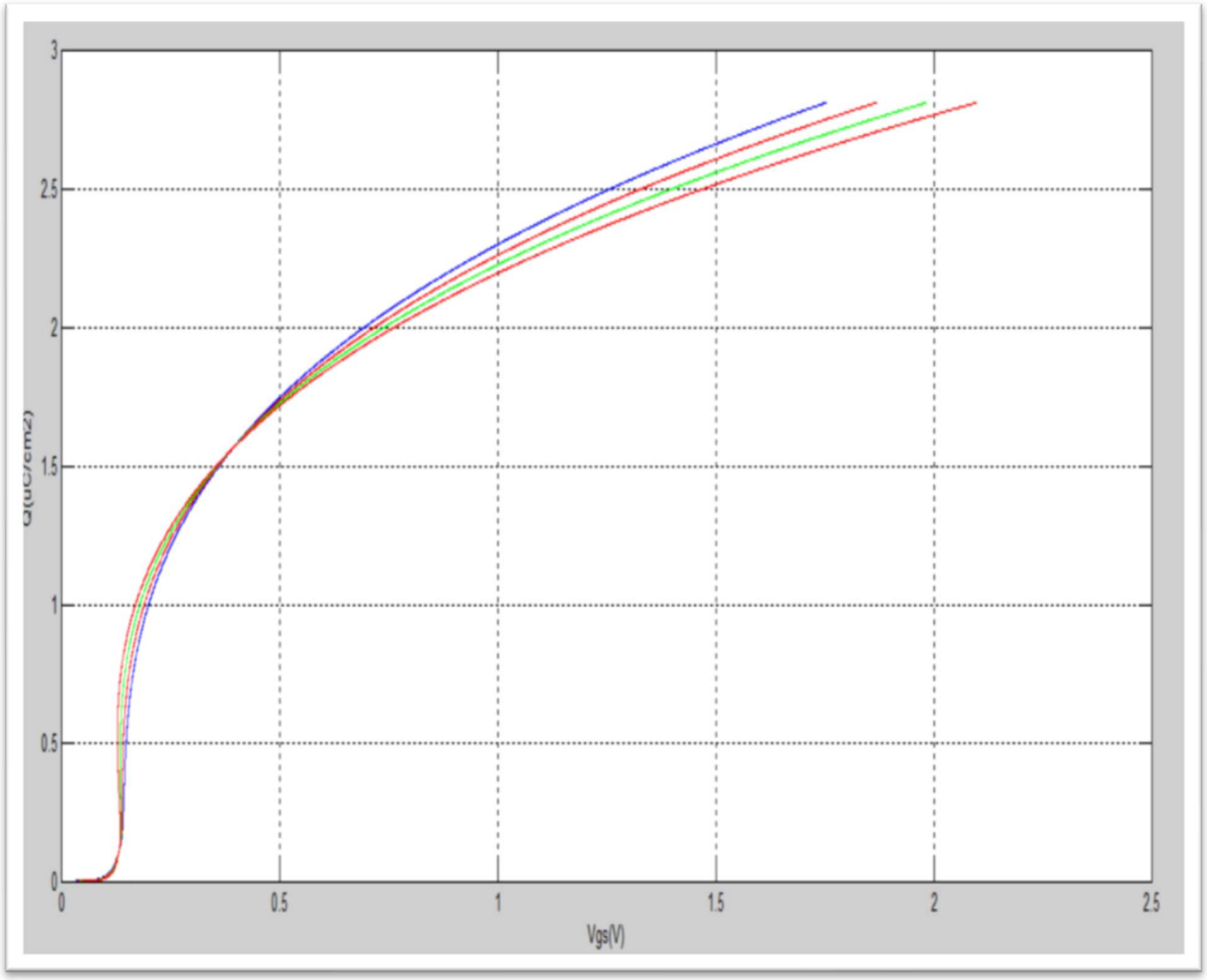


figure 19: charge variation wrt gate voltage for FE2

FE2 shows a unique feature in which at lower gate voltage it mimics the FE1 but at higher gate voltage the properties arevice versa i.e. with decreasing $t_{FE}$the slope increases.

c. COMPARISON OF TWO FERROELCTRICS FOR T_{FE}=10nm

The graph below signifies that the FE1 shows a stable capacitance than FE2 and hence is a better material for NCFETs.

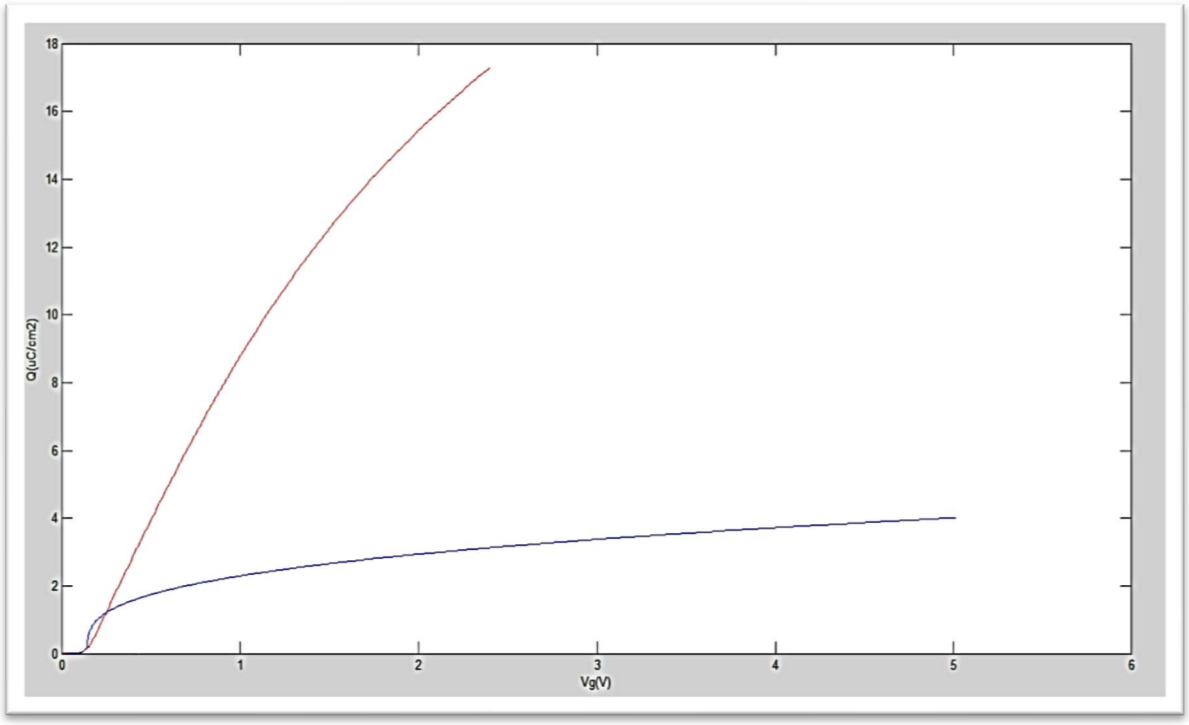


figure 20: comparing charge variation wrt gate voltage for two ferroelectric (blue: FE2)(red: FE1)

3. CAPACITANCE VS VOLTAGE CHARACTERISTICS OF THE MODELED FE–IL-SEMICONDUCTOR GATE-STACK

The capacitance of the gate stack is plotted against the voltage to show how the total capacitance varies with voltage as well as thickness of the FE materials.The total gate capacitance of $C_G \approx 10.4\ \mu F/cm^2$ at $V_G = 1$ V, which is the serial combination of the FE capacitance, IL dielectric capacitance, and the semiconductor capacitance, is larger than the IL dielectric capacitance of $C_{IL} \approx 8.85\ \mu F/cm2$, because of the negative FE capacitance.

a. FE1

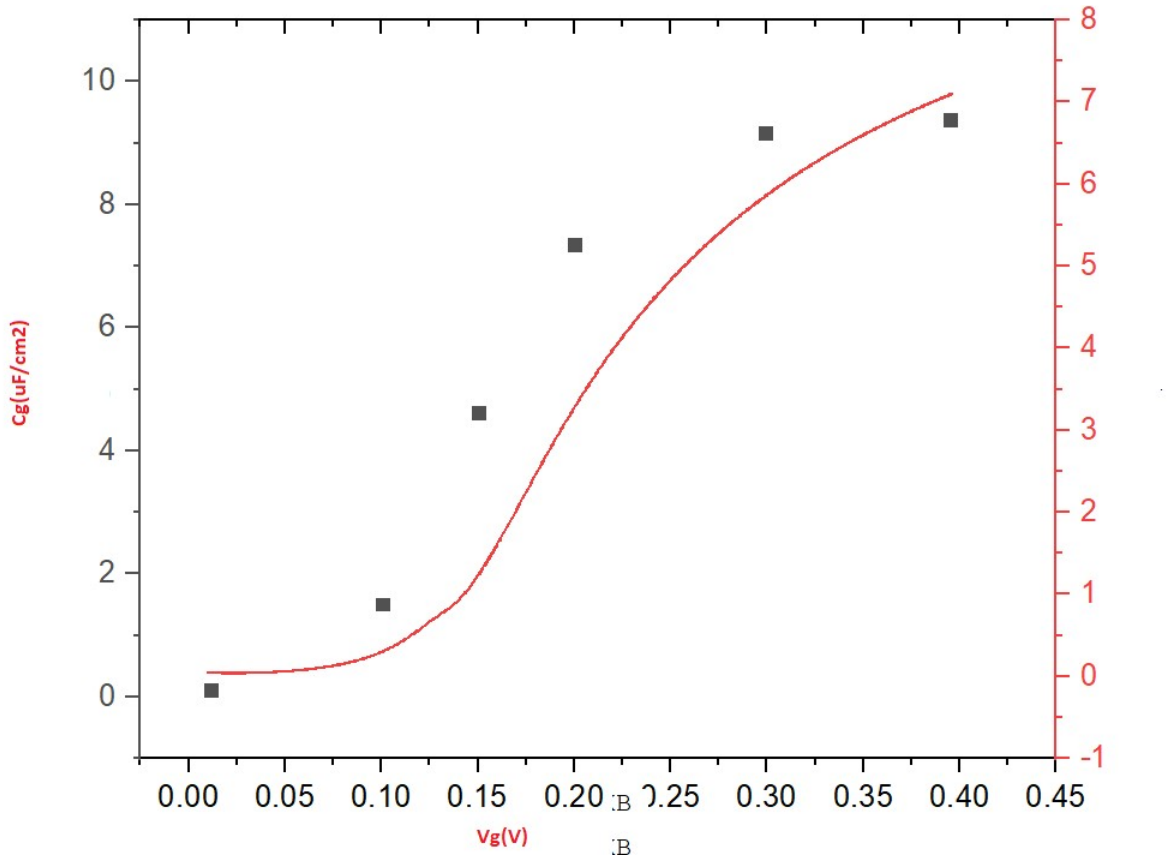


figure 21: capacitance variation wrt voltage for FE1 wrt [39](symbols)

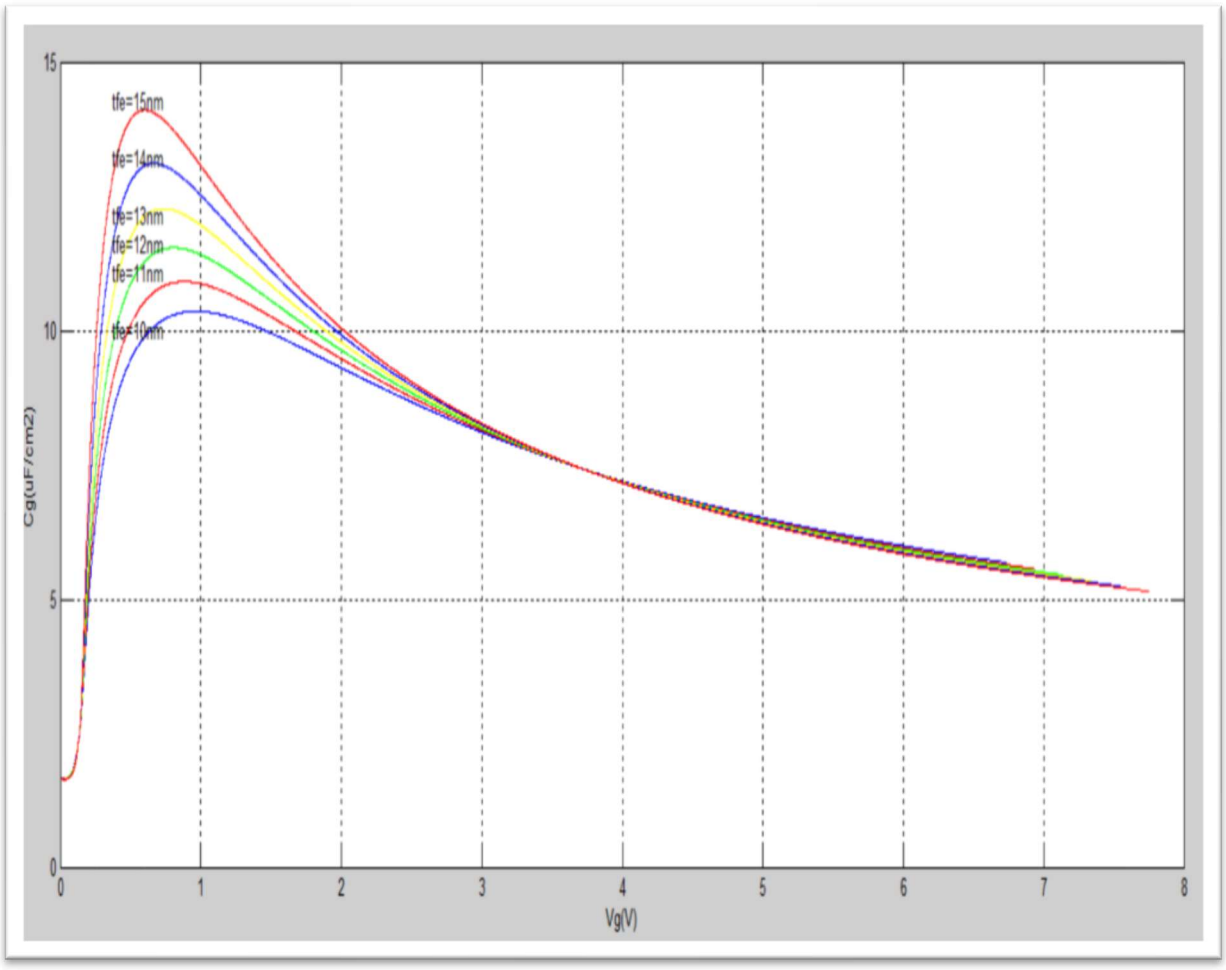


figure 22: capacitance variation wrt Vg for fe1 with varying t_{fe}

b. FE2

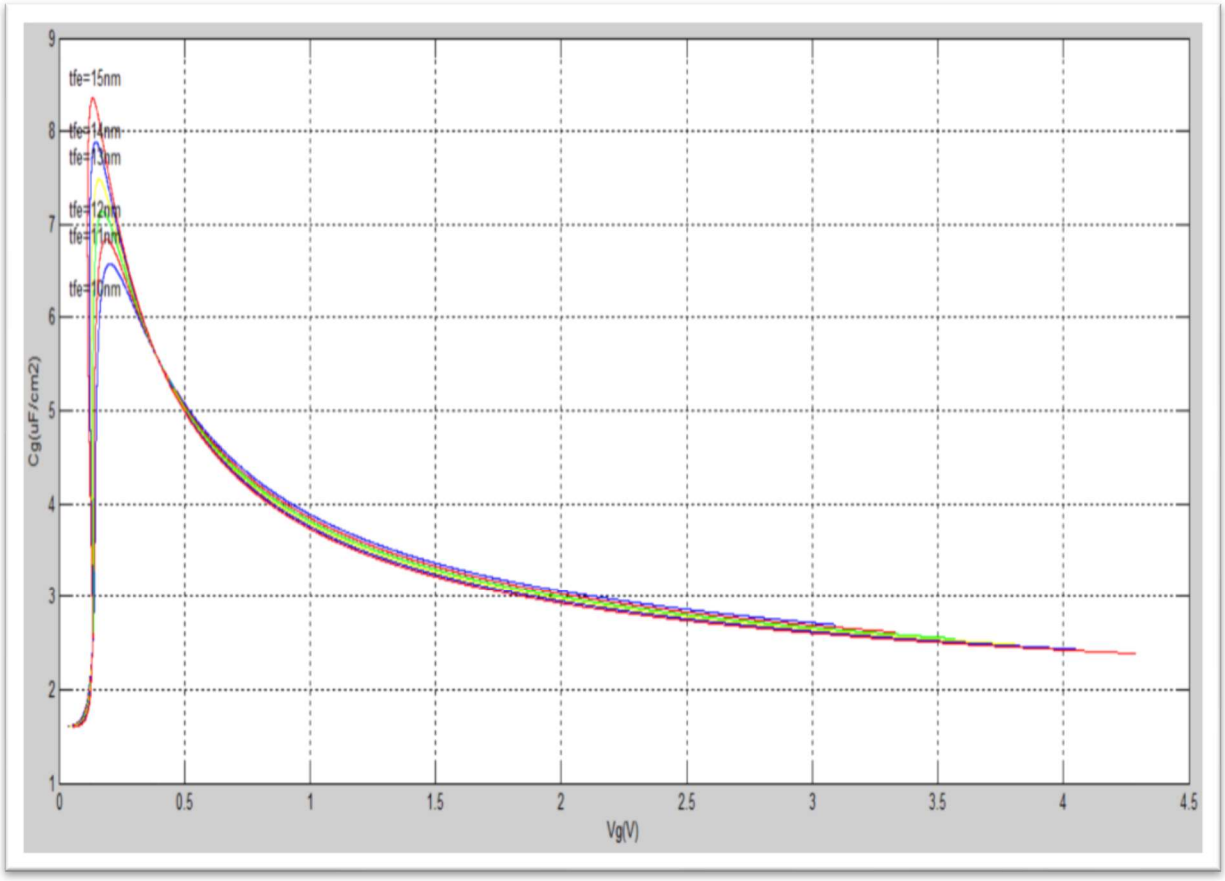


figure 23: capacitance variation wrt gate voltage for FE2 for varying FE thickness

c. COMPARING TWO FE

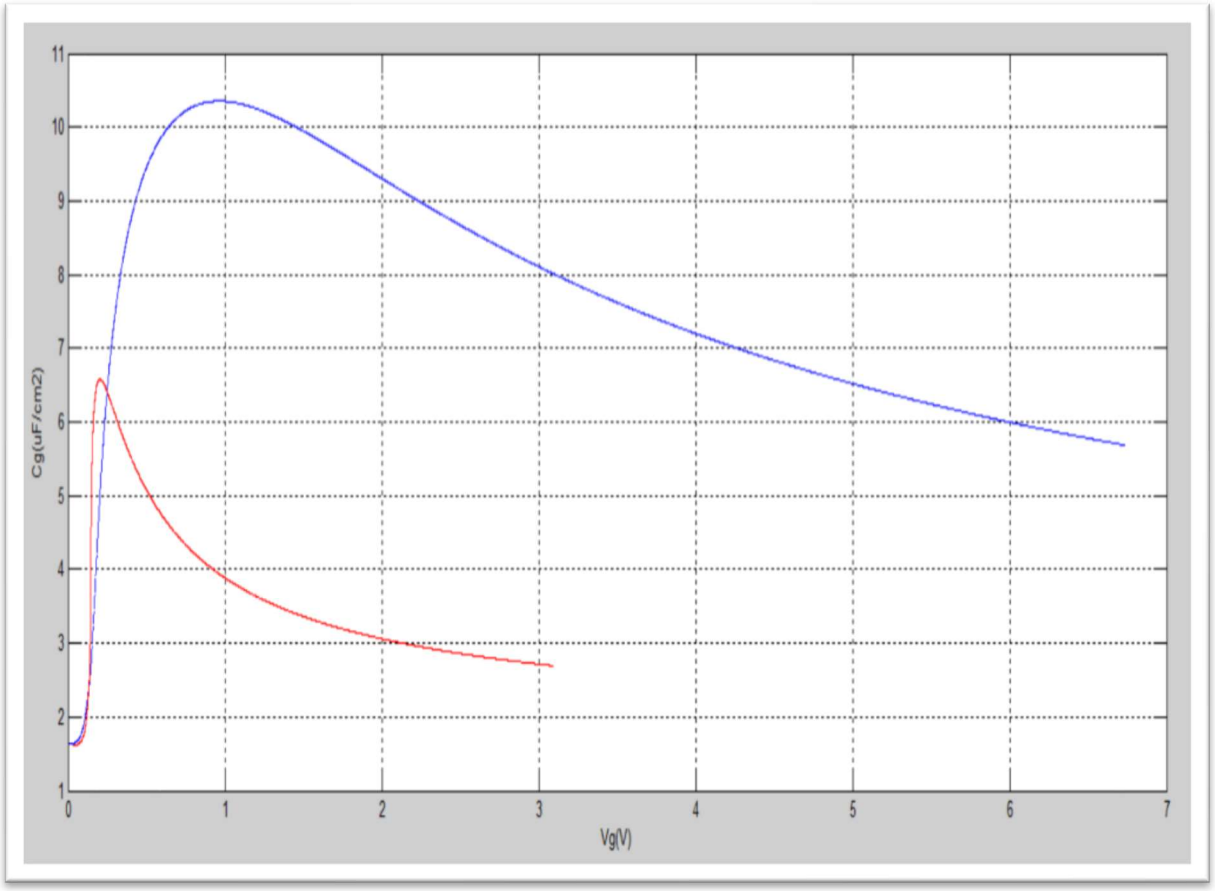


figure 24: charge variation wrt gate voltage characteristics and comparation for FE1(blue) and FE2(red)

4. DRAIN CURRENT VS GATE VOLTAGE

a. FE1 L_g=10nm

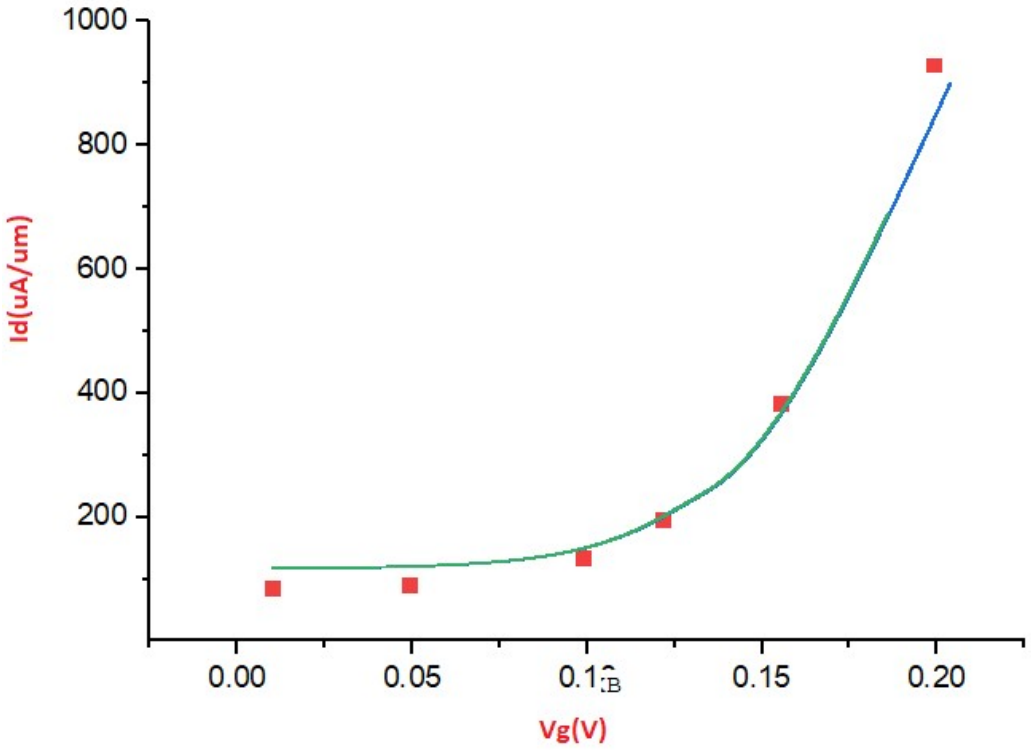


figure 25: drain current variation wrt gate voltage for FE1 and comparing with [39](symbols) for Vd=0.1 V

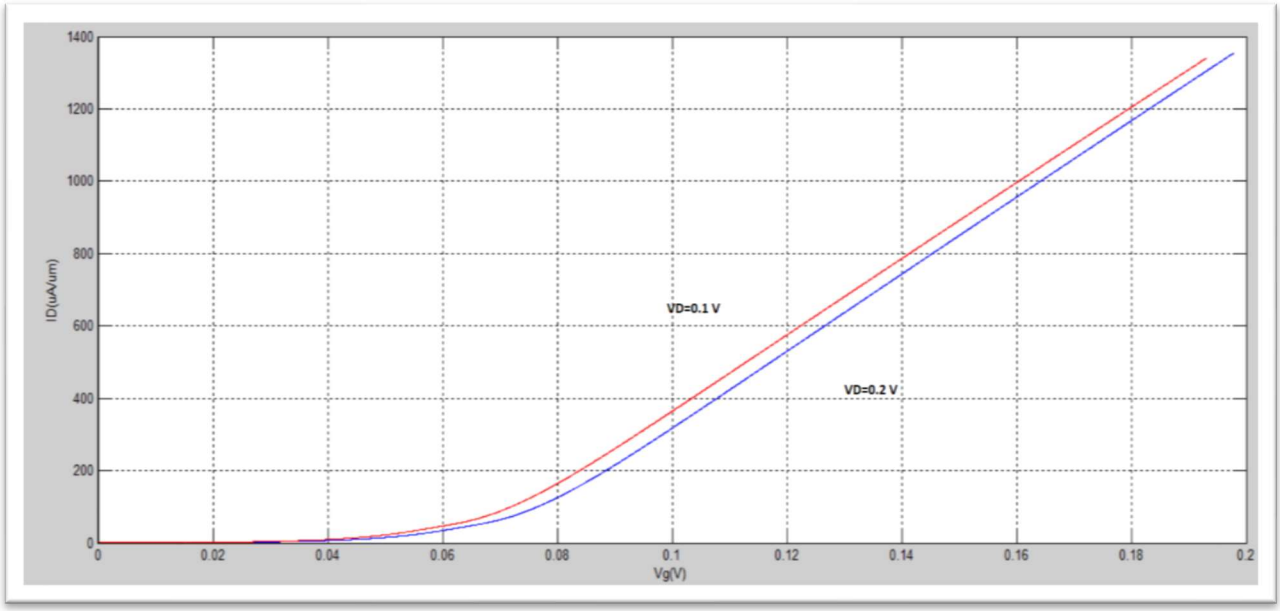


figure 26: drain current variation wrt gate voltage for FE1 varying Vd (drain voltage)

b. FE2 L_g=10nm

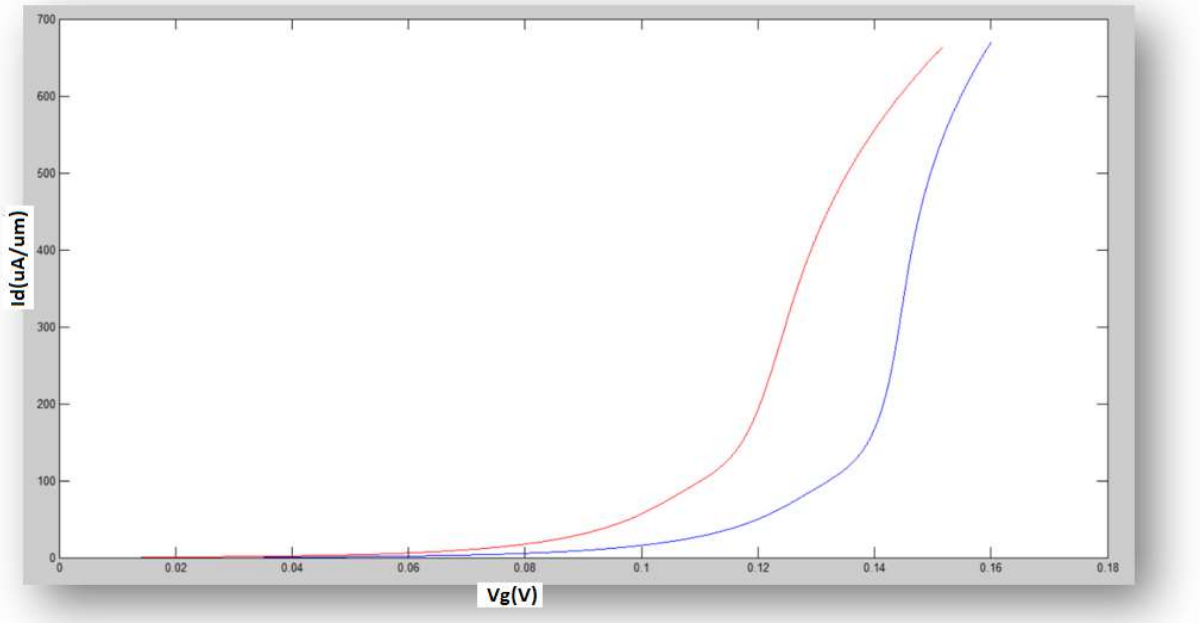


figure 27: drain current variation wrt gate voltage for FE2 (blue= Vg=0.2V; red= Vg=0.1V)

c. FE1 L_g=7nm

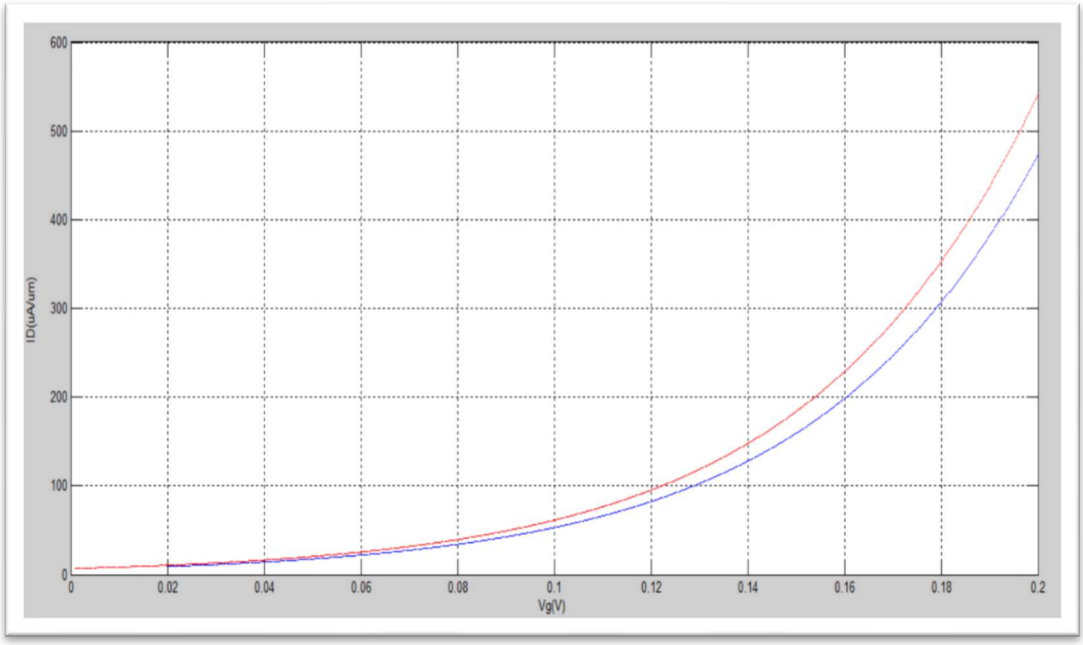


figure 28: drain current variation wrt gate voltage for FE1 at channel length of 7nm (blue= Vg=0.2V; red= Vg=0.1V)

d. FE2 Lg=7nm

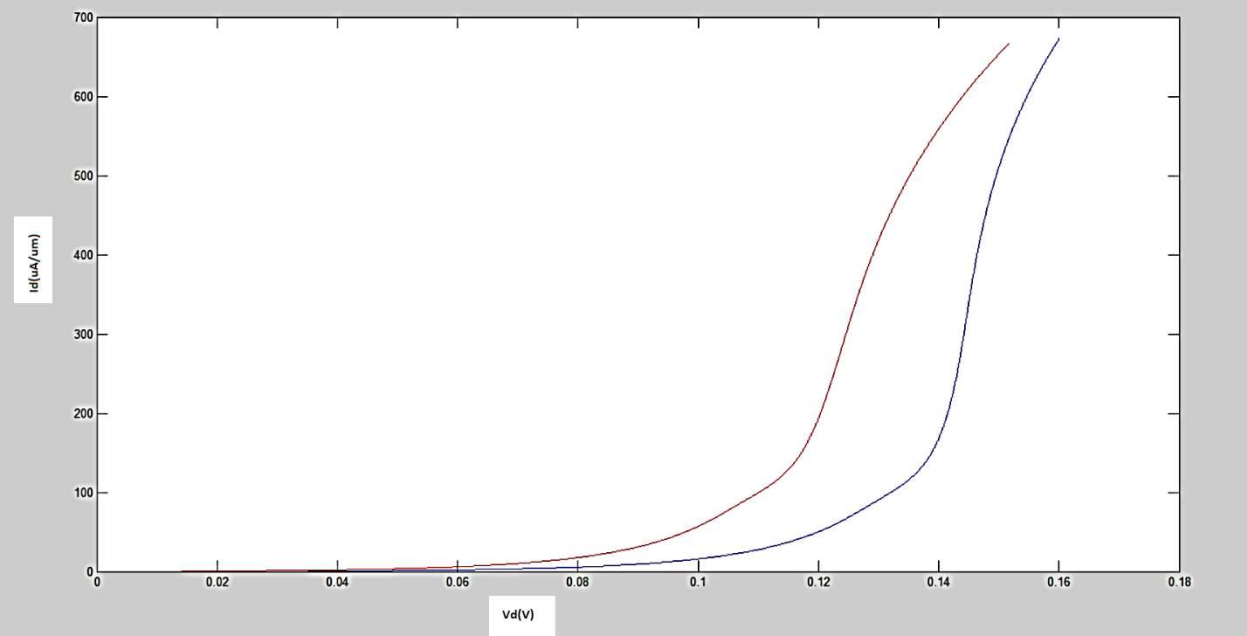


figure 29: drain current variation wrt gate voltage for FE2 (blue= Vg=0.2V; red= Vg=0.1V)

5. DRAIN CURRENT VS GATE VOLTAG FOR FE1

a. FE1 with L_g=10nm

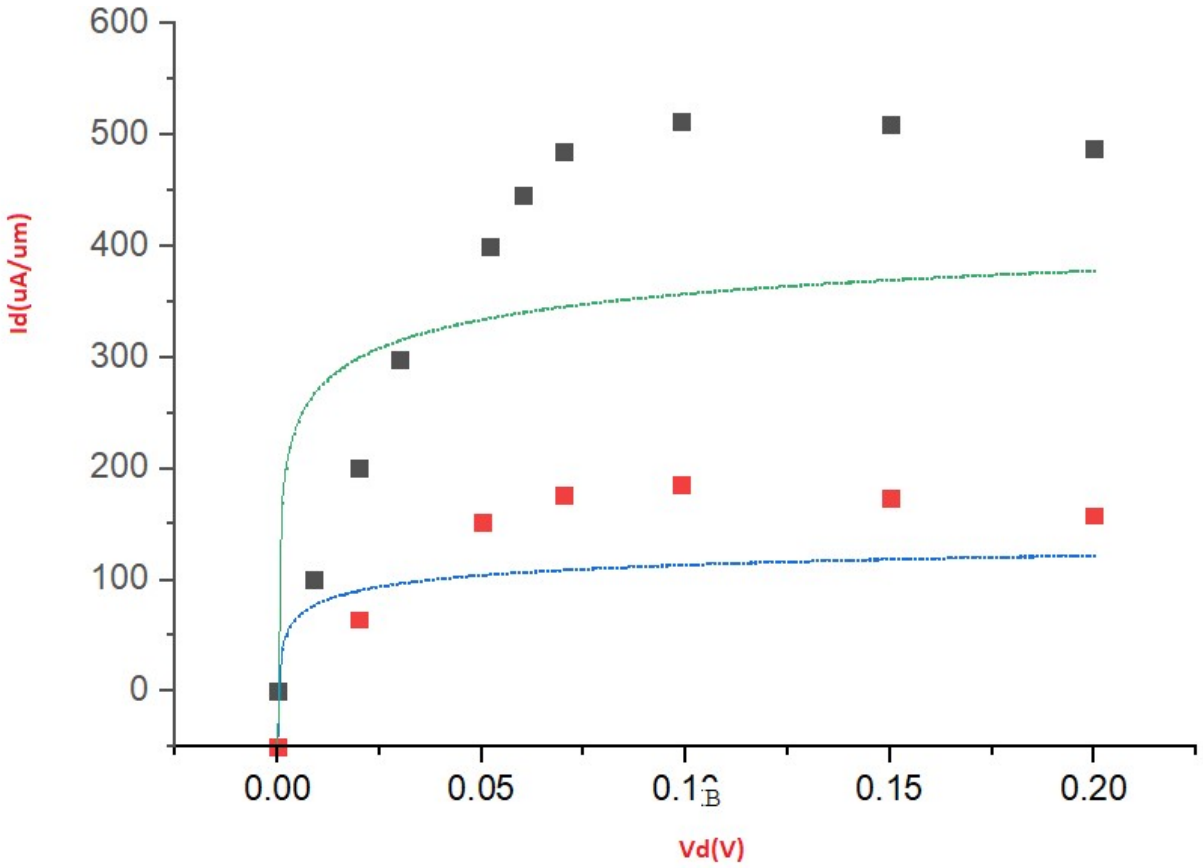


figure 30: Id variation wrt Vd for FE1 and comparing with refernce[39] at vg=0.2v(black symbol and green line) and at Vg=0.16v (red symbols and blue line)

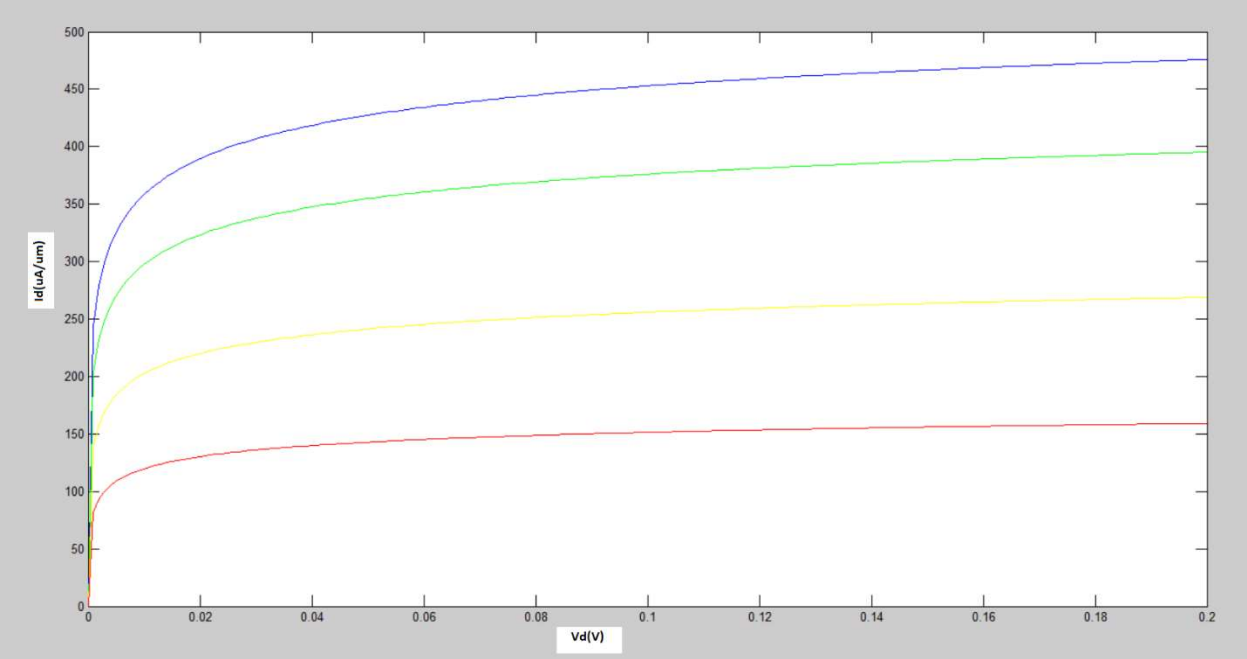


figure 31: Id variation wrt Vd for different Vg (blue= Vd=0.2V; green= Vd=0.18V; yellow= Vd=0.16V; red= Vd=0.14V)

b. FE2 WITH L_g=10nm

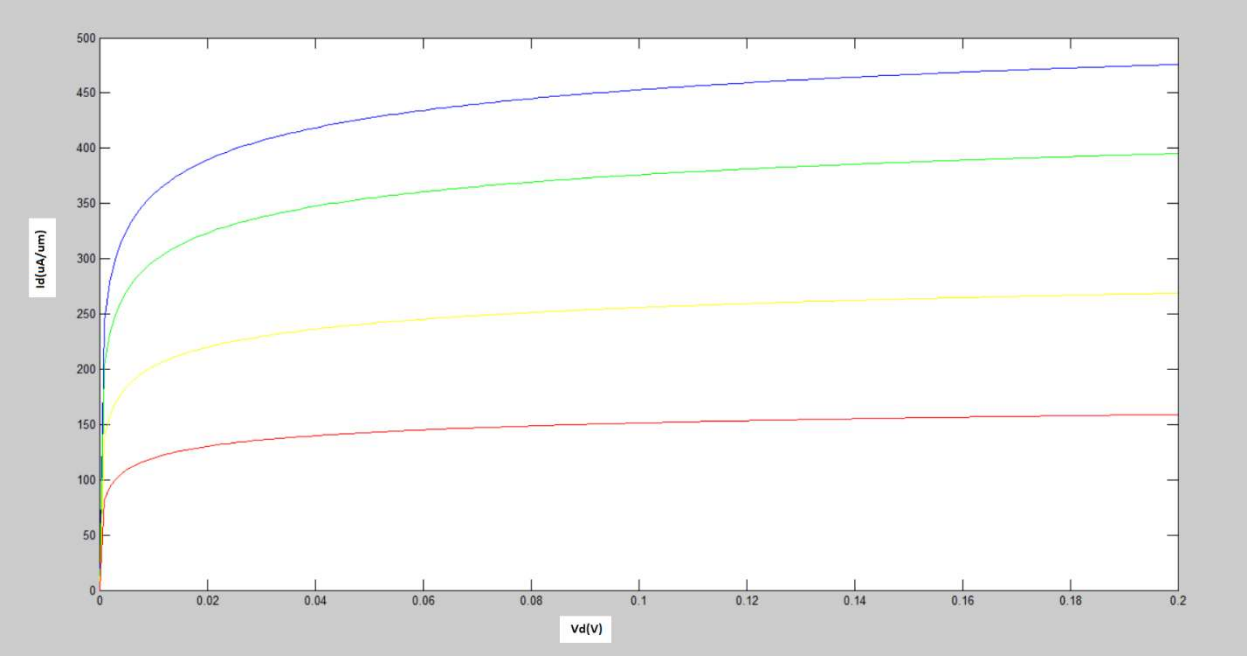


figure 32: : Id variation wrt Vd for different Vg (blue= Vd=0.2V; green= Vd=0.18V; yellow= Vd=0.16V; red= Vd=0.14V)

c. FE1 WITH L_g=7nm

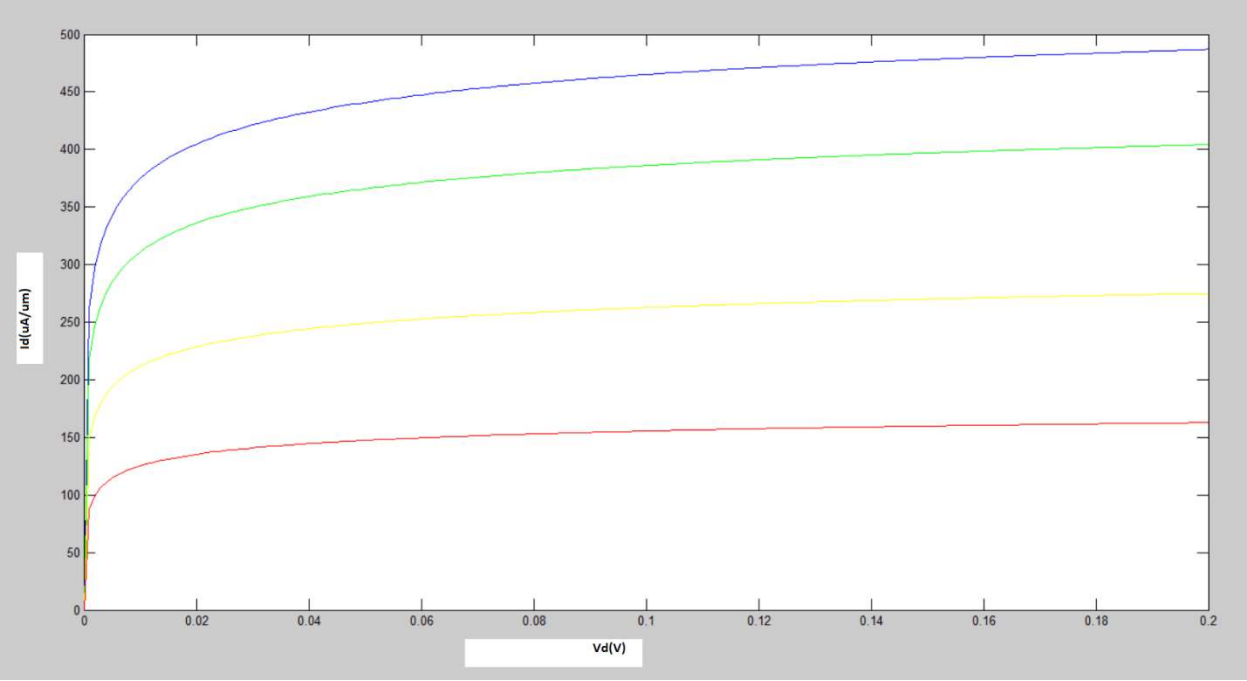


figure 33: : Id variation wrt Vd for different Vg (blue= Vd=0.2V; green= Vd=0.18V; yellow= Vd=0.16V; red= Vd=0.14V)

d. FE2 WITH L_g=7nm

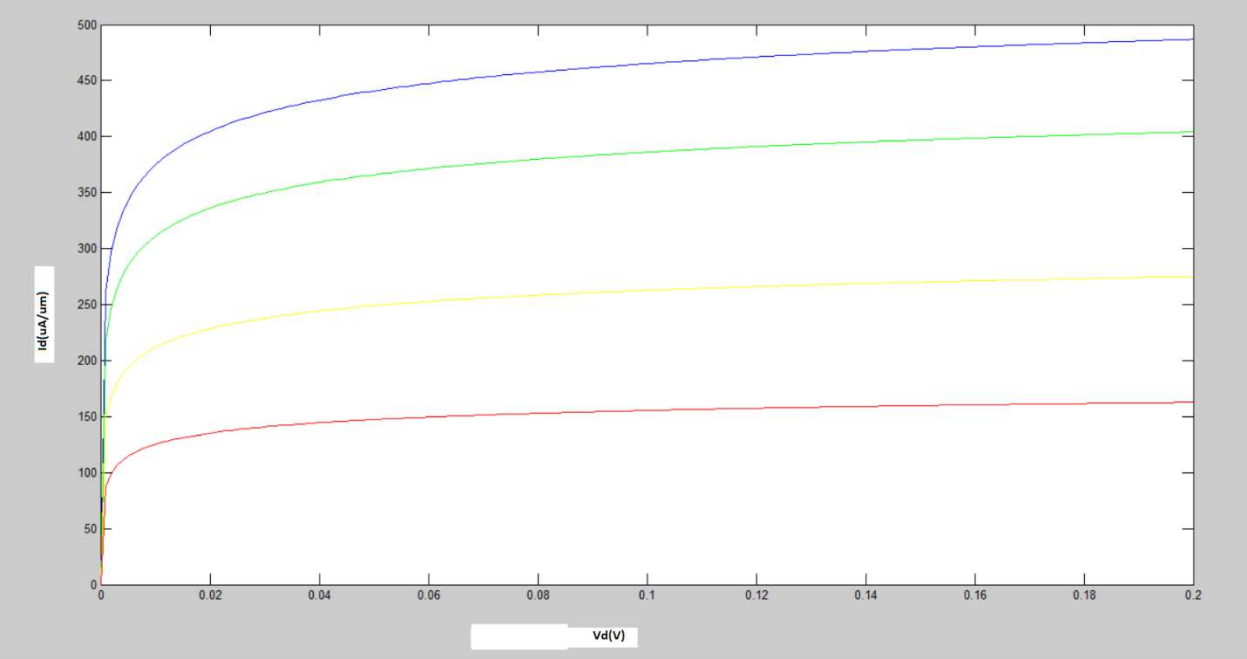


figure 34: : Id variation wrt Vd for different Vg (blue= Vd=0.2V; green= Vd=0.18V; yellow= Vd=0.16V; red= Vd=0.14V)

As we saw, scaling down the gate length in an NC MOSFETs helps in getting larger DIBL, and the smaller Subthreshold Swing.
Based on the model, discussed in Chapter 3, the effective gate voltage is

$$V_G' = V_G - V_{FB} = V_i + V_{FE} = V_i + V_{FEl} + V_{FEnl} \quad \text{.....(44)}$$

where V_{FB} is the flat band voltage.

For the device operating at lower voltage, the potential drop across theFE layer is linearized as $V_{FE} \approx V_{FEl}$, provided the potential drop across thenonlinear oneis smallerrelated to that ofthe linear one, i.e., $V_{FEnl}+V_{FEl}$. The effectivegate voltage can be roughly expressed as

$$V_G - V_{FB} \approx V_i + \alpha t_{FE} Q_{FE} \approx V_i + \alpha t_{FE}(Q_i + C_d(V_i - V_D) \quad \text{.....(45)}$$

Let us consider an NCFET working in the subthresholdregion. Taking partial derivative on Vgin [45] with respect to V_i (45)

$$\frac{\partial Vg}{\partial Vi} \approx 1 + \alpha t_{FE} C_d + \alpha t_{FE} C_{se} \quad \text{.....(46)}$$

where the capacitance C_{se}= $(\partial Q_i/\partial V_i)$, which can becalculated by differentiating equation.

The Subthreshold Swing is given by

$$s \approx \frac{\partial Vg}{\partial \log_{10} I_D} = S_0[1 + \alpha t_{FE} C_d + \alpha t_{FE} C_{se}\ ] \quad \text{.....(47)}$$

Where
S_0=(kT/q)ln(10) is thermal limit of SS.

The value of DIBL can be stated as

$$DIBL = \frac{\partial Vg}{\partial Vd} \approx \alpha t_{FE} C_d \quad \text{.....(48)}$$

Thus, DIBL can betaken as the shift of the threshold voltagein the subthreshold region as the drain voltage increases.Because of α <0, the DIBL is negative, which is reverseof the conventionalFETs.

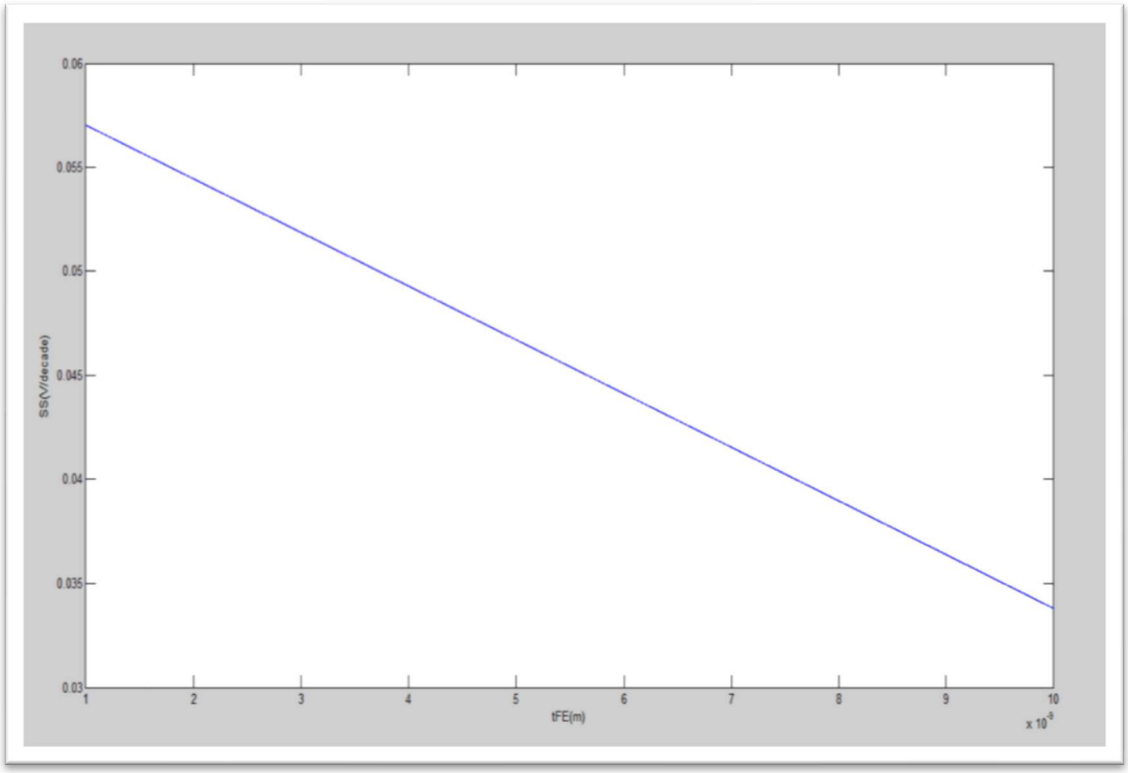


figure 35: subthreshold swing variation wrt FE thickness

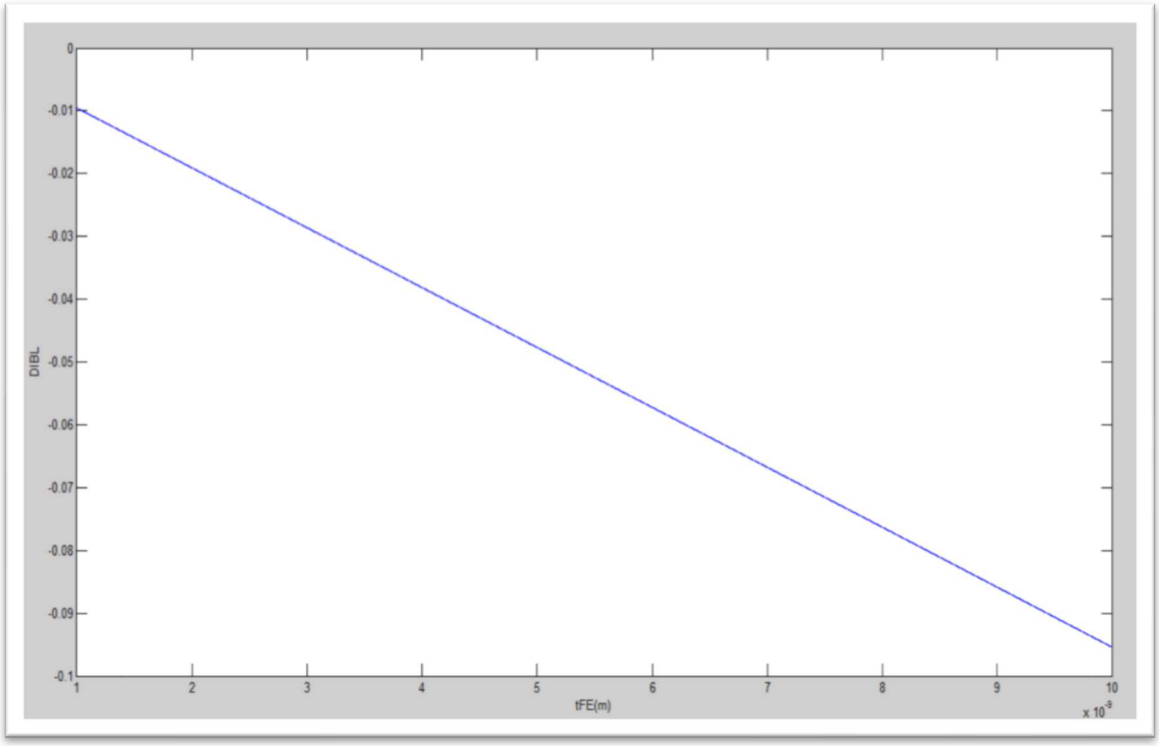


figure 36: DIBL variation wrt FE thickness

DISCUSSION

Figure 14 shows the polarization vs electric field plot of the ferroelectric material that is Si doped. The graph shows comparison between the model and [39]. Figure 15 shows the same for FE2. Figure 16 compare the result for FE1 and FE2. The graph obtained is as S-shaped graph. It is seen that the operating voltage for FE1 is greater than FE2 and hence FE1 can be used as a better material for NCFET. The stability of the NCFET made with FE1 will be better than that made with FE2.

Figure 17 shows the charge vs gate voltage of the FE1 and comparison with [39]. Figure 18 shows the same for different ferroelectric material thickness. It depicts that with decrease in the thickness of FE the rate at which the charge increases with voltage reduces. Figure 19 shows it for FE2. FE2 shows a unique feature in which at lower gate voltage it mimics the FE1 but at higher gate voltage the properties are vice versa i.e. with decreasing t_{FE} the slope increases. In figure 7 comparison of the two FE is made. The graph signifies that the FE1(blue) shows a stable capacitance than FE2 and hence is a better material for NCFETs.

Figure 22-24 shows the capacitance vs gate voltage plot. It is obtained that for lower gate voltage the charge increases and then at higher voltage, the charge is found to decrease. The graph is obtained for different ferroelectric thickness. We found that at lower thickness the maximum charge that can be stored is lesser than for higher thickness. Moreover, FE1 peak is higher and at higher voltage as well.

Figure 25-29 shows the current vs gate voltage. The result is analysed for two different channel length. We found that with the decrease in VD, current increases.

Figure 30-34 shows the current vs drain voltage. The result is analysed for two different channel length. The results show more pronounced 2-D electrostatic effects, with an increase magnitude of the DIBL. At the same time, the SS reduces.
Figure 35 shows that with the increase in ferroelectric material thickness, subthreshold slope decreases. In figure 36 shows that with the increase in ferroelectric material thickness, improvement of DIBL.

CHAPTER 5

CONCLUSION AND FUTURE WORK

A modest model of NCFET is offered, which takes into account the 2-D electrostatic short channel effects, and ballistic to diffusive transport regimes. Mathematicalmodel-based study for the NCFET structure is established. Further, no floating internal gate isconsidered. By applying the proposed model and numerical simulations to a ballistic NCFET with monolayer MoS2 as the channel material, it is revealed that the model can precisely describe the reverse DIBL, and development of the SS, for the NCFETs at the 10-nm scale and below.

The relations specify that as an NCFET ——gages down, the relative enhancement of the SS over the thermionic limit due to 2-D electrostatic effects results in an equally large surge of the reverse DIBL.

Presenting a work opens more scope more future work. This is true in this case as well. Future work may include a new model and study of more physical properties.Till now the work in NCFET or more specifically the model is analysed in 1D and 2D. Thus, in future works complete 3D analysis can be done. This analysis should consider the anisotropic properties of FE materials and the direction of permanent polarization. Mechanical properties of the FE materials can also be studied. Stress and strain effects the FE properties heavily. As in Fabrication process lattice mismatch can induce large stress and strain so proper study needs to be done.Accordingly, Landau parameters alpha, beta and gamma depends on many external parameters like stress, temperature, etc.

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