Optimisation and Analytical Modelling of Tunnel Field Effect Transistor Structures for Low Power Applications

Thesis Submitted in Partial Fulfilment of the Requirements for the Award of the Degree of

Master of Engineering in Electronics and Tele-Communication Engineering

BY

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Contents

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ABBREVIATIONS

Chapter-1

SS: Sub-threshold Swing.

Chapter-2

S.E.: Schrödinger's Equation.

TCAD: Technology Computer Aided Design.

T.I.S.E.: Time Independent Schrödinger's Equation.

WKB: Wentzel, Kramers and Brillouin.

Chapter-3

ALD: Atomic Layer Deposition.

CNT: Carbon Nanotube.

DIBT: Drain Induced Barrier Tunnelling.

DMG DGTFET: Dual Metal Gate Double Gate TFET.

GAA: Gate All Around.

HetJ: Hetero-junction.

HfO_2: Hafnium Dioxide.

HGD: Hetero Gate Dielectric.

HomJ: Homo-junction.

LDD: Lightly Doped Drain.

LGTFET: L-Shaped Gate TFET.

LTFET: L-Shaped TFET.

MIT: Metal-Insulator Transition.

NW: Nano Wire.

PC-TFET: Phase Change TFET.

P(VDF-TrFe): Poly-Vinylidene Fluoride Tri-Fluoro Ethylene.

SiO_2: Silicon Dioxide.

SMG DGTFET: Single Metal Gate Double Gate TFET.

TFET: Tunnel Field Effect Transistor.

TM DGTFET: Triple Metal Double Gate TFET.

UTFET: U-Channel TFET.

VaO_2: Vanadium Dioxide.

Chapter-4

MLDA: Modified Local-Density Approximation.

SCE: Short Channel Effect.

SOI: Silicon on Insulator.

Chapter-5

HDL: Hardware Description Language.

ABSTRACT

At present the MOSFET technology has almost bent the knee in front of the aggressive scaling, which is required in the electronics industry to be able to follow the Moore's law and integrate more and more functionality in ICs, without increasing the power consumption. The Tunnel Field Effect Transistors (TFETs) have gained much attention as the potential successor to the MOSFETs, due to its steeper sub-threshold swing than the MOSFETs (whose sub-threshold swing is limited to 60mV/decade) and also due to its similarity in construction. A plethora of TFET designs have been proposed earlier in the literature, for solving some of the disadvantages associated with the TFETs. We have also tried to suggest a renovated TFET structure, aimed towards low power applications.

In this work, we have emphasized on optimisation of device parameters and analytical modelling of the proposed Broken Gate TFET structure. We have also obtained the device parasitic capacitances through AC simulation. The TFET structure in this work is based on Silicon, as it would be easy to physically implement, due to availability of the already matured silicon based fabrication techniques.

The electrical performance of the proposed structure has been compared with that of other relevant and similar TFET structures which exist in the literature. The device showed significant reduction in ambipolar conduction, improvement in ON current and commendable sub-threshold swing at a short channel length of 21nm.

The work begins with a brief historical view of the evolution of electronic computing, followed by the discussion on the quantum mechanical tunnelling theory, along with its implementation on commercially available device simulators.

The obtained results establish the efficacy of the present structure, which are validated by simulation. As the device has extremely low leakages, faster ON-OFF transition and low parasitic capacitances, it can be implemented in low-power and high-speed electronic applications.

Chapter-1: Introduction

1.1 A Dive into the History of Electronic Computing:

It was the year 1958, when Jack Kilby designed the first Integrated Circuit (IC) [1], as a newly employed engineer at Texas Instrument. After about six months of Jack Kilby's first Integrated Circuit design, Robert Noyce at Fairchild Semiconductor developed his own idea of an integrated circuit that solved many shortcomings of the Kilby's design. Robert Noyce designed the IC using Silicon, unlike Jack Kilby's chip which was made of Germanium. Robert Noyce credited Kurt Lehovec of Sprague Electric for the principle of p–n junction isolation, which was a key concept in the improvement of the IC design [1]. This isolation technique allowed each transistor to operate without any interference to and from the neighbouring transistor, despite being on the same silicon chip.

There is a difference in opinion on whom to be exactly credited for invention of the IC. In the 1960s, four people: Kilby, Lehovec, Noyce and Hoerni, were being recognised by the American press. But by the 1970s the list was curtailed to Kilby and Noyce only. In the year 2000 Jack Kilby was awarded the Nobel Prize in Physics "for his part in the invention of the integrated circuit".[1] In the 2000s, historians Leslie Berlin, Bo Lojek and Arjun Saxena has fallen back to the idea of multiple Integrated Circuit inventors and revised Jack Kilby's Contribution.

After a few years of the invention of Integrated circuit, i.e., in the late sixties, designers were trying to integrate all the components of a central processing unit (CPU)

in a handful of chips and were successful to a certain extent. Ted Hoff and Stanley Mazor, assisted by Masatoshi Shima and Federico Faggin (with his 1968 milestone achievement of designing Fairchild Child's first silicon gate IC, 3708 [3]) designed Intel's first microprocessor, 4004, which had almost all the components of a central processing unit integrated into it, except for the memories, in the year 1971 [4].

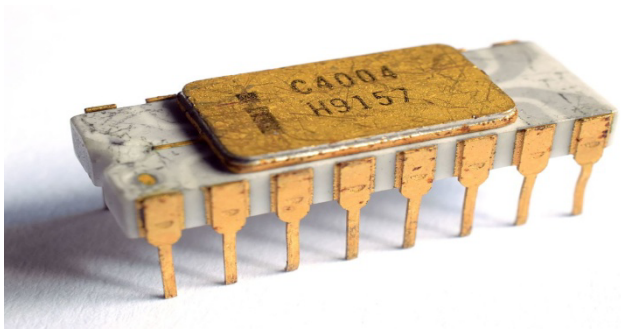

Fig.-1.1: Intel's first Microprocessor C4004.

Source: Wikipedia, obtained through Google Image Search.

The commercialization of microprocessor ICs, led to the computer revolution which changed the future of mankind. The ripples of this major scientific achievement, the commercialization of micro-computers, manifested itself as a huge wave and washed humanity to the shores of the Information age. It is a long way from Charles Babbage's mechanical computer "The Difference Engine" to the Vacuum tube based computers like the Colossus, ENIAC and the commercially available IBM 650, etc., to transistorised ones like Harwell CADET, IBM 604 calculator, etc., and finally to integrated circuit based computers, we see in our everyday lives.

At present, microprocessors and microcontrollers have become an indispensible part of our life. Almost in all everyday items, starting from refrigerators, microwaves, modern toasters, washing machines, sewing machines, to smart-phones and high end digital cameras, etc., electronic computation is omnipresent [12]-[14]. With the gain in traction of Internet of things (IOT) and currently, the Internet of everything (IOE), integration of computers in our daily lives is inevitable.

1.2 The Tale of the Almighty MOSFET:

The Metal Oxide Field Effect Transistor abbreviated as MOSFET or MOS-FET or MOS FET, was conceptualized by Julius Edgar Lilienfeld in 1925. Dawon Kahng and Martin M.

(John) Atalla invented the first MOSFET at Bell laboratory in 1959, as a variation on the patented FET design [5].

As the name suggests, the MOSFET belongs to the category of Field Effect Transistors, like JFETs and unlike BJTs. The main advantages of MOSFETs are based on the facts that its fabrication and integration is simple and it requires negligible drive current at the gate for controlling the load current.

The use of "metal" in the name of MOSFET is not at all justified considering the current technology. The gate is formed using Polycrystalline Silicon (and not metal) due to the ease and accuracy of fabrication, because of its endurance to high temperatures. Also, different high-k dielectric materials are being used as the oxide instead of the more common Silicon Dioxide (SiO_2) [5].

The MOSFET is prevalently used in the Digital circuit domain [5]. Almost all of the digital appliances that we use are primarily based on MOSFET. The MOSFET can be fabricated using n or p-type substrate, leading to p-channel and n-channel MOSFETs respectively. The devices thus formed, are complementary in nature and can be used in pairs to implement different Boolean-logic circuits. These circuits are collectively called as the **C**omplementary **MOS**FET circuits or **CMOS** circuits [5], which are the work-horse of the industry to this day. Due to amazing scaling property of the MOSFET, unlike other transistors, the number of MOSFETs in a digital IC has reached billion [5].

The relentless shrinking in the size of the MOSFETs is only possible due to the advancement in the Silicon-CMOS fabrication technology. Only a decade or two back, the MOSFET channel lengths were in order of micrometers and now it is nearing a few nanometres.

The advantages of having a smaller device are many fold. The reduced device dimension means more number of transistors in a given silicon chip area, which directly translates to more functionality per chip, thus compact appliances [11]. Also, since the cost of fabrication and processing per silicon chip is almost constant, the overall price for a more functionally powerful device is reduced, and the history of prices on consumer electronics bears the proof to this statement. Smaller devices, especially MOSFETs tend to switch faster than it larger channel counterparts. This is because; the main dimensions that are scaled are channel length, channel width, and oxide thickness. When these dimensions are scaled down by an equal factor, the overall channel resistance of the device is not changed, but the gate capacitance is curtailed by a factor,

hence lower time delays and faster switching speeds. Thus scaling has led to faster devices [11].

The aforementioned trend of increasing number of transistors per IC was observed earlier. This trend is popularly known as the Moore's Law. This law predicts that the number of transistors in an Integrated Circuit doubles every eighteen months (or two years as considered originally) [6], [7]. This observation was mentioned in a 1965 paper by Gordon E. Moore, who is also the co-founder of INTEL and Fairchild Semiconductor.

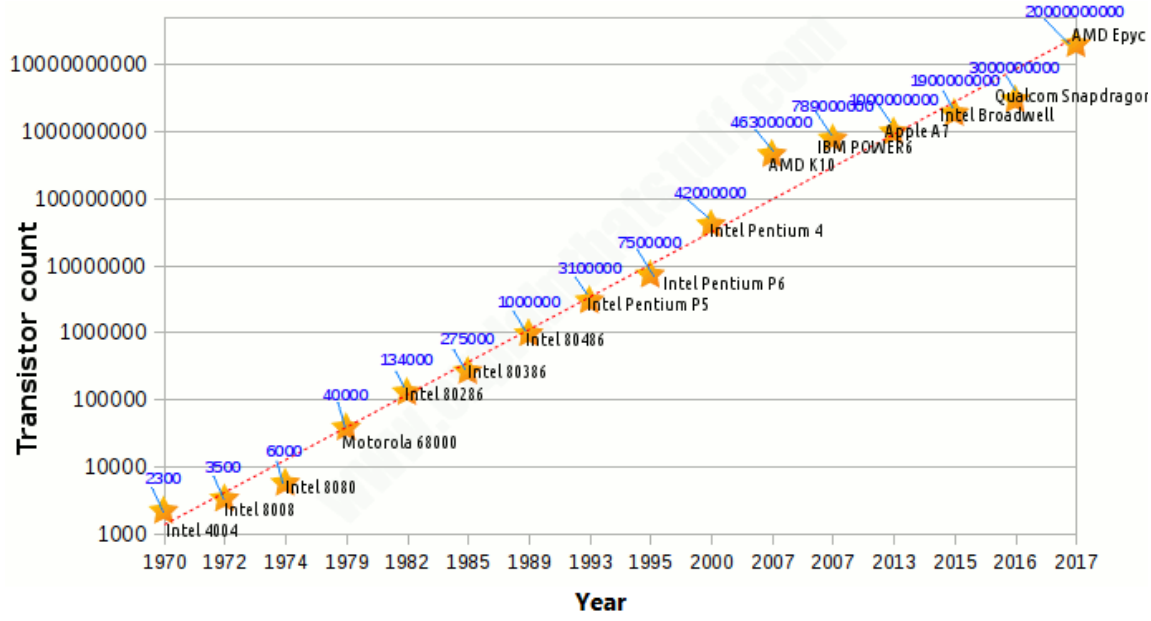

Fig.-1.2: Transistor count per IC over 50 years, obeying the Moore's Law.
Source: www.explainthatstuff.com [2].

1.3 Nothing Lasts Forever: The Problems with MOSFET Scaling:

The famous Moore's have been very successful in predicting the exponential increase in the number of transistor in IC per unit area of silicon, thanks to excellent scalability of MOSFETs [11]. But like many things this might not last forever. The channel length reduction is soon to reach its limit and beyond which we might not be able to reduce the MOSFET's dimensions without the penalties for such reductions weighing out the advantages. Also, it would be unwise, not to mentions the optimistic cries in the electronic device community for "***More than Moore***" [9], [15], [16], [20] approach towards the

future of electronics. Hence, at the end of the day the fact that "nothing lasts forever" might turn out to be good news. We might get more than we bargained for with this new found optimism and zeal, and off-course with hard work, but only future will tell us. Thus, it should be our mission to find alternate devices that can replace MOSFET, just like it replaced it forerunners (BJTs, Vacuum tubes, relays, etc). Before we start looking for alternatives, it is only logical to know about the shortcomings of the MOSFET, which bore the brunt of the electronic industry for so long.

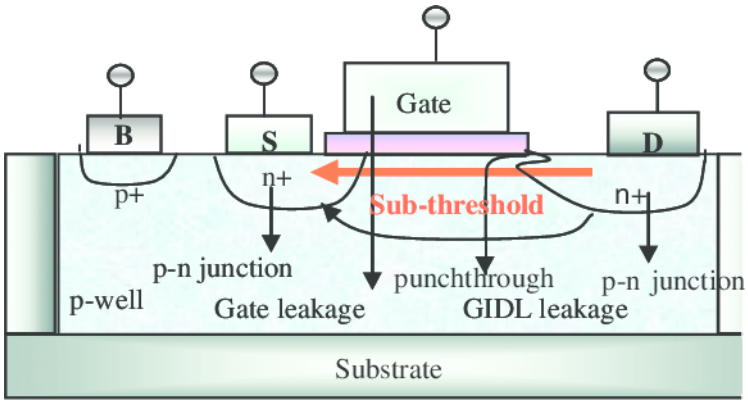

Fig.-1.3: All the current leakages in MOSFET.
Source: ResearchGate, obtained through Google Image Search.

The problems associated with aggressive scaling of MOSFETs [8] can be described briefly as follows:

1. The fabrication of short channel length MOSFETs reliably have always been a problem. But in recent years with the help of Atomic Layer Deposition (ALD) technique, MOSFETs with channel lengths lower than 10s of nm have been fabricated.
2. If the channel length goes down below tens of nanometre, the carriers can just directly tunnel between source and the drain, thus increasing the I_{OFF} current through leakage.
3. As the device dimensions keep on decreasing, the voltages have to be scaled accordingly to reduce the leakage and to reduce the power consumption, but after a while the voltage scaling might not be possible due to compatibility issues with the peripherals and increased delays associated with lower supply voltages.
4. The limited voltage scaling options lead to increased power dissipation per transistor in an IC.

5. Smaller devices are harder to fabricate with consistency and the variability of device performance increases; hence the overall performance of the IC becomes unpredictable, with reliability problems.
6. As, we know, the drain current of MOSFET is dependent on the overdrive voltage (V_{DS}-V_T), the threshold voltage needs to be reduced along with the supply voltage for better current drive.
7. The increase in overdrive voltage (through V_T reduction) not only increases the current drive but also increases the leakage current, increasing the OFF state current exponentially.
8. This exponential increase in OFF state current is due to the fact that the sub-threshold swing (SS) of the MOSFET is not scalable, and has a fixed lower limit, i.e., 60mV/decade at room temperature.
9. Hence, by reducing the power supply voltage and keeping the overdrive constant, it is observed that the leakage increases to unacceptable amounts. Thus, making the option of achieving lower sub-threshold swings a necessity, which as we know is impossible for MOSFET.

1.4 The Motivation:

In a MOSFET, the sub-threshold swing (SS) is limited to a lower value because of the fundamental nature through which the carriers travel through the channel. The current-flow involves the thermionic injection of electrons (for n-channel device), over the source-channel energy barrier. The thermal dependence sets a fundamental limit to the slope of the OFF to ON transition and vice-versa. The sub-threshold swing, *SS* which determines the gate voltage required to change the drain current by an order of 10 (decade) can be written as [10]: $SS = \frac{dV_G}{d\Psi_S}\frac{d\Psi_S}{d(\log I_D)} \approx (1+\frac{C_d}{C_{ox}}(\ln 10)\frac{kT}{q})$ (1.1)

Where, $a = \frac{dV_G}{d\Psi_S}$ is the transistor body factor and $b = \frac{d\Psi_S}{d(\log I_D)}$ is the factor that relates surface potential Ψ_S with the drain current I_D. The C_d and C_{ox} are depletion region and oxide capacitances respectively, while 'k' is boltzman's constant, 'q' is magnitude of electronic charge and 'T' is the temperature in Kelvin.

Now, in the limiting case: $SS = (\ln 10)\frac{kT}{q} \approx 60mV / decade @ 300K$ (1.2)

The above limit can only be reduced by using a physical phenomenon other than thermionic injection for carrier conduction. The solution thus can be broadly classified into two sections, depending upon the 'a' and 'b' factors mentioned in eqn. (1.1).

i. The body factor "a" can be made less than unity by making the gate active in nature, unlike the passive gates employed in MOSFET. The active gate devices such as Negative Capacitance FET (NC-FET) [17], NEM-FET (Nano-Electromechanical FETs) [18] etc can achieve lower SS.

ii. The factor "b" can be made less than (kT/q)ln10, by using different carrier injection mechanism in the channel, like band-to-band (B2B) tunnelling mechanism in Tunnel Field Effect Transistors (TFETs), Impact Ionization in Impact Ionization FETs (IFETs) [19]. Such devices are also capable of achieving less than60mV/decade SS, unlike the MOSFETs.

In this thesis we have concentrated on the Band-to-band tunnelling device, the TFET. This device uses the shortcoming of MOSFET, the leakage due to tunnelling to its advantage. The drain current in TFET is based on tunnelling phenomenon between the source and channel junction. The device easily achieves sub-threshold swings lower than 60mV/decade and have similar construction/structures to that of MOSFET. The similarity in construction ensures that the existing fabrication techniques, which took many years to develop, can be easily translated for fabricating TFET based ICs.

The Tunnel Filed Effect Transistors (TFET) does not suffer from the severity of short channel effects, as in MOSFETs, due to their fundamental difference in operating principles. The TFETs show extremely low OFF state currents when compared to MOSFETs, but at the cost of reduced ON currents (especially in case of Silicon TFETs) [10]. At lower drive voltages, and lower current operations, TFET show faster ON-OFF transitions and even higher ON currents than the MOSFETs as in Fig.-1.4, but if higher load currents are required, the MOSFET are clearly the device of choice.

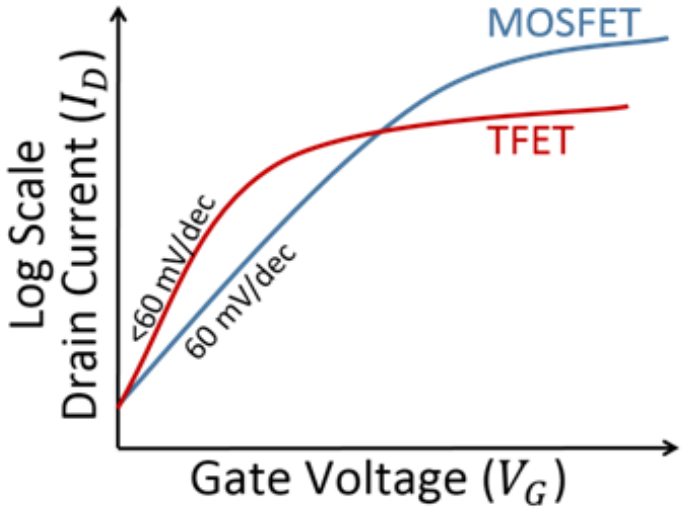

Fig.-1.4: Transfer Characteristics comparison between TFET and MOSFET. Source: Wikipedia.

The present demand for lower power and compact electronic devices is not going to disappear soon. The limitations in power storage of capacity of batteries and the desire of the consumers to stay connected to the network, has clearly marked the beginning of ultra-low power device design. In this scenario, the TFETs can prove to be the worthy successor to MOSFETs, especially in ultra-low power digital applications.

1.5 Organisation of the Thesis:

This thesis has been divided into five chapters. The chapter contents can be described in brief, as follows:

1. Chapter-1, discusses about the evolution of electronic computing, followed by problems associated with MOSFET scaling and why TFETs might be able to succeed MOSFET in the future generation of electronics.
2. In chapter-2, the discussion is concentrated on the quantum mechanical tunnelling concept, its models and finally the model's implementation in commercially available simulators for device simulation.
3. Chapter-3 begins with the discussion on the basic construction of TFET, followed by its working principle and a brief literature study on various TFET structures and designs.

4. In chapter-4, a Broken-Gate TFET structure has been proposed. The choice of such device structure is discussed and the device parameters are optimized. Analytical model for the electrical characteristics of the device is obtained, which is validated against Sentaurus TCAD simulation, followed by comparison with other similar structures available in literature.
5. Finally, the concluding remarks and the scope for future work are presented in chapter-5.

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Chapter-2: Theory of Tunnelling

2.1 What is Quantum Mechanical Tunnelling?

The phenomenon of Band to Band tunnelling is primarily responsible for the current flow in TFETs [7]-[9]. But before we jump in into band-to-band tunnelling, we should get an idea about quantum mechanical tunnelling in general. Unlike in classical mechanics, quantum mechanical particles can tunnel through an energy barrier, even if the energy of the particle is lower than the energy required for overcoming it [1]. The tunnelling phenomenon through a rectangular potential barrier can be described using probability of finding the particle before, inside and after the energy/ potential barrier and can visualized, as in Fig.-2.1.

The probability of a particle tunnelling through a rectangular potential barrier is fairly easy to obtain. By solving the 1-D time independent Schrödinger's equation [10], with the potential term varying as per the region concerned, and using the continuity of wave-function across the regions, the wave-functions (Ψ_i) can be obtained. The tunnelling probability can be obtained as the ration of the magnitude of the wave-functions after the potential barrier and before it, in the direction of particle's trajectory.

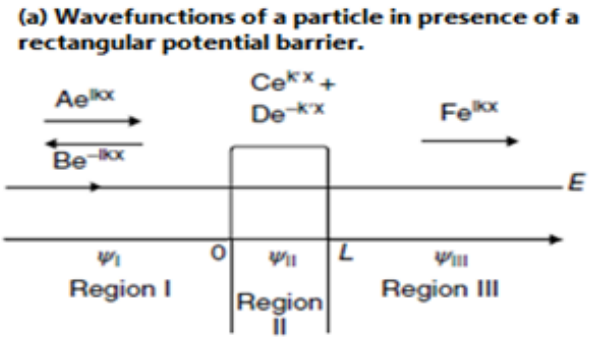

Fig.-2.1: Tunnelling through a rectangular potential barrier.

Source: Page no.-20 of Reference-4.

The 1-D time independent Schrödinger's equation in general can be written as [1], [4]:

$$\frac{\hbar^2}{2m}\frac{\partial^2\Psi_i}{\partial x^2} = (V-E)\Psi_i \tag{2.1}$$

Where, subscript 'i' is for representing regions I, II and III.

The potential profiles for each region can be written as:

$$V(x) = \begin{cases} 0, x \le 0 \\ V, x \in (0, L) \\ 0, x \ge L \end{cases} \tag{2.2}$$

After solving the 1-D T.I.S.E. (time independent Schrödinger's equation) using the boundary conditions and spatially varying potential profile (rectangular in our case) as in eqn. (2.2), we get the region dependent wave-functions, and finally the tunnelling probability as follows:

$$T = \frac{|F|^2}{|A|^2} = \frac{1}{1+\frac{V^2 \sinh^2 k'L}{4E(V-E)}} \tag{2.3}$$

Where, $k' = \sqrt{\frac{2m(V-E)}{\hbar^2}}$ (2.4)

Similar calculations can be performed for triangular potential barrier.

Now, it should be noted that the solution here became easy because of the simplicity of the barrier, in reality; the potential barriers may or may not be in a regular shape. The results thus obtained can be used for random barriers which can be approximated as regular one.

Another popular way of calculating tunnelling probability for general potential barrier is by using the WKB (Wentzel, Kramers and Brillouin) approximation [1], which is a mathematical approach, where we obtain approximated solutions for certain types of

differential equations. The tunnelling probability obtained from WKB approximation is as follows:

$$T = \frac{|F|^2}{|A|^2} = e^{-2\gamma} \tag{2.5}$$

Where, $$\frac{|F|}{|A|} \approx e^{-\int_0^L |k'(x)| dx} \tag{2.6}$$

And $$\gamma = \int_0^L \left| \sqrt{\frac{2m(V-E)}{\hbar^2}} \right| dx \tag{2.7}$$

With the help of eqn. (2.5), tunnelling probability of any particle through a general potential profile can be found for any band structure or material.

2.2 A Brief Introduction to Band-to-Band Tunnelling:

Now, that we have established a basic understanding of how the tunnelling through a general barrier can be predicted, we can concentrate on how the tunnelling is useful in the view of TFETs. In simple words, the band-to-band tunnelling occurs when electrons from the valence band tunnels across the energy band gap to the conduction band. The band-gap is considered as the equivalent to the potential barrier. The band-to-band tunnelling can be shown as in Fig.-2.2. The tunnelling can be direct or indirect in nature.

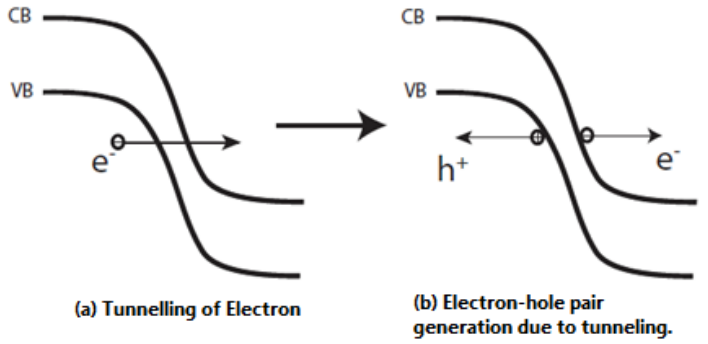

Fig.-2.2: Visualization of Band-to-band Tunnelling.

Source: Reference-5.

(a) ***Direct Tunnelling:*** This occurs in direct band-gap semiconductors, where the maxima of the valence band is aligned with the minima of conduction band at the same 'k' value. The tunnelling phenomenon does not require the help of phonon (or photon depending on the case) or traps to occur. Also, the tunnelling does not cause a change in momentum, especially in the direction perpendicular to the

direction of tunnelling. This type of tunnelling can be seen in gallium Arsenide (GaAs) and not in Silicon (Si) and Germanium (Ge).

(b) ***Indirect Tunnelling:*** This is observed in semiconductors like Silicon and Germanium, where the top of the valence band doesn't align with the bottom of the conduction band at the same 'k'. The tunnelling process requires change in momentum, which is achieved by absorbing and releasing phonons (or photons depending on the case).

2.3 Band-to-Band Tunnelling Models:

The band-to-band tunnelling models can be broadly classified into two types: i. Non-Local Tunnelling models and ii. Local Tunnelling models.

(a) ***Non-local Tunnelling Models:*** In these models, the Schrödinger's equation (S.E.) is solved with respect to the spatial dependence of the parameters. When external voltage/ bias are applied in semiconductors, the shape of the potential barrier is varied, and the variation might not be simple. Thus, in case of Non-local models the solutions might not always end up in a closed form. The band-structure of the semiconductor must be included with the potential (V(x)) while solving for the Schrödinger's equation. All these spatial complications makes the analytical solution to the S.E. almost impossible, hence these types of model are highly dependent on the Numerical Solutions. Hence, such models are mostly used in simulators for accurate results.

(b) ***Local Tunnelling Models:*** The band structure in semiconductors is product of the proximity periodic arrangement of the atoms in the crustal lattice. The energy bands can be viewed in E-k diagram with the bands representing allowed energy states in which the electrons can reside. The band gap separates the valence and conduction bands, acting like a potential barrier. It requires a large amount of energy for an electron through tunnel through this energy gap, in equilibrium conditions.

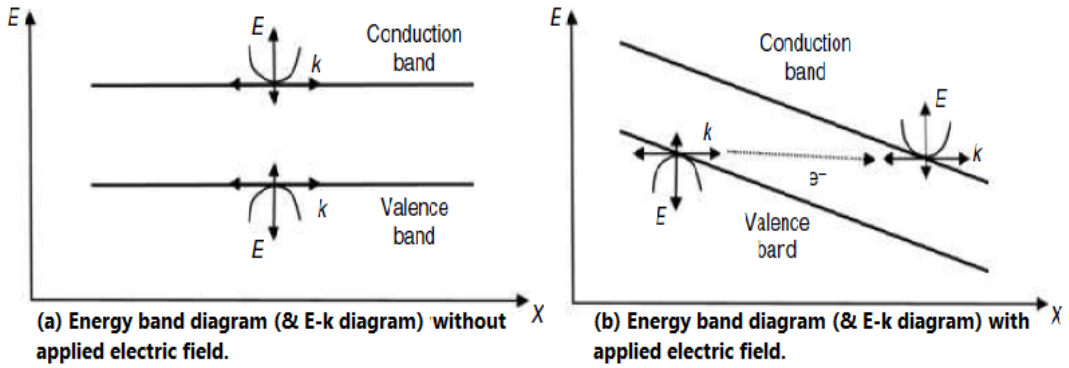

Fig.-2.3: Tunnelling under application of electric field.

Source: Page No.-31 of Reference-4.

If a strong enough electric field is applied, the band structure/ shape would be modified in such a way that the electrons can tunnel through much easily. The application of electric filed aligns the filled valence bands with empty conduction band states in such a way that the potential barrier is thin enough for the electrons to tunnel through, as in Fig.-2.3. If the tunnelling probability is sufficiently large, we can get an appreciable amount of current flow. While deriving the expressions for the local tunnelling models, one of the most important approximations that we have to consider is that the electric field is constant near the region of tunnelling, which is not always true practically. Hence, the local tunnelling model although can arrive at an analytical or closed form expression, the current predicted by such model can vary in accuracy, depending on how cautiously the model is applied to the device under consideration [5]. In these models, the generation and recombination of carriers are not considered, hence the entire tunnelling current is assumed to be dependent on the rate of tunnelling or the tunnelling probability.

2.4 Kane's Local Tunnelling Model:

One of the most important tunnelling models, and probably the most widely used model is Kane's tunnelling model [11]. The popularity of this model is probably due to its simplicity, although the derivation might not be simple. No TFET report is complete

without a discussion on this model. In the upcoming chapter, where we have obtained an analytical expression for our proposed device structure, this model has been used.

The model was originally proposed by ***E.O. Kane*** in the year **1959** [2], [3]. Since the model is local in nature, it deals in E-k diagram rather than spatial coordinates. The derivative terms and the potential profile in the 1-D T.I.S.E. are spatial in nature, hence cannot be directly used for the derivation. The crystal structure in the semiconductor is periodic and the potential distribution is also thus periodic in nature. Hence, the S.E. for such case can be written as follows:

$$-\frac{\hbar^2}{2m}\frac{\partial^2\Psi_i}{\partial x^2}+V_{per}\Psi=E_n\Psi \tag{2.8}$$

Where, V_{per} represents the periodic potential and E_n represents different energies of the energy bands.

The solution for the eqn. 2.8 is known as Bloch function [1] and can be written as follows:

$$\Psi_{n,k}=e^{ikx}u_{n,k}(x) \tag{2.9}$$

Where, $u_{n,k}(x)$ is a function with same periodicity as that of the crystal lattice under consideration. The subscript 'n' is for representing the n^{th} energy band and 'k' the momentum vector for associated wave-function. Finally, a general wave-function for the particle in the crystal can be written as follows:

$$\Psi=\sum a_n(k)\Psi_{n,k} \tag{2.10}$$

Where, $a_n(k)$ is a complex coefficient. Now, if an external field is applied to the device, the S.E. in eqn. (2.8) can be written as:

$$-\frac{\hbar^2}{2m}\frac{\partial^2\Psi_i}{\partial x^2}+(V_{per}-qE_{ext}x)\Psi=E\Psi \tag{2.11}$$

To convert eqn. (2.11) into a function of 'k' instead of spatial coordinate, we need to replace the wave-functions by the Bloch's general wave-function, as in eqn. (2.10). The new form of S.E. thus obtained is a linear combination of Bloch functions, which is as follows: $\sum a_n(k)(\frac{\hbar^2}{2m}\frac{\partial^2\Psi_{n,k}}{\partial x^2}+V_{per}\Psi_{n,k})-\sum a_n(k)qE_{ext}x\Psi_{n,k}=\sum a_n(k)E\Psi_{n,k}$ (2.12)

If, we compare eqn. (2.12) with eqn. (2.8), we can find the analogy between the bracketed terms in eqn. (2.12) and the energy band term E_n. Also, it should be noted that in eqn. (2.12), the there are two energy terms, E_n representing the energy band

energies and E representing the electron energy. The eqn. (2.12) can be written for a single energy, as follows: $a_n(k)E_n - a_n(k)qE_{ext}x = a_n(k)E$ (2.13)

Eqn. (2.13) still contains 'x', a spatial operator. To completely free the equation from this operator, we introduce an "intra-band operator" (iδ/δk) and an "inter-band operator" ($X_{nn'}(k)$) in place of 'x'. The $X_{nn'}(k)$ operator works on an energy band n and other energy band n'. The new S.E. can thus be written as:

$$[E_n(k) - iqE_{ext}\frac{\partial}{\partial k} - E]a_n(k) - \sum_{n'} qE_{ext}X_{nn'}a_{n'}(k) = 0 \quad (2.14)$$

Eqn. (2.14) represents that the electron's position is dependent on the energy band to which it belongs and also on the interaction of the other energy bands with the current one. The intra-band operator deals with spatial interactions inside the energy band, while the inter-band operator deals with the spatial interaction encompassing other energy bands, i.e. it bridges the interaction of electron with multiple energy bands and this soon disappears if the external electric field is removed.

The equation in (2.14), is very tough to solve as it is, hence, we only consider the eigen-functions of the equation, ignoring the $\sum_{n'} qE_{ext}X_{nn'}a_{n'}(k)$ part, as an approximation. This approximation has the consequence of including only the intra-band effects, ignoring the contributions of other bands. After obtaining the eigen-functions in above mentioned manner, they are coupled with inter-band operator $X_{nn'}$, to obtain the tunnelling rates between bands n and n'.

The Kane's model can now be derived for any semiconductor by modelling the periodic potential V_{per} as two interacting bands via k-p perturbation. The band-to-band generation rate thus obtained from the above procedure is as follows:

$$G_{b2b} = \frac{{E_{ext}}^2 {m_r}^{1/2}}{18\pi\hbar^2 {E_G}^{1/2}}\exp\{\frac{-\pi {m_r}^{1/2}{E_G}^{3/2}}{2\hbar|E_{ext}|}\} = A\frac{{E_{ext}}^2}{{E_G}^{1/2}}\exp\{-B\frac{{E_G}^{3/2}}{|E_{ext}|}\} \quad (2.15)$$

Where, "m_r" represents the reduced mass of the charge carrier. The equation presented here is only applicable for direct tunnelling. To incorporate the indirect tunnelling, we should consider the change in momentum associated with it. The generation rate for indirect tunnelling, incorporating the momentum change (i.e. phonon interactions) can be written as follows:

$$G_{b2b} = \frac{{E_{ext}}^{5/2} {m_r}^{1/2}}{18\pi\hbar^2 {E_G}^{1/2}}\exp\{\frac{-\pi {m_r}^{1/2}{E_G}^{3/2}}{2\hbar|E_{ext}|}\} = A\frac{{E_{ext}}^{5/2}}{{E_G}^{1/2}}\exp\{-B\frac{{E_G}^{3/2}}{|E_{ext}|}\} \quad (2.16)$$

Thus, we can observe that the model can be used for either direct or indirect tunnelling by just changing the power to which the externally applied electric field is raised, i.e. 2 for direct tunnelling and 2.5 for indirect tunnelling.

We had begun this section by stating, how popular the Kane's model is, but this model fails to include few important aspects related to the tunnelling phenomenon, such as effects of traps and density of states. Hence, many other tunnelling models (e.g. Hurkx Model, Schenk's Model, etc) have been developed to incorporate what Kane's model has failed to but it has still remained the basis on which these new models are developed.

2.5 A Brief Overview of the Simulator Used:

For our device simulations, in the upcoming chapter, we have used Synopsys Sentaurus TCAD. Here we will briefly discuss about the models that were used during simulations. Although many models were included during simulation of the device, we will concentrate on the tunnelling models. The details of other models such as electron mobility models, quantum correction models, etc can be easily obtained from the simulator manual [6]. Also, it should be noted that, another similar device simulator is commercially available from Silvaco, the ATLAS TCAD.

The simulators available, models the band-to-band tunnelling under the case of generation-recombination. The device simulator considers the device as an interconnection/ mesh of nodes and meshes. During the simulation for TFET, the simulator calculates tunnelling rates at each node, using Kane's model or some variation of it. The band-structure at the specific mesh point under consideration is analysed and taken into account. The different models in simulator mainly differ from each by how they treat the band structures and this adversely affects the TFETs predicted ON current. As discussed before, the models available in the simulators can also be classified into local and non-local models.

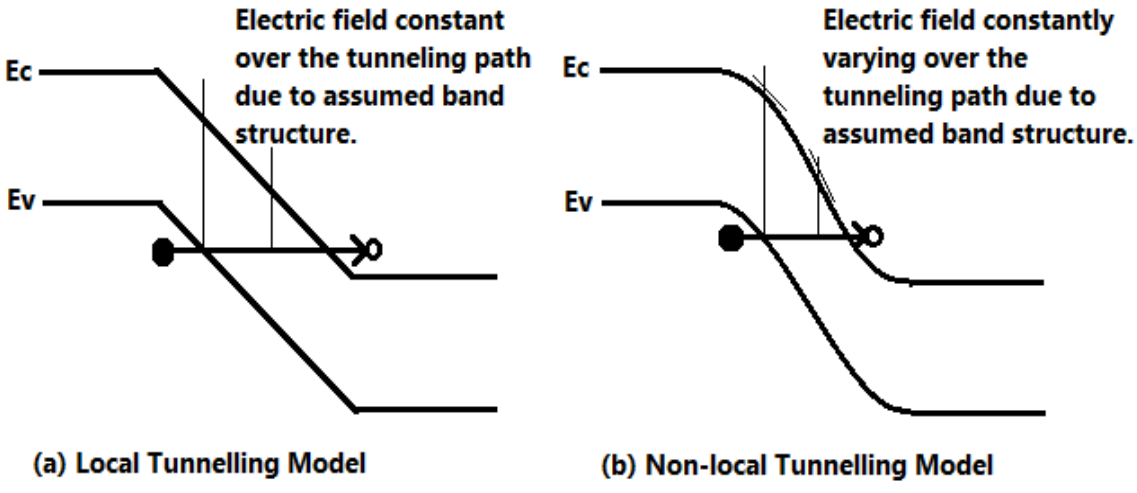

Fig.-2.4: Comparison of the tunnelling models available in device simulator [5], [6].

The local models, as can be seen form Fig.-2.4 (a), approximates the band diagram to be triangular in nature, making the electric field constant at each point in the tunnelling path, as it is the gradient of the energy band. In reality the electric field in the tunnelling path is not uniform and the non-local model incorporates this non-uniformity by considering the band diagram in more detail without linear approximation, as in Fig.-2.4(b). Also, in case of local models, as discussed as the shortcoming in Kane's model, the simulator considers the electron and hole generation profiles to be same. But in case of non-local model the electrons are considered to be generated at the end of the tunnelling path, while the holes at the beginning of the tunnelling path, as in Fig.-2.2 (right). The Sentaurus TCAD, used for our simulations has the capability to simulate both two dimensional and three dimensional device structures. For two dimensional simulation cases, the width of the device is considered to 1um thick by default, and the simulation is done on one negligibly thin slice of the thickness [6]. The simulator contains many Local and Non-local models; here we will discuss a few models belonging to the two main types, which are related to the simulations presented in this report. For detailed information on all the other models and the models discussed here, the "sdevice" part of the Sentaurus manual [6] must be consulted.

2.5.1: Sentaurus Local Tunnelling Models:

The Sentaurus Simulator supports a basic local tunnelling model based on the Kane's model. The band-to-band generation rate for this model is very similar to the expression in eqn. (2.15) derived using Kane's theory and is represented as follows [6]:

$$G_{b2b} = A_{path} \mid F \mid^{P} \exp(-\frac{B_{path}}{E_G}) \tag{2.17}$$

The parameter "P" in the above equation can be set to 1, 1.5 and 2. The generation rate is solely dependent on electric field "F", hence the current at zero drain-to-source voltage (V_{DS}=0V) is non-zero, which is undesirable. The problem of non-zero current is solved in Hurkx model [6], whose generation rate expression is as follows:

$$G_{b2b}{}^{net} = A_{path} D \mid \frac{F}{1V/cm} \mid^{P} \exp(-\frac{B_{path} E_G(T)^{3/2}}{E_G{}^{3/2}}) \tag{2.18}$$

Where, $D = \frac{n.p - n_{i,eff}^2}{(n + n_{i,eff})(p + n_{i,eff})}(1 - \mid \alpha \mid) + \alpha$ (2.19)

The Hurkx model is useful since, it incorporates the temperature dependence of the energy band gap. Hence, once the model is calibrated at a certain temperature, device currents at other temperatures can be predicted. Not only that, the model can show zero generation rates at zero drain-to-source voltage (V_{DS}=0V). Schenk's band-to-band model is another similar model to the ones discussed here. Still, the local models consider uniform electric field at the tunnelling path, thus largely over-predicting the tunnelling currents.

2.5.2: Sentaurus Non-Local Tunnelling Model:

The simulator also supports non-local tunnelling model. The application of such model requires construction of non-local meshes in the regions in which the tunnelling is expected to occur. The addition of non-local mesh is little more time consuming and sensitive. Thus for most of the simulations performed in this report, we have used the Dynamic Non-local Tunnelling which does not require construction of these extra meshes. The model dynamically locates the tunnelling path with the help of energy band structure instead of using the pre-constructed non-local meshes. Thus the model can be used for almost any device structure which is not of conventional planar design.

Unlike the local models, this model incorporates both direct and phonon assisted generation of electron and holes, at the end and beginning of the tunnelling path respectively. The model determines the electric field according to the energy band edge profile at each point in the tunnelling path; hence the electric field thus obtained is dynamically changing. One drawback of this model is that it is not fully compatible with AC analysis and most of the Quantum correction models.

The net recombination rates for the model with non-local electric field assume a very large expression, which is available in the simulator's manual. ***Under consideration of "uniform electric field" the net recombination rate for non-local model*** reduces to:

$$R_{net} = A\left(\frac{F}{F_0}\right)^{P} \exp\left(-\frac{B}{F}\right) \qquad (2.20)$$

The expression is similar to the Kane and Keldysh models which are local in nature. The value of 'P' can be 2 for direct tunnelling (for hetero-structure devices) and 2.5 for phonon-assisted tunnelling, as in Silicon and Germanium devices. The value of F_0 is 1V/cm. Also, the expressions for A and B can be found in the manual, which will be useful for calibration. The default values of 'A' and 'B' are $4x10^{14}$ $cm^{-3}s^{-1}$ and $1.9x10^{7}$ V/cm respectively [6]. The simulator supports up to three non-local tunnelling paths, the default values of 'A' and 'B' for other two paths are zero.

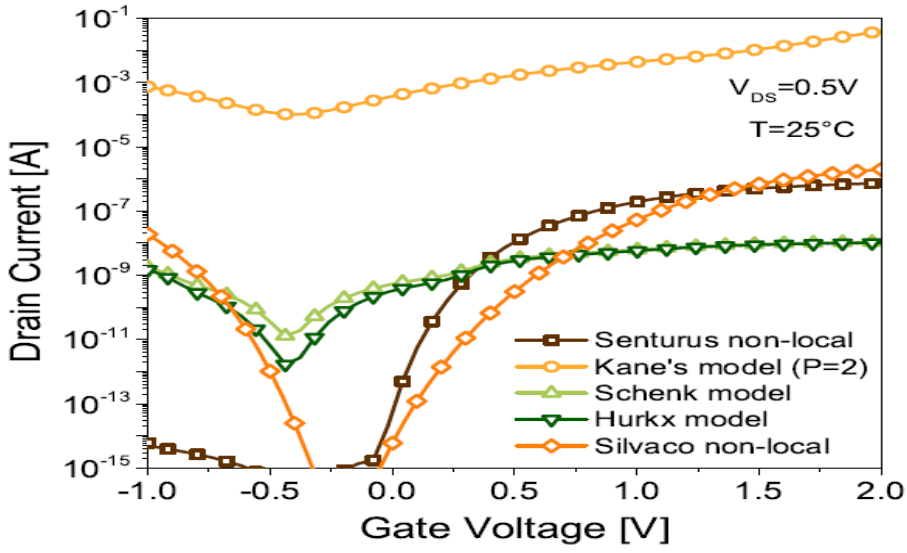

Fig.-2.5: Comparison between different tunnelling models supported by the simulators.

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Fig.-2.5 shows the I_D vs. V_{GS} plots for a 100nm channel length DG-TFET, with different simulation models available in Sentaurus TCAD and also compares the non-local tunnelling model with ATLAS TCAD. All the simulations performed with default parameters. It should be noted that the SILVACO TCAD always predicts the drain current more generously than the Synopsys TCAD.

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Chapter-3: The Tunnel Field Effect Transistor (TFET).

3.1 Basic Construction of TFET:

The most important reason for the popularity of TFET as a replacement of MOSFET is the similarity in construction. If the doping in the source region of a MOSFET is reversed, we obtain a basic TFET. Also, the channel region in TFET is made intrinsic or very lightly doped in nature, unlike MOSFET, where the channel is mostly lightly doped. The basic single MOSFET and TFET structures are shown in Fig.-3.1.

For an n-channel TFET, the source is p-type doped and the drain is n-type doped. The doping is just reversed for p-channel TFET. Similar construction is followed for Double gate structure [35], [36]. Almost all of the MOSFET structures [31], [34] can be converted to TFET, just by alternating the source doping.

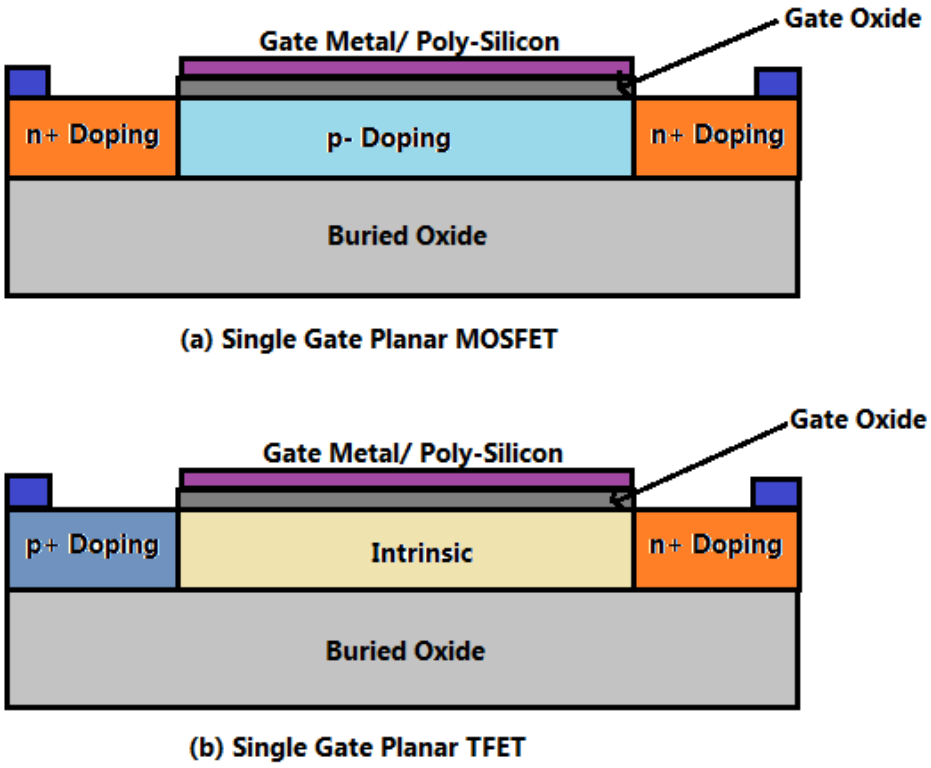

Fig.-3.1: Comparison between basic MOSFET and TFET Structure.

3.2 Working Principle of TFET in Brief:

The Tunnel Field Effect Transistor (TFET) belongs to a section of devices known as steep sub-threshold devices. The basic working principle of TFET is based on quantum mechanical tunnelling. The carriers tunnel through the band-gap, which acts as a potential barrier in the source channel junction. Due to the fundamental difference in carrier generation/ transport phenomenon from the MOSFET [37], the TFETs can achieve sub-threshold slopes lower than 60mV/decade. The tunnelling theory is briefly described in Chapter-2.

The tunnel field effect transistors can be visualized as gated PIN diodes. The potential at the gate is used to control the tunnelling barrier height, thus effectively controlling the device current. The device has extremely low OFF state current, as the leakage current is mostly due to a reverse biased diode. The ON current of the device is comparatively

lower than MOSFET, but the situation can be improved by using high-k dielectrics and a method called line-tunnelling. In the TFET structure presented in Fig.3.1 and also in similar double gate structures, the band-to-band generation is confined to a small circular region or a point at the source-channel interface, near the gate oxide-semiconductor interface only. Thus the volume over which the carrier generation takes place is small, leading to small ON currents. Such type of tunnelling is aptly called Point tunnelling.

a. **Point Tunnelling:** This is the most common type of carrier generation method. The maximum carrier generation rate is almost confined to a point. The barrier in OFF state is too large for the electrons to overcome or tunnel. But as the gate potential is increased (assuming n-TFET), the conduction band in channel region aligns with the valence band of source region. The valence of p-type source is full of electrons but the intrinsic channels conduction band has no free states for the electrons to tunnel. With sufficient drain voltage, the conduction band at the channel starts to get Free states and hence the electrons now can tunnel and contribute as device current. Thus, unlike MOSFETs, there is no ON state without current flow. Also, the TFET has two threshold voltages, one for the gate bias and another for drain bias. Fig.-3.2 shows the energy band structure for n-TFET in ON and OFF state.

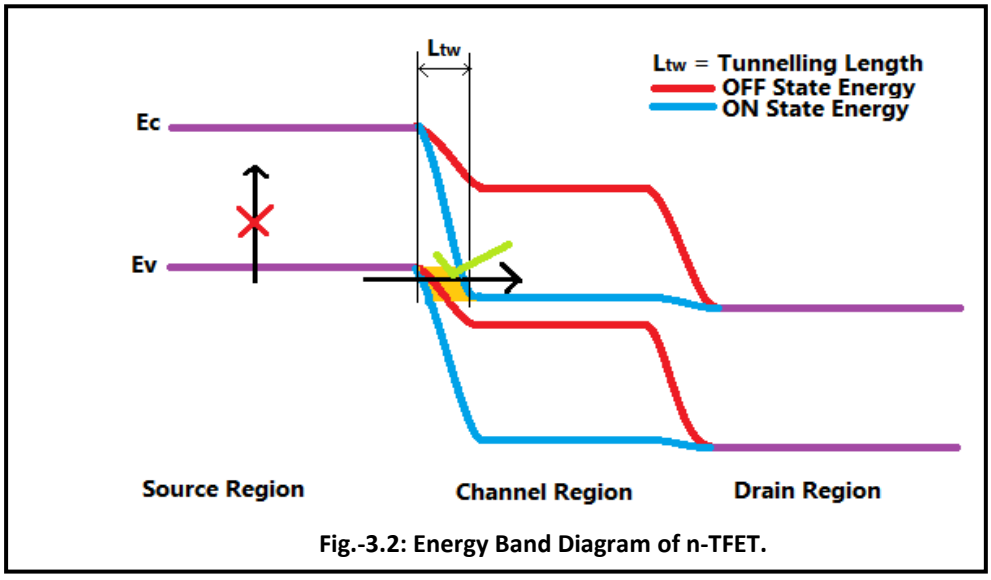

Fig.-3.2: Energy Band Diagram of n-TFET.

Line Tunnelling: In order to increase the ON current in TFET, often the method of line tunnelling is applied. Here a gate overlap is created over the source region. The electric

field thus formed has to in a direction that aids tunnelling. The electrons from the inner parts of the source tunnel to the inversion region formed near the surface of the source (for n-TFET). The carrier generation takes place in a line, near the source-gate oxide interface, hence the name. Since the carrier generation area/ dimension is larger than point tunnelling, the ON current increases. The phenomenon of point and line tunnelling are illustrated in Fig.-3.3.

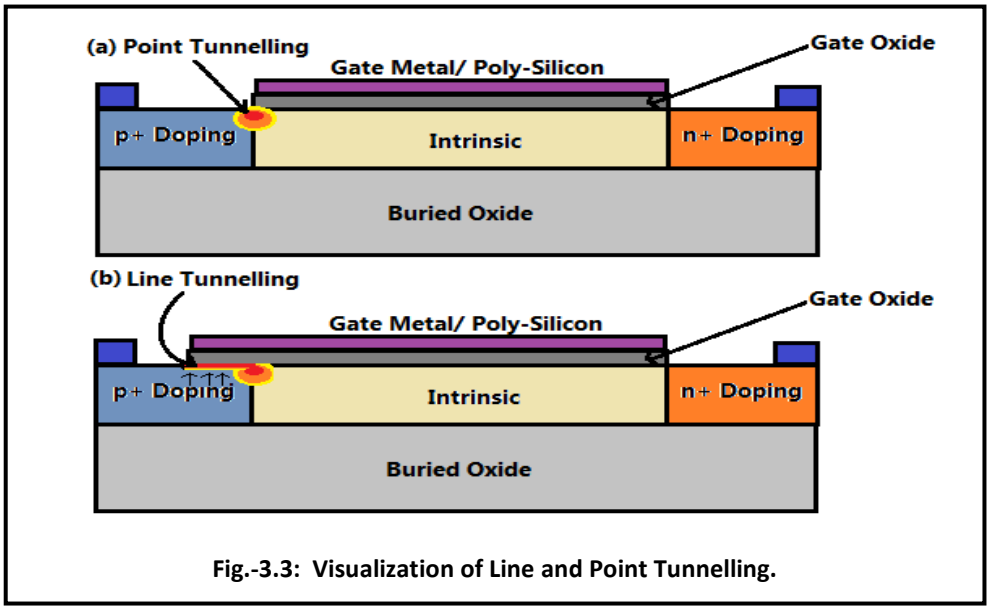

Fig.-3.3: Visualization of Line and Point Tunnelling.

3.2.1: Pinning of Channel Potential:

As discussed earlier, the gate bias causes the energy band in the channel to modulate, thus enabling or disabling tunnelling of carriers. However, for very high gate voltages ($V_{GS} > V_{DS}$), the inversion charges generated at the semiconductor-gate oxide interface becomes comparable to the electron density in the n-type drain region (assuming n-TFET). In such case the channel can be considered to be effectively shorted or pinned to the drain, this phenomenon is known as channel pinning. The pinning of the channel potential does not occur precisely at $V_{GS} = V_{DS,}$ but near to that value, as the inversion charge varies constantly. Due to pinning, the drain current becomes less responsive to the change in applied gate voltage. After a certain value of gate voltage, the increase in drain current, corresponding to the change in gate voltage reduces. The reduction in drain current is due to the fact that the conduction band does not dip further to place more unoccupied states for electrons to tunnel from the valence band in source region. The pinning of channel potential is demonstrated in Fig.-3.4.

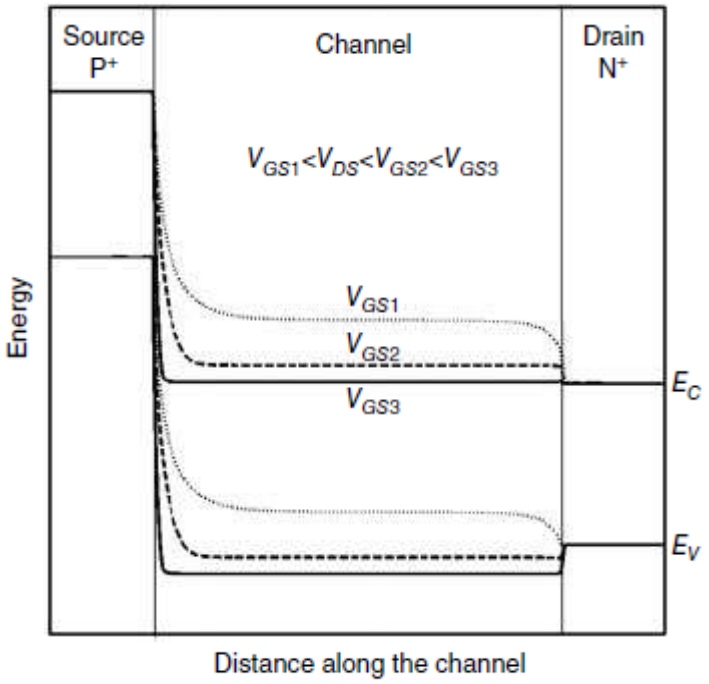

Fig.-3.4: Channel Pinning in N-TFET.

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3.2.1: Ambipolarity in TFETs:

The characteristic curve of a basic TFET reveals that they conduct for negative values of gate voltage in case of n-TFET and vice-versa for p-TFET. The energy band diagram in case of ambipolar conduction is illustrated in Fig.-3.5.

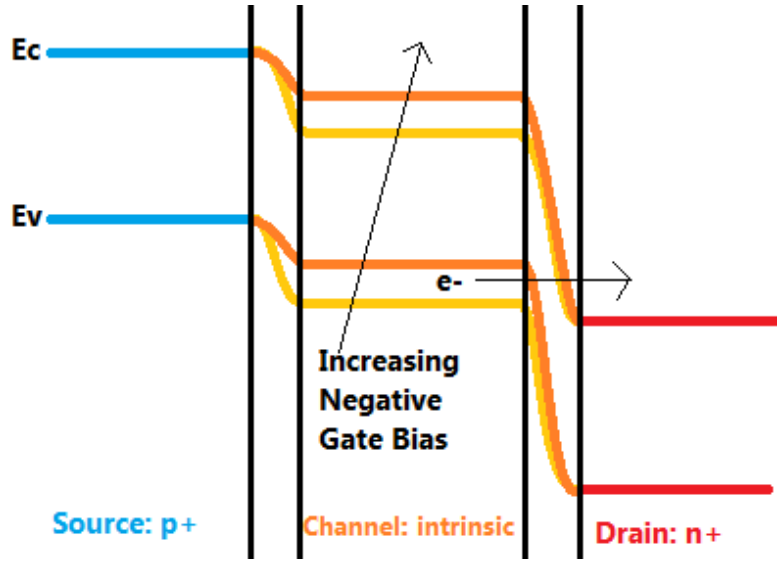

Fig.-3.5: Energy Band Diagram along the surface of n-TFET during ambipolar conduction at positive drain bias.

With a certain amount of negative gate bias, the valence band in the channel region starts to align with the conduction band in the drain region. The positive drain bias causes the electrons to tunnel across the channel-drain junction, which results in drain current conduction. This behaviour is known as ambipolarity in TFET. The problem with ambipolarity is that it degrades performance when TFETs are used in digital circuit applications. The reverse conducting behaviour of TFETs make to them harder to use in applications running on bi-polar or even uni-polar power supplies. Any amount of reverse voltage on gate during the supposedly OFF state of the device will make it conduct and increase leakage and affect the voltage level of the logic circuit. Thus a plethora of solutions for reducing the ambipolar nature of the TFET have been proposed with varying degree of success. A few of the solutions/ modifications done to TFET structure for reduction of reverse conduction is discussed in the upcoming section.

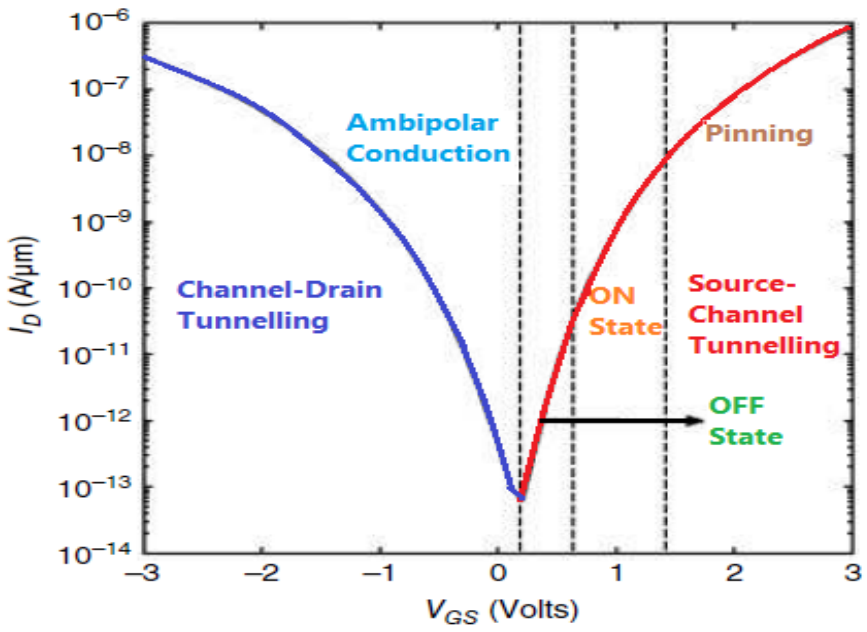

Fig.-3.6: Transfer Characteristic of n-TFET, showing all the important regions of operation.

Source: Page no.-53 of Reference-1.

Fig.-3.6 shows the transfer characteristic of n-TFET, highlighting the ambipolar conduction and channel pinning.

3.3 A Brief Literature Review on various TFET Designs for Performance Enhancement:

3.3.1. Using multiple Gate Oxide Materials: The use of high-k dielectric is desirable in TFETs as their ON current is inherently smaller than MOSFETs. With high-k dielectrics, the gate to source electric field can be enhanced, leading higher band-to-band generation rate and hence, higher ON currents. Unfortunately, the same is also true for the channel-drain junction, thus the reverse conduction current also increases with the use of high-k dielectric. The solution to this problem is to use separate dielectrics near the source-channel and channel-drain junctions. The high-k gate oxide should be placed near the source and the low-k dielectric near the drain, in order to maintain the high ON current and reduce the reverse gate voltage current. The device structure is available in [2]. The single gate structures are mostly outdated and currently only Double Gate TFETs are of interest in research.

The lengths of the high-k and low-k dielectrics can be optimized to obtain the least ambipolar nature and highest ON current. The optimization for high-k dielectric length for the dual material gate oxide structure has been performed in the work of R. Narang et al [2] where it is referred as the hetero-gate (HG) TFET. The result thus obtained can also be found in page no.-5 of reference-2. The doping at source and drain are p+ and n+ respectively with concentration of 10^{20} cm^{-3}. The high-k dielectric is HfO_2 with $k=21\varepsilon_0$ and low-k is SiO_2 with $k=3.9\varepsilon_0$. The channel length is kept at 45nm, with silicon thickness of 10nm and oxide thickness of 3nm.

It is observed that the I_{ON} degrades for both the extreme case of high-k dielectric length [2]. The ambipolarity and gate capacitance increases with increasing length of high-k dielectric.

3.3.2. Using Multiple Materials as Gate Metal: To enhance the drain current and make it comparable to MOSFET and at the same time subdue the inherent ambipolar nature of the TFET, two different materials can be used over the channel with different work function [3]. Basically the variation in work function is made such that there is an increase in the electric field at the source channel junction so as to effectively increase the tunnelling of the carriers, and at the same time just the opposite at the drain end is achieved. Thus, there is a boost in the ON current and reduction in ambipolar current. If looked closely, the principle is very similar to dual material gate oxide implementation. The construction of Dual Material Gate Metal TFET is shown in page no.-2 of reference-3. The length of auxiliary gate and tunnelling gate can be optimized to obtain highest possible ON currents and lowest possible ambipolar current. The gate length optimization curves are presented in page no.-3 of reference-3. All the data presented here are borrowed from the work of S. Saurabh et al [3].

The basic idea for such device (n-TFET) is to place the metal with lower work-function (known as the tunnel gate) near the source-channel interface and metal with higher work-function (known as the auxiliary gate) at the channel-drain interface. The work-function of the tunnelling gate can also be optimized, given the metal with the required work-function is available and compatible with the fabrication procedure.

From the work-function variation curve in page no.-3 of reference-3, it is clear that the ON current increases with lower work-functions. Finally, we need to compare the Dual metal gate with our conventional single metal gate TFET. The comparison is again performed by S. Saurabh et al [3], and available in page no.-3 of reference-3. The comparison between conventional and dual metal gate TFET clearly shows that the DMG DGTFET is better than SMG DGTFET with lowest leakage currents and comparable ON currents.

The improvement over the Dual Metal Gate TFET was proposed by N. Bagga et al [4]. The renovated device is provided with triple metal at the gate, instead of two. The gate work-function engineering possibilities are greater with more number of metals, as the effectiveness of work-function control over channel improves due to more spatial resolution. The paper under consideration [4], also includes analytical modelling of the device, but here we will only concentrate on the qualitative behaviour of the device.

The transfer characteristics of the TM-DGTFET for varying silicon film thickness are shown in page no.-6 of reference-4. The oxide thickness for the device is 2nm, with overall channel length of 60nm with different metal lengths: L_1, L_2, L_3 values of 10nm, 20nm and 30nm respectively. The doping concentrations are $2x10^{20}$ cm^{-3} p-type at source and n-type at drain.

3.3.3. Lightly Doped Drain: The ambipolar nature of TFET is caused by channel-drain tunnelling. The ambipolarity in TFET becomes prominent when the channel length goes below 10nm [5], both the OFF current and sub-threshold swing increases, because of source-drain tunnelling. The tunnelling of electrons is possible only if filled valence band aligns with empty conduction band states, which can easily occur in degenerated semiconductors. Thus, to reduce channel-drain tunnelling, the doping in the drain can be reduced, as the channel is already very lightly doped. This reduced drain doping effectively lowers the ambipolar current.

The TFET used for simulation in reference-5, is a Hetero-TFET, with Source of AlGaAsSb and Channel of InAs. The plot in page no.-2 of [5] shows that with decrease in drain doping, the sub-threshold swing, OFF current and ambipolar conduction reduces.

The reduced drain doping has the disadvantage of increasing the contact resistance at the drain. Thus, in most cases a lightly doped pocket region is formed before the drain of same type of doping as that of the drain. The drain can now be highly doped for maintaining low contact resistance without affecting the OFF state leakage or ambipolarity.

3.3.4. PNPN or NPNP TFET Structure: One way of increasing the drain current is to introduce a small but highly doped region near the source of opposite doping type to that of the source. The pocket doping causes an augmented dip in the conduction band near the valence band in the source (considering PNPN device) even at V_{GS}=0V. This increases the tunnelling probability as the number of aligned states for electrons to tunnel increases. Due to such doping, the lateral electric field also increases, meaning more current due to higher band-to-band generation. According to [6], the optimum

pocket doping length is around 4nm. If the pocket doping created is too long, the region might not be fully depleted causing the device to lose Gate control, thus curtailing the sub-threshold swing. Also, fabricating devices with very narrow pocket doping is difficult. Even if by implantation a thin doping is introduced, the dopants diffuse during other high temperature fabrication steps and thus increasing the overall pocket doping length. For a basic PNPN structure, the Source is p+-doped, a pocket doping of n+ type is introduced, followed by very light p-type doped channel, ending with n+ doped Drain region.

3.3.5. Raised Germanium Source Structure: The band-to-band generation rate increases with use of lower band gap materials, as Germanium (Ge) [7]. Thus, using lower band gap semiconductor at the source increases the ON state current. As an improvement to this concept S.H. Kim, et al [7] proposed the raised germanium source TFET. The proposed structure increases the overlap of gate with the source, thus increasing the chance of line tunnelling.

The proposed structure is illustrated in page no.-2 of reference-7. The Ge-Source region is doped p-type with concentration of $1x10^{19}$ cm^{-3}. Drain is doped n-type with concentration of $1x10^{19}$ cm^{-3}. The silicon thickness is 100nm, with effective SiO_2 thickness of 1nm. The channel region is moderately doped at $1x10^{18}$ cm^{-3} p-type. The gate length is kept at 30nm and the buried oxide thickness at 200nm. The Germanium layer thickness of 25nm for partially elevated and 65nm thick for fully elevated structure is grown in-situ over the initially present silicon source. The simulation is performed with calibrated TCAD model. The calibration curve and the transfer characteristics are shown in page no.-2 of [7]. The calibrated local band-to-band tunnelling model's coefficients are: $A = 1.46 \times 10^{17}$ $cm^{-3}s^{-1}$ and $B = 3.59 \times 10^{6}$ Vcm^{-1}.
The raised source structures provide good amount of ON current. The current can further be increased by using pocket doping, as mentioned in the previous section.

3.3.6. Si-Ge Source UTFET: The device structure was proposed by W. Wang et al [8]. The device has a U-shaped channel, due to which an effectively longer channel can be contained in a smaller dimension. Because of the longer channel, the leakage current is reduced. On a basic UTFET structure with p+ doped source followed by p+ doped Si-Ge

layer, an n+ doped delta layer with doping concentration of $5x10^{19}$ cm^{-3} is introduced. This delta layer reduces the band-to-band tunnelling length, hence effectively increasing the ON current. The basic UTFET structure and the delta doped structures are presented in page no.-1 of reference-8. The depth of the TFET gate is 120nm, length of the gate is 16nm and the oxide thickness is 1.2nm.

The U-Gate TFET can achieve relatively high ON/ OFF ration of current, with a value of 10^8, as observed from the figure in pageno.-2of [8]. The mentioned ON/ OFF ratio can be achieved at relatively low voltages, V_{GS}=0.7V and V_{DS}=0.7V. The results are better than similar planar-TFET with 16nm channel length.

3.3.7. L-Shaped TFET (LTFET): The device was proposed and fabricated by S.W. Kim et al in the year 2012 [9]. The device is called L-Shaped TFET, because the channel region of the TFET resembles the letter 'L'. The LTFET is fabricated using Mesa etching technology, especially the elevated source region. The gate oxide is SiO_2 with a thickness of 2nm. High-k dielectric (like HfO_2) can be added by Atomic Layer Deposition (ALD) technique for enhanced ON currents. The elevated source region makes line tunnelling possible, as the gate region is directly over/ side by side with the source, increasing the region over which the tunnelling is possible. The source, drain and channel region are doped p+, n+ and p- with concentrations $1x10^{20}$, $1x10^{18}$ and $1x10^{15}$ cm^{-3} respectively. The device structure is provided in page no.-2 of reference-9.

The transfer characteristic of the LTFET along with its comparison with a planar TFET is shown in the figure at page no.-3 of [9]. Clearly, the LTFET has more ON current and better sub-threshold swing than the planar TFET, as evident from the figure.

The main drawback of LTFET is that it suffers from significant ambipolarity problem. The solution to this problem was provided by C. Li, et al [10] in 2018. By introducing a low doping region near the drain, the drain side tunnelling can be arrested, resulting in lower ambipolar conduction. The proposed HGD (Hetero-Gate-Dielectric) and LDD (Lightly Doped Drain) shows negligible ambipolarity and good RF-performance, according to simulation data. The LDD region reduces ambipolarity without affecting the Drain region doping, which maintains low contact resistance unlike other device

structures where the drain doping is reduced to curb the ambipolarity which results in increased contact resistance.

The paper compares performance of four different LTFET structures, with combinations of with and without HGD and LDD. It was observed that HGD-LDD-LTFET shows the lowest ambipolar conduction, with very slight reduction in current. Hence, the HGD-LDD structure is desirable.

The transfer characteristics and the device structures of the new proposed structure of LTFET are presented in page no.- 2 of [10].

3.3.8. L-Shaped Gate TFET (LG-TFET): The device structure was proposed by Z. Yang in year 2016 [11]. The device has a gate structure similar to the UTFET, but with an extended region over the source. This extended region helps in increasing the drain current by ~50% over the basic L-Channel TFET. Also, a pocket doping is added for the same purpose of increasing the drain current. The device structure is depicted in page no.-1of reference-11.

The transfer characteristic of the LG-TFET is compared with the L-TFET and UTFET structures in page no.-2 of [11]. Clearly, the LG-TFET has more ON current and better sub-threshold slope than the others. The advantage of this structure is that it combines the merits of both LTFET and UTFET structures. The doping concentrations are: Ns =$1x10^{20}$ cm^{-3}, N_D=$1x10^{20}$ cm^{-3}, N_C=$1x10^{17}$ cm^{-3} and n+ pocket doping N_P = $1x10^{19}$ cm^{-3} with 5nm thickness. The oxide thickness is kept at 2nm. Height of Source region (H_s) is 30nm and that of Drain region (H_d) is 10nm. The depth of Gate region (H_g) is 40nm with a width (W_g) of 6nm.

3.3.9. Doping-less TFET: The Doping-less TFET [12] is built on the concept of charge plasma. With the use of metals with appropriate work-functions at source and drain, the intrinsic semiconductor at source and drain region can be made to behave as n-type or p-type as per requirement. The absence of doping makes the device exclusive of any high-temperature fabrication steps. Hence, it is suitable for making mono-crystalline silicon based device on variety of substrates, especially glass. It should be noted that unlike schottky diodes, where a junction is formed between metal and semiconductor,

in doping-less TFET, the main working junction, i.e. the source-channel junction is still a homo-junction. The device structure is as presented in page no.-1 of [12].

The whole device is constructed using intrinsic silicon with n/p-type doping concentration of $1x10^{15}$ cm^{-3}. The carrier concentration at the source and the drain are induced by the respective metal contacts, especially under the overlap regions. The overlap regions are comprised of Metal-Oxide-Silicon layer. To maintain uniform carrier concentrations over the entirety of the source and drain region, the silicon film thickness is kept lower than the debye length. The debye length is given as $L_D=((V_T\varepsilon_{Si})/(qN))^{0.5}$, where is the '$V_T$' thermal voltage, 'q' is the magnitude of electronic charge, 'ε_{Si}' is the permittivity of silicon and 'N' the carrier concentration in the body. The silicon body's doping concentration can be up to$1x10^{17}$ cm^{-3} without any significant variation in the result. This is particularly helpful as the device body can be accidently doped during the fabrication process.

The source and drain doping for this TFET is created by the charge plasma concept as in [13]. For creating a p+ equivalent source, platinum with work-function 5.93eV is used at the source region. Similarly, Hafnium with work-function 3.9eV was employed at the drain region. The gate metal can be either aluminium or poly-silicon as per requirement. A thin SiO_2 film of 0.5nm was placed between source metal and silicon film at the top, to avoid silicide formation. The oxide thickness at the drain end was kept at 3nm, as little less carrier concentration is desirable at the drain for prevention of ambipolarity, as discussed in earlier sections [5]. The channel of the device is kept at 50nm. The simulated results for the doping-less TFET are obtained using ATLAS Silvaco's non-local tunnelling model. The transfer characteristic of the device and conventional double gate TFET of similar dimension are compared in the plot at page no.-4 of [12]. The comparative plots from [12] reveal that the performance of doping-less TFET is similar to that of the conventional TFET.

3.3.10. III-V Semiconductor Homo and Hetero-Junction TFETs:

The work of D.K. Mohata et al [14], demonstrates the homo-junction and hetero-junction III-V TFETs. The band engineered III-V TFETs show incredibly large ON currents at moderately low voltages, resembling the ON state of MOSFETs but with faster turn OFF.

The study is based on four different TFET structures. The devices were epitaxially grown using solid source MBE. The $In_{0.53}Ga_{0.47}As$ homo-junction or "**Large Eg HomJ**" TFET and the $GaAs_{0.5}Sb_{0.5}/In_{0.53}Ga_{0.47}As$ lattice matched hetero-junction or "**Moderate HetJ**" TFET were grown layer by layer on lattice matched InP substrate. On the other hand, the $In_{0.7}Ga_{0.3}As$ homo-junction or "**Small Eg HomJ**" TFET and the $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ lattice matched hetero-junction or "**High HetJ**" TFET was also grown by layers, metamorphically on lattice mis-matched Indium-Phosphide substrate, using linearly graded $Al_xIn_{1-x}As$ as buffer. The device structures under consideration can be illustrated as block diagrams in page no.-2 of [14].

The energy band alignment diagrams for the TFET structures under consideration are shown in page no.-2 of [14]. With increase in the Indium mole-fraction in $In_xGa_{1-x}As$ (i.e., from x=0.53 to x=0.7), the energy band-gap E_G or the effective tunnelling barrier $E_{B,eff}$ reduces from 0.74eV to 0.58eV. A type-II staggered hetero-structure is formed from the lattice matched $GaAs_{1-y}Sb_y/In_xGa_{1-x}As$ hetero-interface. Again, with increase in 'In' mole-fractions from x=0.53 to x=0.7 and 'Sb' mole-fractions from y=0.5 to y=0.65 i.e., Moderate HetJ to High HetJ, the effective tunnel barrier $E_{B,eff}$ reduces from 0.5eV to 0.25eV because of the increase in stagger.

The transfer characteristics of the III-V TFET structures, as discussed till now are shown in page no.-3 of reference-14. All the data presented in these curves are experimental in nature [14]. The "High HetJ" TFET has the highest ON current. The homo-junction TFETs show better I_{ON} to I_{OFF} ratios but lower ON currents than the hetero-junction ones.

3.3.11. Ferroelectric TFETs:

The use of ferroelectric material as dielectric in MOSFET was demonstrated by Salahuddin and Datta [15]. The ferroelectric materials are supposed to display negative capacitance behaviour, which can be used to multiply the voltage supplied at the gate of the device. The effect of such voltage multiplication at the gate of any field controlled device results in very small sub-threshold swings. No direct experimental proof has been found for the existence of negative capacitance. In spite of the lack of evidence for negative capacitance, the use of ferroelectric material in general has the advantage of acting like an active capacitor, i.e. the permittivity of the material changes with application electric field. The ferroelectric material is in general stacked with the conventional gate oxide of the device.

The ferroelectric TFET device was proposed by A.M. Ionescu et al [16]. The device under consideration is a single gate TFET, but with tri-layer gate oxide. The first layer, above the silicon is SiO_2, followed by a high-k dielectric (Al_2O_3) and finally the ferroelectric material. The ferroelectric material used is a Fe-copolymer, poly-vinylidene fluoride tri-fluoroethylene [P(VDF-TrFe)]. An effective gate oxide thickness of 14nm was achieved, which implies that the gate leakage will be negligible. The thermally formed SiO_2 thickness is 2nm, followed by 5nm thick Al_2O_3 formed by ALD (atomic layer deposition) and finally 30nm thick P(VDF-TrFe). The buried oxide thickness is 150nm, formed on p-type uni-bond silicon substrate of 65nm thickness. The device is simulated using Sentaurus TCAD using Schenk band-to-band tunnelling model. The qualitative transfer characteristic and device structure are shown as a figure in page no.-2 of reference-16.
The experimental and simulated data for channel length and width of 5um and 20um respectively are plotted in page no.-4 of [16].The characteristic curve of Ferroelectric TFET shows hysteresis of about 1V. This property can be levied for implementing single transistor RAM cells.

3.3.12. Phase Change TFET (PC-TFET):

In recent years, the phase change materials (such as correlated functional oxides) have shown promise as good beyond CMOS solution in electronics. The phase change materials are interesting as they exhibit phase transitions with respect to external physical stimulus [18], [19]. The phase transition can cause large change in electrical conduction property.
Currently, Vanadium Dioxide has gained much attention as a phase change material. It shows metal-to-insulator phase transition (MIT) with temperature. The critical temperature at which the transition happens is 340K for bulk vanadium dioxide. Below the critical temperature the VaO_2 is in a monoclinic phase, but above the critical temperature it transitions to a tetragonal rutile structure. The tetragonal phase has energy band gap of ~0.6eV at the 3d conduction band, thus it is conducting in nature unlike the monoclinic phase which behaves as an insulator. The change in conductivity is in order of five decades, which is considerable and can resemble a switch. The only drawback of the VaO_2 based two-terminal MIT switch is that the leakage current is not negligible, due to its small band-gap in the monoclinic/ insulating state.
Initially, MOSFETs based on VaO_2, as semiconductor, were designed but the conduction modulation due to the gate voltage was not significant [20]-[22]. To solve this problem,

electrolyte based gate MOSFETs were introduced, so that the ionic gate electrolyte and vanadium dioxide interface would increase the effective electric field. This solution to weak conduction modulation served its purpose, but it was found that the electrolytic gate devices were slower than conventional devices [23]-[25]. Thus, a new design of transistors, incorporating phase change materials was desired. Here we will be discussing about the new PC-TFET device proposed by W.A. Vitale et al [17] in Scientific Reports published by Nature.

The qualitative transfer characteristic of the PC-TFET device and other contemporary devices are illustrated in page no.-2 of the paper [17]. The PC-TFET shows hysteresis behaviour similar to the ferroelectric TFET.

The MIT material when used in Gate region of the TFET helps combat the leakage as the gate itself is insulated by the presence of the gate oxide. Alternatively, the MIT material can be used in series with the channel, after the Source, where the ON current flow is comparable to the two terminals MIT switch's ON current and will not be hindered. At the same time the leakage current will be controlled by both the channel and MIT switch's OFF state itself.

In the implementation of PC-TFET using MIT switch at the gate and source, the state transition of the MIT switch is controlled by the gate voltage V_{GS}. The state transition induces an internal differential amplification ($dV_{GS,int}/dV_{GS} >> 1$) of the voltage drop between the gate and the source ($V_{GS,int}$), which results in very steep rise in the drain current. The experimental transfer characteristics of the PC-TFET for MIT switch at the Gate and MIT switch at the Source are presented in page no-5 and page no.-6 of reference-17 respectively.

The TFET used for implementation with the MIT switch is a Strained Silicon Gate All Around (GAA) Nanowire (NW) TFET. The cross section of the Nanowire used in the TFET is $40x5nm^2$. The gate length of the TFET is 350nm. The concept of Gate All Around TFET (GAA-TFET) is discussed in the upcoming section.

3.3.13. Tri-Gate or Fin-TFET: The Fin-FET or Tri-Gate structure is now commercially in use for MOSFETs [27], first introduced by INTEL in its 22nm technology node. Hence, like all the other MOSFET structures/ architecture, this structure has also been translated to TFETs [26]. The increased number of gates or the increase in effective area of channel under the gate region leads to desirable outcomes due to enhanced Gate

control, such as Higher ON currents, steeper sub-threshold swings and lower short channel effects. Since, the difference between TFET and MOSFET is mainly on the Source doping, it is very likely that the Fin-TFET will come into production, like the Fin-FET.

3.3.14. Gate All Around TFET (GAA-TFET): The increased gate control, observed in double and triple gate TFET is further enhanced in Gate All Around (GAA) TFET [28]. A basic structure of Gate All Around Nanowire TFET is mostly implemented as a cylinder. The structure consists of a silicon nanowire with diameter in order of tens of nanometres, which is followed by an oxide layer of a few nanometres in order and finally, the whole structure is wrapped around by the gate metal. Such all around wrapping of gate over the channel provides excellent electrostatic control. The short channel effects are at minimum, because all the electric fields emanating from the drain end at the gate without reaching the source region as there is no path available, unlike double and triple gate TFETs. The geometry increases the tunnelling area, and electric field at the source-channel junction, effectively increasing the ON current. Steeper sub-threshold swings and lower DIBT (drain induced barrier tunnelling) than the Fin-TFET are observed.

3.3.15. Carbon Nanotube and Graphene TFETs: Till now we have discussed mostly about silicon TFETs, which due to the existing and matured fabrication technology are easier to manufacture. The main drawback of Silicon TFET is that the ON current is very low, which is in order of 10s to 100s of uA/um. Such ON currents are far cry from the ON currents provided by MOSFET, which makes the TFETs incompatible as CMOS replacement. Using Germanium at the source might alleviate the problem a little bit but the results are far away from ideal requirements. The III-V TFET structures show ON currents comparable to MOSFETs, but their practical realisation is limited with the fabrication technology. Also the III-V TFETs fail to conserve the steep sub-threshold slopes over a larger span of gate voltages. Thus, recently designing TFETs with different materials have become popular. The two-dimensional materials like Graphene and Carbon Nano-tubes (CNTs) are very promising [1].

The advantage of such 2D materials is that they have very less amount of dangling bonds, which results in exceptionally high gate controls leading to steeper sub-

threshold swings. Also, the band-gap in case of graphene is very low, which leads to higher ON currents. Similarly in CNTs faster transport of carriers are possible due to high mobility in such materials. Recently Graphene nano-ribbon TFET and CNT-TFET have shown exceptional performances but their difficult fabrication is a trade-off.

In this section we have discussed about various TFET designs for performance enhancements. The list by no means is exhaustive, yet we have qualitatively covered a diverse range of TFET structures. Some other important TFET structures are the split-drain[29], [32], T-shaped channel [30] and graded metal gate [33], [38], [39] structures. The split-drain and graded metal alloy gate structures reduce the ambipolar conduction in TFET by drain engineering and by controlling the gate control over the channel (i.e. achieving desired energy band diagram in the channel of the device, from source to drain,) respectively. The T-shaped channel design helps increase the device current by the phenomenon of line tunnelling, at the same time also curtails the ambipolarity.

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Chapter-4: Analytical Modeling and Simulation based Optimization of Broken Gate TFET Structure for Low Power Applications

4.1 Introduction:

From the discussion in Chapter-1 it is clear that the trend to follow the famous Moore's Law has led to tremendous reduction in size of the transistors [1]. This drastic reduction in transistor dimensions helped in packing a huge amount of functionality in the ICs, but such amount of scaling has increased the power dissipation and introduced various short channel effects (SCEs) in MOSFETs[2], [3], [44],[45].

The Tunnel Field Effect Transistor (TFET) has proven to be one of the potential successors of MOSFET [4], due to resemblance of their basic structures, as discussed in Chapter-3. The working principle of TFET, which is based on the phenomenon of band to band tunnelling, is fundamentally different from that of MOSFET. This difference in the working principle helps the TFET in achieving sub-threshold swings lower than 60mV/decade, which makes the TFET very desirable for low power applications. The TFETs themselves are not free from drawbacks, the ambipolarity and reduced ON current being the most important ones [5], [6].

A plethora of TFET structures have been proposed to resolve the previously mentioned problems, such as gate metal engineered TFETs [7], [11], [36] for reduced channel to drain tunnelling and hetero-junction TFETs[8], [10], high-k gate dielectrics[8], [9], etc for increasing ON currents. The other way of increasing the ON state current is by modifying the device structure [12], [13], [37], [38] instead of using new materials [16], [18]. An L-shaped channel [12], [14] increases the effective source-channel junction area under the Gate's electric field in order to increase the current and improve the sub-threshold swing. But the LTFET suffers from acute ambipolarity [12], [14]. Previously, methods such as reduced drain doping[15] and addition of low doping region near drain have been proposed with considerable success at the cost of reduced ON current[15], [19].

Here, in this work, we have proposed the Broken Gate TFET structure after the brief literature study in Chapter-3. The proposed device is an amalgamation between the double gate TFET [8], [17] and LTFET. The device presented here boasts higher ON current and sharper sub-threshold characteristics than the silicon based LTFET [15] structure without compromising on the uni-directionality of the current. We have performed device dimension and doping concentration optimizations for better sub-threshold swing and reduced ambipolar nature without drastically reducing the ON current.

The analytical modeling section in this chapter contains two separate pair of surface potential and electric field models, one for the whole device and the other region specific, for the drain current modeling. For generating compact model (e.g. in Verilog-A) the equations in the drain current modeling section would be sufficient. All the models are validated against Synopsys Sentaurus TCAD[24] simulations.

4.2 The Device Structure:

The structure of the proposed device is illustrated in Fig.-1. We have considered a Silicon based TFET structure, as the fabrication technology for Silicon is matured, due to years of development, unlike many other new materials. Because of this, we expect a higher probability of successful integration of the proposed device in ICs. The device has four separate gates, two at the top and two at the bottom. The structure is derived by modifying the common double gate TFET structure, such that each of the top and the

bottom gates are now broken or separated into two due to the abrupt change in thickness of the channel. For all the simulations and analysis presented in this paper, the gates are simultaneously provided with the same external gate voltage. The metal contacts at the gates are considered Aluminum for simulation purpose. The gate dielectric near the source region is Hafnium Dioxide (HfO_2) and while that near the drain end is Silicon Dioxide (SiO_2) for reduced ambipolarity [15]. The source is doped p^+-type, the channel is lightly doped (n-type in our case) and the drain is n^+-type doped, but with doping concentration lesser than the source region, again to suppress the ambipolarity. The increased channel thickness near the source decreases the effect of drain voltage in the band to band generation process (which is concentrated near the edges as in Fig.-10), leading to exclusive gate control over the current and reduced short channel effects. The thinner channel near the drain region with low-k dielectric helps suppress the reverse gate bias tunneling current [14] and improve the sub-threshold swing and R.F.-performance [15].

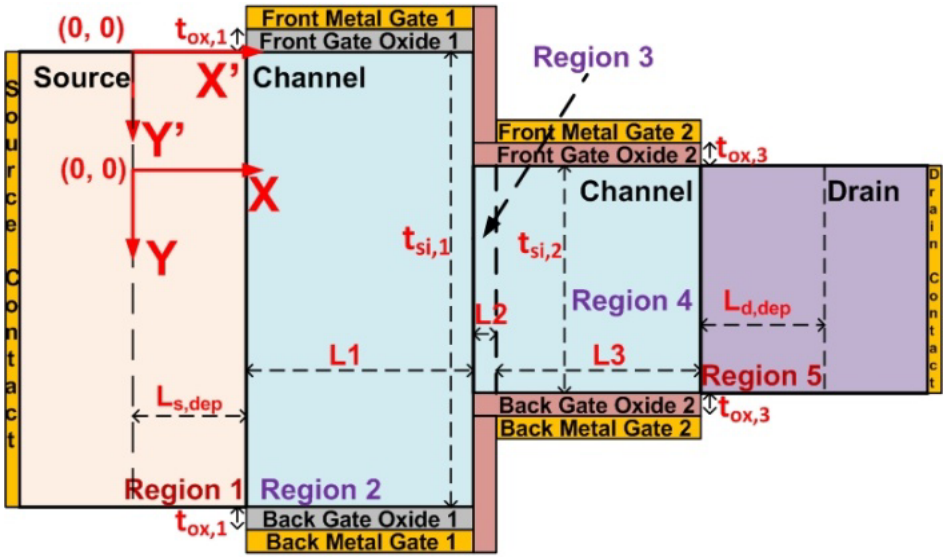

Fig.-1: Broken Gate TFET Structure.

Some possible fabrication steps for the device are illustrated in Fig.-2, denoting the feasibility of fabrication. The fabrication steps are inspired from the LTFET fabrication techniques mentioned in [12].

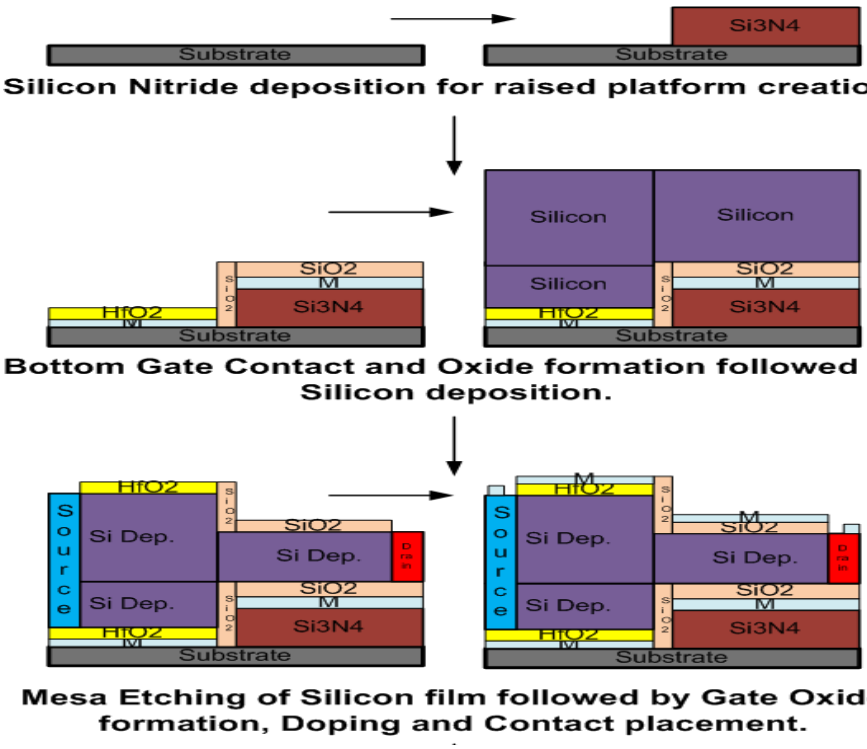

Fig.-2: Illustration of few possible device fabrication steps.

4.3 Optimisation of the Device Structure:

The optimizations were done by observing the simulated I_D vs. V_{GS} plots at V_{DS} = 1V. The main objectives of the optimization procedure were to obtain highest possible ON current, lower OFF state current with reduced ambipolarity and good sub-threshold swing. As the objectives were not independent, (e.g. trying to increase the ON current tends to increase the OFF current; similarly trying to reduce the ambipolarity decreases the ON current), the final dimensions or doping values are chosen as a compromise between all the four objectives. The plots in Fig.-3 to Fig.-5 is based on forward ON current measured at 1.5V and reverse current at -1.5V. The threshold voltage is considered at a current of 10^{-7} A/um and OFF state voltage at 10^{-15} A/um. The average sub-threshold swing is calculated over eight decades of current from 10^{-15} to 10^{-7} A/um.

From Fig.-3, the silicon film thickness of 18nm is chosen as it provides the highest ON current and in the consecutive steps with other parameters the sub-threshold swing and reverse tunnelling currents were also optimized. It was observed that with increase in the length of the drain region the ambipolar nature reduces. Also for our case, overall

sub-thresholds swing increased with increase in channel length as in Fig.-4. Thinner oxides provide better results but to prevent excessive gate leakage, the oxide thicknesses were kept constant at 2nm[32].

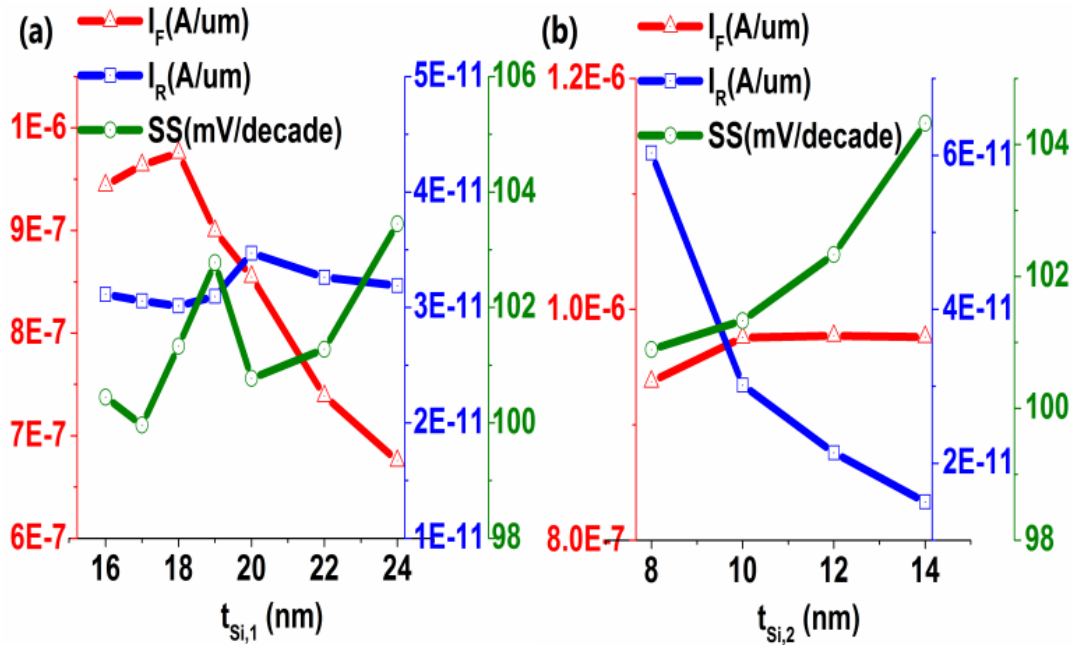

Fig.-3: Silicon Film Thickness Optimization (a) $t_{Si,1}$ (b) $t_{Si,2}$.

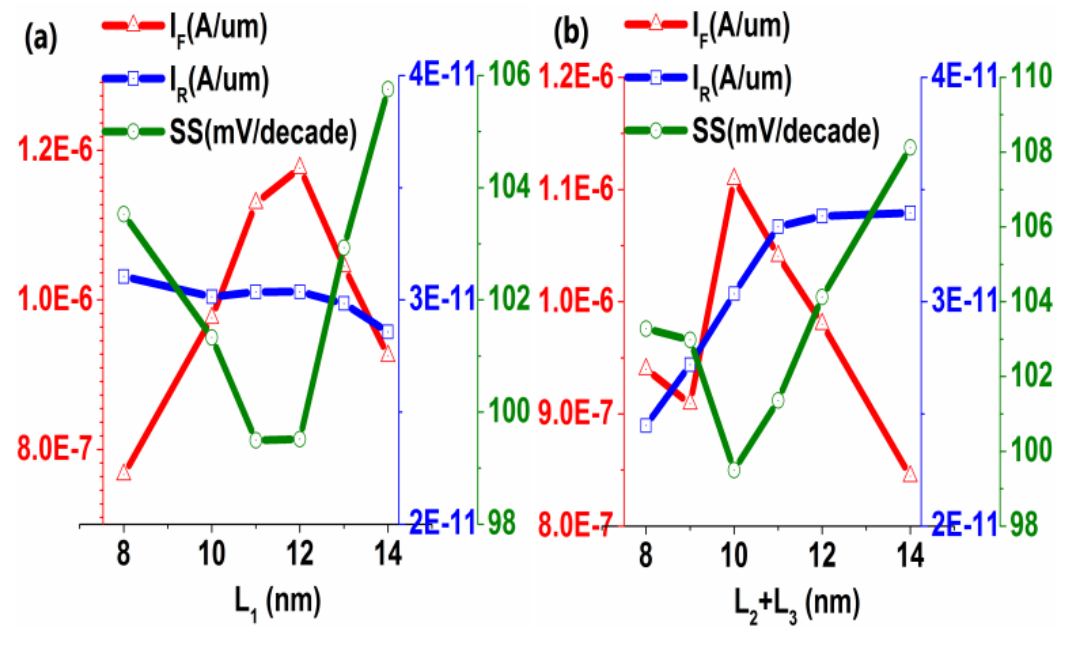

Fig.-4: Channel Length Optimization (a) L_1, (b) $L_2 + L_3$.

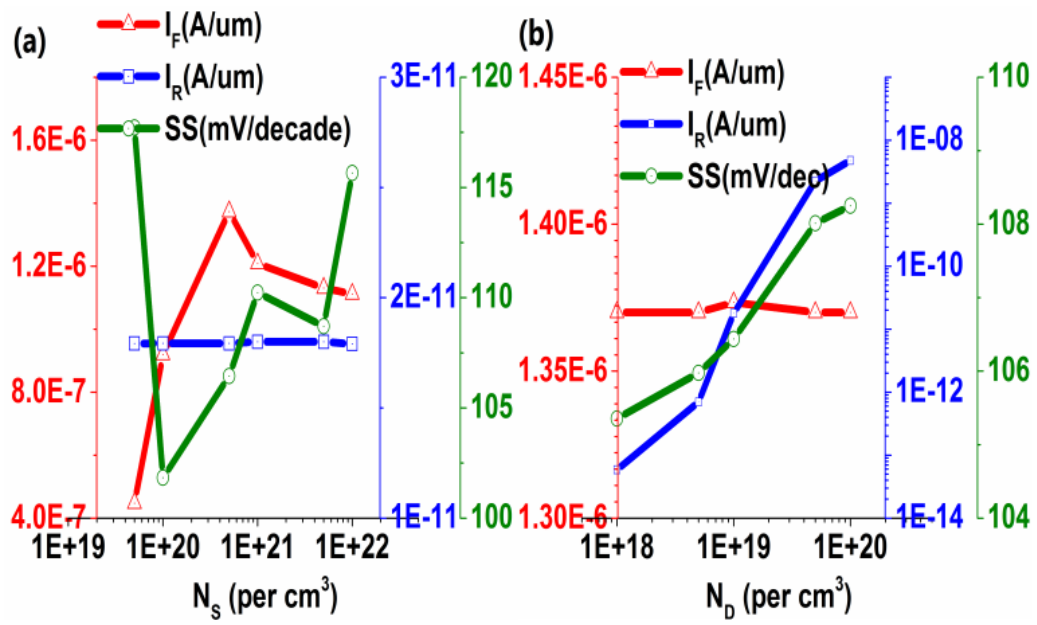

Fig.-5: Doping Concentration Optimization (a) N_S (b) N_D.

The initial and final optimized parameter values for the devices are presented in Table-1. The optimized values obtained here are by no means rigid, and the parameter values can be chosen in such a way as to favour one criterion over another.

TABLE: 1

Parameters	**Initial Values**	**Final Values**
L1, L2, L3	10nm, 2nm, 8nm	**11nm**, 2nm, 8nm
$t_{si,1}$,$t_{si,2}$	20nm, 10nm	**18nm**, 10nm
$t_{ox,1}$,$t_{ox,2}$	2nm, 2nm	2nm, 2nm
Source Length	10nm	10nm
Drain Length	10nm	**16nm**
Source Doping Conc. (N_S)	10^{20} /cm^3	**$5x10^{20}$ /cm^3**
Drain Doping Conc. (N_D)	10^{19} /cm^3	**$5x10^{18}$ /cm^3**
Channel Doping Conc. (N_C)	10^{17} /cm^3	10^{17} /cm^3

In Fig.-6(a) the transfer characteristics comparison shows minimum ambipolarity and maximum current for our proposed device after optimization. Also, in Fig.-6(b) the effect of quantum confinement on the device is shown with the help of I_D vs. V_{GS} plots. MLDA (modified local-density approximation) quantum correction model [24, Chp.-14] was

used, as it is applicable for ultra-thin SOI device structures (unlike Van-Dort model) and is also faster and more robust than 1D-Schroedinger model available in Sentaurus TCAD. An expected reduction in ON-current [30] (of less than a decade) and small variations in threshold voltage and average sub-threshold swing [29] were observed. The effect of quantum confinement is more pronounced in devices with channel thickness less than 10 nm [8],[27-28] and also if considerable gate-source overlap is present[31], both of which are not applicable for our device. Hence, dynamic non-local tunnelling model without any quantum correction was used in our simulations for parameter optimization and in the analytical modelling section for comparison with the derived model.

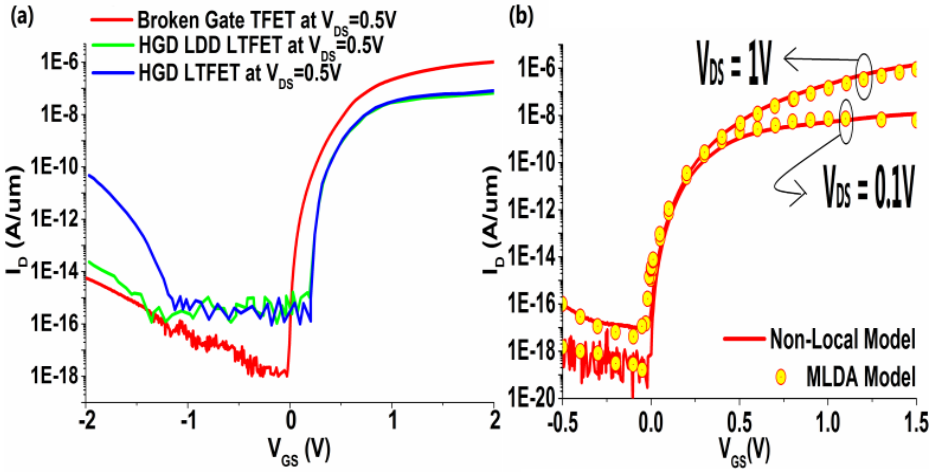

Fig.-6: (a) Ambipolarity Comparison with LTFET structures in [15] (b) I_D vs. V_{GS} plot with and without Quantum Correction.

It is to be noted that quantum correction models are not fully coupled with the band-to-band tunnelling model, hence results might somewhat vary in reality.

4.4 Derivation of the Analytical Model:

4.4.1. Expression for the Surface Potential: The 2D Poisson's equation in general can be written as follows:

$$\frac{\partial^2 \Psi(x,y)}{\partial x^2} + \frac{\partial^2 \Psi(x,y)}{\partial y^2} = \frac{-qN_i}{\varepsilon_{Si}} \quad (1)$$

Where, N_i represents the doping concentration at different regions. $N_i = N_S$, N_D and N_C for regions 1, 5 and (2, 3, 4) respectively, with "+" sign for p-type and "-" sign for n-type doping. $\Psi(x, y)$ represents the electrostatic potential and 'q' represents the magnitude of electronic charge. Our device structure is horizontally divided into five regions, to aid our calculations and have used the coordinates (X, Y) vertically near the middle of the device, as in Fig.-1. In each region the solution to the Poisson's equation is assumed to be parabolic in nature, according to Young's parabolic potential approximation. The generic solution to equation (1), neglecting the influence of mobile charges [21], can be written as follows:

$$\Psi_i(x,y) = C_{0,i}(x) + C_{1,i}(x)\,y + C_{2,i}(x)\,y^2 \quad (2)$$

Where, the subscript 'i' represents each of the five regions.

The following boundary conditions are required for obtaining the coefficients $C_{j,i}(x)$,

$$\Psi_i(x,0) = \Psi_{s,i}(x) \quad \& \quad \Psi_i(x,t_{Si,i}) = \Psi_{s,i}(x) \quad (3a)$$

$$\left.\frac{\partial \Psi_{s,i}(x)}{\partial y}\right|_{y=0} = \eta_i \frac{\Psi_{s,i}(x) - \Psi_{G,i}}{t_{Si,i}} \quad (3b)$$

$$\left.\frac{\partial \Psi_{s,i}(x)}{\partial y}\right|_{y=t_{Si,i}} = -\eta_i \frac{\Psi_{s,i}(x) - \Psi_{G,i}}{t_{Si,i}} \quad (3c)$$

Where, $\eta_i = C_{ox,i} / C_{Si,i}$ for i=1, 2, 3, 4 & 5 and $C_{ox,i} = \varepsilon_{ox,i} / t_{ox,i}$ for i=1, 2, 4 only.

For the narrow, Region 3, $C_{ox,3} = (2/\pi)(\varepsilon_{ox,3} / t_{ox,3})$ which is due to the fringing field effect and it is approximated by considering the conformal mapping techniques[25][26]. Similarly for regions 1 & 5; $C_{ox,1} = (2/\pi)(\varepsilon_{ox,1} / t_{ox,1})$ and $C_{ox,5} = (2/\pi)(\varepsilon_{ox,5} / t_{ox,5})$ respectively. The $C_{ox,i}$ terms represent the oxide capacitances at each region and the silicon film capacitance is denoted as $C_{Si,i} = \varepsilon_{Si,i} / t_{Si,i}$.

Where, $t_{Si,i}$ is $t_{Si,1}$ for regions 1, 2 and $t_{Si,2}$ for regions 3, 4, and 5, as in Fig.-1. For our device $t_{ox,i}$ for regions 1, 2 are same and represented by $t_{ox,1}$, and $t_{ox,2}$ for regions 3, 4, 5. Similarly, for $\varepsilon_{ox,i}$, $\varepsilon_{ox,1}$ and $\varepsilon_{ox,2}$ represents regions 1, 2 and 3, 4, 5 respectively. And for

all regions $\varepsilon_{Si,i}$ is ε_{Si}.

The equations (3b) and (3c) are obtained from the continuity of electric flux at the semiconductor-dielectric boundary. Also, equations in (3a) are written assuming symmetry in the device across the x-axis, with $\Psi_{s,i}(x)$ representing the surface potential at the i^{th} region. The gate potential is represented as Ψ_G, where, $\Psi_{G,i} = V_{G,i} - V_{fb}$ and $V_{fb} = \phi_M - \phi_{Si}$, such that $\phi_{Si} = \chi_{Si} - E_g/2$, χ_{Si} is the electron affinity and E_g is the energy band gap of silicon (in eV).

Equations in (3) are modified to a certain extent for accommodating the salient nature of Regions 1 & 2, as shown in the Fig.-1. The modified boundary conditions for the first two regions can be written as follows:

$$\Psi_i(x, y = -\frac{t_{Si,1} - t_{Si,2}}{2}) = \Psi_{s,i}(x) \quad (4a)$$

$$\Psi_i(x, y = \frac{t_{Si,1} + t_{Si,2}}{2}) = \Psi_{s,i}(x) \quad (4b)$$

$$\left.\frac{\partial \Psi_{s,i}(x)}{\partial y}\right|_{y=-\frac{t_{Si,1}-t_{Si,2}}{2}} = \eta_i \frac{\Psi_{s,i}(x) - \Psi_{G,i}}{t_{Si,1}} \quad (4c)$$

$$\left.\frac{\partial \Psi_{s,i}(x)}{\partial y}\right|_{y=\frac{t_{Si,1}+t_{Si,2}}{2}} = -\eta_i \frac{\Psi_{s,i}(x) - \Psi_{G,i}}{t_{Si,1}} \quad (4d)$$

From the equations in (3), the coefficients $C_{j,i}(x)$are obtained as follows:

$$C_{0,i}(x) = \Psi_{s,i}(x) \quad (5a)$$

$$C_{1,i}(x) = \eta_i(\Psi_{s,i}(x) - \Psi_{G,i}) / t_{Si,1} \quad (5b)$$

$$C_{2,i}(x) = -\eta_i(\Psi_{s,i}(x) - \Psi_{G,i}) / t_{Si,1}^{\,2} \quad (5c)$$

These represent the values of coefficients for the potential at Regions-3, 4 & 5. For Regions-1 & 2, the values are as follows:

$$C_{0,i}(x) = \alpha_i^2 \Psi_{s,i}(x) - \beta_i \Psi_{G,i} \quad (6a)$$

$$C_{1,i}(x) = \eta_i(\Psi_{s,i}(x) - \Psi_{G,i}) t_{Si,2} / t_{Si,1}^{\,2} \quad (6b)$$

$$C_{2,i}(x) = -\eta_i(\Psi_{s,i}(x) - \Psi_{G,i}) / t_{Si,1}^{\,2} \quad (6c)$$

Where, $\alpha_i^2 = 1 + \beta_i$ (7) and $\beta_i = (\eta_i/2) \times (t_{Si,2}/t_{Si,1})(1 - t_{Si,2}/t_{Si,1}) + (\eta_i/4) \times (1 - t_{Si,2}/t_{Si,1})^2$ (8)

For i = 1 and 2.

Now the coefficients $C_{j,i}(x)$ are substituted in equation (2), to obtain the electrostatic potential $\Psi(x,y)$, whose value was put back in equation (1). Finally a differential equation in terms of the surface potential is obtained as follows:

For Regions 1 & 2:

$$\frac{\partial^2 \Psi_{s,i}(x)}{\partial x^2}(\alpha_i^2 + \frac{\eta_i t_{Si,2}}{t_{Si,1}^{\ 2}} y + \frac{\eta_i}{t_{Si,1}^{\ 2}} y^2) - \frac{2\eta_i(\Psi_{s,i}(x) - \Psi_{G,i})}{t_{Si,1}^{\ 2}} = \frac{-qN_i}{\varepsilon_{Si}} \quad (9a)$$

In Regions 1 & 2, the surface potential cannot be directly equated with the surface potential of the adjacent regions at the boundary. Instead we consider a "pseudo" surface potential for the first two regions at y=0 and use that to form boundary conditions required for the solution of equations in (9c).

Thus, the "pseudo" surface potential based differential equation, obtained from (9b) by putting y=0, can be written as follows:

$$\alpha_i^{\ 2} \frac{\partial^2 \Psi_{s,i}(x)}{\partial x^2} - \frac{2\eta_i \Psi_{s,i}(x)}{t_{Si,1}^{\ 2}} = \frac{-qN_i}{\varepsilon_{Si}} - \frac{2\eta_i \Psi_{G,i}}{t_{Si,1}^{\ 2}} \quad (9b)$$

Now, all the differential equations for all regions can be written in a compact form as:

$$\frac{\partial^2 \Psi_{s,i}(x)}{\partial x^2} - k_i^{\ 2} \Psi_{s,i}(x) = -k_i^{\ 2} \Psi_{C,i} \quad (9c)$$

Where, $k_i = \sqrt{2\eta_i / t_{Si,i}^{\ 2}}$ for Regions-3, 4 & 5 and $k_i = \frac{1}{\alpha_i}\sqrt{\frac{2\eta_i}{t_{Si,i}^{\ 2}}}$ for Regions 1 & 2.

The parameter '$1/k_i$' is termed as the characteristic length or decay length of the surface potential in each region. Also the term $\Psi_{C,i}$ is region dependent, with the expression as follows:

$$\Psi_{C,i} = \Psi_{G,i} + qN_i / (k_i^{\ 2} \varepsilon_{Si}) \quad (10a)$$

for Regions-2&3, with the following for Regions-1, 2:

$$\Psi_{C,i} = \Psi_{G,i} + qN_i / (\alpha_i^{\ 2} k_i^{\ 2} \varepsilon_{Si}) \quad (10b)$$

Finally, the solution for the differential equation in (9c) is as follows:

$$\Psi_{S,i}(x) = A_i\, e^{-k_i(x - \sum x_{i-1})} + B_i\, e^{k_i(x - \sum x_{i-1})} + \Psi_{C,i} \quad (11)$$

Where $x_1 = L_{S\_dep}$, $x_2 = L_1$, $x_3 = L_2$, $x_4 = L_3$, and $x_5 = L_{D\_dep}$.

The value of the coefficients A_i and B_i can be found from other set of boundary conditions, discussed later.

4.4.2. Expression for the Electric Field: In the previous section, expression for the surface potential has been obtained, given in equation (11). By substituting the surface potential values from equation (11) in the equation set (5), we obtain the final expression for the potential inside each region of the device. The X and Y components of

the electric fields in the device, given in equation set (14) have been obtained from the potential using the relations in (12) & (13).

$$E_{X,i} = -\left.\frac{\partial \Psi_i(x,y)}{\partial x}\right|_{y=0} \quad (12)$$

$$E_{Y,i} = -\left.\frac{\partial \Psi_i(x,y)}{\partial y}\right|_{x=cons\tan t} \quad (13)$$

$$E_{X,i} = -(-k_i A_i e^{-k_i(x-\sum x_{i-1})} + k_i B_i e^{+k_i(x-\sum x_{i-1})}) \quad (14a)$$

$$E_{Y,i} = -C_{1,i}(x) - 2yC_{2,i}(x) \quad (14b)$$

For i = 1, 2, 3, 4 & 5.

4.4.3. Effect of Drain Voltage on the Surface Potential: To increase the accuracy of the analytical model, inclusion of the effect of high positive and negative drain voltages on the surface potential due to formation of inversion layer in the channel, becomes necessary, especially for short channel devices like the one under consideration. A semi-empirical approach for inclusion of such effect in the analytical model has been discussed in [21]. We have utilized this approach as this method does not require numerical solution, unlike previous works in [20]. The surface potential variation in response to the change in drain voltage has been captured by substituting Gate potential Ψ_G by a new value $\Psi_{G,eff}$ which in turn was used for calculation of the term $\Psi_{C,i}$, while obtaining surface potential. The expression for $\Psi_{G,eff}$ is as follows:

$$\Psi_{G,eff} = \Psi_G - \eta\Phi_t \ln(1+\exp(\frac{\Psi_G - \Psi_D}{\Phi_t})) + \eta\Phi_t \ln(1+\exp(\frac{\Psi_S - \Psi_G}{\Phi_t})) \quad (15)$$

Where, ϕ_t and η are the curve fitting parameters, obtained by varying them and comparing the simulated and analytical surface potential value at x = ($L_{S,dep}$+L1+L2+L3+ $L_{D,dep}$)/2, until a good fit was observed for a range of gate voltage.

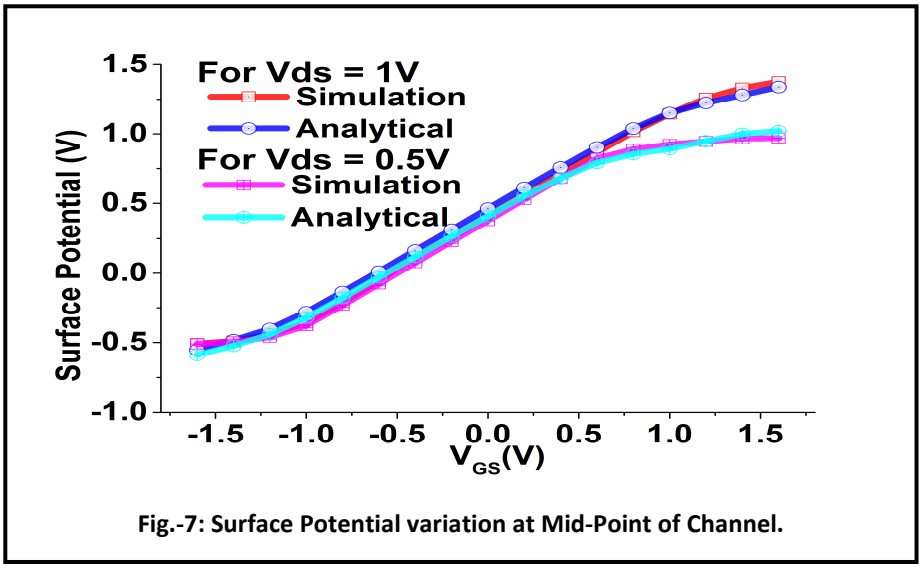

Fig.-7: Surface Potential variation at Mid-Point of Channel.

The curve fitting is illustrated in Fig.-7. ϕ_t=0.1 and η=0.6 were found to be the optimum values. Also, Ψ_S and Ψ_D represents the source and drain potentials respectively.

4.4.4. Obtaining the Depletion Region Widths: In Fig.-1, we have illustrated the depletion regions and have included them in the analysis for accurate modelling.

Obtaining the depletion region width is generally done by iterative methods, but for simplicity we can assume the device as a PIN diode and obtain the approximate source and drain depletion region widths using well known equations available in the literature, as follows:

$$L_{S\_dep} = \sqrt{\frac{2\varepsilon_{Si}\,|\Psi_{C,2} - \Psi_S|\,N_C}{qN_S(N_S + N_C)}} \quad \& \quad L_{D\_dep} = \sqrt{\frac{2\varepsilon_{Si}\,|\Psi_D - \Psi_{C,4}|\,N_C}{qN_D(N_D + N_C)}} \tag{16}$$

4.4.5. Solving for the Surface Potential: In the equation set (10), the gate potential is generalized as $\Psi_{G,i}$, but under the current scenario, the gate potential is one and the same, represented by Ψ_G, which again is substituted by $\Psi_{G,eff}$, as mentioned in the previous section.

The boundary conditions required for obtaining the values of the coefficients A_i and B_i are as follows: $\Psi_{s,i}(x) = \Psi_{s,i+1}(x)$ & $\Psi'_{s,i}(x) = \Psi'_{s,i+1}(x)$ (17a, b)

$$\Psi_{s,1}(x=0) = \Psi_S = V_S - v_T \ln(N_S / n_i) \quad (17c)$$

$$\Psi_{s,5}(x=L_{S\_dep}+L_1+L_2+L_3+L_{D\_dep}) = \Psi_D = V_D + v_T \ln(N_D / n_i) \quad (17d)$$

The value of the coefficients A_i and B_i can be obtained by applying the conditions in equation set (17). We obtain ten simultaneous equations from the boundary conditions and solving them manually become cumbersome. Instead we represent the equations in Matrix form as in (18) and obtain the coefficient values using MATLAB or similar software.

AX = C (18)

Where,

$$A = \begin{bmatrix} 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ a_1 & b_1 & -1 & -1 & 0 & 0 & 0 & 0 & 0 & 0 \\ -k_1 a_1 & k_1 b_1 & k_2 & -k_2 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & a_2 & b_2 & -1 & -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & -k_2 a_2 & k_2 b_2 & k_3 & -k_3 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & a_3 & b_3 & -1 & -1 & 0 & 0 \\ 0 & 0 & 0 & 0 & -k_3 a_3 & k_3 b_3 & k_4 & -k_4 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & a_4 & b_4 & -1 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & -k_4 a_4 & k_4 b_4 & k_5 & -k_5 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -k_5 a_5 & k_5 b_5 \end{bmatrix} \quad X = \begin{bmatrix} A_1 \\ B_1 \\ A_2 \\ B_2 \\ A_3 \\ B_3 \\ A_4 \\ B_4 \\ A_5 \\ B_5 \end{bmatrix} \quad C = \begin{bmatrix} C_1 \\ C_2 \\ 0 \\ C_3 \\ 0 \\ C_4 \\ 0 \\ C_5 \\ 0 \\ C_6 \end{bmatrix}$$

Where, $C_i = \Psi_{C,i} - \Psi_{C,i-1}$ for i = 2 to 5; and $C_1 = \Psi_S - \Psi_{C,1}$,

$C_6 = \Psi_D - \Psi_{C,5}$ and $a_i = e^{-k_i x_i}$; $b_i = e^{k_i x_i}$.

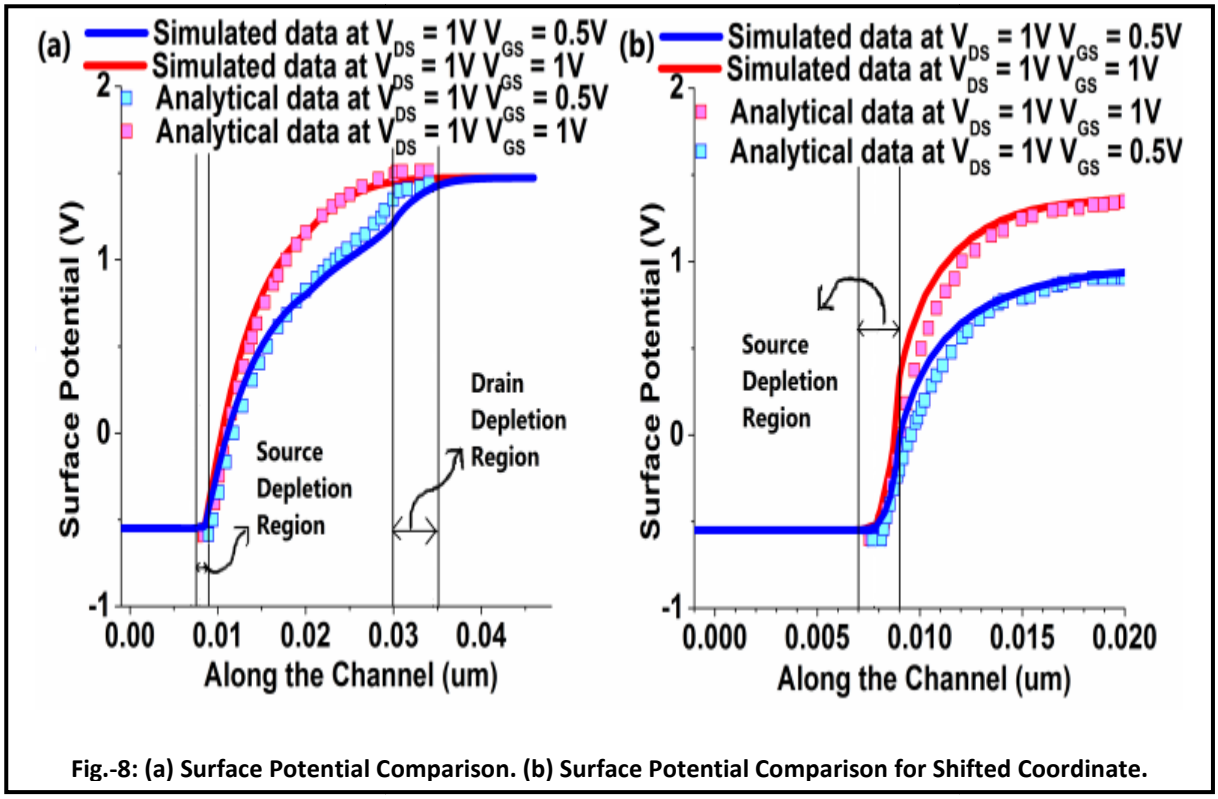

Fig.-8: (a) Surface Potential Comparison. (b) Surface Potential Comparison for Shifted Coordinate.

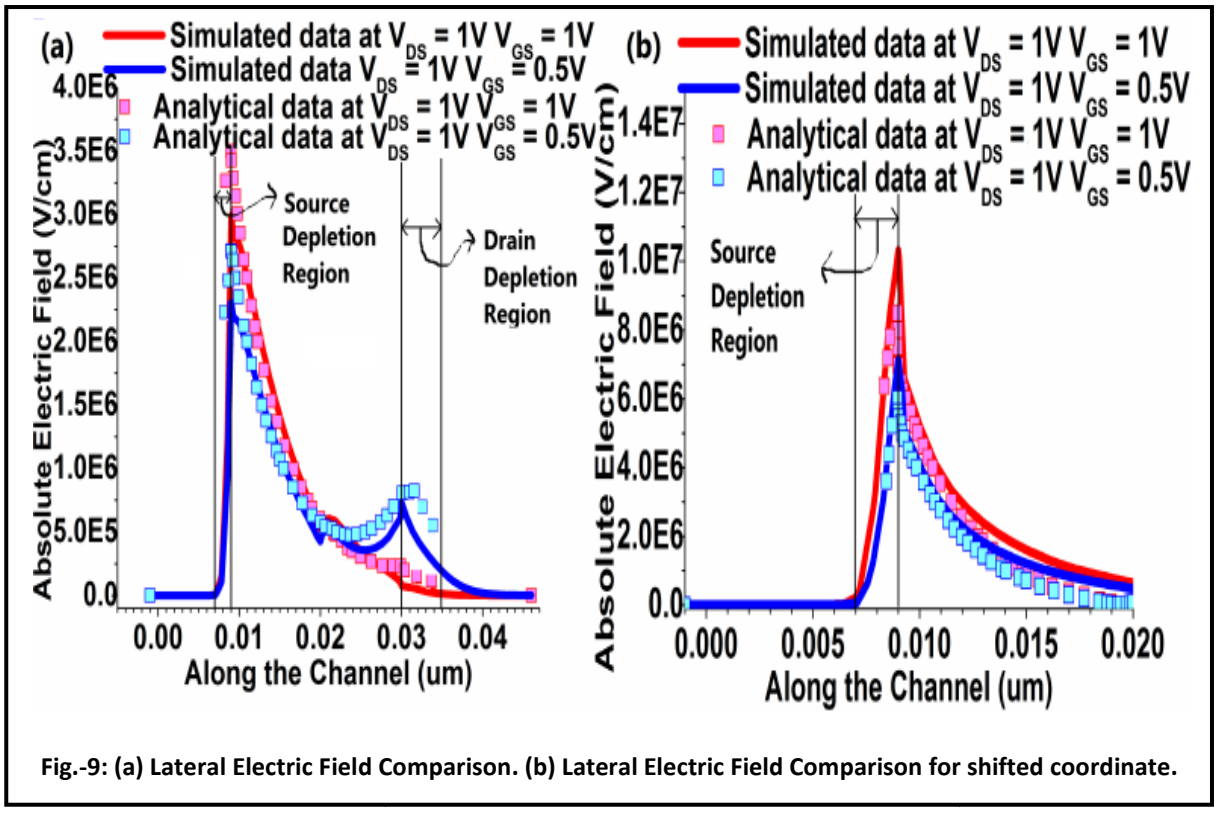

Fig.-9: (a) Lateral Electric Field Comparison. (b) Lateral Electric Field Comparison for shifted coordinate.

4.4.6. The Drain Current Modelling: The analytical model for Surface potential and Electric field derived till now is not suitable for obtaining the expression for current, as the band to band generation is concentrated mostly near the Gates at the Source-Channel region, as in Fig.-10.

Thus we need to formulate another set of equations for the surface potential and electric field in the extended potion of the channel, which incorporates the abrupt nature of it.

The coordinates are now shifted (X', Y'), as in Fig.-1. Proceeding similarly as before, we obtain:

$$\Psi_{S,ii}(x) = A_{ii}\, e^{-k_{ii}(x-\sum x_{i-1})} + B_{ii}\, e^{k_{ii}(x-\sum x_{i-1})} + \Psi_{C,ii} \tag{19}$$

$$E_{Y,ii} = -C_{1,ii}(x) - 2yC_{2,ii}(x) \tag{20}$$

$$E_{X,ii} = -(-k_{ii}A_{ii}e^{-k_{ii}(x-\sum x_{i-1})} + k_{ii}B_{ii}e^{+k_{ii}(x-\sum x_{i-1})}) \tag{21}$$

For i = 1, 2, the $\Psi_{C,i}$ and $C_{j,i}$ expressions are same as equations (10a) and (5) respectively.

The boundary conditions for obtaining the coefficients A_{ii} and B_{ii} are as follows:

$$\Psi_{S,11}(0,0) = \Psi_S = V_S - v_T \ln(N_S / n_i) \tag{22a}$$

$$\Psi_{S,11}(x) = \Psi_{S,22}(x) \tag{22b}$$

$$\left.\frac{\partial \Psi_{S,22}(x)}{\partial x}\right|_{x=L_{S,dep}+L_1} = \eta_{eff}(V_G - \Psi_{S,22}(x=L_{S,dep}+L_1))/t_{Si,1} \tag{22c}$$

Where $\eta_{eff} = C_{eff} / C_{Si,1}$, $C_{eff} \approx \varepsilon_0.\varepsilon_{ox,3} / (\varepsilon_{ox,3}.t_{eff} + \varepsilon_0.t_{ox,3})$ and $t_{eff} = (t_{Si,1} - t_{Si,2})/2 - L_2$

Considering a series capacitance, comprising of SiO_2 layer and the free space between the gate metal near the drain region and the vertical wall of the channel near the source.

Finally, by solving the equations in (22), we get:

$$B_{11} = (w_2 - u_2(\Psi_S - \Psi_{c11}))/(v_2 - u_2) \tag{23a}$$

$$A_{11} = (\Psi_S - \Psi_{c11}) - B_{11} \tag{23b}$$

$$A_{22} = (u_1(-k_{11}A_{11}\, e^{-k_{11}L_{S,Dep}} + k_{11}B_{11}\, e^{k_{11}L_{S,Dep}}) + k_{22}w_1)/c_{11} \tag{23c}$$

$$B_{22} = (k_{22}w_1 - v_1(-k_{11}A_{11}\, e^{-k_{11}L_{S,Dep2}} + k_{11}B_{11}\, e^{k_{11}L_{S,Dep2}}))/c_{11} \tag{23d}$$

Where, the expressions for u_i, v_i, w_i and c_{11} are given in the Appendix section.

The drain current is dependent on the tunnelling generation rate, which in turn is exponentially dependent on the electric field. The highest generation rate is observed at the source-channel interface, where the electric field is also at its peak. The generation rate along with the electric field falls off drastically as we move farther away from the source-channel interface, as in Fig.-10. The figure suggests a semi-circular region of peak carrier generation at each side of the device. Thus, a total circular area of maximum band to band generation is obtained with area: $A_{tun} = \pi * tun\_rad^2$, where "tun_rad" is the radius of tunnelling, as in Fig.-10. Tunnelling radius of 1.3nm was found to be best fit. The drain current for TFET can be obtained by integrating the generation rate over the tunnelling volume: $I_D = q \int_{vol} G_{b2b} dV$

Where, according to [22],[23] the generation rate is given as:

$$G_{btbt} = A_{Kane}(\left|E^2_{avg}\right| / \sqrt{E_g}) \exp(-B_{Kane} E_g^{3/2} / \left|E_{avg}\right|) \quad (24)$$

The E_{avg} is dependent on the minimum tunnelling length $L_{t,min}$,. The point (x= $L_{t,min}$) is where the surface potential changes from the initial value by a magnitude of "$\sim E_g$ (in eV)".

$$L_{t,\min} = (1/k_{22}) \ln\left(\frac{\sqrt{(\Psi_{c22} - E_g)^2 - 4A_{22}B_{22}} - (\Psi_{c22} - E_g)}{2B_{22}}\right) \quad (25)$$

Now, from the minimum tunnelling length the average electric field can be calculated, as: $E_{avg}=E_g/ L_{t,min}$. We can assume the generation rate in equation (24) to be dominant, as it is obtained from the highest electric field present in the device and also constant over the relatively small tunnelling area.

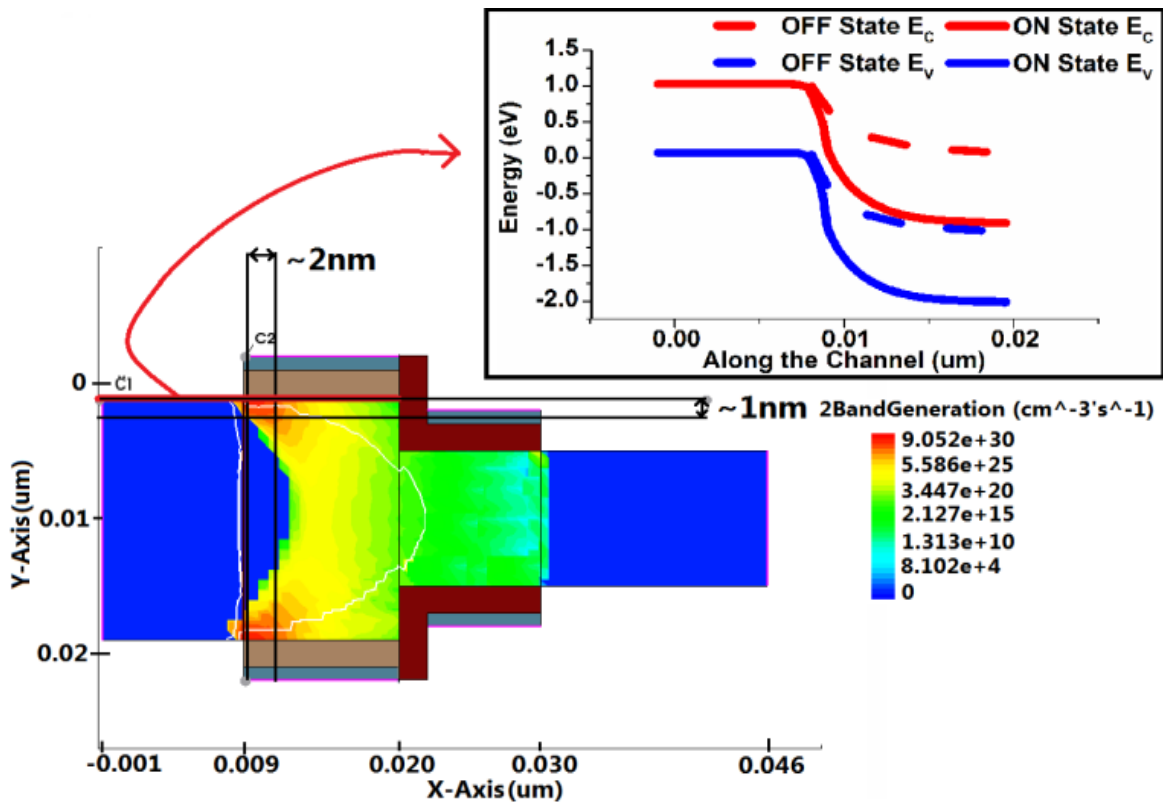

Fig.-10: Localization of b2b generation rate in the device at V_{DS} = 1V and V_{GS} = 1.5V (Inset: Energy Band Diagram).

Now, rather than integrating the generation rate, we can simply multiply the generation rate in (24) with the tunnelling area "A_{tun}", and obtain the current per unit width of the device. The final relation for the drain current can be written as:

$$I_D = qA_{tun}A_{Kane}\left(\left|E^2{}_{avg}\right| / \sqrt{E_g}\right)\exp\left(-B_{Kane}E_g{}^{3/2} / \left|E_{avg}\right|\right) \quad (26)$$

Where A_{Kane} and B_{kane} are the Kane's parameters with best fit values of $A_{Kane} = 9.25\text{x}10^{14}$ $eV^{1/2}um^{-1}V^{-2}s^{-1}$ and $B_{kane} = 2.36\text{x}10^{7}$ $Vcm^{-1}eV^{-3/2}$ for our analytical model. The fitted values are close to the values mentioned in [22] & [31].

At low value of V_{GS}, the surface potential variation may not be as large as E_g (in eV), hence equation (25) will fail. In such cases the L_{tmin} is replaced by L_1 during the analysis.

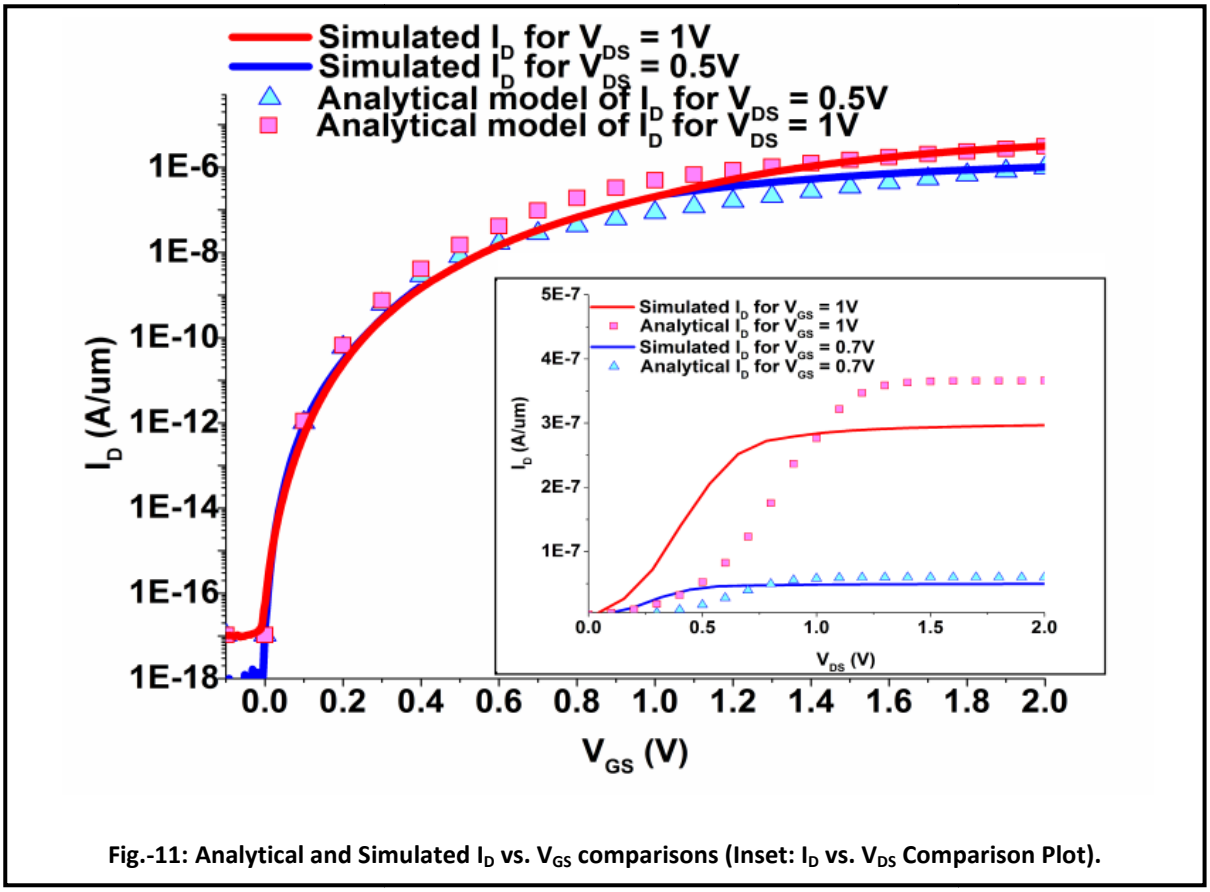

Fig.-11: Analytical and Simulated I_D vs. V_{GS} comparisons (Inset: I_D vs. V_{DS} Comparison Plot).

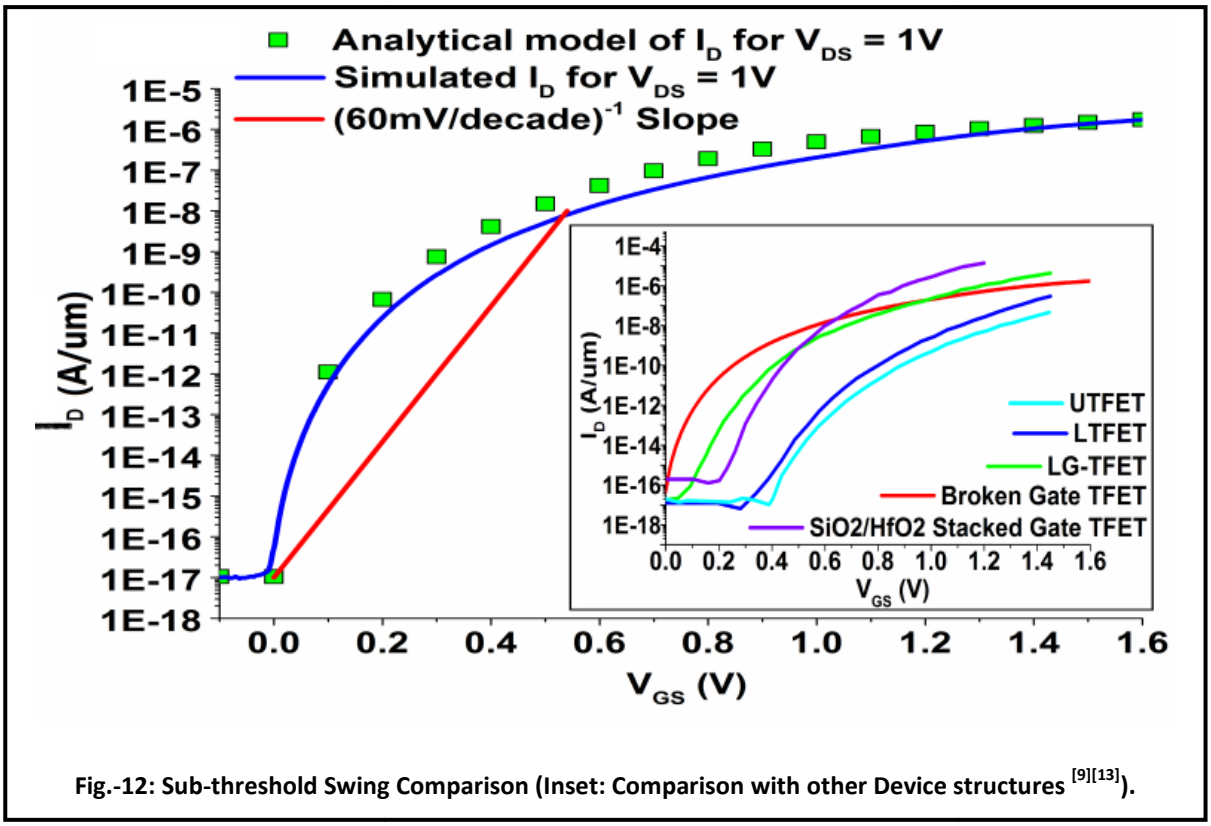

Fig.-12: Sub-threshold Swing Comparison (Inset: Comparison with other Device structures [9][13]).

4.4.7. Discussion on the results obtained so far: The analytical versus simulated surface potential and lateral electric fields comparisons are shown in Fig.-8 and Fig.-9 respectively at V_{DS} = 1V. In both the figures red colour represents V_{GS} = 1V and blue implies 0.5V, with solid lines and symbols indicating simulated and analytical data, respectively. The drain current of the device is compared in Fig.-11. The I_D vs. V_{GS} characteristics of the proposed structure (in red) is compared with other relevant structures, especially LTFETs and DGTFETs, in Fig-12 (inset). The outer figure shows average sub-threshold swing (ss) of 60mV/decade over nine decades of current (10^{-17} to 10^{-8} A/um), also SS ≈25mV/decade is observed over two decades of current (10^{-15} to 10^{-13} A/um). The proposed device shows steep sub-threshold-swing and moderate ON state current (better than the original LTFET and UTFET) with negligible ambipolar conduction (Fig.-6 (a)) at a channel length of 21nm.

4.5 Parasitic Capacitances in Broken Gate TFET Structure:

Parasitic capacitances are important for predicting analog and R.F.-performances. They are the dominant parameter in determining the device's speed of operation. We have presented the capacitance versus gate voltage plots for our device in Fig.-13-15. The capacitance values were obtained from Sentaurus TCAD AC simulation for drain-to-source voltage values of 0V, 0.5V and 1V. The parasitic capacitances of the proposed device were compared with the HGD-LDD-LTFET structure, and found to be approximately 37.5% lower. Thus, the Broken Gate TFET should be a faster device. It should be noted that the gate to drain capacitance (C_{gd}), followed by gate capacitance ($C_{gg}=I_d/(dV_{gs}/dt)$) are dominant in the voltage range we have plotted in Fig.-13-15.

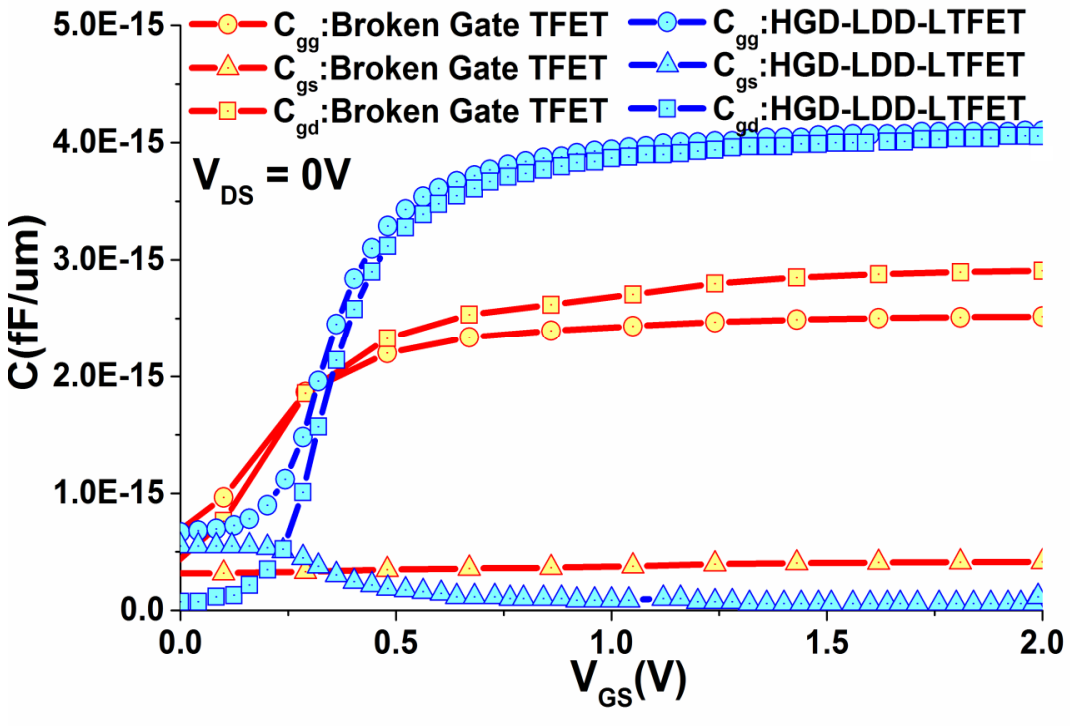

Fig.-13: Parasitic Capacitance Comparison between Broken Gate TFET and HGD-LDD-LTFET[15] at V_{DS}=0V.

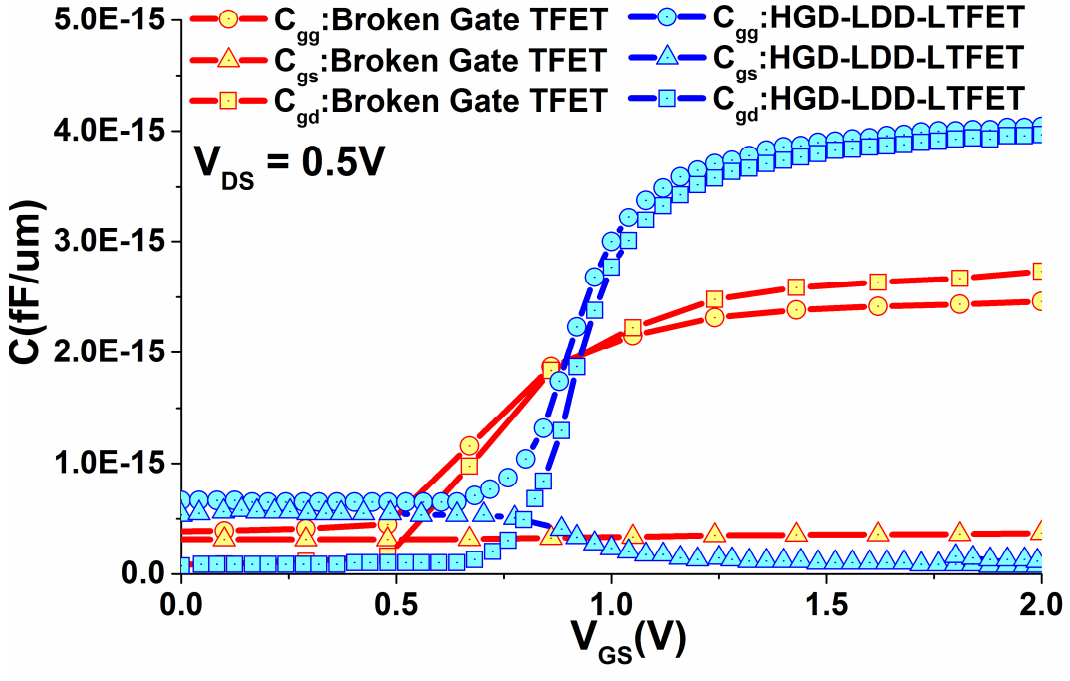

Fig.-14: Parasitic Capacitance Comparison between Broken Gate TFET and HGD-LDD-LTFET[15] at V_{DS}=0.5V.

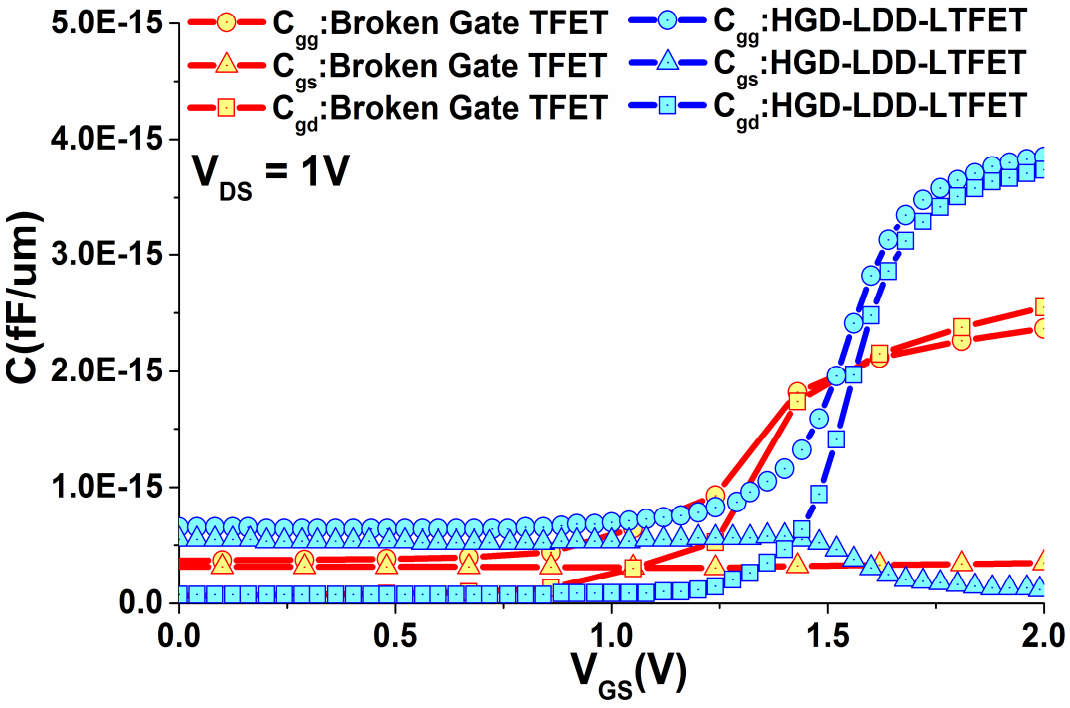

Fig.-15: Parasitic Capacitance Comparison between Broken Gate TFET and HGD-LDD-LTFET[15] at V_{DS}=1V.

From the above plots, it is clear that the device has very low parasitics, meaning it should be faster in operation. It is important to note that the predicted parasitic capacitances might increase depending on the substrates used in the SOI (Silicon-on-Insulator) implementation/ fabrication, which would degrade the performance. Thus, SON (Silicon-on-Nothing) [34], [35], [39]-[43] implementation is preferable, for obtaining performances closer to the predicted values.

4.7 Appendix:

$$u_1 = e^{-k_{22}L_1}\left(-k_{22} + \frac{\eta_{eff}}{t_{Si,1}}\right);$$

$$v_1 = e^{k_{22}L_1}\left(k_{22} + \frac{\eta_{eff}}{t_{Si,1}}\right);$$

$$w_1 = \frac{\eta_{eff}}{t_{Si,1}}\left(V_G - \Psi_{c22}\right);$$

$$c_{11} = k_{22}(u_1 + v_1)$$

$$u_2 = e^{-k_{11}L_{S,Dep}}(1 + k_{11}u_1c_{11} - k_{11}v_1c_{11})$$

$$v_2 = e^{k_{11}L_{S,Dep}}(1 - k_{11}u_1c_{11} + k_{11}v_1c_{11})$$

$$w_2 = 2c_{11}k_{22}w_1 + \Psi_{c22} - \Psi_{c11}$$

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Chapter-5: Conclusion and Scope for Future Work

5.1. Conclusion.

5.2. Scope for Future Work.

5.1 Conclusion:

The work presented here is aimed at studying the importance of Tunnel Field Effect Transistors (TFETs) in the view of low power electronic computing. Depending on the application, with the help of some modifications in the basic device structure, the efficacy of such device can be improved drastically.

In **Chapter-1**, the history of electronic computing has been discussed followed by the requirement for low power devices. The motivation for the current work stems from the shortcomings of the MOSFET, especially when subjected to aggressive scaling. From Fig.-1.4 of this chapter, it is clear that TFETs have sharper ON-OFF characteristics than MOSFETs; hence they are a viable replacement for CMOS based circuit in near future.

In **Chapter-2,** we have discussed about the quantum mechanical tunnelling theory, followed by the concept of band-to-band tunnelling in semiconductor devices. We have briefly discussed about the models used for band-to-band tunnelling, especially the Kane's model. Finally, a brief overview of the device simulator used for our simulations was given. The simulator supports different models, each with their merits in specific applications. The models were compared with themselves and similar models of another simulator in Fig.-2.5, revealing the difference in prediction of current in the simulated device. It can be concluded from the figure that the non-local tunnelling models predict the current much realistically, and the Atlas TCAD simulator predicts higher ON currents than Sentaurus TCAD.

Chapter-3 begins with the comparison between the basic structures of TFET and MOSFET, followed by a brief discussion on the working principle of TFET. Finally, we go through a brief qualitative discussion on various TFET designs. We can broadly classify the vast range of TFET designs for our ease in considering the structural modifications as per requirement. The TFET designs are strongly motivated by two main short-comings of TFET: i. the ambipolar conduction and ii. low ON current.

The TFET designs that are primarily designed for ambipolar conduction suppression are as follows:

1. Hetero Gate Dielectric (HGD) TFETs.
2. Dual and Triple Metal Gate TFETs.
3. Lightly Doped Drain TFET.
4. Doping-less TFET.

The TFET designs which are primarily aimed for increasing the ON currents are as follows:

1. PNPN or NPNP TFET.
2. Raised Germanium Source TFET.
3. UTFET.
4. L-TFET.
5. L-Shaped Gate TFET.
6. III-V Homo-junction and Hetero-junction TFETs.
7. Ferroelectric TFET.
8. Phase Change (PC) TFET.
9. Fin-TFET.
10. Gate All Around (GAA) TFET.
11. Carbon Nano-tube (CNT) and Graphene TFET.

For the reduction of ambipolar conduction multiple dielectrics or using multiple gate metals techniques can be applied. Depending on the ease of fabrication, one can prefer one over other. Although finding a compatible metal with required work-function might be somewhat limiting. Both of these techniques require modification in fabrication process, hence their fabrication might not be cost or time effective. The easier method is to use lightly doped drain method, which is much less complicated. The drawback of

lightly doped drain is the increased contact resistance, which might or might not be problem depending upon the application.

The designs for increasing the ON current of the TFET can be broadly classified into two categories:

1. ON current improvement based on Structural Modification:
    i. PNPN or NPNP TFET.
    ii. Raised (Ge) Source TFET.
    iii. UTFET.
    iv. L-TFET.
    v. L-shaped Gate TFET.
    vi. Fin-TFET.
    vii. GAA TFET.
2. ON current improvement based on usage of New Materials:
    i. III-V Homo and Hetero-junction TFETs.
    ii. Ferroelectric TFET.
    iii. Phase Change TFET.
    iv. CNT and Graphene TFETs.

From the data obtained from the references in Chapter-3, it is clear that the structural modification for achieving higher ON current is possible but not as effective as the beyond silicon materials. Although the structural modifications complicate the fabrication process, they are still viable because of the matured silicon based fabrication technology. For TFETs based on the new materials, mostly isolated devices are fabricated at laboratories for research purposes only. Full-fledged integration of such non-silicon device in form of an IC is yet to be fully tested and their maturity for commercial use is yet to be achieved. Thus, we see that the trade-off for ON current is the fabrication technology. It is very likely that the non-silicon fabrication technology will develop very fast in recent future, enabling more powerful device to be fabricated and integrated, but here we have concentrated more on the Silicon based TFETs.

In **Chapter-4**, the Broken Gate TFET structure has been proposed. Its device dimensions and doping concentrations have also been optimised through simulation.

After optimization, an average sub-threshold swing (ss) of < 30mV/decade over three decades of current (10^{-15} to 10^{-13} A/um) and ≈ 60mV/decade from 10^{-17} to 10^{-18} A/um was observed at a short channel length of 21nm, according to Fig.-12 of Chapter-4. The analytical models for the surface potential and electric field inside the device have also been obtained. Semi-empirically, the effect of drain voltage on surface potential is included to improve accuracy of the model. A closed form expression for the drain current was obtained, which makes the simulation model fast. The device shows negligible reverse gate bias tunneling current, good sub-threshold swing, and high I_{ON}/I_{OFF} ratio considering the short channel length. The device also has very low parasitic capacitances (lower than LTFET structure), as evident from the plots in Fig.-13 to Fig.-15. From the data thus observed, we can conclude that the device's operation will be faster than most of the contemporary Silicon based TFET designs.

As we have used Silicon as the material, its availability and familiar fabrication technology, should make the translation of the device structure from concept to reality possible. Careful simulation and analysis of the Broken Gate TFET design showed that its ON current is better than few of the previously proposed TFET structures. The structure proposed also showed reduced ambipolar nature and steeper sub-threshold swings than many contemporary TFET designs. Thus, the Broken Gate TFET structure has managed to overcome the two main barriers in Silicon Based TFETs to a large extent.

From the above points it is clear that the proposed device structure shows strong potential for its usage in fast, low-power and complementary circuit based applications.

5.2 Scope for Future Work:

After careful evaluation of the available literature on TFETs, we have proposed a renovated TFET structure in Chapter-4, as mentioned earlier. The device proposed in this report is somewhat orthodox in nature owing to its silicon based design, this was done to ease the fabrication procedure. We have compared the results of the proposed device with other existing TFET designs. It was clear from the comparison that the concept although showed desired improvement in ON currents and reduction in leakage and ambipolar conduction, there is enough room for improvements. The following points indicate few of the areas in which further work can be done:

1. In this work, although we have performed some simulations incorporating quantum confinement effect for the proposed Broken Gate Device, we have not included the same for all the simulated results. This is because of the limited compatibility of the quantum correction models with the non-local band-to-band tunnelling model used. In the future, more accurate quantum based simulation can be performed and also a quantum mechanical model can be obtained for the device. This will help obtain a much more accurate device model.
2. The ON current of the device is greater than many Silicon based TFET designs available in the literature, but it is still very less compared to the MOSFETs load currents. The ON current can be improved by considering III-V semiconducting materials, as discussed in literature review section of the report.
3. Only a brief idea of fabrication steps is provided in this report. A detailed process simulation must be performed, followed by device simulation to obtain the realistic performance characteristics, especially in application specific environment.
4. We have obtained a close form expression for the drain current of the device and have also obtained the parasitic capacitance values through simulation, so that a compact model can be easily implemented using hardware description languages (HDLs) like Verilog-A. In future, the device model should be implemented for designing some basic circuits in SPICE tool for performance comparison with other contemporary device based circuits.

List of Publications

1. **Rounak Dutta**, Subir Kumar Sarkar: "**Analytical Modelling and Simulation based Optimization of Broken Gate TFET Structure for Low Power Applications**", communicated with IEEE Transactions on Electron Devices (under second revision).