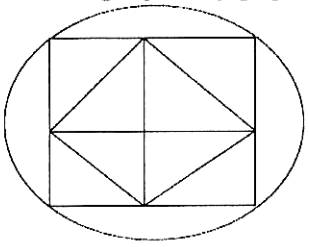
Bachelor of Computer Science and Engineering 4th Year Examination – 2019

Subject: VLSI Systems

Time : Three hours **Full Marks: 100**

Different parts of the same question should be answered together.

CO1 [10]	Answer any one from (a) and (b) in this block [1]
	(a) (i) What is the significance of stick diagram, as applicable in the design of VLSI? What is its advantage and limitation? (ii) Draw the coloured stick diagram for implementing the following Boolean functions using CMOS : $g = W\ \bar{X}Z + \bar{W}\ \bar{Y}$ 5+5
	(b) (i) Implement the Boolean function $f = ab + bd + cd$ using single complex cell designs in four different ways (consider that for any input, its complement is also available). (ii) Implement the Boolean function $f = ab + bd + cd$ using CMOS NAND gates (consider that for any input, its complement is not available). 6+4
CO2 [20]	[2] (i) How do you define LSI and VLSI? (ii) What is Moore's Law? Why and how was it modified in 1975? (iii) What is polysilicon? What is its use in fabrication process? (iv) are the advantage and disadvantage of CMOS? How does CMOS work as an inverter? (v) Explain VLSI design Cycle. [2+3+4+6+5]
CO3 [20]	*Answer any* **two(2)** from **(a), (b)and (c)** *in this block:* [3] (a) (i) Define Floorplanning problem. Define sliceable and non-sliceable floorplan with examples. (ii) Obtain the rectangular dual of the following adjacency graph below.  5+5
	(b) (i) What is placement problem in VLSI physical design? (ii) State the consequences of placement in VLSI Design. (iii) What are constrained and un-constrained placement? (iv) Explain the force directed placement algorithm. 2+2+2+4
	(c) (i) In a hierarchical florrplan sizing problem, there are given two subfloorplans corresponding to two subtrees of a node v, one with t and other with s nonredundant implementations, prove that v has at most s+t-1 nonredundant realizations. (ii) Explain the quadratic placement approach. State the pros and cons of quadratic placement approach. 5+5
CO4 [10]	*Answer any* **one(1) from (a) and (b)** *in this block:* [4] (a) (i) State Kernighan-Lin algorithm for partitioning. (ii) Consider a complete binary tree with n nodes. Apply Kernighan-Lin algorithm to this graph. As the initial partition, let v_a, for all internal vertices, be in one set and v_b, for all leaves, be in the other set. 3+7
	(b) Present the Fiduccia-Mattheyses Algorithm. The following matrix provides 4 modules a,b,c,d with their entries representing the number of connections between the two modules. Apply Fiduccia-

Mattheyses Algorithm heuristic to obtain the partitioning.

	a	b	c	d
a	0	1	2	3
b	1	0	1	4
c	2	1	0	3
d	3	4	3	0

3+7

CO5
[40]

Answer any **two(2)from (a), (b) and (c)** *from this block:*

[5]

(a) (i) What are the advantages of Fiduccia-Mattheyses algorithm over Kernighan-Lin algorithm? What are the similarities between Fiduccia-Mattheyses algorithm and Kernighan-Lin algorithm?

(ii) What is simulated annealing? How can simulated annealing approach be applied in Floorplanning? Given a Polish expression corresponding to a given slicing floorplan. Show that the expression 12+3+4+.....+n+ can be reached, and vice versa, using three operations in simulated annealing approach of floorplan. (+ and * represent horizontal and vertical bisection respectively.)

(iii) State the various approaches for placement problem- Top-down, iterative, constructive.

[5+9+6]

(b) (i) Define routing problem. What are different routing regions?

(ii) Define Channel, terminal, switch with respect to routing.

(iii) Give an example for the worst case of Soukup's maze router.

(iv) Route the following channel of 11 columns using the Left edge algorithm, where 0 indicates an empty Position.

TOP = 3 4 0 1 2 4 3 5 2 1 0

BOT = 1 0 3 0 4 0 5 2 1 4 5

2+6+5+7

(c) (i) What is dogleg in routing? Use Dogleg router to to route the following channel.

1 0 0 3 0 2 0 1 0 3 0 4 1 3 4 5

0 2 1 0 3 4 0 2 0 5 0 5 0 0 3 0

(ii) Explain YK algorithm in routing. Route the channel shown in question 5(c)-(i) using YK algorithm

[10+10]