B.E. COMPUTER SCIENCE AND ENGINEERING SECOND YEAR FIRST SEMESTER – 2019

Subject: DIGITAL CIRCUIT | Time: 3 Hrs. | Full Marks: 100

Answer any five questions

1. a) Define propagation delay of a digital circuit. Why does propagation delay hazard occur? Explain it with a proper example.
   b) Summarize the advantages of Active pull-up network over passive pull-up network.
   c) State the advantages of Enhancement MOSFET over Depletion MOSFET for switching circuit design.
   d) What are the disadvantages of DTL family over TTL family? (3+5)+5+4+3

2. a) Design a RTL XOR gate with minimum number of transistors.
   b) Design CMOS circuit for the given Boolean functions :
   i) $y = a(b + c)$; ii) $y = ab + \bar{c}$ 10+ (5+5)

3. a) Design an ECL NOR gate with practical transistor and explain its operation. State the advantages of ECL gate over RTL gate.
   b) Design NAND gate using DTL family and explain its operation. (7+3)+10

4. a) Define sampling theorem and explain the oversampling condition.
   b) What is Quantization. Draw a block diagram of an A/D converter.
   c) Design Binary Weighted Resister D/A Converter and explain its operation. 6+6+8

5. a) Draw the block diagram of NE555 timer IC and explain its architecture.
   b) Design an astable multivibrator using NE555 timer IC to generate the 2Khz clock frequency and duty cycle will be 70%. Consider the value of capacitor 0.1uF. Draw the timing diagram of capacitor charge and discharge cycle for this multivibrator. 8 +6 +6

6. a) What is PROM ? Sketch a six transistor static RAM cell and explain its operation.
   b) Summarize the advantages of SRAM over DRAM.
   c) What is Volatile memory and its applications. (2+8)+5+5

7. a) What is the disadvantage of DCTL over DTL family.
   b) What is Totem-pole architecture ? Design a TTL NAND gate and explain its operation.
   c) Design and describe the function of HTL NAND gate. 3+(3+7) + 7
