## B.E. Computer Science and Engineering 2<sup>nd</sup> Year 1<sup>st</sup> Semester Examination 2019 Subject: Computer Organisation

Time: 3hrs Full Marks: 100

## Answer any five

Answer all the sub-parts of a question in adjacent location

1	a.	With the help of a diagram discuss about the Von-Neumann architecture.	8
	b.	Mention the different steps of a complete instruction execution cycle.	3
	c.	How is branch prediction performed when dealing with microinstruction?	3
	d.	List steps which are followed during compilation process.	3
	· e.	What sort of steps need to be followed during context switching?	3
2	a.	Mention the pros and cons of (i) Sign-magnitude, (ii) 2's complement representation of numbers.	4
	b.	Describe the usage of stack in subroutine call.	3
	c.	Pictorially show how stack can be designed using shift registers.	3
	d.	Consider the example: $Z = (A + B) \times (A + B)$ ; implement this using 2-address, 1-	10
		address and 0-address machines respectively.	
3	a.	Mention few advantages of Micro-programmed Control Unit over Hardwired Control Unit.	2
	b.	Explain the working principle of <i>Wilkes'</i> design. Assume 3-bit address fields, and required number of control signals. Consider that the external source provides the starting address of a microprogram stored in the control memory (CM). Keep the facility when control unit can suitably respond to external signals or conditions.	8
	c.	Mention few ways to improve the processor organization.	4
	d.	Discuss how co-processor works.	6
4	a.	Discuss about precise and imprecise exceptions in superscalar processor.	4
	b.	What are the ways to get rid of these?	4
	c.	Illustrate the issues related to data hazard and control hazard (you are expected to	12
		discuss about the some problems and corresponding solutions).	

5	a.	Diagrammatically show the different register organization of CPU.	5	
	b.	Discuss about the basics issues related to floating point arithmetic unit.	5	
	c.	Define the four requirements to be satisfied by an instruction set.	4	
	d.	Describe how bit-sliced ALU works.	6	
6		Explain how prefetching and look-up free cache enhances the performance of the stem.	4	
	(b)	Discuss the cache coherence problem with solution.	4	
	(c) Identify the advantages of interleaving procedure in memory system.			
	(d)	Explain the functionality of a SRAM cell (circuit diagram is required).	6	
	(e)	Illustrate how write-back protocol differs from write-through protocol.	4	
7	Discuss about the following (any two)			
		a. Cache Memory mapping methods		
		b. Multiplication <b>OR</b> Division method in Computer		
		c. Nanoprogrammed Control Unit		
		d. Direct Memory Access		