Ref. No.: Ex/CSE/T/115A/2019(OLD)

B.E. Computer Science and Engineering,
1^{st} Year, 1^{st} Semester Examination(OLD), 2019
Digital Logic

Full Marks: 100 Time : 3 Hr

Make assumptions wherever necessary. Do not BREAK questions parts and their corresponding groups.
Marks Distribution : Group A, C, D = 20 each; Group B = 40

GROUP A: Answer any ONE question

(Q 1) (a) Perform the following operations using binary 8-bit arithmetic : $(3 \times 2 = 6)$
(i) Add +14 to -17
(ii) Sub +21 from -13

(b) What is the difference between synchronous counter and asynchronous counter? [4]

(c) A multiplier circuit takes a 2 bit binary numbers y_1y_0 and x_1x_0 and produces an output number $z_3z_2z_1z_0$ that is equal to the arithmetic product of the two input numbers. Design the logic circuit for multiplier. [10]

(Q 2) (a) Design a BCD ripple counter. [5]

(b) Minimize the following function using K-Map and Quine–McCluskey method. Give the equivalent logic diagram of the minimized circuit: $(5 + 8 + 2 = 15)$

$$f(A, B, C, D) = \sum(0, 1, 4, 6, 9, 12, 15) + D(2, 3, 6)$$

GROUP B

Answer all questions $20 \times 2 = 40$

(Q 1) Perform subtraction using 2's complemented method : 01100 – 00011

(Q 2) Convert the following binary number to octal and then to decimal : 11011100.101010

(Q 3) Encode the decimal number 46 to Gray Code

(Q 4) Convert $(6.75)_{10}$ to binary.

(Q 5) How many binary bits are necessary to represent 748 different numbers?

(Q 6) What is Positive Logic.

(Q 7) Convert the following SOP expression to an equivalent POS expression :
$A.B.C + A.\overline{B}.\overline{C} + A.\overline{B}.C + A.B.\overline{C} + \overline{A}.\overline{B}.C$

(Q 8) Design an XOR gate using minimum NAND gates

[Turn over

(Q 9) Prove that NOR is a universal gate.

(Q 10) State Duality Theorem.

(Q 11) Show that the dual of the Exclusive OR is equal to its complement. (Note : Do not use truth table)

(Q 12) Design the expression $A.B + C$ using minimum NOR Gates

(Q 13) How many 3-line-to-8-line decoders are required for a 1-of-32 decoder?

(Q 14) How many outputs would two 8-line-to-3-line encoders, expanded to a 16-line-to-4-line encoder, have?

(Q 15) State Race Around condition

(Q 16) Master-slave J-K flip-flops are called pulse-triggered or level-triggered devices because input data is read during the entire time the clock pulse is at a LOW level. State **TRUE/FALSE**

(Q 17) Design a J-K Flip-flop using NAND and NOR gates respectively.

(Q 18) At what moment of the clock-pulse a correct output is achieved from a master-slave J-K flip-flop, when its inputs are stable ?

(Q 19) What kind of logic device or circuit is used to store information?

(Q 20) Using four cascaded counters with a total of 16 bits, how many states must be deleted to achieve a modulus of 50,000?

GROUP C: Answer any one question

(Q 1) (a) Design a full subtractor using NAND gates only [5]

(b) Design a 3-bit Carry Look Ahead Adder considering an initial carry C_I. [10]

(c) Determine the minimal sum-of-products expression for [5]

$$f(w,x,y,z) = \sum(0,2,4,9,12,15) + \sum_{\phi}(1,5,7,10)$$

(Q 2) (a) Convert an S-R flip-flop to J-K flip-flop. [4]

(b) State the logic circuit, truth table and derive the equivalent logic expression from the truth table of the following Boolean expression $Y = A\overline{B} + \overline{B}C$ $[1 + 2 + 3 = 6]$

(c) Explain the operation and outline the problems associated with synchronous and asynchronous counters. Draw a graph of the outputs to help explain your answer. [10]

GROUP D: Answer any one question

(Q 1) Design a 3-bit synchronous UP/DOWN counter using J-K flip-flop

(Q 2) Design a MOD-12 synchronous counter using D-Flip-flops