Renovated Nano TFET Structures for Performance Improvement: Analytical Modeling and Simulation Based Validation

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ABBREVIATIONS:

TFET-Tunneling **F**ield **E**ffect **T**ransistor

SRH – **S**hockley-**R**ead-**H**all

BTBT- Band **T**o **B**and **T**unneling

QCE-Quantum **C**onfinement **E**ffect

LS-HS-DM-DG TFET- L-shaped **H**fO_2-**S**iO_2 **D**ouble **M**etal **D**ual **G**ate **TFET**

LS-SH-DM-DG TFET- L-shaped **S**iO_2- **H**fO_2 **D**ouble **M**etal **D**ual **G**ate **TFET**

LS-SS-DM-DG TFET- L-shaped **S**iO_2- **S**iO_2 **D**ouble **M**etal **D**ual **G**ate **TFET**

DTG-CSC-TFET - Double **T**rench **G**ate **C**overed **S**ource-**C**hannel **TFET**

ABSTRACT

This work focuses on emphasizing the drawbacks of MOSFETs which paved the way for the conception of novel Tunneling Field Effect Transistors (TFETs). TFETs offer several advantages as compared to MOSFETs owing to the band-to-band tunneling phenomenon that is inherent in these devices. TFETs exhibit subthreshold swing below 60mV/decade (which is the limit for MOSFETs) and increased immunity to short channel effects. Moreover, the integration of the TFET fabrication process with the existing MOSFET fabrication process is feasible. The conventional TFETs suffer from ambipolar conduction and low ON-current. Hence, considerable research endeavors have been focused on developing novel TFET structures, based on structural and material variations. The work presented in this thesis aims at incorporating these variations in order to obtain novel TFET structures that show low subthreshold swing, high ON-current and reduced ambipolarity. Firstly, the basic operating principles of TFETs are briefly divulged upon. The output characteristics and the transfer characteristics are explained based on the underlying device physics. The dependence of the device performance on various parameters is highlighted. TFET operation is based on band-to-band tunneling mechanism and the tunneling current is directly proportional to the tunneling probability.

The first work introduces a novel gate-engineered Double Metal Dual Gate TFET with L-shaped dielectric. Gate engineering in this structure is achieved by varying the oxide material along the L-shaped dielectric region. Three structural variations have been obtained namely, LS-HS-DM-DG TFET, LS-SH-DM-DG TFET, and LS-SS-DM-DG TFET. The performance parameters of the three variants have been contrasted using Silvaco, Atlas simulations. LS-HS-DM-DG TFET exhibits a subthreshold swing of 24mV/decade which is the lowest amongst the three variants. This structure also shows better suppression of ambipolar conduction. Hence, LS-HS-DM-DG TFET is deemed to be the most optimized structure in this work.

The second work introduces a novel Double Trench Gate Covered Source-Channel TFET (DTG-CSC-TFET). The configuration of the structure, including the extended source region, maximizes the band-to-band tunneling area thereby resulting in higher ON-current. Analytical current modeling of the DTG-CSC-TFET has been presented to account for line tunneling and

point tunneling mechanisms inherent in the proposed device. The essential device parameters have been simulated using Silvaco, Atlas. The quantum confinement effect (QCE) has been studied using simulation by including the Schrodinger-Poisson model to account for the effects of energy band discretization in the regions where channel thickness is sub-5nm. The proposed DTG-CSC-TFET has a very high ON-current and a minimum subthreshold slope of 22mV/decade thus having promising implications in future applications.

CHAPTER 1

INTRODUCTION AND ORGANIZATION OF THE THESIS

1.1 Introduction and Motivation
1.2 Literature Survey and Background Research
1.3 Organization of the Thesis

1.1 Introduction and Motivation

The last few decades have witnessed a phenomenal growth in the electronics industry owing to advancements in the development of solid state devices and integrated circuits (ICs) technology. This furtherance fueled a rapid expansion in the fields of application of ICs, ranging from telecommunication, high-performance computing to consumer electronics. Demands for improved performance and increased functionality led to a boost in the semiconductor industry which observed an era of continual scaling of transistors resulting in increased packing density. Intel co-founder, Gordon Moore predicted back in 1965, that the number of transistors in a given chip area would double every 18 months, which in turn would enhance the performance. This law was fulfilled for several years and the industry moved through phases of Medium Scale Integration (MSI), Large Scale Integration (LSI), Very Large Scale Integration (VLSI) and Ultra Large Scale Integration (ULSI). Researches in the field of device and material science have tried

to abide by the prescripts of Moore's law to sustain the growing needs of modern technology-driven human civilization. At every technology node, concepts of new devices and novel structures have emerged. The amalgamation of nanotechnology and nanoscience research has transformed microelectronics into present-day nanoelectronics. Groundbreaking research in the field of nanoelectronics has resulted in the conception and realization of Carbon nanotube transistors, quantum computing devices, spintronics, single electronics devices, optoelectronics technology, etc.

The scaling of CMOS transistors adheres to the International Technology Roadmap for Semiconductor (ITRS) [1]. As per ITRS, the gate length of the transistors was expected to be scaled down to 22nm by the year 2012 and beyond. Currently, the ITRS community has undertaken a "technology push" strategy to develop a roadmap for the "More than Moore" trend. For several decades, MOSFETs have been the device of choice in CMOS technology. Scaling of MOSFET feature size not only increased the packing density, it also led to reduced gate lengths, thereby reducing gate capacitances. This ultimately led to higher switching speeds. Furthermore, voltage scaling which is a predominant means of device miniaturization meant reduced power consumption for the devices. However, the scaling of transistors came at the cost of exponential increase in the investments that went into the semiconductor foundries. This is owing to the fact that reducing feature sizes impinges the need for much higher resolution of photo-lithography, excellent process control and enhanced reliability. Moreover, there is a physical limit for reduction in feature size.

Fundamentally, MOSFET operation is based on the principle of thermionic emission between source and channel, which subsequently results in drain current. It is known from semiconductor physics, that the flow of current in the channel is dependent on the creation and sustenance of an inversion layer below the gate oxide. If the gate bias is lower than the threshold necessary for inversion, no carriers flow through the channel. Increasing the gate voltage leads to the lowering of the potential barrier, causing thermionic injection into the channel. However, for small-geometry MOSFETs, the potential barrier is controlled not only by the gate-to-source voltage (V_{GS}) but also by the drain-to-source voltage (V_{DS}). The increase in the drain voltage, in such a scenario, leads to the lowering of the potential barrier in the channel. Essentially, a situation may

arise whereby the channel conducts current even when the V_{GS} is less than the threshold voltage, due to the drain voltage (V_{DS}). This current conduction, below the threshold voltage, is termed as subthreshold current. Small-geometry MOSFETs also suffer from various second order effects such as threshold voltage roll-off, Hot Carrier Effects (HCEs), Drain Induced Barrier Lowering (DIBL), carrier voltage saturation, Channel Length Modulation, etc. which leads to high leakage currents. Hence, reducing the feature size, leads to increased OFF-state current owing to subthreshold conduction and higher subthreshold slope in case of MOSFETs. The subthreshold slope (SS) of a MOSFET is defined by the change in the gate voltage V_{GS} necessary to increase the drain current (I_{DS}) by a factor 10. In order to obtain a higher I_{ON}/I_{OFF} ratio it is desired that the value of subthreshold slope be low. This would lead to a lower I_{OFF} implying reduced OFF-state power dissipation. The lowest value of the subthreshold slope of a MOSFET is 2.3kT/q, which at room temperature is 60mV/decade. Hence, in order to obtain an I_{ON}/I_{OFF} ratio of 10^5, the applied gate voltage would have to be 5×60 mV=0.3V. Such an extent of voltage scaling is not feasible in MOSFETs due to its physical limits. As a result of this, I_{ON}/I_{OFF} ratio is considerably low for MOSFETs. The aforementioned drawbacks deemed it a necessity to explore alternative devices for ICs.

A plausible solution to the drawbacks of MOSFETs came in the form of tunneling field effect transistors (TFETs) that were able to exhibit subthreshold slopes less than 60 mV/decade. This was possible due to the stark contrast in operating principles between the two devices. As discussed previously, the current in MOSFET depends upon thermionic emission of carriers across the source to the channel overcoming the potential barrier. TFETs operate on the principle of band-to-band tunneling through the potential barrier between the source valence band and the channel conduction band. In OFF-state the potential barrier is wide enough to prevent any OFF-state carrier conduction. Additionally, as the TFET and MOSFET structures are fundamentally similar, with the only difference being dissimilar doping types at the source and drain, the integration of the TFET fabrication process with the existing MOSFET fabrication process is facile. The main focus of this thesis work is to divulge upon various existing and novel TFET structures that can achieve high I_{ON}/I_{OFF} ratio and low subthreshold slopes. This will enable further lowering of supply voltage and device dimensions.

1.2 Literature Survey and Background Research

In the year 1994, Reddick and Amaratunga [2] proposed the first Silicon-based BTBT transistor. They were motivated by the scope for increased functionality due to negative differential resistance that was prevalent in existing tunneling devices. They were able to fabricate the proposed reverse biased diode on bulk silicon. This structure was able to achieve modulation in tunneling current upon modulation of tunneling width, which itself is a function of applied bias, depletion width and energy bang gap Eg. They also acknowledged that the mechanism of the BTBT transistor could lay the foundation of a new class of devices that had the potential to replace MOSFETs and allow further scaling in feature size.

TFET structures are broadly classified as-(1) planar TFETs that possess a planar current carrying surface, (2) three dimensional TFETs whereby the current carrying surface extends over all three dimensions. The early TFETs were SOI (Silicon on Insulator) based. The buried oxide layer served to block any leakage paths from the source to the drain, in the bulk region. Additionally, since the source-body and drain-body depletion regions are limited, the structure provides better gate control. However, conventional planar TFETs usually have very low I_{ON} and also suffer from poor SS. This is mainly due to poor BTBT rates observed during practical demonstrations, as opposed to the theoretical expectations. Several structural and material variations been proposed to overcome the limitations of the conventional planar TFETs.

Similar to Double Gate MOSFETs [3-6], the concept of Double Gate TFETs (DGTFETs) was being explored in the 2000s. In 2010, Hoof *et.al*. [7] presented a pseudo-2D surface potential model for DGTFETs, thus laying the foundations for quantification of electrical parameters for the proposed device. In 2011, M. J. Kumar *et.al*. [8] estimated the effects of process induced variations on DGTFETs and proposed strained Double Gate [9] TFETs (SDGTFET) to reduce the impact of process-induced variations on the performance characteristics, thereby improving the reliability of DGTFETS for future applications in CMOS technology. Basically, double gate

TFETs comprise of two gates, the top/ front gate and the bottom/back gate. Such a configuration enhances the electrostatic control of the gates on the channel, as the gate electric field lines from one gate terminate on the other gate, instead of the channel. Also, the presence of two gates ensures the formation of two channels and hence, escalates the amount of current that can flow through the device.

In 2011 M. J. Kumar *et.al*. [10] proposed a dual material gate TFET (DMG TFET) based on the concept of dual material gate MOSFETs [11-12]. This structure comprised of two gate metals with different work functions. The gate near the source was called the tunneling gate, as the source-channel interface is where the useful BTBT occurs, and the gate near the drain was termed as auxiliary gate. Taking the example of p-type DMG TFET it was justified that if the tunneling gate had a higher work function material compared to the auxiliary gate, a higher potential difference between the source and the channel would result in reduced tunneling length and subsequently, increased I_{ON}. Similar arguments can be made to justify the usage of lower work function metal at the drain end, which results in reduced I_{OFF}. Such a structure has better subthreshold slope and is less prone to DIBL effects.

In 2008, Woo *et.al*. [13] introduced the concept of PNPN type configuration. In the PNPN TFET [14] configuration, the P+ source is followed by an N+ pocket doping region. The channel and the drain are intrinsic and N+, respectively. The pocket so formed, creates a conduction band edge (E_C) local minima when V_{GS}=0. This creates a region of abrupt change and a significant lowering of the tunneling width. Moreover, the structural modification enhances the lateral electric field at the source-channel interface resulting in higher I_{ON}.

In 2010, Liu *et.al*. [15] proposed a raised Ge-source TFET to overcome the limitations of Si-based TFETs. Owing to low bandgap, germanium is a popular replacement for silicon as source material. The raised source configuration serves to increase the tunneling area as the entire lateral extent of the source is interfaced with the channel region. Due to increased tunneling area, BTBT is enhanced leading to high I_{ON}.

In 2011, Dutta *et.al*. [16] conceptualized the formation of a heterojunction at the source channel interface for achieving higher I_{ON}. This laid the basis for a new class of TFETs known as the

heterojunction TFETs. The proposed structure comprised of $In_{0.7}Ga_{0.3}As$ as the material of choice for the drain and channel, and $GaAs_{0.35}Sb_{0.65}$ as the source material. This leads to staggered characteristics in the band diagram at the source-channel junction that results in shorter tunneling barrier width.

In 2016, Yang [17] proposed an L-shaped gate TFET (LG-TFET) which consisted of an inverted L-shaped gate metal region inserted into the channel. The resultant channel was hence, U-shaped. The P+ source was enveloped by an N+ pocket rendering this structure a PNPN configuration. The structure ensured a relatively large tunneling area as the tunneling junction was perpendicular to the channel. The LG-TFET exhibited a minimum SS of 38.5 mV/decade at V_{GS}=0.2V.

In 2018, Rafat *et.al.* [18] proposed a novel line TFET structure that consisted of a gate over source-channel overlap pockets (GO-SCOPs). This structure provided an inverted C-shaped junction, enabling both vertical and lateral tunneling. The structure was able to achieve an average SS of 48 mV/decade at V_{GS}=2V and V_{DS}=0.5V.

In 2019, Park *et.al.* [19] conceptualized and simulated a double gate TFET having vertical channel regions sandwiched between lightly doped Si (VS-TFET). The vertical junction at the source end enabled steeper subthreshold swing and higher I_{ON} by restricting the tunneling width and increasing the tunneling area. The structure exhibited a minimum SS of 17mV/decade and maintains SS value less than 60mV/decade over a considerable range of $I_{D.}$

In 2019, Kim and Woo [20] presented a novel covered source-channel TFET (CSC-TFET) with a trench gate configuration. This structure aided the enhancement of the tunneling junction area and was able to achieve I_{ON}/I_{OFF} ratio of 10^{10}, subthreshold swing below 40 mV/decade and I_{ON} of approximately 10^{-5} A/μm.

Wu *et.al.* [21] in 2019 proposed a Si-based fin-type TFET where the traditional semiconductor material drain was replaced by a metal silicide drain. Hence, a P-I-M TFET was achieved instead of the conventional P-I-N TFET. TCAD simulations revealed that with appropriate work function of 4.25eV the ambipolar effect was greatly suppressed and the OFF-state current was improved by a factor of 276. This was due to reduced Band-to-Band Tunneling (BTBT) and low

Shockley-Read-Hall (SRH) recombination rate at the channel-drain interface due to the metal silicide drain. The I_{ON} remains unchanged while altering the metal silicide work function as it depends only on the BTBT at the source-channel interface.

With feature sizes of 20nm or less, present-day TFET structures suffer from quantum confinement effect (QCE). It is hence, imperative to the study the effect of this phenomenon on the performance of TFETs. In 2019, Najam and Yu [22] explored the impact of geometrical quantum confinement effect (QCE) in LTFET that was proposed by [23]. Such a consideration was necessary as the overlapped channel between the source and gate was of length 4 nm. This work describes the discretization of the conduction band into energy subbands while the valence band remains continuous, under the QCE. The quantum confinement effect in the proposed structure was visualized by employing the self-consistent Schrödinger-Poisson (SP) model which solves the Schrödinger and Poisson equations for bound state energies and potential, respectively. It was revealed that at V_{GS}=0.2V, without including the QCE, Band-to-Band Tunneling is possible as E_C and E_V are aligned. However, by considering QCE, the first discrete energy subband in the conduction band is not in alignment with the source valence band. This stalls BTBT in the overlapped region of the channel at the given V_{GS}. Hence, higher gate bias is necessary in the LTFET while considering QCE.

1.3 Organization of The Thesis

The present dissertation has been organized into the following chapters:

- ***Chapter 1*** formally introduces the work presented in this thesis. It highlights the drawbacks of MOSFETs which instigated the search for novel devices and how Tunneling Field Effect Transistors (TFETs) overcome most of these drawbacks. A concise literature survey propounds the research developments in the field of TFETs over the last two decades.

- ***Chapter 2*** aims to briefly describe the basic structure of a TFET and explains the underlying device physics. It dedicates a section to discuss the dependence of the device performance on several parameters. Finally, an attempt is made to quantitatively account for the Band-to-Band tunnelling mechanism using WKB approximation.

- ***Chapter 3*** introduces a novel gate engineered L-shaped Dielectric Double Metal Dual Gate TFET structure. Three structural variations have been presented by altering the gate oxide material used in the L-shaped dielectric region namely, LS-HS-DM-DG TFET, LS-SH-DM-DG TFET, and LS-SS-DM-DG TFET. The device performance metrics are compared using Silvaco Atlas simulations. A subthrehsold swing of 24mV/decade is observed for LS-HS-DM-DG TFET which is most optimized for this structure. The LS-HS-DM-DG TFET also achieves suppressed ambipolar conduction.

- ***Chapter 4*** introduces a novel Double Trench Gate Covered Source-Channel TFET (DTG-CSC-TFET). This structure seeks to maximize the band-to-band tunneling area in order to enhance the ON-current. An analytical current model has been presented to account for the total current that results as a consequence of line and point tunneling mechanisms that prevail in the DTG-CSC-TFET. The essential device parameters have been simulated using Silvaco Atlas. The quantum confinement effect (QCE) has been studied using simulation by including the Schrodinger-Poisson model to account for the effects of energy band discretization in the regions where channel thickness is sub-5nm. The proposed DTG-CSC-TFET has a very high ON-current and a minimum subthreshold slope of 22mV/decade thus having promising implications in future applications.

- ***Chapter 5*** concludes the thesis and discusses the future scope for research.

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CHAPTER 2

INTRODUCTION TO TUNNELING FIELD EFFECT TRANSISTORS

2.1 Structure and Operation of TFETs

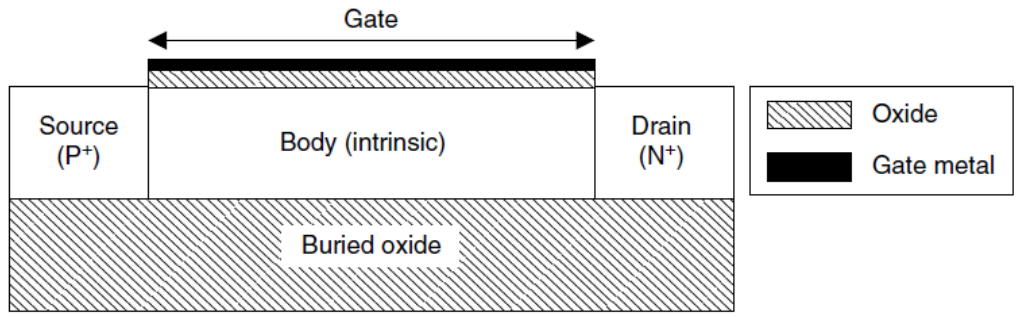
2.2 Device Characteristics

2.3 Dependence of Performance on Device Parameters

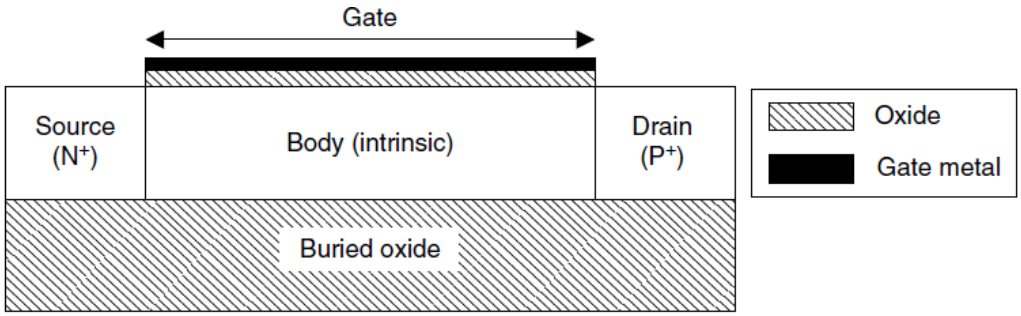
2.4 Band-to-Band Tunnelling (BTBT) Mechanism

2.1 Structure and Operation of TFETs

Tunneling Field Effect Transistors are fundamentally gated p-i-n diodes. Fig. 2.1 (a) illustrates the typical structure of a conventional planar SOI n-channel type TFET [1]. It is observed that unlike n-channel MOSFET [2-3] which has n-type doped source and drain regions, the n-channel TFET has a p-type source doping. This may be regarded as the only major structural difference between a MOSFET and TFET. Fig. 2.1 (b) shows the structure of a similar p-channel TFET depicting the n-type source doping. The channel region is generally intrinsic or is lightly doped. The source and drain regions are heavily doped.



(a)



(b)

Fig. 2.1 Basic Structure of (a) n-channel TFET (b) p-channel TFET

The operation of any device is better understood by its current characteristics under different biasing conditions. For transistors, it is essential to study the transfer and output characteristics in order to appreciate the underlying device physics. The band diagrams of the TFET under various biasing conditions give us a qualitative understanding of the resultant variation in drain current. Fig 2.2 shows the band diagram of the TFET in Fig. 2.1(a), under thermal equilibrium [$V_G=V_S=V_D=0$]. Under this condition, two depletion regions are present - at the source-channel interface and at the channel-drain interface. The OFF-state of the TFET is when the drain voltage $V_{DS}>0$ and $V_{GS}=0$. Under such conditions, charge carriers present in the channel can drift towards the drain. However, only a few electrons may reach the drain via this mechanism. This is due to the fact that the n-TFET has a P+ source and may only have a few electrons in its

conduction band that can be injected into the channel. Hence, OFF-state current in TFETs is negligible. This can be contrasted with MOSFETs where the N+ source which may furnish electrons to the channel by thermionic emission and result in high OFF-state current. Tunneling of electrons does not occur at the source-channel interface as there are no available energy states in the channel conduction band.

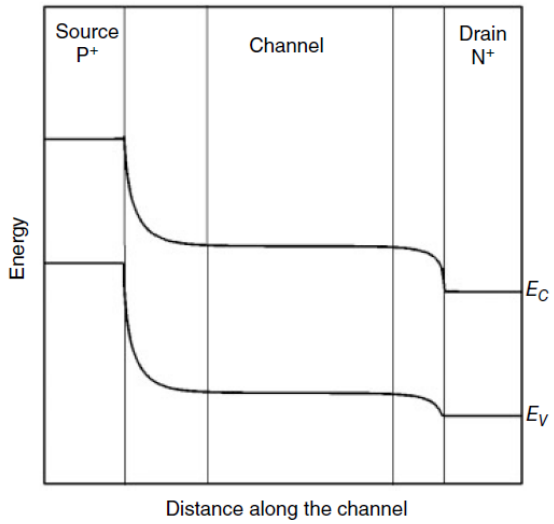


Fig. 2.2 Band Diagram of n-TFET under Zero Bias (Thermal Equilibrium)

This is demonstrated in Fig. 2.3. Increasing the gate voltage V_{GS} has the effect of lowering the energy bands in the channel with respect to the source. At a certain value of V_{GS}, the source valence band just aligns with the channel conduction band as shown in Fig. 2.4 (a). Hence, electrons in the source conduction band can effectively tunnel through the potential barrier formed by the bandgap E_g and occupy the available states in the channel conduction band. As V_{GS} is further increased, the energy bands in the channel are further lowered. Hence, all the electrons in the source valence band occupying energy levels between the channel conduction band edge ($E_{C,\ Channel}$) and the source valence band edge ($E_{V,\ Source}$) may tunnel to the channel conduction band. The TFET is said to be in ON-state under such biasing conditions. Once the electrons reach the channel conduction band, they effectively drift towards the drain and contribute to the drain current. A steep increase in the drain current is observed with increasing V_{GS} in the ON-state. Fig. 2.4 (b) shows the band diagram when the TFET is deep into ON-state.

It can be observed from the figure that higher gate bias leads to greater electric field and a consequent reduction in the tunneling length. The tunneling length corresponding to the energy level $E_{C,\ Channel}$ is t_2 and it is shown that an electron in the source valence band having energy greater than $E_{C,\ Channel}$ has corresponding tunneling length t_1. Tunneling probability is inverse exponentially dependent on the tunneling length. Hence, increase in gate bias not only increases the electrons available for tunneling but also enhances the tunneling probability.

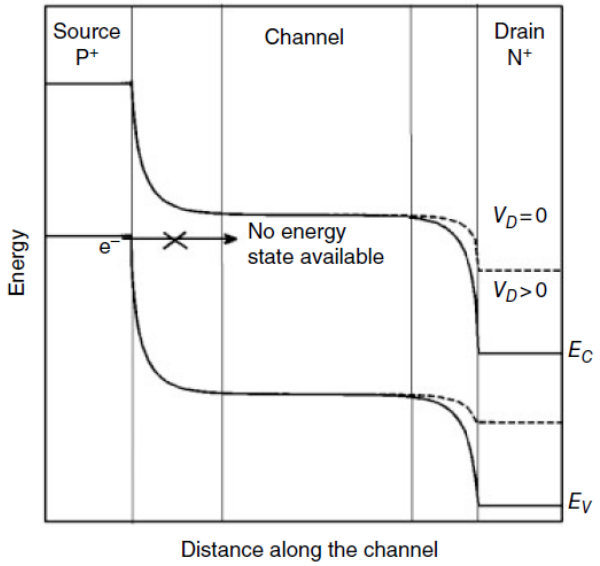


Fig. 2.3 Band Diagram of n-TFET in OFF-state

It can also be inferred that contribution the total current is less for electrons that occupy lower energy levels in the source valence band as the tunneling probability decreases. Further increase in the positive gate bias ($V_{GS}>0$) tends to cause inversion in the channel region below the oxide. This inversion layer comprises of electrons. At a certain value of V_{GS}, the magnitude of the inversion charge layer becomes comparable to the N+ doping at the drain. The channel then becomes effectively shorted to the drain and the channel potential becomes approximately equal to the drain potential. Any further increase in V_{GS} does not cause lowering of the channel energy bands. The channel potential gets pinned to the drain potential. This condition is known as the pinning of channel potential. This occurs when V_{GS} becomes comparable to V_{DS} and the gate

control over the channel potential is completely lost for $V_{GS}>V_{DS}$. The pinning phenomena can be observed from Fig. 2.5.

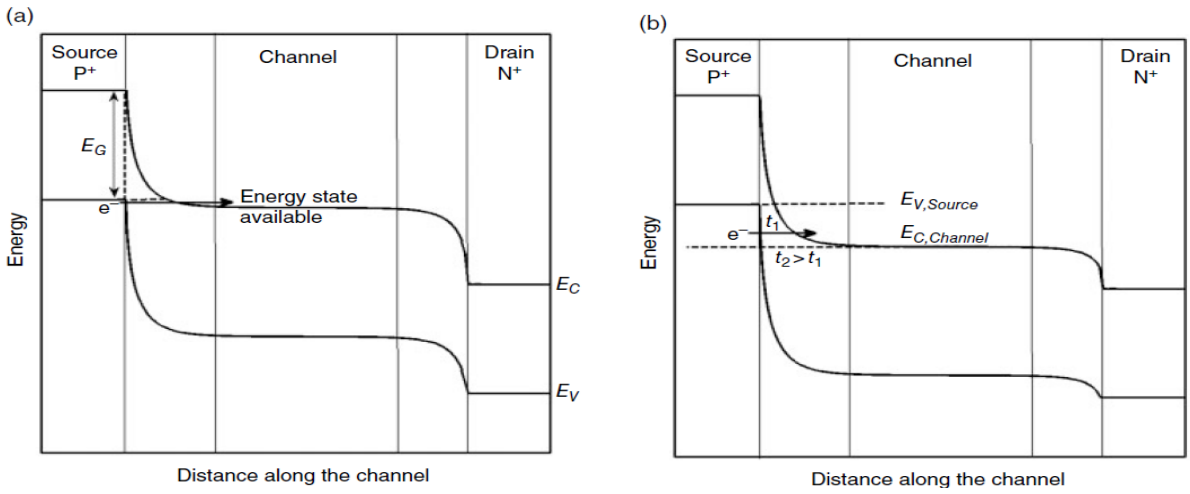


Fig. 2.4 Band diagram along the surface of n-TFET (a) at the beginning of ON-state (b) well-into the ON-state

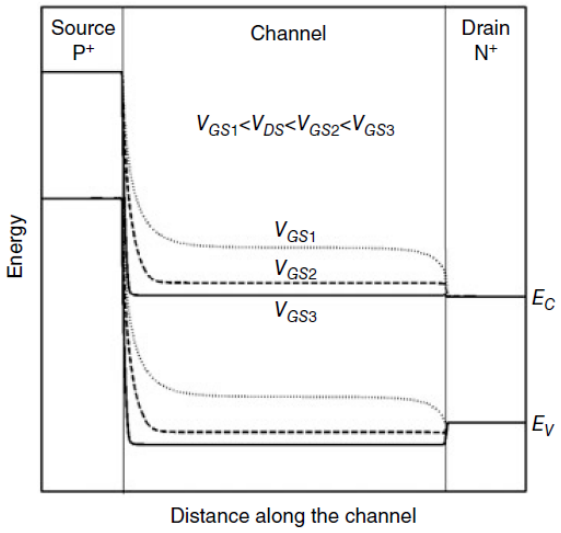


Fig. 2.5 Band Diagram along the surface of n-TFET with increasing value of V_{GS} under ON-state conditions.

2.2 Device Characteristics

Instead of applying positive gate bias, if we apply negative V_{GS} to an n-channel TFET, we observe a phenomenon known as ambipolar conduction. The negative gate bias has the effect of raising the channel energy bands with respect to the source. As shown in Fig. 2.6, at a certain negative bias, the channel valence band gets aligned to the drain conduction band, at the channel-drain junction. Hence, electrons tunnel from the channel to the drain leading to current flow. It is worth noting that the polarity of the current is the same for both positive and negative gate bias as the direction of flow of electrons remains unchanged in both the cases. Such conduction of current for negative V_{GS} is known as ambipolar conduction. Further increase in V_{GS} reduces the tunneling length and hence increases the tunneling probability. This leads to steep rise in current. At a certain value of V_{GS} the channel potential gets pinned to the source potential.

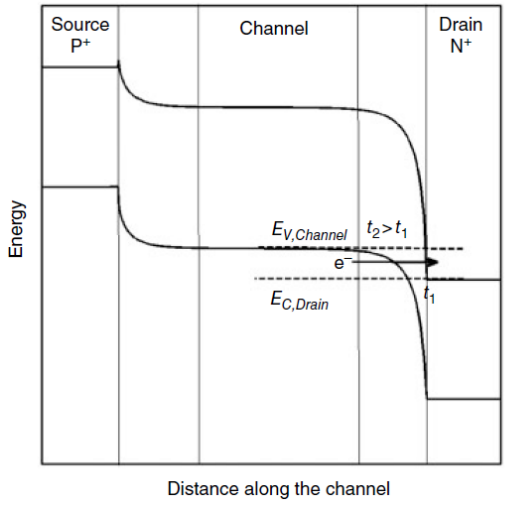


Fig. 2.6 Band Diagram depicting ambipolar conduction in n-channel TFET for $V_{GS}<0$

Fig. 2.7 shows the transfer characteristics of the n-TFET shown in Fig. 2.1 (a). It is observed that for lower values of V_{GS}, the TFET remains in OFF-state as the channel energy band bending is not sufficient to provide available energy states for tunneling from the source valence band. As, V_{GS} is increased and tunneling is facilitated by channel energy band bending, the current rises

steeply. When the V_{GS} becomes comparable to or greater than V_{DS}, the channel potential gets pinned to the drain potential and the gate loses control of the channel potential. Consequently, the current no longer rises steeply due to pinning. Similar characteristic is observed for negative gate bias when ambipolar conduction occurs. Hence, when V_{GS} is positive, electrons tunnel at the source-channel junction and when V_{GS} is negative, electrons tunnel at the channel-drain junction.

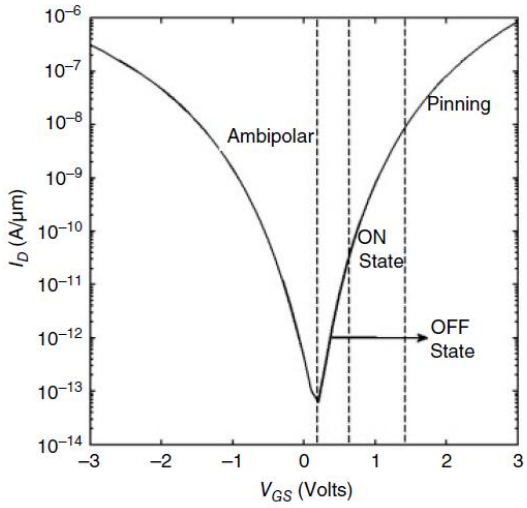


Fig. 2.7 Transfer characteristics of n-TFET under different biasing conditions for $V_{DS}>0$

In order to study the effect of varying drain voltage, the gate voltage V_{GS} is fixed at a certain $V_{GS}>0$. While $V_{DS}<V_{GS}$, the channel potential remains pinned to the drain potential. Due to this, as V_{DS} increases, the drain as well as channel energy bands get lowered as compared to the source energy bands. This results in enhanced tunneling at the source-channel junction. Hence, increase in V_{DS} leads to increase in drain current for a given $V_{GS}>0$. When V_{DS} approaches the V_{GS}, the channel potential is no longer pinned to the drain potential. Hence, current saturates at this point. Fig. 2.8 depicts the band diagram to explain the effect of varying drain voltage for a fixed gate voltage. Fig. 2.9 shows the output characteristics of n-TFET.

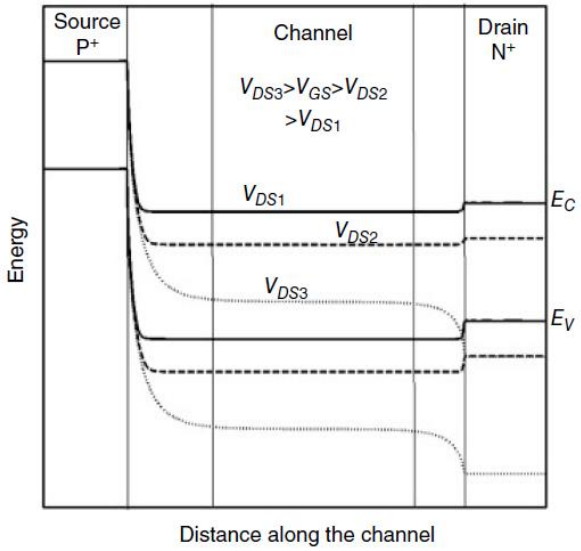


Fig. 2.8 Band diagram along the surface of n-TFET at different values of V_{DS} for a fixed positive V_{GS}

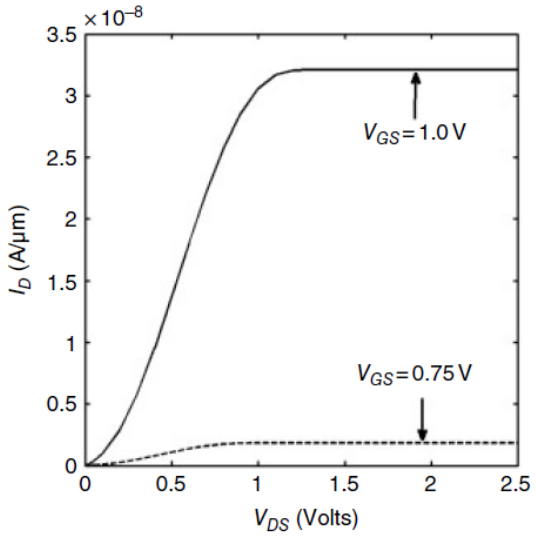


Fig. 2.9 I_D-V_{DS} plot of an n-TFET for different values of gate bias V_{GS}

2.3 Dependence of Performance on Device Parameters

2.3.1 Variation in Doping

The major difference between TFETs and MOSFETs is variation in source doping type. We know that n-channel TFETs have P+ doping at the source. Due to this P+ source doping and light/intrinsic doping at the channel, the depletion at the source-channel interface is a function of the doping concentration of the source. So, if we consider two doping concentrations, N_{A1} and N_{A2}, where $N_{A1}>N_{A2}$, then the depletion region at the source-channel junction will be shorter for the case of N_{A1} than N_{A2}. Hence, the tunneling distance L_{t1} is less than L_{t2} as shown in Fig. 2.10. Thereby, tunneling probability is greater when the source doping is increased. By a similar argument it can be said that the drain doping should be low in order to suppress ambipolar conduction as shown in Fig. 2.11.

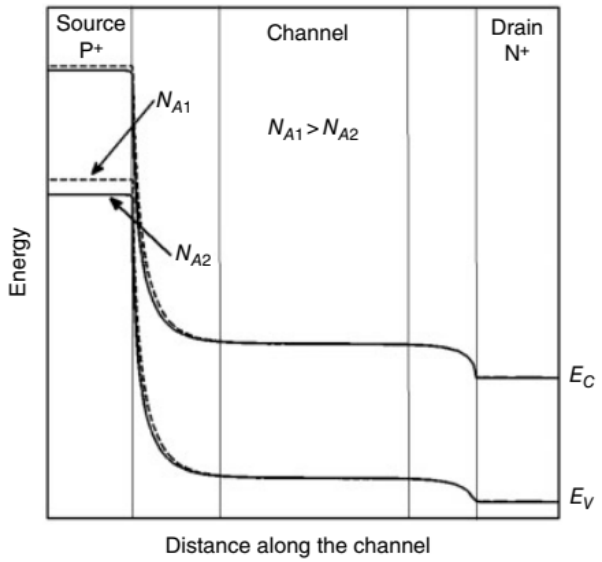


Fig. 2.10 Band diagram at the surface of n-TFET with different source doping concentrations

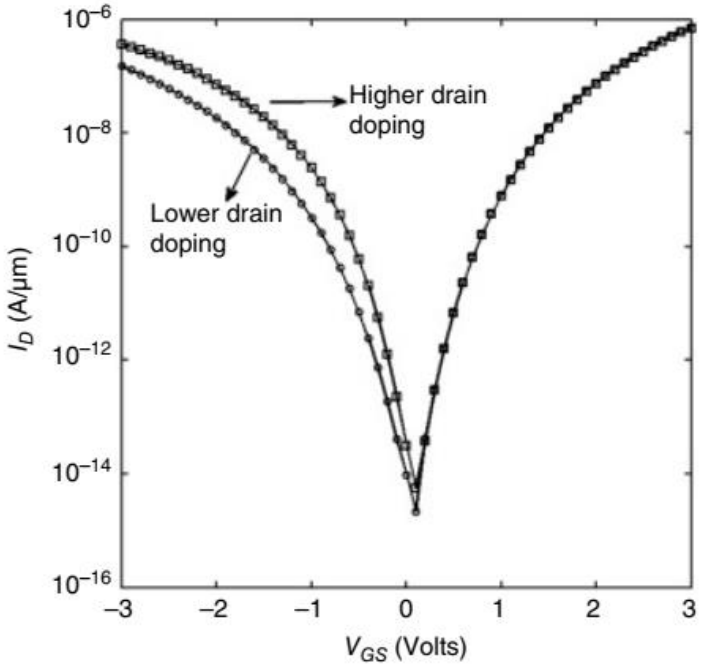


Fig. 2.11 Transfer characteristics of an n-TFET with different drain doping concentrations at a fixed drain voltage (V_{DS})

2.3.2 Variation in Gate Work Function

The band structures for the two TFETs with different gate work functions are shown in Fig. 2.12, where the higher gate work function is ϕ_{G1} and the lower gate work function is ϕ_{G2}. In the latter case, the inversion charge layer is enhanced leading to lowering of energy bands. As a result of this, the source-channel tunneling increases and hence, higher I_{ON} is observed.

2.3.3 Variation in Gate oxide material

The gate oxide enables proper control of the electrostatics in the channel. It is known that gate oxide capacitance is $C_{ox}=\varepsilon_{ox}/t_{ox}$. Here, ε_{ox} is the permittivity of the oxide material and t_{ox} is the oxide thickness. Using a high k dielectric near the source region, increases the C_{ox}. This in turn

improves the gate control over the channel electrostatics and induces a stronger electric field at the source-channel inteface. This culminates in enhanced band bending and increased $I_{ON.}$

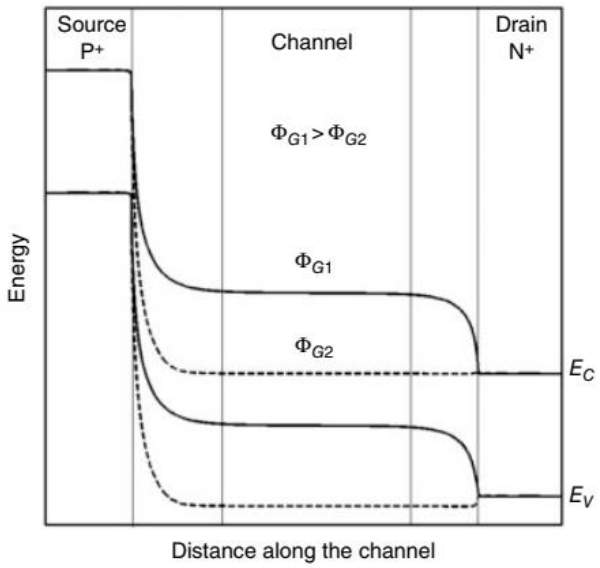


Fig. 2.12. Band diagram at the surface of n-TFET with different gate metal work function values

2.4 Band-to-Band Tunnelling (BTBT) Mechanism

It has been established that the underlying working principle in TFETs is band-to-band tunneling. Developed by Wentzel, Kramers and Brillouin, the WKB approximation is widely used for determining tunnelling probability. The tunneling barrier is assumed to be a triangular potential barrier [4]. Employing the WKB approximation, it is deduced that the Band-to-Band tunneling current is proportional to the tunnelling probability and is given by:

$$I_{BTBT} \propto T_t \approx \exp\left(-\frac{4\lambda\sqrt{2m^*}E_g^{3/2}}{3\hbar\left(\Delta\phi + E_g\right)}\right) \tag{2.1}$$

where, λ is the tunneling width, Eg is the energy band gap, m* is the effective mass of carrier and Δϕ is the range of energy over which tunneling occurs. λ and Δϕ have been shown in Fig. 2.13.

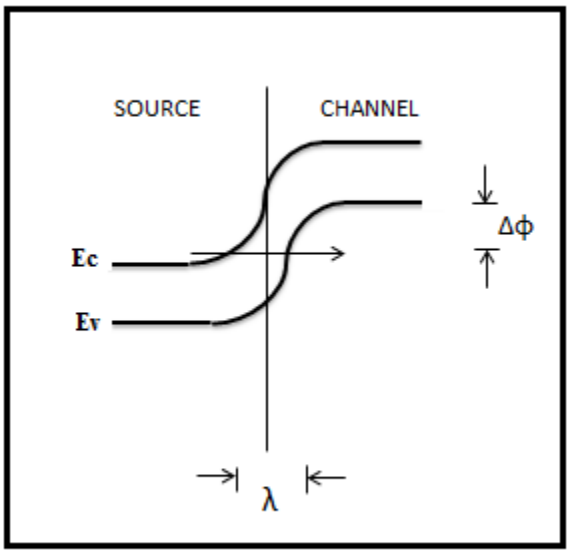


Fig. 2.13. Energy band cross section of a TFET representing Δϕ and λ. Redrawn from [5]

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CHAPTER 3

GATE ENGINEERED TFET: DOUBLE METAL DUAL GATE TFET WITH L-SHAPED DIELECTRIC

3.1 Overview and Proposed Structure

3.2 Device Structure and Simulation Setup

3.3 Results and Discussion

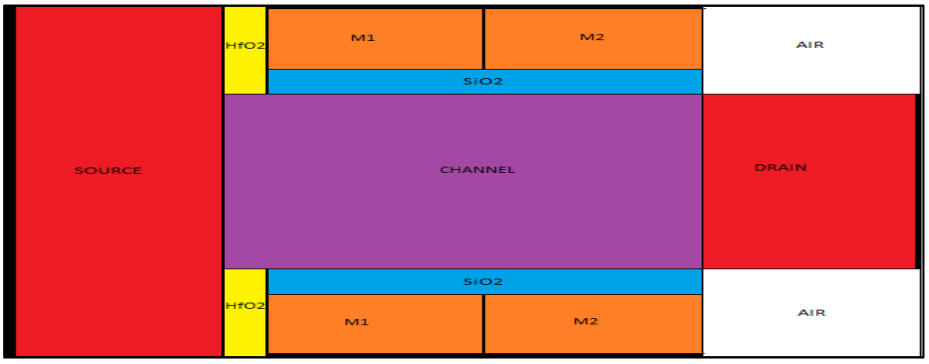
3.1 Overview and Proposed Structure

This work proposes a gate engineered [1-6] L-shaped dielectric double metal dual gate [7-9] TFET to suppress ambipolar conduction thereby rendering it suitable for circuit applications [10-14]. The gate engineering is obtained by using different materials along the L-shaped dielectric region in the double metal dual gate structure. As explained in section 2.3.2, the inclusion of a high k dielectric near the source enhances the gate control over the channel and increases the electric field at the source-channel interface. This in turn causes higher band bending which results in increased band-to-band tunnelling. Three structural variations have been proposed and simulated for the purpose of optimization. The structures have been named according to the corresponding dielectric materials used in the gate-oxide regions respectively, (a) L-shaped HfO_2-SiO_2 Double Metal Dual Gate TFET (LS-HS-DM-DG TFET: vertical portion has HfO_2 and horizontal portion has SiO_2), (b) L-shaped SiO_2-HfO_2 Double Metal Dual Gate TFET (LS-SH-

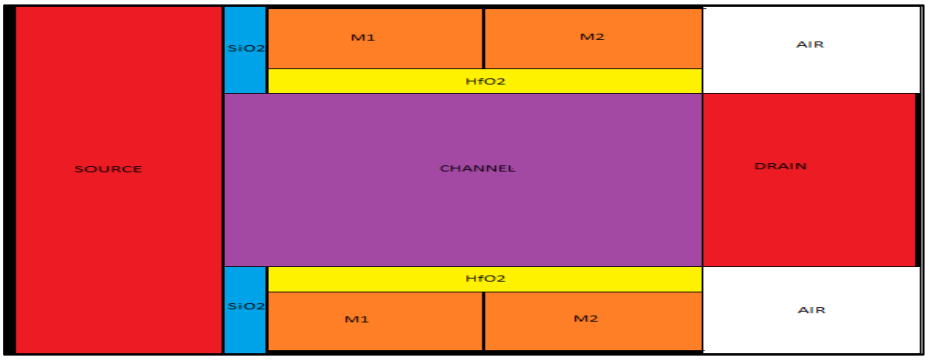
DM-DG TFET: vertical portion has SiO_2 and horizontal portion has HfO_2), (c) L-shaped SiO_2-SiO_2 Double Metal Dual Gate TFET (LS-SS-DM-DG TFET: total L-shape comprised of SiO_2). The electric field profile for the proposed structure has been studied to show reverse band bending in the drain-channel interface. This has the effect of greatly reducing the tunneling probability at the drain end of the structure, such that ambipolar conduction may be effectively suppressed. The OFF current is in the range of 10^{-18}A, thereby offering high I_{ON}/I_{OFF} and hence reduced subthreshold slope. The effects of varying the gate bias and oxide permittivities on the band diagram and other parameters such as the electric field and potential profile, have been analyzed and the ramifications of the structural variations and materials used for optimal evaluation have been reported.

3.2 Device Structure and Simulation Setup

The 2D cross-sectional view of the proposed n-channel TFET structure is shown in Fig. 3.1.(a) L-shaped HfO_2-SiO_2 Double Metal Dual Gate TFET (LS-HS-DM-DG TFET), (b) L-shaped SiO_2-HfO_2 Double Metal Dual Gate TFET (LS-SH-DM-DG TFET), (c) L-shaped SiO_2-SiO_2 Double Metal Dual Gate TFET (LS-SS-DM-DG TFET). The total length of the device is 34 nm while the channel length is 14 nm. The device has L-shaped oxide region in both upper and lower side. By varying the components of the oxide layers, three different structures are constructed. For LS-SS-DM-DG TFET the total oxide layer is of SiO_2, while the other two structures contain combination of SiO_2 and HfO_2. The Source region is extended with vertical dimension of 25 nm with 10 nm horizontal length. The drain regions in all the three devices are of heavily doped N+ type with doping concentration of 10^{18} cm^{-3} with vertical length of 15 nm and horizontal extent of 10 nm. The doping concentration of the source is 10^{20} cm^{-3} (p type) and that of the channel region is 10^{12} cm^{-3} (p-type). For symmetry, air is considered as the dielectric above and below the drain region. Thickness of the oxide region t_{ox} above and below the channel is 2 nm whereas the vertical section of the oxide has thickness of 3 nm. The double metal comprises of metals M1 and M2 with work functions 5.1 eV and 4.1 eV, respectively.



(a)



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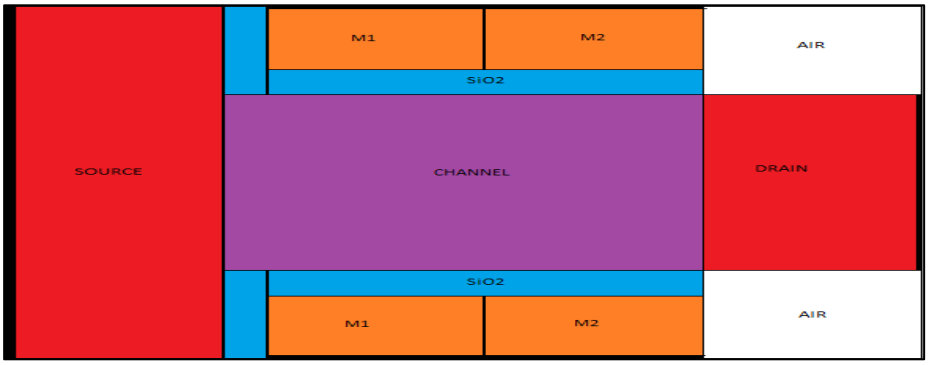

(c)

Fig. 3.1. 2D Cross-sectional Model for (a) L-shaped HfO_2-SiO_2 Double Metal Dual Gate TFET (LS-HS-DM-DG TFET), (b) L-shaped SiO_2-HfO_2 Double Metal Dual Gate TFET (LS-SH-DM-DG TFET), (c) L-shaped SiO_2-SiO_2 Double Metal Dual Gate TFET (LS-SS-DM-DG TFET).

All the simulations have been performed using Silvaco Atlas version 5.20.2.R by including appropriate models such as nonlocal BTBT (BBT.NONLOCAL), Auger recombination model, Lombardi mobility model (CVT), the Shockley–Read–Hall, Fermi–Dirac statistics, bandgap narrowing model, and Drift-diffusion carrier transport have been used. The band structures have been demonstrated under various biasing conditions.

3.3 Results and Discussion

3.3.1 Band Diagram Analysis

Fig. 3.2. compares the ON-state band diagram of the (a) L-shaped HfO_2-SiO_2 Double Metal Dual Gate TFET (LS-HS-DM-DG TFET), (b) L-shaped SiO_2-HfO_2 Double Metal Dual Gate TFET (LS-SH-DM-DG TFET), (c) L-shaped SiO_2-SiO_2 Double Metal Dual Gate TFET (LS-SS-DM-DG TFET). The band structures suggest better tunneling profile, reduced leakage and lower ambipolar conduction in comparison to conventional planar TFETs.

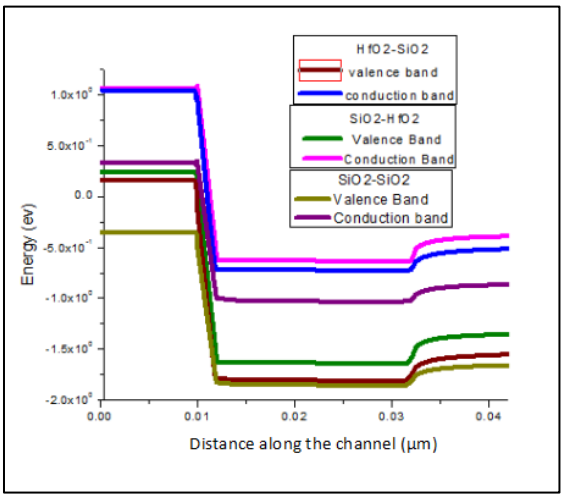

Fig. 3.2. ON-state band diagram of (a) L-shaped HfO_2-SiO_2 Double Metal Dual Gate TFET (LS-HS-DM-DG TFET), (b) L-shaped SiO_2-HfO_2 Double Metal Dual Gate TFET (LS-SH-DM-DG TFET), (c) L-shaped SiO_2-SiO_2 Double Metal Dual Gate TFET (LS-SS-DM-DG TFET).

The tunneling length, which is inversely related to the tunneling probability, is lower for LS-HS-DM-DG TFET and LS-SH-DM-DG TFET as compared to LS-SS-DM-DG TFET. This indicates better tunneling in the former two structures. Reverse band bending as observed from the energy band diagrams is indicative of reduced ambipolar conduction. There is stronger reverse band bending at the channel-drain interface of LS-HS-DM-DG TFET and LS-SH-DM-DG TFET as compared to LS-SS-DM-DG TFET. So, it can be concluded that LS-HS-DM-DG TFET and LS-SH-DM-DG TFET structures are more immune to ambipolar conduction as compared to the LS-SS-DM-DG TFET structure. The energy band diagram can be further optimized by modulation in dimensions of the structure and variation in the doping profile.

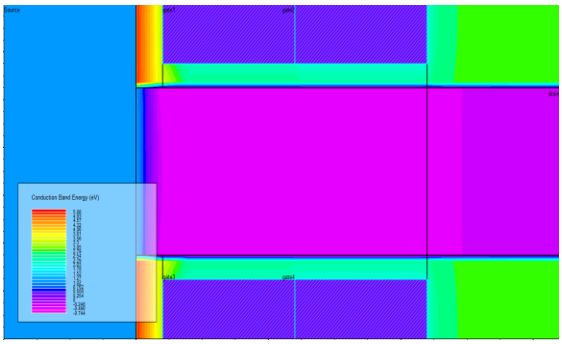

Fig. 3.3. Conduction Band Energy profile for LS-HS-DM-DG TFET

The Fig. 3.3. shows conduction band energy for the LS-HS-DM-DG TFET structure. The conduction band energy profile of the other two structures are almost similar to the one in Fig. 3.3. As expected the conduction band energy is highest at the source end, reduces at the source-channel interface and is lowest at the drain end.

3.3.2 Potential Profile and Electric Field Profile Analysis

A comparative analysis of the potential profile is presented in Fig. 3.4. for the three structures. The peak in the potential profile at the source-channel interface is indicative of the overall tunneling. It can be seen from the figure that overall tunneling is better for LS-HS-DM-DG TFET as compared to LS-SH-DM-DG TFET and LS-SS-DM-DG TFET. The potential profile of the latter two structures are almost overlapped. Higher value of potential at the channel-drain

interface indicates that the electrons which tunnel at the source-channel interface effectively reach the drain.

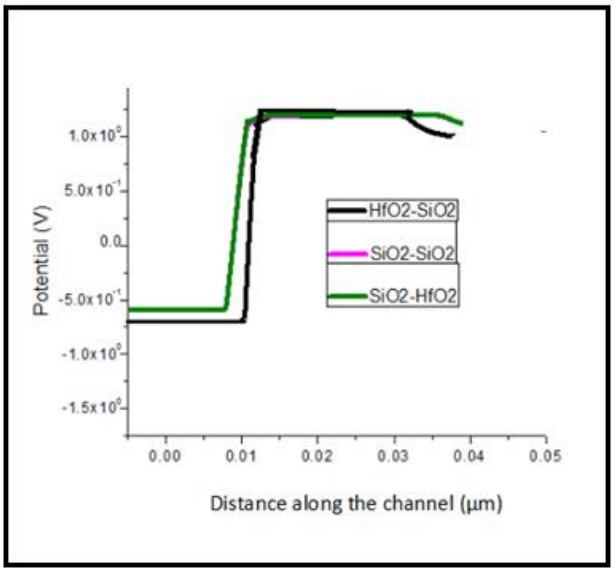

Fig. 3.4. Potential Profile of (a) L-shaped HfO_2-SiO_2 Double Metal Dual Gate TFET (LS-HS-DM-DG TFET), (b) L-shaped SiO_2-HfO_2 Double Metal Dual Gate TFET (LS-SH-DM-DG TFET), (c) L-shaped SiO_2-SiO_2 Double Metal Dual Gate TFET (LS-SS-DM-DG TFET).

The electric field for all the three structures has been shown in Fig. 3.5. Maximum overshoot at the source-channel interface is seen for LS-HS-DM-DG TFET suggesting highest degree of tunneling in this structure. The peak in the electric field profile at the channel-drain interface acts as barrier to reverse tunneling. This peak indicates immunity to DIBL. The peak of the electric field profile at the channel-drain interface is lower than that in the source-channel interface implying reduced hot carrier effect at the drain end. The contour diagrams of the Potential profile and the Electric Field profile for the LS-HS-DM-DG TFET structure have been shown in Fig. 3.6. and Fig. 3.7, respectively.

The band-to-band tunneling profile is shown for all the three structures in Fig. 3.8. The sharpest reverse peak at the source-channel interface for the LS-HS-DM-DG TFET structure is indicative of superior band-to-band tunneling for this structure. This is attributed to the presence of the

high-k dielectric at the source end. The presence of HfO_2 near the source ensures a sharp electric field overshoot at the source-channel interface, thereby enhancing band-bending. The reduction of tunneling width is a direct consequence of band-bending and leads to a sharp increase in the band-to-band tunneling rate. This is also reflected in the transfer characteristics of the structures. LS-HS-DM-DG TFET shows most favorable outcomes in terms of Potential profile and Electric field Profile.

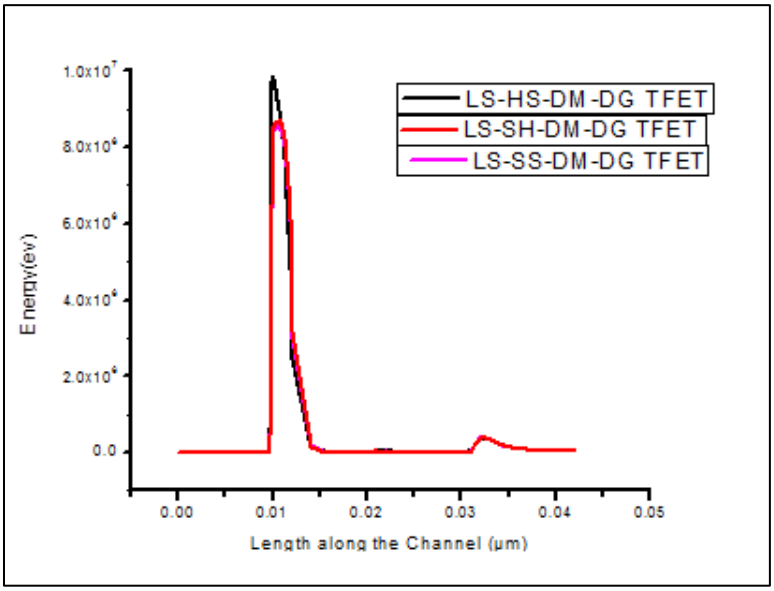

Fig. 3.5. Electric Field Profile of (a) L-shaped HfO_2-SiO_2 Double Metal Dual Gate TFET (LS-HS-DM-DG TFET), (b) L-shaped SiO_2-HfO_2 Double Metal Dual Gate TFET (LS-SH-DM-DG TFET), (c) L-shaped SiO_2-SiO_2 Double Metal Dual Gate TFET (LS-SS-DM-DG TFET).

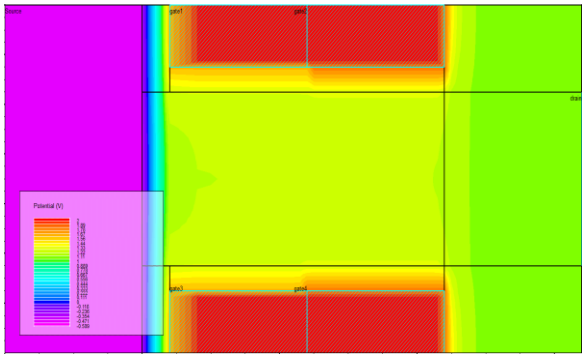

Fig. 3.6. Potential Profile of LS-HS-DM-DG TFET.

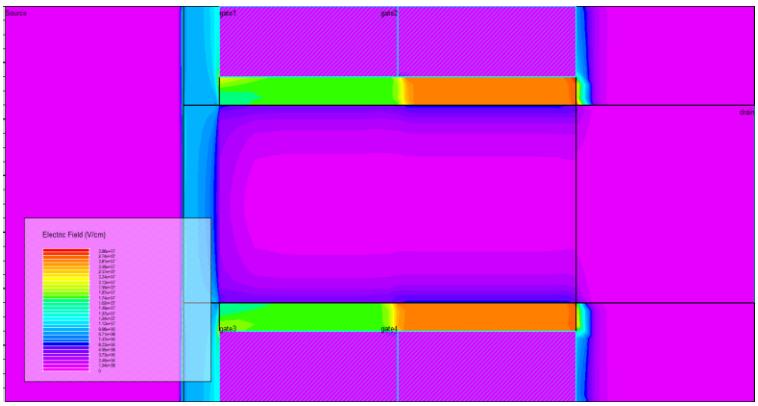

Fig. 3.7. Electric Field Profile of LS-HS-DM-DG TFET

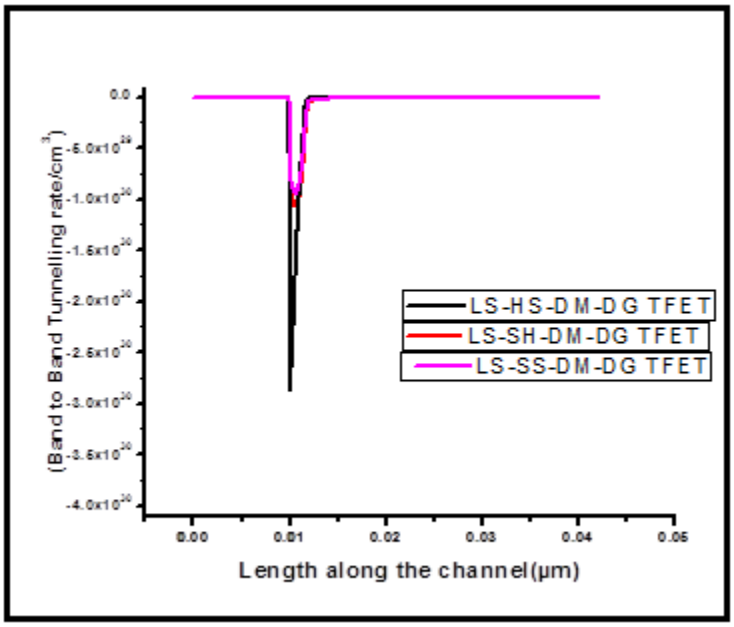

Fig. 3.8. Band-to-Band tunneling Profile of (a) L-shaped HfO_2-SiO_2 Double Metal Dual Gate TFET (LS-HS-DM-DG TFET), (b) L-shaped SiO_2-HfO_2 Double Metal Dual Gate TFET (LS-SH-DM-DG TFET), (c) L-shaped SiO_2-SiO_2 Double Metal Dual Gate TFET (LS-SS-DM-DG TFET).

3.3.3 Transfer Characteristics

The transfer characteristics for all the three structures of L-shaped dielectric Double Metal Dual Gate TFET is shown for in Fig. 3.9. Highest I_{ON}/I_{OFF} ratio is observed for LS-HS-DM-DG TFET and is approximately 10^{12}, while it is lowest for LS-SS-DM-DG TFET (10^{7}). The subthreshold slope is 24mV/dec for LS-HS-DM-DG TFET, 34mV/dec for LS-SH-DM-DG TFET and 60mV/dec for LS-SS-DM-DG TFET. Also, suppressed ambipolar conduction is clearly observed from the transfer characteristics of LS-HS-DM-DG TFET. This is attributed to the presence of low-k dielectric at the channel drain interface. The electric field at this end is lower for LS-HS-DM-DG TFET as compared to the other two structures. This minimizes the possibility of tunneling at the channel drain interface for negative values of V_{GS}.

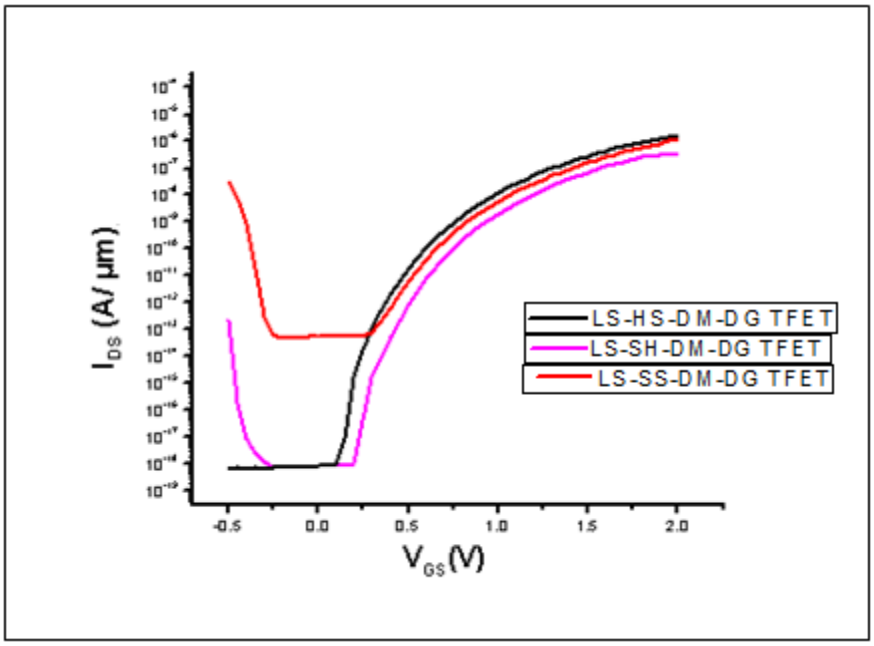

Fig. 3.9. Transfer Characteristics of (a) L-shaped HfO_2-SiO_2 Double Metal Dual Gate TFET (LS-HS-DM-DG TFET), (b) L-shaped SiO_2-HfO_2 Double Metal Dual Gate TFET (LS-SH-DM-DG TFET), (c) L-shaped SiO_2-SiO_2 Double Metal Dual Gate TFET (LS-SS-DM-DG TFET).

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CHAPTER 4

DOUBLE TRENCH GATE COVERED SOURCE-CHANNEL TFET (DTG-CSC-TFET)

4.1 Overview of the Proposed Structure

4.2 Device Structure and Fabrication

4.3 Analytical Modeling

4.4 Results and Discussion

4.1 Overview of the Proposed Structure

In this work, a novel Double Trench Gate Covered Source-Channel TFET [DTG-CSC-TFET] has been proposed. An analytical current model has been presented to obtain the expression for the ON-current in the DTG-CSC-TFET.The parameters have been optimized and the analytical model has been validated through Silvaco, Atlas simulations. The Double Trench-Gate with Covered Source-Channel allows for remarkable increase in tunneling area which is reflected in sharply enhanced band-to-band tunneling rates. Hence, this device has greatly increased I_{ON} as compared to conventional planar TFETs. The proposed structure is depicted in Fig. 4.1. The source is extended well into the channel in order to maximize the region of channel that lies between the source and the gate. The trench gate height is denoted by L_T, the source extension length is denoted by L_S, the thickness of the channel between the source and gate is represented by t_{Si} and the oxide thickness is t_{OX}. The oxide material near the source is HfO_2, which is a high-k dielectric and that near the drain is SiO_2, which is a low-k dielectric. Such a configuration

enhances BTBT at the source-channel junction and reduces BTBT at the channel-drain junction, thereby suppressing the possibility of ambipolar conduction. The low doped drain (LDD) region at the drain end also aids ambipolar current suppression.

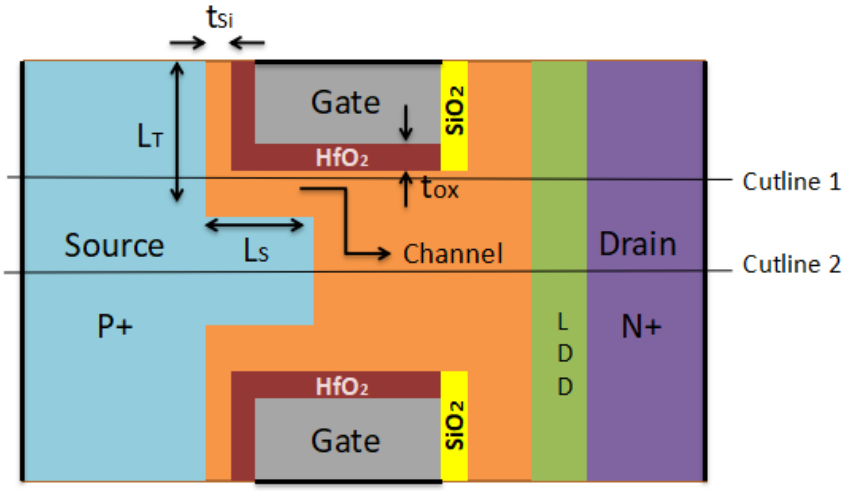


Fig. 4.1. Schematic of the proposed DTG-CSC-TFET

Conventional Tunnel Field Effect Transistors (TFETs) that are fabricated on Si-substrates exhibit relatively lower I_{ON} as compared to their Metal Oxide Semiconductor Field Effect Transistor (MOSFET) counterparts. This is due to limited band-to-band tunneling (BTBT) in such TFETs. In order to overcome the low I_{ON} several structural and/or material variations have been studied extensively and exhaustively [1-11]. TFETs based on Si-channel have better process compatibility than those with III-V compound based channels and heterojunctions. Materials such as germanium (Ge) and III-V compounds are neither compatible with established conventional CMOS processes nor are they applicable to SOC designs that are presently based on silicon transistors [10]. In lieu of this, structural variations are plausible for addressing critical issues such as poor subthreshold slope and low I_{ON}. In order to ensure practical feasibility and viability, the proposed structure is an Si-based TFET. Owing to the practical limitations on material variations, newer TFET models are being proposed by incorporating a variety of innovative structural modifications. Most recently line-tunneling type Z/ U/ L-shaped TFETs [12-14] have been considered to achieve better subthreshold swing and higher ON-current. Essentially, these structures comprise of a source/channel/gate overlap region whereby the band-

to-band tunneling is aligned parallel with the gate electric field. Such modifications achieve higher ON-currents as - (1) BTBT paths are short and 1D (2) the tunneling area is maximized. This is the motivation behind the proposed structure.

The advantage of our proposed structure is that it enhances the I_{ON} not only due to the double gate structure but also due to the two band-to-band tunneling mechanisms that inherently occurs in the structure. The tunneling mechanism at the lateral part of the extended source region is point tunneling. Hence, tunneling takes place at the source-channel interface in the direction along the channel and parallel to channel-gate oxide interface, under the influence of the gate. A second type of tunneling occurs in the part of the channel which lies between the source and the gate. BTBT occurs under the influence of the high vertical electric field in the narrow channel region, in the direction perpendicular to channel-gate oxide interface. The carriers so generated, are swept towards the drain end under the lateral electric field generated by the drain bias. This type of tunneling is known as line tunneling. From Fig. 4.1. it may be assumed that $2(L_T+L_S)$ is the total length along which line tunneling occurs. This length hence plays a crucial role in determining the amount of BTBT that takes place in the structure. Also, Fig. 4.1. shows two cutlines which will be needed later for the analysis of the device parameters.

4.2 Device Structure and Fabrication

4.2.1 Device Structure

The device dimensions and doping concentrations are highlighted in this section. The source is heavily doped P+ (10^{20} cm^{-3}), the channel is lightly doped n-type (10^{12} cm^{-3}), the LDD region is doped N (10^{17} cm^{-3}) and the drain region has N+ doping (10^{19} cm^{-3}). The oxide thickness is t_{OX}=2nm. The total lateral extent of the device is 74nm while the vertical extent is 60nm. The length of the source excluding the extended-source region is 20nm. The extended-source region length is denoted by L_S, as previously mentioned. The t_{Si} as denoted in Fig. 4.1. is 5nm. This value is optimum for studying quantum confinement effect which will be presented in section 4.4. The vertical extent of the extended-source region is 20nm. The LDD and drain regions have lateral dimensions of 5nm and 15nm, respectively. It is evident that the structure is symmetrical about cutline 2. The width between the extended source and the gate is 8nm. The lateral extent of

the gate is 20nm. The work function of the gate metal has been fixed at 4.85eV for the purpose of simulation. Device optimization has been achieved by varying the value of L_S (10nm, 15nm, 20nm) as will be shown in section 4.3. The doping profile for the three structural variations have been shown in Fig. 4.2.

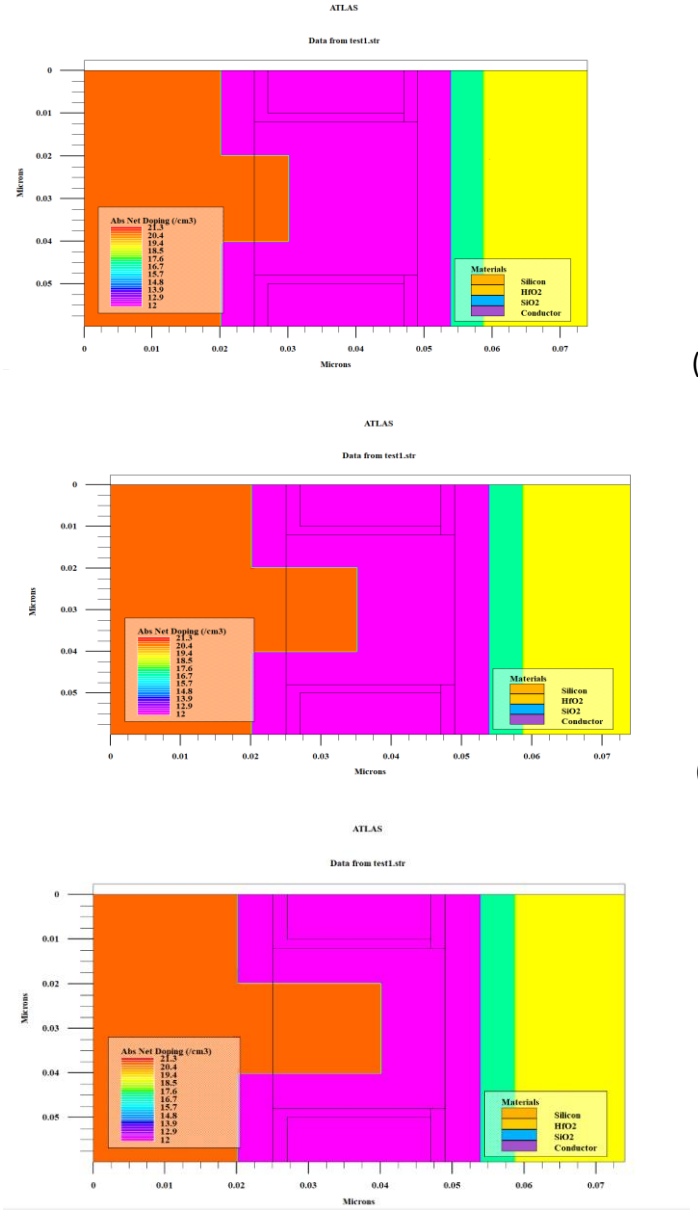


Fig 4.2. Absolute net doping profile of DTG-CSC-TFET for (a) L_S=10nm, (b) L_S=15nm, (c) L_S=20nm

4.2.2 Fabrication Steps

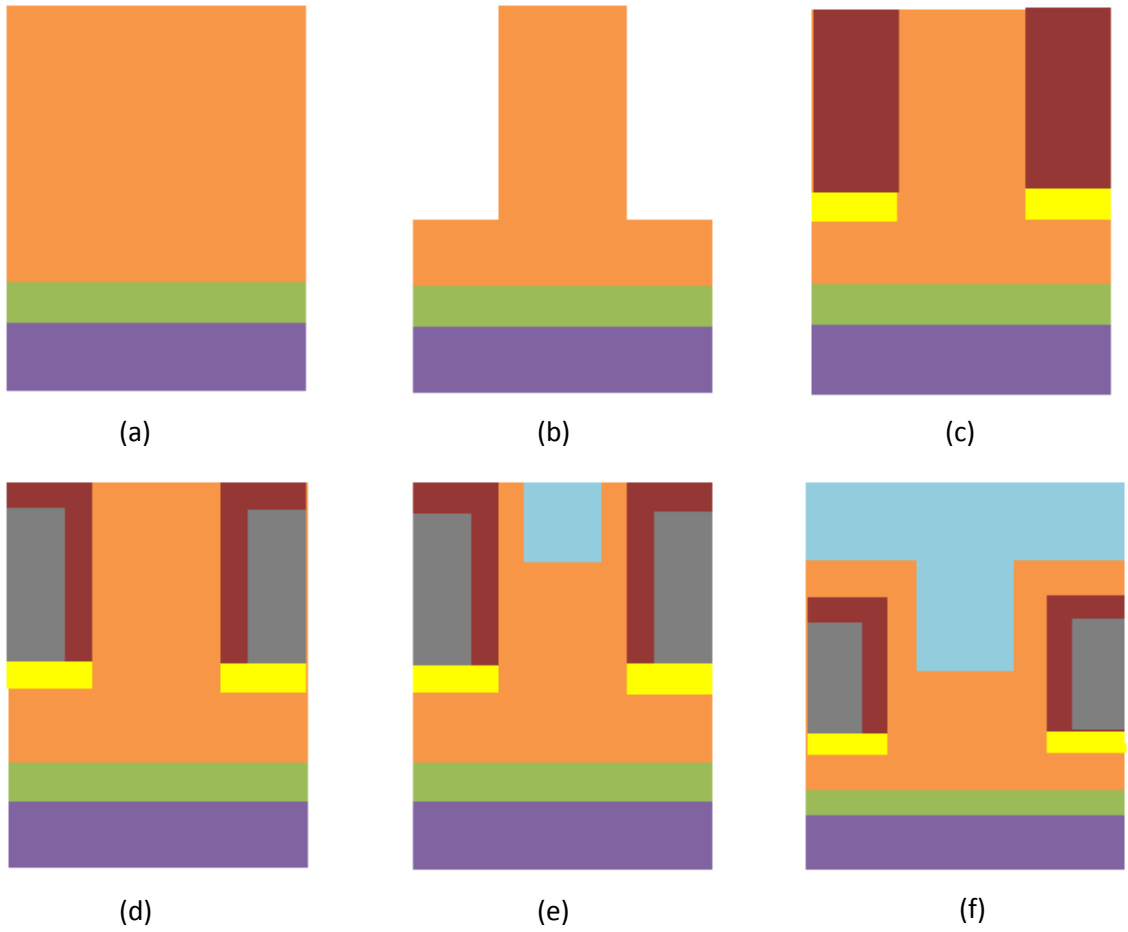


Fig 4.3 (a)-(f) Steps for the fabrication of the proposed DTG-CSC-TFET

Fig. 4.3. summarizes the fabrication steps for the DTG-CSC-TFET. The N+ drain, LDD and n-substrate are grown epitaxially. Selective lateral etching is used to create pockets for developing the gate region of the double gate structure as shown in Fig. 4.3(b). This is followed by the lateral oxidation process. Firstly, SiO_2 layer is deposited by thermal oxidation. This is followed by the deposition of HfO_2 by the atomic layer deposition (ALD) process, as shown in Fig. 4.3(c). Dry plasma removal of HfO_2 is performed to create pockets for depositing the gate metal. This is followed by metallization to obtain the gate. A diffusion step is crucial to create the extended source region where the depth of diffusion can be controlled, as shown in Fig. 4.3(e). Subsequent

expitaxial growth steps are instrumental to the development of the covered source-channel region and the P+ source region, as shown in Fig 4.3(f).

4.3 Analytical Modeling

In order to determine the total current, the contributions of the line tunneling and the point tunneling phenomena are calculated separately and the resultant currents are added. In practice, one tunneling mechanism may dominate the other depending on the oxide thickness, source doping concentration, and biasing conditions [15].The carrier generation rate is calculated using Kane's Model as:

$$G = A\frac{\varepsilon^{D}}{\sqrt{E_G}}\exp\left(-BE_G^{\,3/2}/\varepsilon\right)$$

or,

$$G = A\frac{E_G^{\,D-1/2}}{q^{D}w_{tun}^{\;D}}\exp\left(-Bq\sqrt{E_G}w_{tun}\right) \qquad (4.1)$$

where Ɛ is the average electric field and is given as:

$$\varepsilon = \frac{E_G}{qw_{tun}} \qquad (4.2)$$

In the above equations, G is the generation rate which is expressed as the no. of carriers generated per unit volume per unit time, q is the charge, w_{tun} is the tunneling width, E_G is the energy bandgap and A, B & D are the Kane's model parameters whose values are material dependent. The default value of D is 2. Kane's model is applicable for the dimensions considered in the proposed DTG-CSC-TFET in accordance with [16].

The total current in the TFET may be determined by integrating the generation rate over the volume as:

$$|I| = q\int GdV \tag{4.3}$$

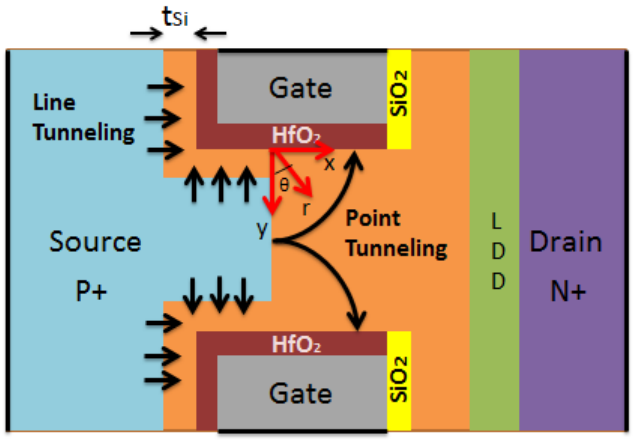


Fig. 4.4. Pathway of Point Tunneling and Line Tunneling

Point Tunneling

The concept of point tunneling has been discussed qualitatively in section 4.1. Fig.4.4. depicts the pathway of point tunneling. Here, the co-ordinates are so chosen that x=0 represents the source channel interface and y=0 is indicative of the gate & gate dielectric interface. In order to simplify the calculations the following assumptions have been made: (1) Potential drop due to depletion in the source is zero and the potential at x=0 is equivalent to the source potential. (2) Effect of charge in the channel on the channel potential is neglected. (3) Any charge that may be present in the gate dielectric is neglected. (4) Gate dielectrics with same electrical thickness will result in similar potential profile in the channel region. Towards assumption (4), the semiconductor equivalent thickness of the gate oxide is calculated as:

$$t_{ox}^{'} = t_{ox}\frac{\varepsilon_{Si}}{\varepsilon_{ox}} \tag{4.4}$$

where, ε_{Si} and ε_{ox} are the silicon and gate dielectric constants and t_{ox} is the physical dielectric thickness. The potential in the gate dielectric as well as the channel follow Poisson's Eq. as:

$$\nabla^2\psi = -\frac{\rho}{\varepsilon} \tag{4.5}$$

where Ψ represents semiconductor valence band edge potential and ρ is the charge density. As per the assumptions, ρ = 0 in the gate dielectric and channel. Hence, Eq. 4.5 reduces to Laplace Eq. Furthermore, the electrostatic potential obeys the following boundary conditions: $\Psi(0,y) = \Psi_S$ and $\Psi(x,0) = \Psi_G$. Assume that $\Psi_S = 0$ and $\Psi_G = V_{GS}-V_{FB}$, where V_{GS} is the applied gate bias and V_{FB} is the flatband voltage. Let the semiconductor extend towards infinity for (x>0 & y>0). Using the polar co-ordinates for the curved electric field lines, we represent potential as:

$$\psi(x,y) = \psi_G \frac{2}{\pi}\theta \ ; \text{for } 0 \le \theta \le \pi/2 \tag{4.6}$$

Here, $x = r\sin\theta$ and $y = r\cos\theta$. For 2D potential, the tunneling path length is expressed as the length of an arc along an electric field line:

$$w_{tun} = r\theta_0 \tag{4.7}$$

where,

$$\theta_0 = \frac{\pi E_G}{2q\psi_G} \tag{4.8}$$

θ_0 is the angle between two equipotential lines whose potential difference is E_G/q. To get the total point tunneling current we must integrate the generated charge over the entire tunneling area:

$$I = qW\int_{r_0}^{\infty}\int_{\theta_0}^{\arccos(t_{ox}^{'}/r)} \mathrm{G(r).rd}\theta\mathrm{dr}$$

$$I = qW\int_{r_0}^{\infty}\int_{\theta_0}^{\arccos(t_{ox}^{'}/r)} A\frac{E_G^{\,D-1/2}}{q^D w_{tun}^{\,D}}\exp(-Bq\sqrt{E_G}w_{tun})r\mathrm{d}\theta dr$$

$$\Rightarrow WA\int_{r_0}^{\infty}\int_{\theta_0}^{\arccos(t_{ox}^{'}/r)} \frac{E_G^{\,D-1/2}}{q^{D-1}(r\theta_0)^D}\exp(-Bq\sqrt{E_G}r\theta_0)r\mathrm{d}\theta dr$$

$$\Rightarrow WA\int_{r_0}^{\infty}\int_{\theta_0}^{\arccos(t_{ox}^{'}/r)} \frac{E_G^{\,D-1/2}}{q^{D-1}(r\theta_0)^D}\exp(-Bq\sqrt{E_G}r\theta_0)r\mathrm{d}\theta dr$$

$$\Rightarrow WA\int_{r_0}^{\infty}\int_{\theta_0}^{\arccos(t_{ox}^{'}/r)} \frac{E_G^{\,D-1/2}}{q^{D-1}r^{D-1}\theta_0^{\,D}}\exp(-Bq\sqrt{E_G}r\theta_0)dr\mathrm{d}\theta$$

$$\therefore I = WA\int_{r_0}^{\infty}\int_{\theta_0}^{\arccos(t_{ox}^{'}/r)} \left(\arccos\left(t_{ox}^{'}/r\right)-\theta_0\right)\frac{E_G^{\,D-1/2}}{q^{D-1}r^{D-1}\theta_0^{\,D}}\exp(-Bq\sqrt{E_G}r\theta_0)dr \qquad (4.9)$$

where,

$$\theta_0 = \arccos\left(t_{ox}^{'}/r_0\right)$$

To solve Eq. 4.9 we perform first order Taylor expansion about r = r_0 :

$$f(r_0) = \left(\arccos(t_{ox}^{'}/r_0)-\theta_0\right)\frac{E_G^{\,D-1/2}e^{-Bq\sqrt{E_G}r_0\theta_0}}{q^{D-1}r_0^{D-1}\theta^D} \qquad (4.10)$$

B

$$f'(r_0) = \frac{d}{dr_0}\underbrace{\left[\arccos(t'_{ox}/r_0)\frac{E_G{}^{D-1/2}e^{-Bq\sqrt{E_G}r_0\theta_0}}{q^{D-1}r_0^{D-1}\theta_0{}^{D}}\right.}_{A} - \left.\theta_0\frac{E_G{}^{D-1/2}e^{-Bq\sqrt{E_G}r_0\theta_0}}{q^{D-1}r_0^{D-1}\theta_0{}^{D}}\right] \tag{4.11}$$

A

$$\frac{dA}{dr_0} = \frac{E_G{}^{D-1/2}e^{-Bq\sqrt{E_G}\theta_0}}{q^{D-1}\theta_0{}^{D}}\frac{d}{dr_0}\left[\frac{\arccos(t'_{ox}/r_0)e^{r_0}}{r_0^{D-1}}\right]$$

$$= \frac{E_G{}^{D-1/2}e^{-Bq\sqrt{E_G}\theta_0}}{q^{D-1}\theta_0{}^{D}r_0^{2(D-1)}}\left[r_0^{D-1}\frac{d}{dr_0}\left\{\arccos(t'_{ox}/r_0)e^{r_0}\right\} - \arccos(t'_{ox}/r_0)e^{r_0}\frac{d}{dr_0}r_0^{D-1}\right]$$

$$= \frac{E_G{}^{D-1/2}e^{-Bq\sqrt{E_G}\theta_0}}{q^{D-1}\theta_0{}^{D}r_0^{2(D-1)}}\left[r_0^{D-1}\left\{\arccos(t'_{ox}/r_0)e^{r_0} - e^{r_0}\frac{1}{\sqrt{1-\left(\frac{t'_{ox}}{r}\right)^2}}\right\} - \arccos(t'_{ox}/r_0)e^{r_0}(D-1)r_0^{D-2}\right]$$

$$= \frac{E_G{}^{D-1/2}e^{-Bq\sqrt{E_G}r_0\theta_0}}{q^{D-1}\theta_0{}^{D}r_0^{D-1}}\left[\arccos(t'_{ox}/r_0) - \frac{1}{\sqrt{1-\left(\frac{t'_{ox}}{r}\right)^2}} - \frac{D-1}{r_0}\arccos(t'_{ox}/r_0)\right]$$

(4.12)

$$\frac{dB}{dr_0} = \frac{d}{dr_0}\left[-\theta_0 \frac{{E_G}^{D-1/2} e^{-Bq\sqrt{E_G} r_0 \theta_0}}{q^{D-1} r_0^{D-1} {\theta_0}^{D}} \right]$$

$$= -\theta_0 \frac{{E_G}^{D-1/2} e^{-Bq\sqrt{E_G}\theta_0}}{q^{D-1}{\theta_0}^{D}} \frac{d}{dr_0}\left[\frac{e^{r_0}}{r_0^{D-1}} \right]$$

$$= -\theta_0 \frac{{E_G}^{D-1/2} e^{-Bq\sqrt{E_G}\theta_0}}{q^{D-1}{\theta_0}^{D}} \left[1 - \frac{(D-1)}{r_0} \right]$$

$$= \frac{{E_G}^{D-1/2} e^{-Bq\sqrt{E_G} r_0 \theta_0}}{q^{D-1} {r_0}^{D-1} {\theta_0}^{D}} \cdot \frac{1}{\sqrt{1 - \left(\frac{t_{ox}^{'}}{r_0} \right)^2}}$$

(4.13)

Finally, putting the value of $f(r_0)$ and $f'(r_0)$ in the formula of Taylor expansion, and neglecting $\cos(\theta_0)$ w.r.t. unity we obtain:

$$f(r) = f(r_0) + f^{'}(r_0)(r - r_0)$$

$$I \approx \frac{WAE_G{}^{D-1/2}}{q^{D-1} {r_0}^{D-1} {\theta_0}^{D}} \int_{r_0}^{\infty} \frac{t_{ox}^{'}(r - r_0) e^{-Bq\sqrt{E_G} r \theta_0}}{{r_0}^2 \sqrt{1 - \left(\frac{t_{ox}^{'}}{r_0} \right)^2}} dr$$

$$\approx \frac{WAE_G{}^{D-3/2} t_{ox}^{'}}{q^{D-1} B^2} \cdot \frac{1}{{\theta_0}^{D+2} {r_0}^{D+1}} e^{-Bq\sqrt{E_G} r_0 \theta_0}$$

(4.14)

Approximating r_0 as a function of gate potential:

$$r_0 = t_{ox}^{'} / \cos\theta_0$$

$$\Rightarrow r_0 = \frac{t_{ox}^{'}}{\cos\left(\frac{\pi}{2}\frac{E_G}{q\psi_G}\right)}$$

$$\Rightarrow r_0 = \frac{t_{ox}^{'}}{\sin\left(\frac{\pi(q\psi_G - E_G)}{2q\psi_G}\right)}$$

$$\therefore r_0 \approx t_{ox}^{'}\frac{2q\psi_G}{\pi(q\psi_G - E_G)}$$

(4.15)

Hence, finally putting the value of θ_0 and the default values for Kane's model parameters we obtain an expression of current as:

$$I = WP\frac{q\psi_G}{E_G}\left(\frac{q\psi_G}{E_G} - 1\right)^3 e^{\frac{Q}{\left(\frac{q\psi_G}{E_G} - 1\right)}}$$

where,

$$P = \frac{2A\sqrt{E_G}}{\pi q^3 B^2 t_{ox}^{'}}$$

$$Q = -Bq\sqrt{E_G}t_{ox}^{'}$$

(4.16)

The total point tunneling current is twice the current in Eq. 4.16. as it is contributed both by the top gate and bottom gate of the DTG-CSC-TFET.

$$\therefore I_{point} = 2WP\frac{q\psi_G}{E_G}\left(\frac{q\psi_G}{E_G} - 1\right)^3 e^{\frac{Q}{\left(\frac{q\psi_G}{E_G} - 1\right)}} \quad (4.17)$$

Line Tunneling

It is assumed that line tunneling occurs along the entire region of the channel that lies between source and gate. For the region $2(L_T+L_S)$, where the electrostatic potential is predominantly controlled by the gate, the effect of drain bias may be neglected to simplify the calculations. To this effect, we consider a one-dimensional potential profile in the semiconductor while considering line tunneling:

$$\psi(y)=\frac{qN_A}{2\varepsilon_S}(y-y_{\max})^2$$
$$E(y)=-\frac{d\psi(y)}{dy}=-\frac{qN_A}{\varepsilon_S}(y-y_{\max}) \qquad (4.18)$$

where y_{max} is the length of the depletion region, which depends on the gate voltage, as shown in Fig. 4.5.

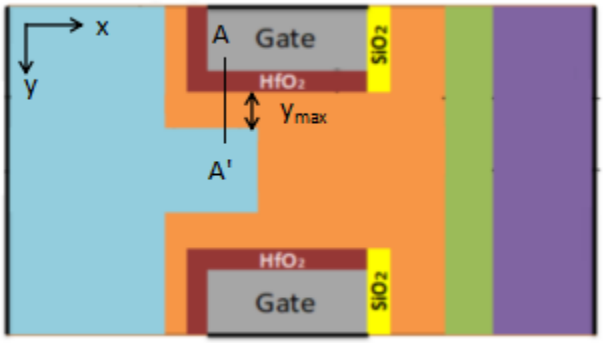


Fig.4.5. Cutline shown for quantifying Line tunneling, where y_{max} represents the depletion region when positive gate bias is applied for the proposed n-DTG-CSC-TFET

The tunneling width may be defined as the distance between the valence band and conduction band corresponding to equal energy level. The average electric field in y direction is:

$$E_{y,avg}=\frac{E_G}{qw_{tun}} \qquad (4.19)$$

In order to calculate w_{tun} the y coordinates of the same potential in the valence band and conduction band are taken into consideration (as shown in Fig. 4.6.):

$$\psi_v(y_1) = \frac{qN_A}{2\varepsilon_S}(y_1 - y_{\max})^2 + \frac{E_G}{q}$$
$$\psi_C(y_2) = \frac{qN_A}{2\varepsilon_S}(y_2 - y_{\max})^2 \qquad (4.20)$$

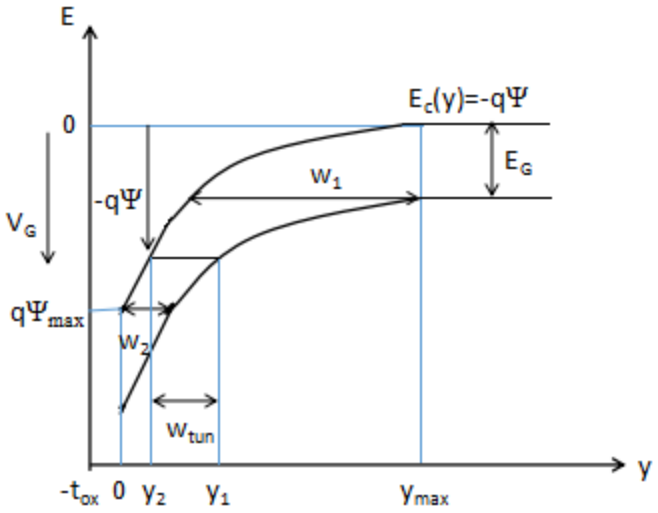


Fig. 4.6. Band Diagram along cutline AA' of Fig. 4.5. depicting w_{tun}.

It can be deduced that:

$$w_{tun} = y_1 - y_2$$
$$\psi_v(y_1) = \psi_c(y_2) \qquad (4.21)$$

Expressing y_2 as a function of w_{tun}:

$$\therefore y_1 = w_{tun} + y_2$$

$$\frac{qN_A}{2\varepsilon_S}(y_1 - y_{\max})^2 + \frac{E_G}{q} = \frac{qN_A}{2\varepsilon_S}(y_2 - y_{\max})^2$$

$$\Rightarrow (y_1 - y_{\max})^2 + \frac{2E_G\varepsilon_S}{q^2N_A} = (y_2 - y_{\max})^2$$

$$\Rightarrow (w_{tun} + y_2 - y_{\max})^2 + \frac{2E_G\varepsilon_S}{q^2N_A} = (y_2 - y_{\max})^2$$

$$\Rightarrow {w_{tun}}^2 + 2w_{tun}(y_2 - y_{\max}) + (y_2 - y_{\max})^2 + \frac{2E_G\varepsilon_S}{q^2N_A} = (y_2 - y_{\max})^2$$

$$\Rightarrow 2w_{tun}y_{\max} = 2w_{tun}y_2 + {w_{tun}}^2 + \frac{2E_G\varepsilon_S}{q^2N_A}$$

$$\Rightarrow y_{\max} = y_2 + \frac{1}{2}\frac{{w_{tun}}^2 + {2E_G\varepsilon_S}/{q^2N_A}}{w_{tun}}$$

$$\Rightarrow y_2 = y_{\max} - \frac{1}{2}\frac{{w_{tun}}^2 + {2E_G\varepsilon_S}/{q^2N_A}}{w_{tun}} \qquad (4.22)$$

Differentiating Eq. 4.22 to obtain an expression for dy:

$$\frac{dy}{dw_{tun}} = 0 - \frac{1}{2}\left[\frac{d}{dw_{tun}}w_{tun} + \frac{d}{dw_{tun}}\frac{2E_G\varepsilon_S}{q^2N_Aw_{tun}}\right]$$

$$\Rightarrow \frac{dy}{dw_{tun}} = -\frac{1}{2}\left[1 - \frac{2E_G\varepsilon_S}{q^2N_A{w_{tun}}^2}\right]$$

$$\Rightarrow dy = -\frac{1}{2}\left[1 - \frac{2E_G\varepsilon_S}{q^2N_A{w_{tun}}^2}\right]dw_{tun} \qquad (4.23)$$

Combining Eq. 4.1, 4.3 and 4.23, we obtain:

$$|I| = qWL\int G\,dy$$

$$|I| = \frac{qWLA}{2}\int_{w_1}^{w_2}\frac{E_G^{D-1/2}}{q^D{w_{tun}}^D}e^{-Bq\sqrt{E_G}w_{tun}}\left(1 - \frac{2E_G\varepsilon}{q^2N_A}\frac{1}{{w_{tun}}^2}\right)dw_{tun} \qquad (4.24)$$

In DTG-CSC-TFET total tunneling length $2(L_T+L_S)$.

$$\therefore \left|I_{line}\right| = qW\left(L_T + L_S\right)\int_{w_1}^{w_2} \frac{E_G^{D-1/2}}{q^D w_{tun}{}^D} e^{-Bq\sqrt{E_G} w_{tun}} \left(1 - \frac{2E_G \varepsilon_S}{q^2 N_A} \frac{1}{w_{tun}{}^2}\right) dw_{tun} \tag{4.25}$$

Therefore, the total current expression is obtained from Eq. 4.17 and 4.23 as:

$$\left|I_{total}\right| = \left|I_{point}\right| + \left|I_{line}\right| \tag{4.26}$$

The current expression obtained in Fig. 4.26. is for the ON-current. The band-to-band tunneling at the channel-drain interface is not considered in the calculations as the applied gate bias is positive and as such tunneling distance between the channel valence band and the drain conduction band is very large. Hence, no tunneling occurs at the channel-drain interface under the given gate bias. The calculation of ambipolar current for negative gate bias has not been considered in this treatment.

4.4 Results and Discussion

4.4.1 Simulation Setup

Silvaco, Atlas version 5.20.2.R was utilized to perform all the simulations. Appropriate mathematical models such as Lombardi Mobility Model, non-local BTBT model (BBT.NONLOCAL), Fermi Dirac Statistics, bandgap narrowing model, Auger and Shockley-Read Hall (SRH) recombination models and Drift diffusion carrier transport models were included to account for the underlying device physics of the proposed DTG-CSC-TFET. The non-local BTBT model calculates the carrier generation rate at the source-channel and channel-drain junctions. The carrier model, Fermi Dirac Statistics accounts for the carrier concentration in order to state the mobility of the field. It accounts for the high carrier concentration statistics. To determine the carrier energy in the surrounding lattice and carrier lifetime, SRH and Auger recombination models have been used. In the later part of section 4.4, the quantum confinement effect in the proposed structure has been studied. For the purpose of quantum simulations, the

self-consistent Schrodinger-Poisson model has been used. This model accounts for the quantum mechanical effects under very low device dimensions.

4.4.2 Voltage Optimization

Voltage optimization was performed by comparing the subthreshold swing (SS), I_{ON}/I_{OFF} ratio and threshold voltage (V_{th}) for the proposed DTG-CSC-TFET for varying L_S (10nm, 15nm, 20nm) under five different values of drain voltage (V_{DS}). These calculations were performed on the Silvaco, Atlas software by use of appropriate codes as available in [17]. Ideally, subthreshold swing (SS) must be low, I_{ON}/I_{OFF} ratio must be high and the threshold voltage (V_{th}) must be low. Fig. 4.7 shows a bar graph for comparing the I_{ON}/I_{OFF} ratio of the three structural variations. It is seen that the device has similar I_{ON}/I_{OFF} ratio for V_{DS}=0.1V and V_{DS}=0.2V which is approximately 10^{12} for all the three structural variations (L_S = 10nm, 15nm, 20nm). This result is quite good compared to previous literature [18]. Such high I_{ON}/I_{OFF} is obtained in the DTG-CSC-TFET due to the double gate configuration and the remarkably high tunneling area that results in increased ON-current. It is also worth noting that I_{ON}/I_{OFF} ratio is, in general, higher for L_S=20nm than for L_S=10nm. This is discussed in details in the forthcoming sections.

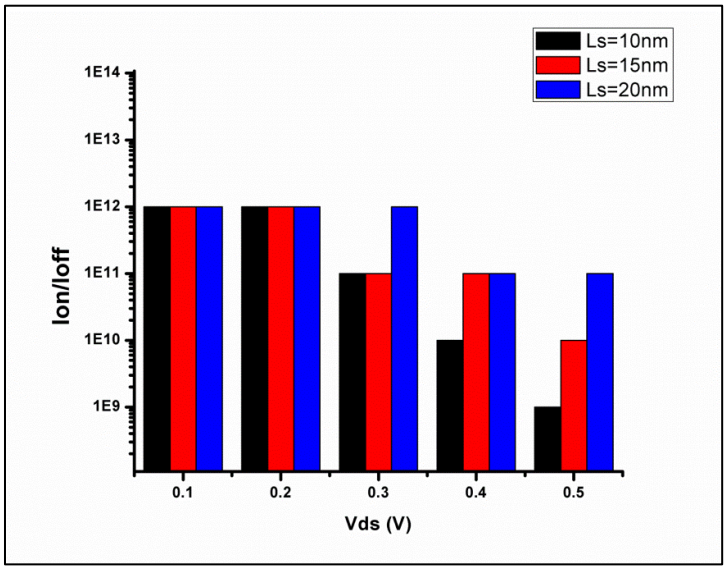


Fig 4.7. Bar graph for comparing the approximate I_{ON}/I_{OFF} ratios of the three structural variations (L_S = 10nm, 15nm, 20nm)

Fig 4.8 shows a bar graph for comparing the subthreshold swing (SS) for varying L_S (10nm, 15nm, 20nm) under five different values of the drain voltage (V_{DS}). We know that lower subthreshold swing value is preferred under the prescripts of device miniaturization. The lowest values of SS is obtained at V_{DS}=0.1V for all the three structural variations (L_S = 10nm, 15nm, 20nm), with the lowest recorded value of 22 mV/decade for L_S=20nm. Fig. 4.9. shows a bar graph for the comparison of threshold voltage (V_{th}). It can be observed that the lowest recorded threshold voltage value is obtained for V_{DS}=0.1V. The V_{th} values are almost same for L_S=15nm and L_S=20nm. It can be concluded from the Fig. 4.7, 4.8 and 4.9 that the drain voltage V_{DS}=0.1V is the most optimized value for the proposed structure. Such low values of drain voltage agree well with the results presented in [19]. Hence, this device is best suited for low power applications. All further simulations presented in this chapter have been performed for V_{DS}=0.1V.

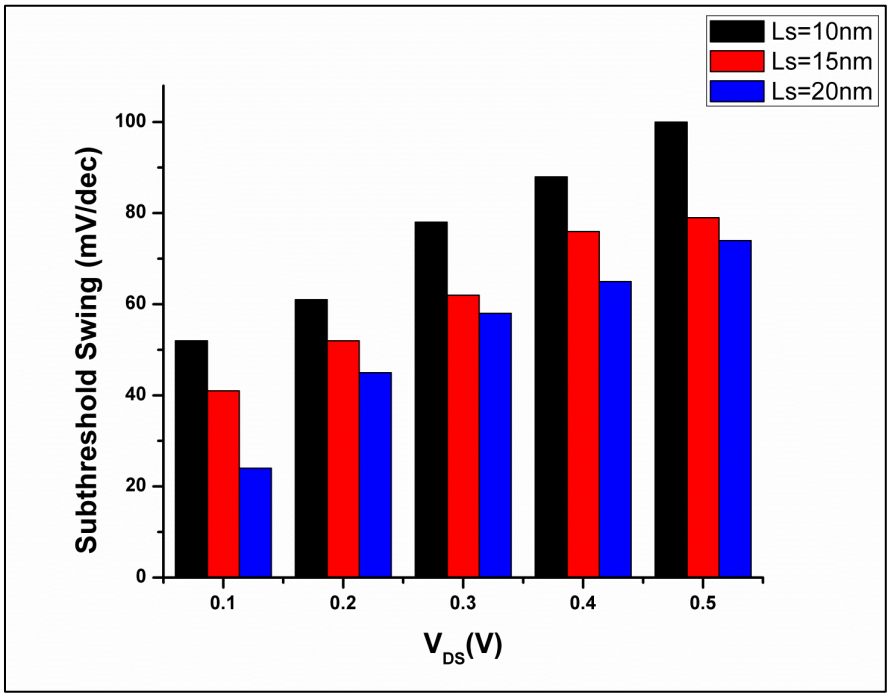


Fig 4.8. Bar graph for comparing the Subthreshold Swing (SS) of the three structural variations (L_S = 10nm, 15nm, 20nm)

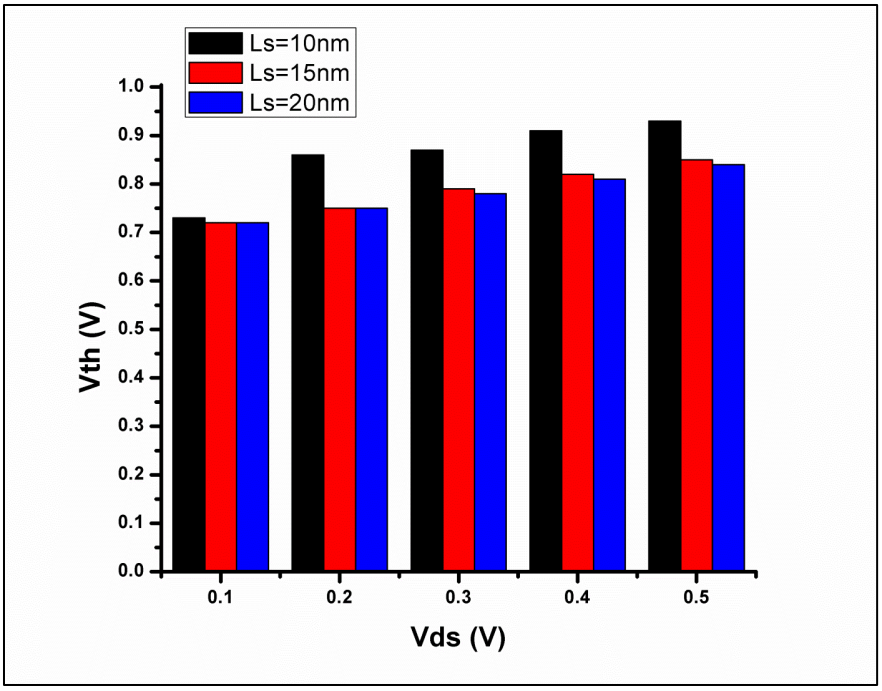


Fig 4.9. Bar graph for comparing the Threshold Voltage (Vth) of the three structural variations (L_S = 10nm, 15nm, 20nm)

4.4.3 Variation of Extended Source Length L_S

It has been previously assumed that line tunneling occurs for a total length of $2(L_T+L_S)$. Hence, this value is indicative of the band-to-band tunneling area. In order to validate this assumption, three different values of L_S have been taken as L_S=10nm, L_S=15nm and L_S=20nm. The effect of this structural variation on the energy band diagram, electric field, potential and transfer characteristics have been compared in this section. Also, the aforementioned parameters have been compared for two different cutlines that were shown in Fig. 4.1. The transfer characteristics obtained from the analytical model has been compared with the simulation results.

4.4.3.1 Energy Band Diagram

The energy band diagrams have been plotted for the DTG-CSC-TFET for L_S=10nm, L_S=15nm and L_S=20nm under ON-state at cutline 1. It is known that tunneling probability is inverse

exponentially related to the tunneling length. From Fig. 4.10, it is evident that the least tunneling length occurs for L_S=20nm. Hence, the tunneling probability is highest in this case. The slightly bent energy band characteristics at the drain end is due to LDD and as such is responsible for reduced ambipolar conduction for the proposed structure. Fig. 4.11 shows the comparison of the energy band diagrams for cutline 1 and cutline 2. It is seen that the tunneling probability is higher in case of cutline 1 than for cutline 2. The cutline 2 passes through the middle of the extended source region and hence, the source-channel interface is well ahead along the x-axis to that in case of cutline 1. This difference in tunneling probabilities is evident from Fig. 4.12 which shows the contour diagram of the BTBT rates for cutline 1 and cutline 2.

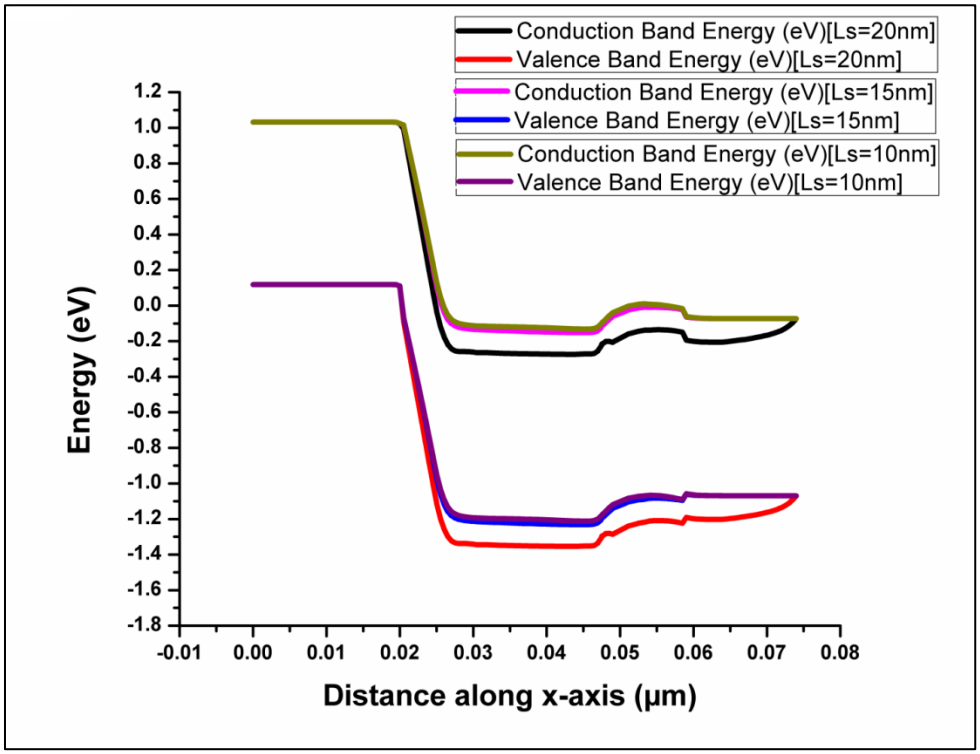


Fig 4.10. Comparison of the Energy Band Diagrams of the three structural variations (L_S = 10nm, 15nm, 20nm) for DTG-CSC-TFET

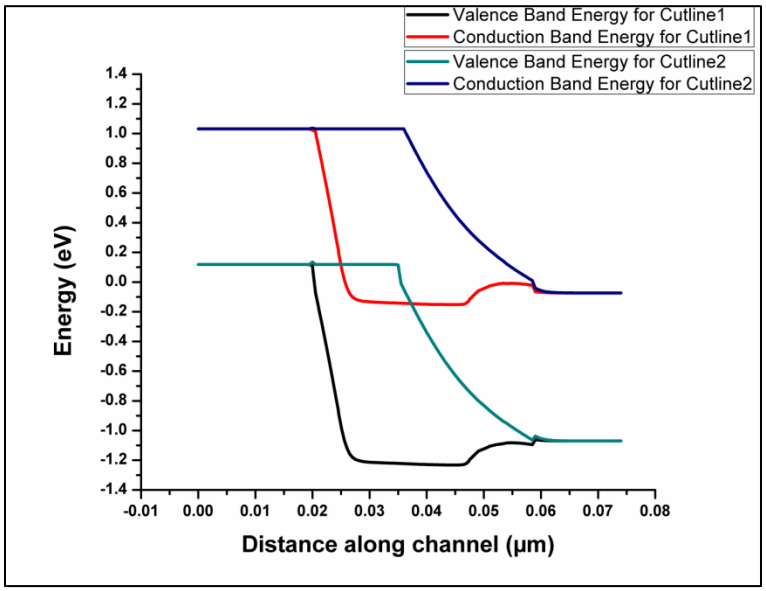


Fig 4.11. Comparison of the Energy Band Diagrams for cutline 1 and cutline 2 for L_S = 15nm

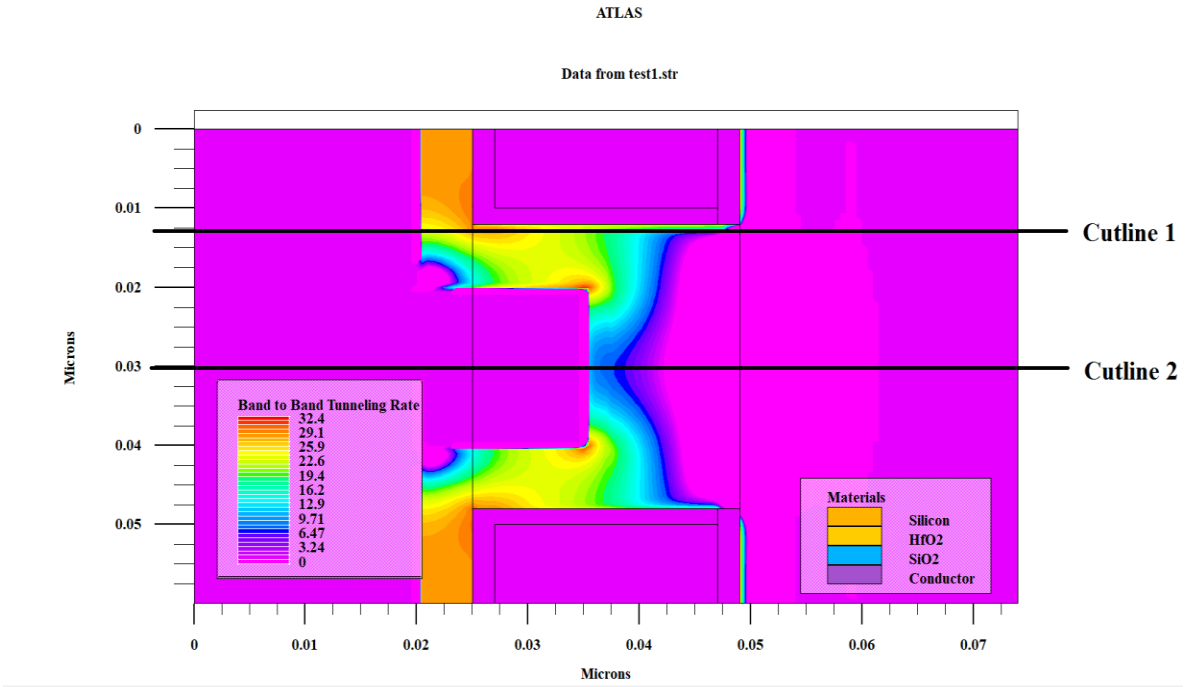


Fig. 4.12 The contour diagram of the BTBT rates for cutline 1 and cutline 2

4.4.3.2 Electric Field

The peak overshoot in the electric field at the source-channel interface is an indicative of the extent of tunneling. The electric field is compared for all the three structural variations at cutline 1 in Fig. 4.13. The highest peak is observed for L_S=20nm at the source channel junction for cutline1. The electric field characteristic remains high for a considerable channel length owing to the covered-source configuration of the DTG-CSC-TFET. The presence of a peak at the channel drain interface indicates suppressed reverse ambipolar tunneling. This peak also suggests the impact of DIBL effect. It is seen that the electric field peak is slightly higher for L_S=10nm at the channel drain interface as compared to the other two variations suggesting lower DIBL effect for this structure. The electric field at the source channel junction is much higher than that at the channel-drain junction suggesting reduced hot carrier effect in the proposed device.

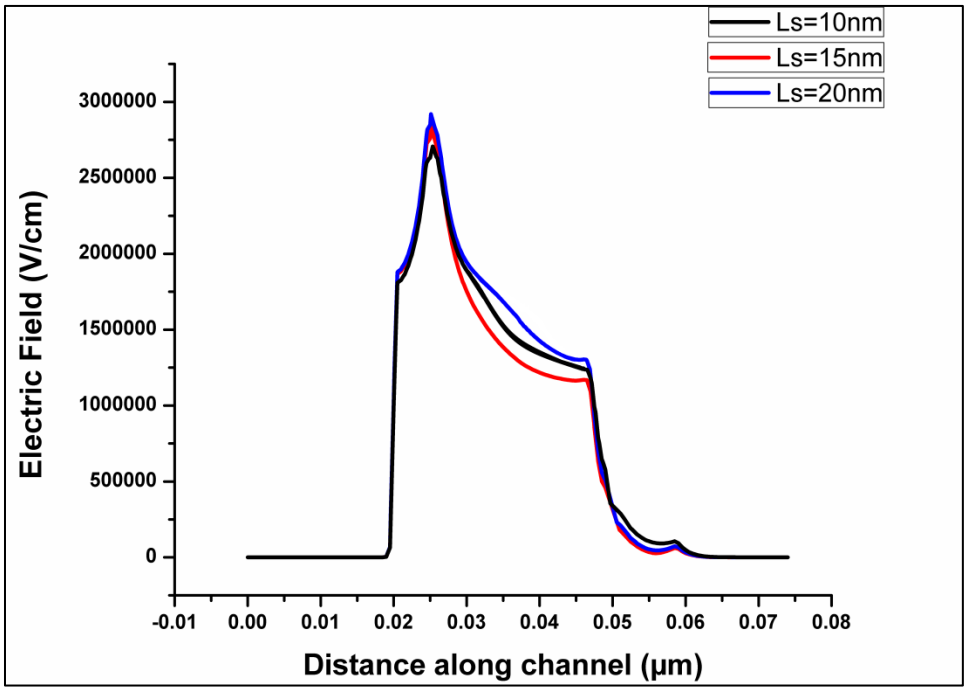


Fig 4.13. Comparison of the Electric Fields of the three structural variations (L_S = 10nm, 15nm, 20nm) for DTG-CSC-TFET

Fig. 4.14. shows the electric field for cutline 1 & cutline 2 for the sake of comparison. It is clear that the peak overshoot is higher for the cutline 1 than for cutline 2, indicating greater degree of tunneling for the former. Fig. 4.15. shows the electric field contour diagrams for all the three structural variations.

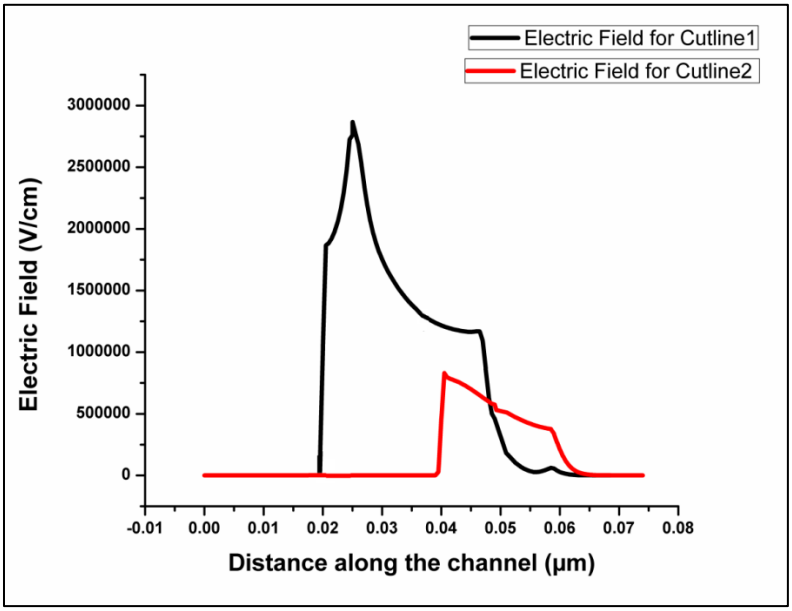
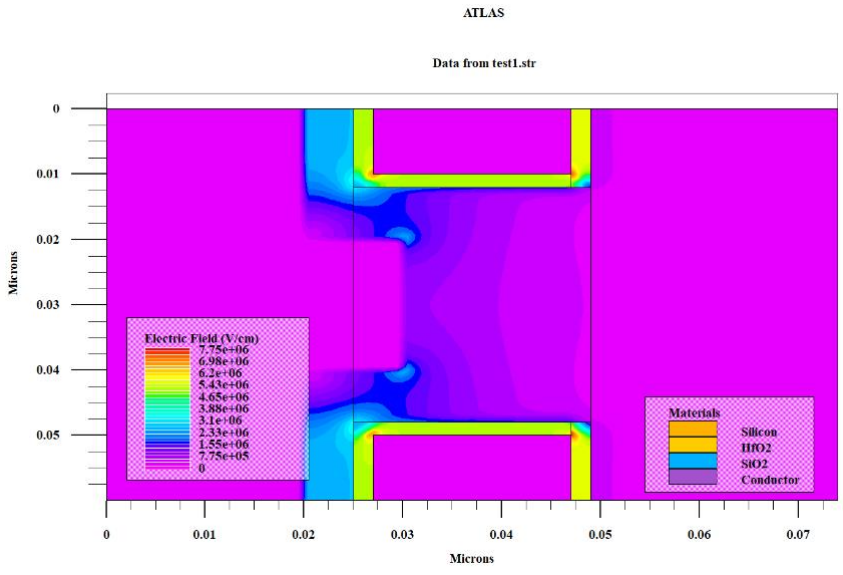
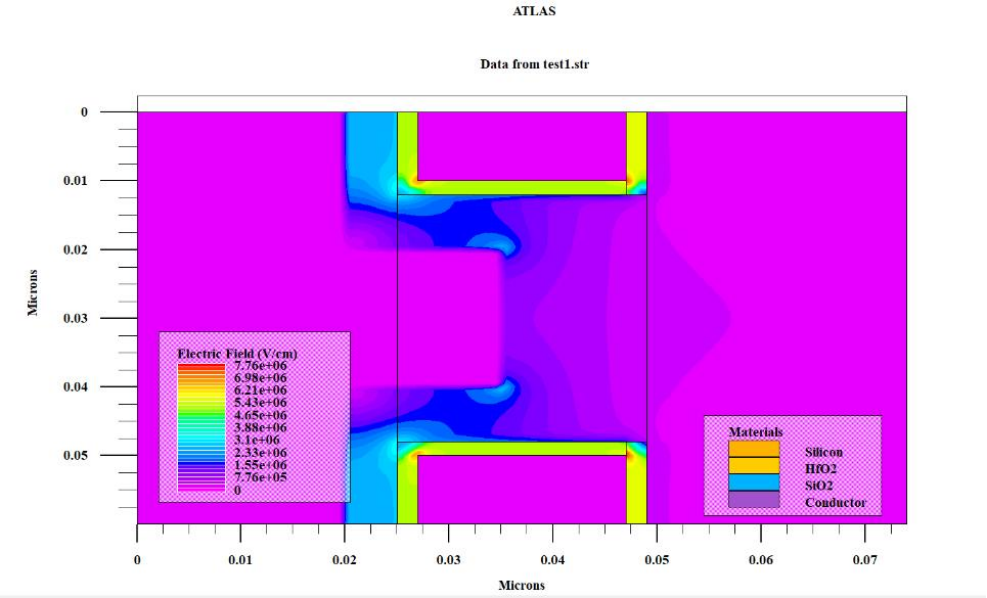


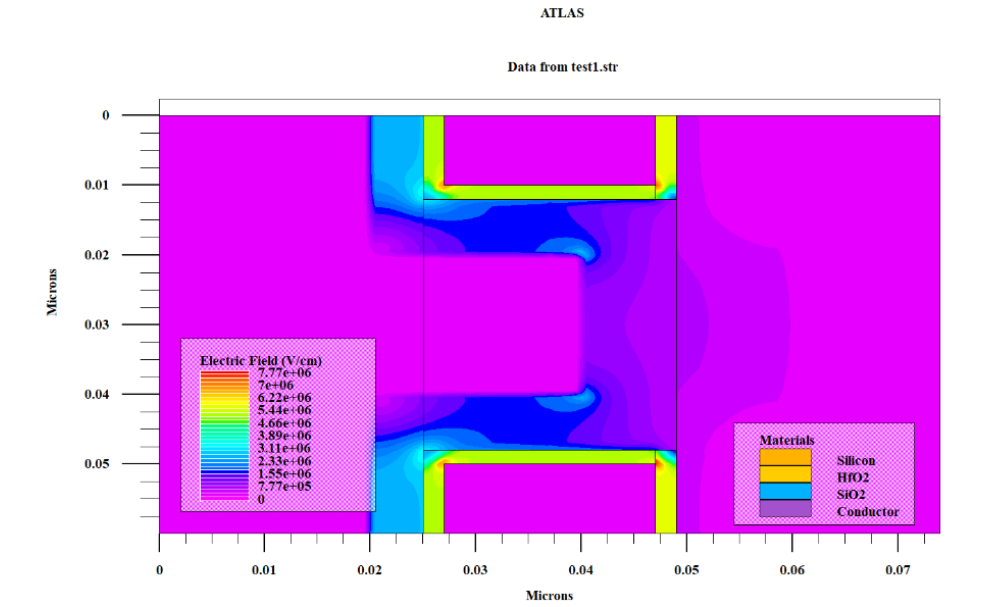
Fig 4.14. Comparison of the Electric Fields for cutline 1 and cutline 2 for L_S = 20nm



(a)



(b)



(c)

Fig 4.15. Contour Diagram of the Electric Field for the three structural variations: (a) L_S = 10nm (b) L_S = 15nm (c) L_S = 20nm of the DTG-CSC-TFET

4.4.3.3 Potential Profile

The peak in potential profile at the source channel junction gives a measure of the overall tunneling. It can be observed form Fig. 4.16. that the overall tunneling is highest for L_S=20nm. Moreover, greater value of potential at the channel drain junction suggests that the electrons which tunnel at the source channel interface effectively reach the drain end. This is the case for L_S=20nm. Fig. 4.17. compares the potential profiles for cutline 1 and cutline 2 for L_S=20nm. It is seen that the potential value is higher for cutline 1 than for cutline 2 suggesting lower extent of overall tunneling at the cutline 2. This agrees well with the observations from Fig. 4.12. Fig. 4.18. shows the contour diagrams of potential profiles for all the three structural variations.

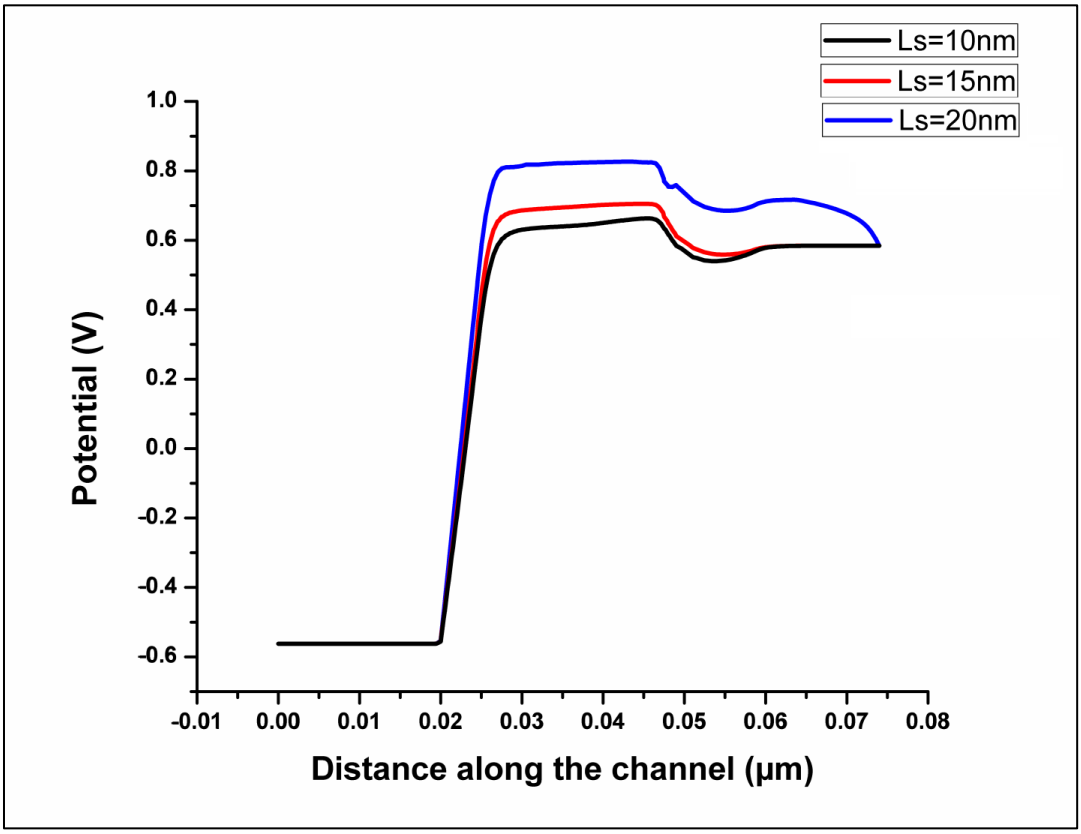


Fig 4.16. Comparison of the Potential Profile for the three structural variations (L_S = 10nm, 15nm, 20nm) of DTG-CSC-TFET

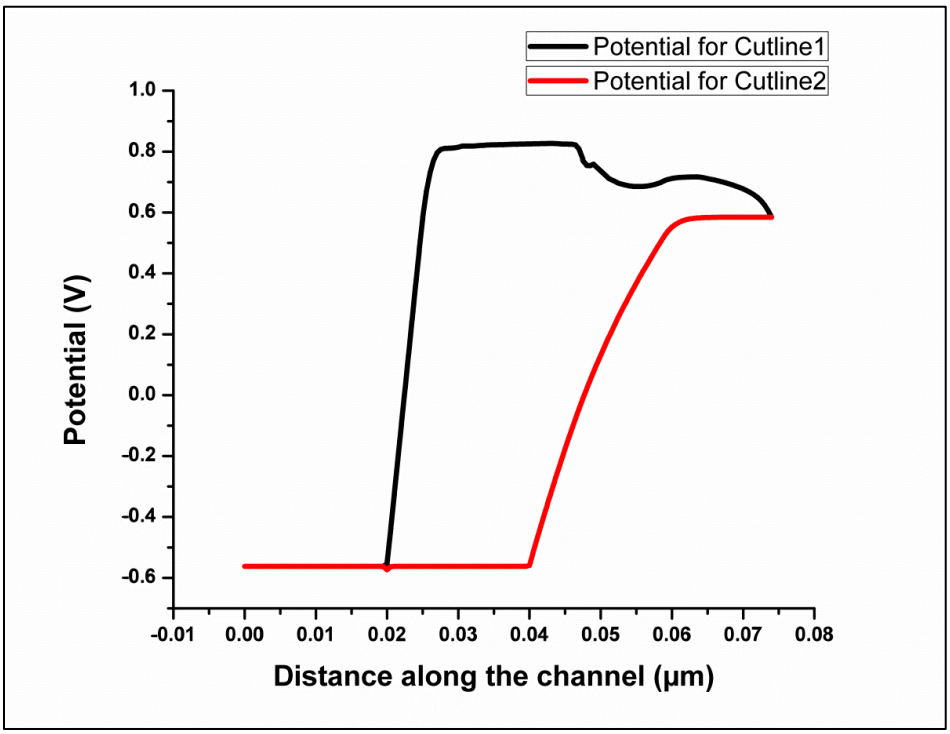
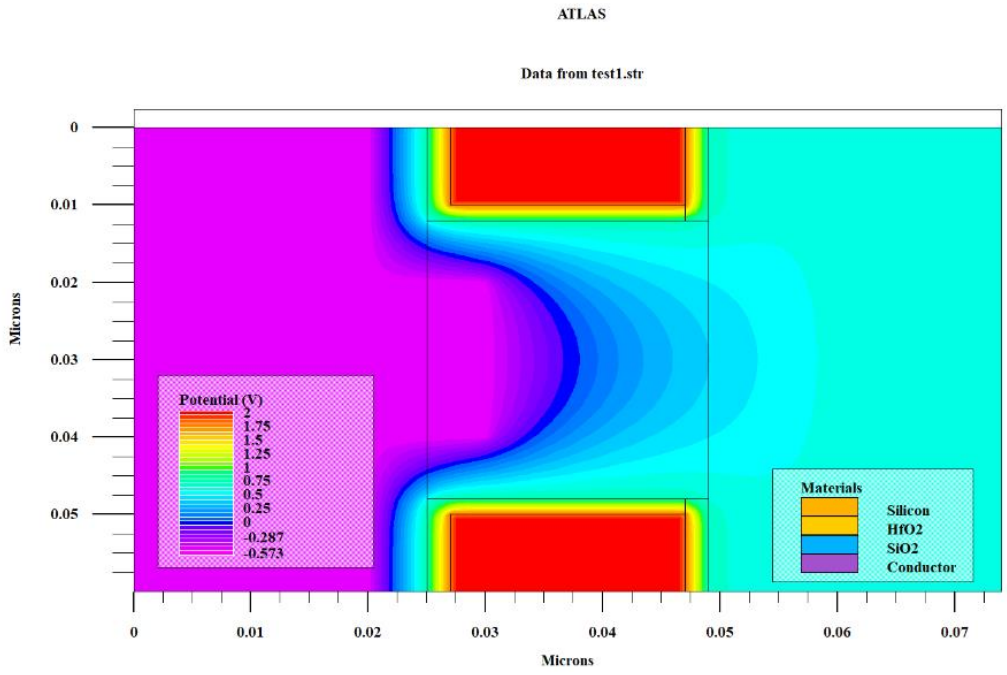
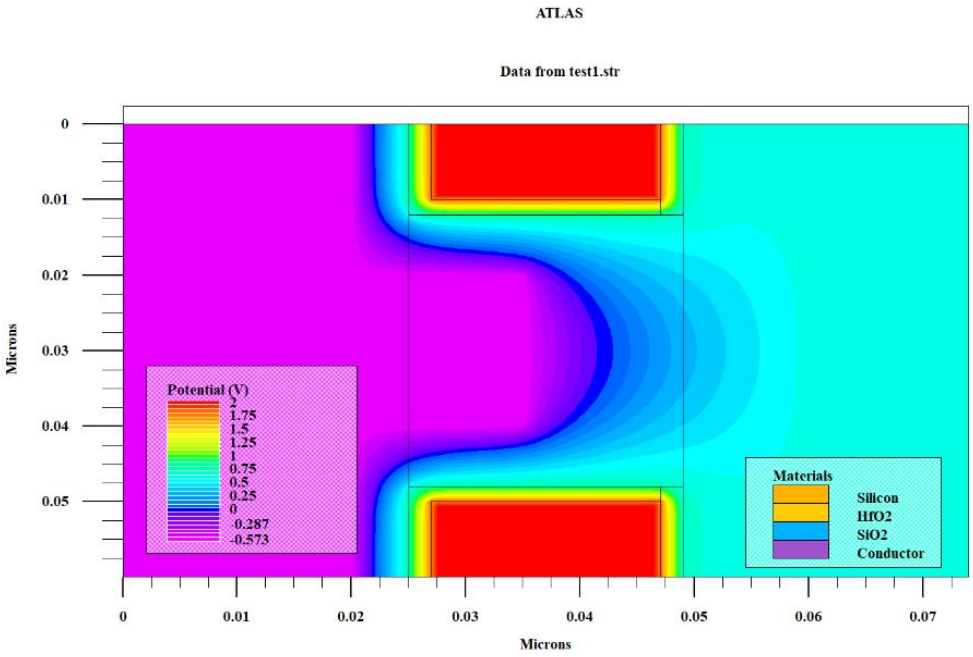


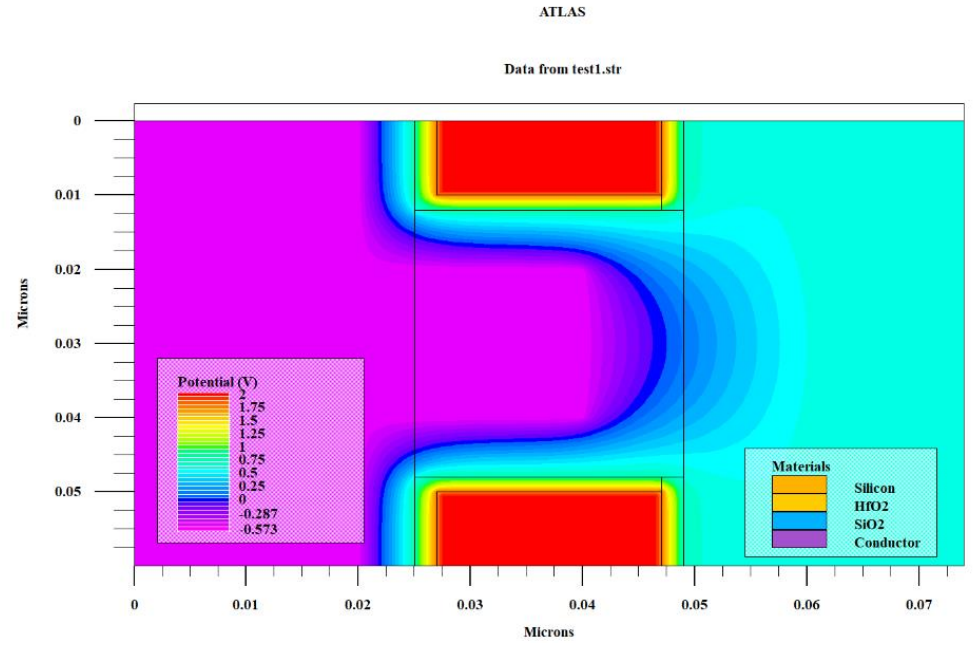
Fig 4.17. Comparison of the Potential Profile for cutline 1 and cutline 2 for L_S = 20nm



(a)



(b)



(c)

Fig 4.18. Contour Diagrams of the Potential Profile of the three structural variations (a) L_S = 10nm (b) L_S = 15nm (c) L_S = 20nm for the DTG-CSC-TFET

4.4.3.4 Transfer Characteristics

Fig.4.19. shows the linear plot of I_D-V_{GS} transfer characteristics for the different values of L_S (10nm, 15nm, 20nm). It is seen that as L_S increases, more BTBT occurs due to enhanced tunneling area. This results in higher I_{ON} because the extended portion is where line tunneling occurs. Fig. 4.20. shows the log transfer characteristics. It is evident that the subthreshold swing (SS) is 22mV/decade for L_S=20nm, 41mV/decade for L_S=15nm and 52mV/decade for L_S=10nm. Furthermore, as was evident from Fig. 4.9. the threshold voltage (V_{th}) decreases with an increase in L_S as the BTBT electrons are generated at lower values of gate voltage. From all the analysis presented, it can hence be concluded that L_S=20nm is the most optimized structural variant.

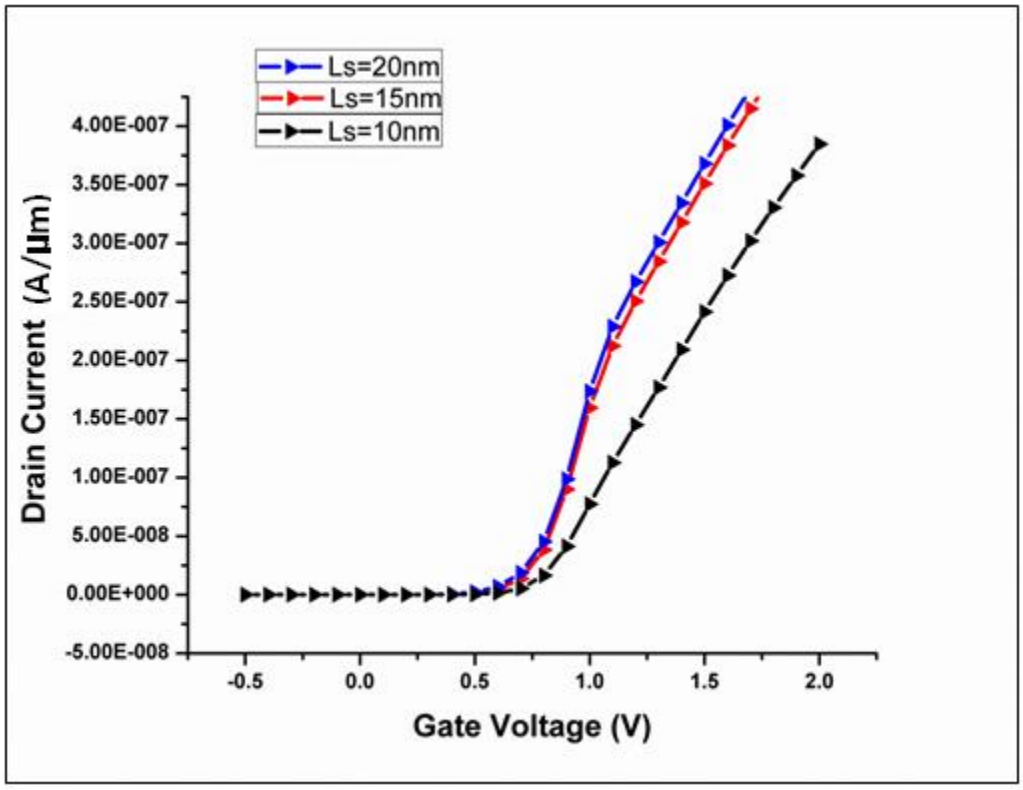


Fig. 4.19. Linear Scale plot of Transfer Characteristics for the DTG-CSC-TFET for the three structural variations (L_S = 10nm, 15nm, 20nm)

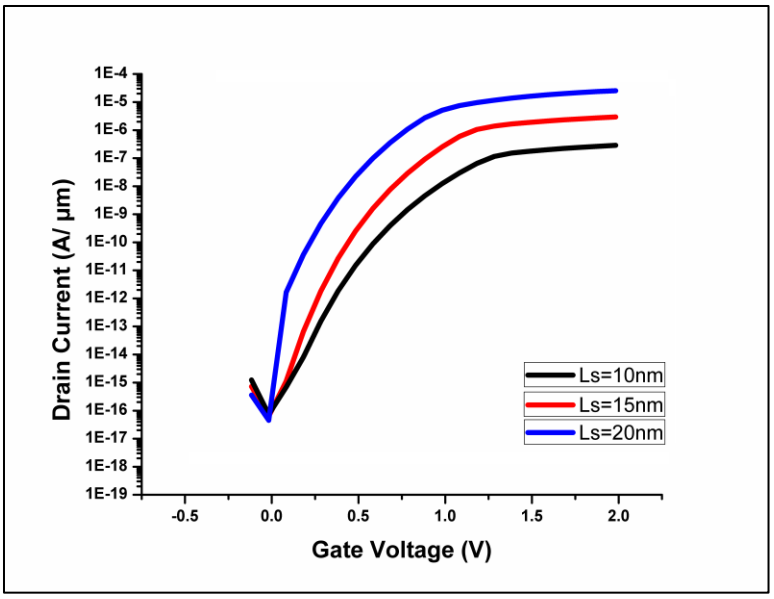


Fig. 4.20. Log Scale plot of Transfer Characteristics for the DTG-CSC-TFET for the three structural variations (L_S = 10nm, 15nm, 20nm)

4.4.3.5 Simulation based Validation of Analytical Model

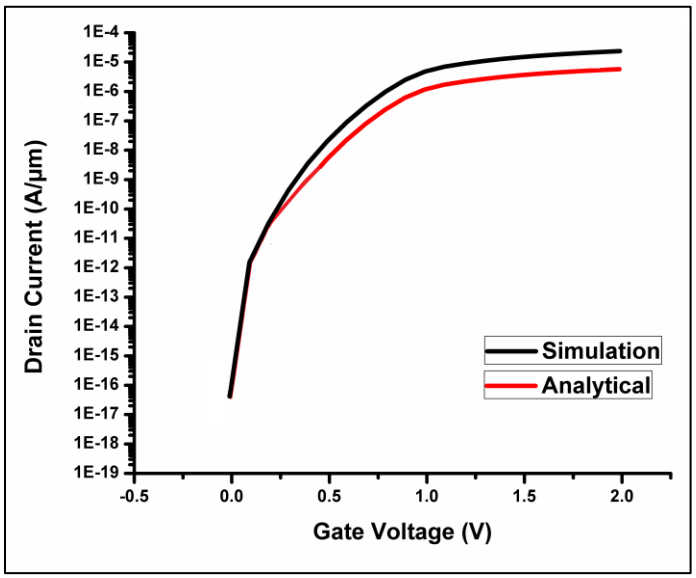
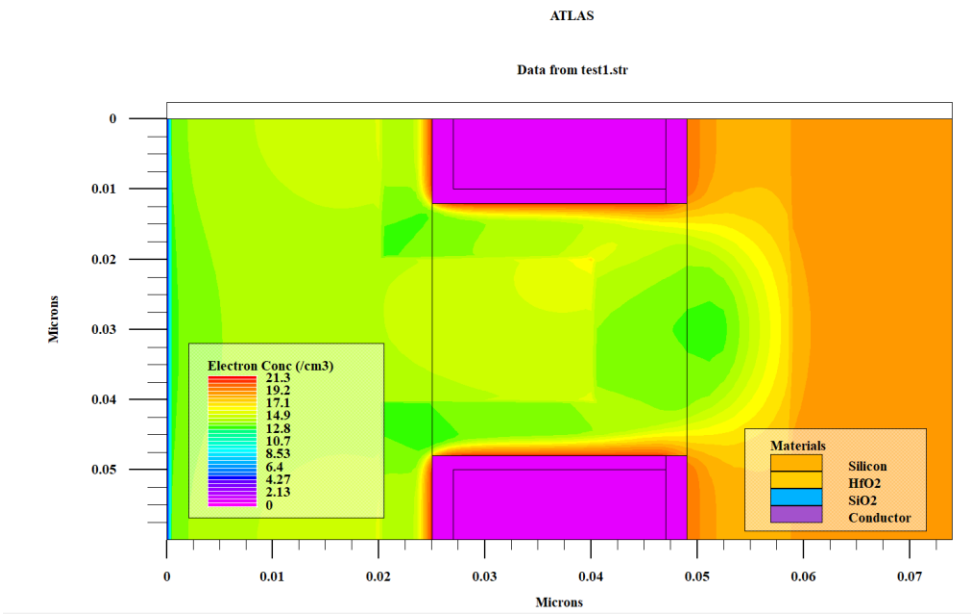


Fig. 4.21. Simulation based validation of the Analytical Model for the DTG-CSC-TFET for L_S = 20nm

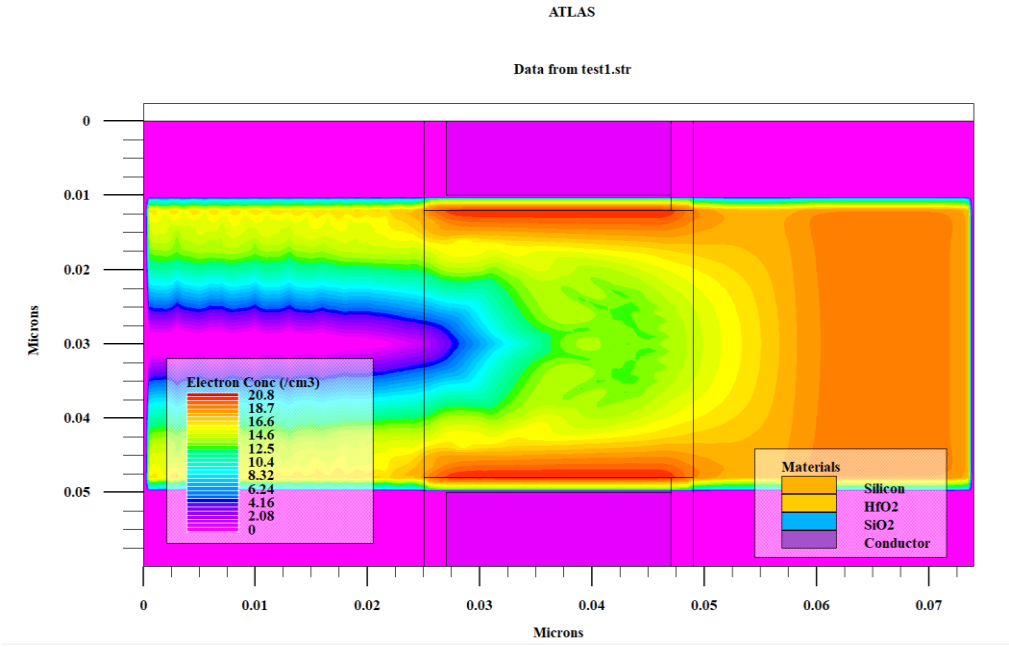
Fig. 4.21 shows a comparison between the transfer characteristics depicting the curve for ON-current as obtained from simulation and analytical modeling for the most optimized structural variant L_S = 20nm. The two curves agree well with one another, thus validating the proposed model.

4.4.4 Consideration of Quantum Confinement Effects

Owing to extensive scaling, in the present nanodevice scenario, a phenonmena known as quantum[20] confinement effect (QCE) has become more pronounced. In this phenomenon, the enrgy band structure is altered under the influence of ultra-low length scale. For group IV, II-V and II-VI, the length scale between 1 to 5 nm corresponds to the pronounced quantum confinement regime. Such low dimensions impose geometrical constraints on the electrons. In particular, as the particle size approaches the Bohr exciton radii, the QCE becomes more pronounced. Thus, in QCE the continuous energy bands of the bulk material collapse into discrete energy levels. The QCE in the proposed DTG-CSC-TFET was visualized by employing the self-consistent Schrödinger-Poisson (SP) model on Silvaco, Atlas. This was necessary as the t_{Si} of the proposed structure is 5nm. Due to energy band discretization, the conduction band-valence band overlap region gets significantly reduced at the source channel junction resulting in greater tunneling length. This reduces the extent of BTBT significantly. Fig.4.22. shows a comparison between the electron concentration for L_S=20nm with and without considering QCE. Carrier confinement is clearly seen in Fig. 4.22(b) where negligible carriers are present along the channel region with thickness t_{Si}. It is also seen that a confined region just below the gate oxide has very high electron concentration. As a direct result of this, the transfer characteristics with and without consideration of quantum confinement effect is different, with poor SS and reduced ON-current in case of the QCE consideration. The comparison in transfer characteristics is shown in Fig. 4.23. for L_S=20nm.



(a)



(b)

Fig. 4.22. Electron Concentration for L_S=20nm (a) without including Quantum Models (b) including Quantum Models

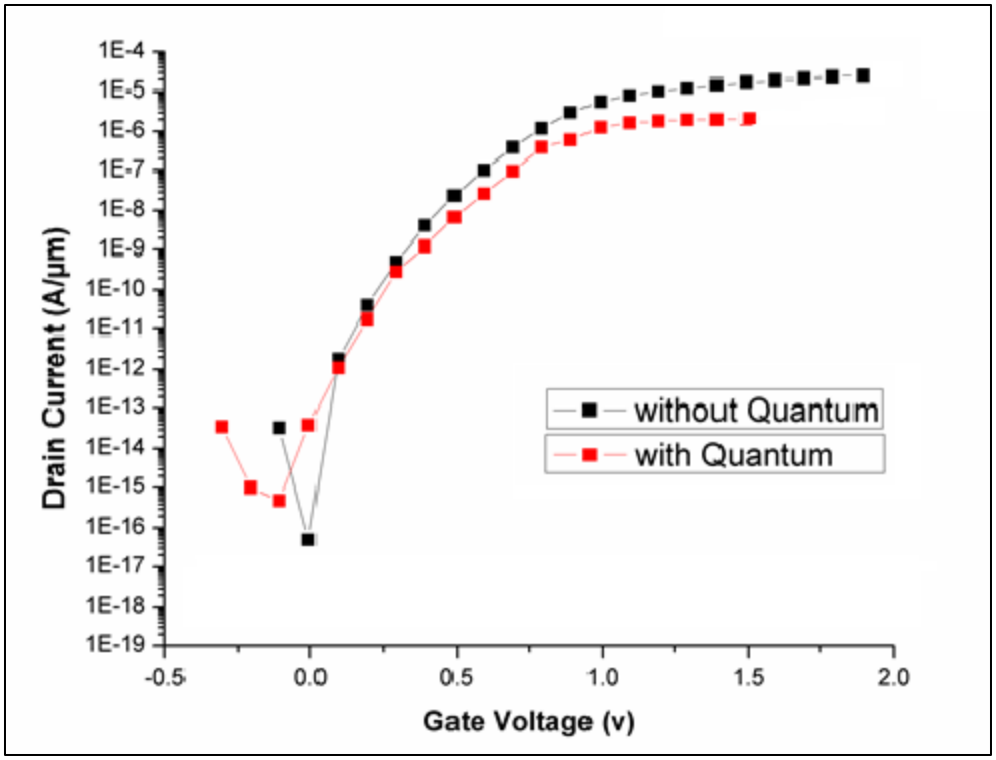


Fig. 4.23. Transfer Characteristics for L_S=20nm with and without including Quantum Models

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CHAPTER 5

CONCLUSION AND FUTURE SCOPE

5.1 Conclusion

5.2 Future Scope

5.1 Conclusion

The objective of this thesis was to explore material and structural variations on the conventional TFETs in order to achieve reduced subthreshold swing, increased I_{ON}/I_{OFF} ratio, high I_{ON} and reduced threshold voltage V_{th}. As MOSFETs are failing to keep up with the growing demands for miniaturization, the interest in alternative devices has grown in last two decades. TFETs are being considered as a potential replacement of MOSFETs in the present technology node. Two independent structures have been proposed. The first structure is based on gate material variation (gate engineering) and introduces an L-shaped dielectric Double Metal Dual Gate TFET. The second work is based structural variation and introduces a novel Double Trench Gate Covered Source-Channel TFET (DTG-CSC-TFET).

In the first work, the effects of the gate-engineering on the performance parameters of L-shaped dielectric Double Metal Dual Gate TFET (Fig. 3.1) has been demonstrated through Silvaco,

Atlas simulations. The L-shaped dielectric ensures improved tunneling at the source-channel interface. Three structures have been proposed according to the dielectric material used and compared. LS-HS-DM-DG TFET shows lowest subthreshold slope of 24 mV/dec, as shown in Fig. 3.9, and superior potential and electric field profiles as compared to the other two structure (Fig. 3.4 and 3.5). Hence, it can be concluded as the most optimized structure in this work. All structures indicate better characterization than conventional TFETs. Also, the ambipolar conduction is reduced as indicated from the electric field profiles and the transfer characteristics of the proposed structures.

In the second work, the proposed Double Trench Gate Covered Source-Channel TFET (DTG-CSC-TFET) has been analytically modeled and validated by Silvaco, Atlas simulations. The configuration of the double trench gate along with the covered source-channel ensures very large tunneling area. Both line tunneling and point tunneling mechanisms contribute to the ON-current. The device parameters such as energy band diagram, electric field, potential profile as well as the transfer characteristics were compared for different values of the extended source length L_S (10nm, 15nm, 20nm). The voltage was optimized at V_{DS}=0.1V. It was observed that the structural variation with L_S=20nm exhibited highest degree of tunneling and superior subthreshold swing (Fig. 4.20). It is hence, the most optimized structure. This is expected, as increasing L_S increases the tunneling area. The simulated transfer characteristics agree well with the analytical model. The BTBT is observed to be lowest along cutline 2. The SS obtained for the optimized structure is 22mV/decade and the I_{ON}/I_{OFF} ratio is 10^{12}. Increasing Ls also resulted in reduced threshold voltage. The proposed DTG-CSC-TFET structure exhibits excellent SS, high I_{ON}/I_{OFF}, high ON-current of about 10^5 A/μm, whilst operating at very low drain bias of 0.1V. This structure is hence a promising candidate for the next generation ultra-low power technology.

5.2 Future Scope

The TFET structures that have been studied in this thesis show superior performance characteristics as compared to conventional planar TFETs. The proposed structures will be further explored for low power, RF and analogue applications, in future works. The quantum confinement effect has been introduced for DTG-CSC-TFET and simulated with Schrodinger-Poisson model. Quantum Analytical modeling will be further explored to obtain realistic models that can capture the quantum confinement effect in highly miniaturized devices in the sub-20 nm node. Further optimization will enhance the viability and feasibility of the proposed TFETs in circuit applications which is the ultimate aim of device research.

List of Publications Relevant to the Thesis:

Accepted papers in Conferences:

1. Bijoy Goswami, **Sutanni Bhowmick**, Arindam Haldar, Debadipta Basak, Goutika Paul and Subir Kumar Sarkar, "Implementation of L-shaped Double Metal Dual Gate TFET towards Improved Performance Characteristics and Reduced Ambipolarity" in Information, Photonics and Communication 2019 (IPC'19) 1 st -3rd February, 2019, B. P. Poddar Institute of Management and Technology (BPPIMT), Kolkata **(WIE Best Student/Research Scholar Paper Awarded)**

2. Bijoy Goswami, Debadipta Basak, Ayan Bhattacharya, Koelgeet Kaur, **Sutanni Bhowmick**, Subir Kumar Sarkar "Analytical Modeling and Simulation of Low Power Salient Source Double Gate TFET" ,Kalyani University, 23-24 March,2019

3. Bijoy Goswami, **Sutanni Bhowmick** ,Debadipta Basak, Ayan Bhattacharya, Arindam Halder, Subir Kumar Sarkar "2-D Analysis of a Centrally Aligned PNPN-DG TFET to Preclude Ambipolar Conduction" , ECTI CON 2019, Thailand.

Journals:

4. Bijoy Goswami, Debadipta Basak, Ayan Bhattacharya, **Sutanni Bhowmick**, Koelgeet Kaur, Subir Kumar Sarkar, "Analytical Modeling and the Impact of Quantum Confinement on Subthreshold Swing of Salient Source DG-TFET" [Communicated]

5. **Sutanni Bhowmick**, Bijoy Goswami, Debadipta Basak, Koelgeet Kaur, Ayan Bhattacharya and Subir Kumar Sarkar, "Analytical Modeling and Simulation of Double Trench Gate Covered Source-Channel TFET towards Improved ON-Current" [Communicating]

6. Debadipta Basak, Bijoy Goswami, **Sutanni Bhowmick**, Koelgeet Kaur, Ayan Bhattacharya, Subir Kumar Sarkar, " Analytical Modeling and Simulation Based Validation for Gate Centric Extended Source SOI TFET" [Communicating]

7. Koelgeet Kaur, Bijoy Goswami, **Sutanni Bhowmick**, Debadipta Basak, Subir Kumar Sarkar, "Analytical Modeling and Simulation Based Validation of Dual source TFET" [Communicating]