ANALYTICAL MODELLING & SIMULATION BASED VALIDATION OF DUAL SOURCE TFET

Thesis Submitted In Partial Fulfillment Of The Requirements For The Award Of The Degree Of

Master Of Technology In

VLSI Design And Microelectronics Technology

By

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CERTIFICATE OF EXAMINATION

This is to certify that the thesis entitled "**Analytical Modelling and Simulation Based Validation of Dual Source TFET**" has been carried out by **KOELGEET KAUR (Roll No: 001610703016, Examination Roll No: M6VLS19006 and Registration No:137288 of 2016-17)** under my guidance and supervision and can be accepted in partial fulfilment for the degree of Master of Technology in VLSI Design and Microelectronics Technology. In my opinion the work fulfils the requirement for which it is submitted. To the best of my knowledge, the matter embodied in the thesis has not been submitted to any other organization.

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Abstract

Tunnel field-impact transistor (TFET) has developed as a substitute for regular CMOS by empowering the supply voltage (V_{DD}) scaling in ultra-low control, energy efficient processing, because of its sub-60 mV/decade sub-threshold slope (SS).

A comprehensive research of TFETs was activated around 2004 with the successful establishment of the subthreshold swing underneath 60 mV/decade and the need for a gadget that can substitute traditional MOSFETs for low-control vitality proficient circuits. Thereafter the number of research activities on TFETs have been developed exponentially. Various kinds of semiconducting materials have been deployed to produce TFETs and have yielded empowering results. It appears that there is significant research activities in the area of TFETs and their application in circuits. In view of the above citation I have done research work on the same line which are briefly described here below.

In this work, an innovative approach to enhance ON-current and suppress the OFF-current in Tunnel FETs (TFET) using Synopsys Sentaurus TCAD simulation has been proposed. A Silicon based Double Source Trench Gate Split Drain (DSTGSD) TFET structure has been proposed for which the results show a significant increment in ON-current and a momentous decrement in leakage current. The DSTGSD-TFET structure shows an Ion/Ioff ratio of approximately 10^{12} in contrast with the conventional Planer TFET structure with a single source and single drain region. The impact of various device geometry variations has been studied and optimized accordingly. Also we have included Quantum Confinement model in our optimized structure and a comparison of the transfer characteristics and electron density for Quantum and Classical models are shown. In this work for the DSTGSD-TFET structure, Kane's model is used and an analytical expression for the ON-current through the TFET is derived. Furthermore, a compact expression for the TFET ON-current is derived and conclusions concerning TFET design are drawn. The obtained analytical expressions are compared with results from a 2D device simulator and are found to be in good agreement.

Chapter 1

Introduction

1.1 Introduction

For the last three decades, the microelectronic industry has enormously benefitted by downscaling the size of the semiconductor device in terms of achieving higher circuit speed low power consumption, and incremented efficiency. It all commenced with the invention of Integrated circuits in 1959 that led to the birth and expansion of the modern day semiconductor industry. Integrated circuits have promoted the invention of incipient practical devices and gadgets that have ameliorated the lifestyle of the present age of human civilization. Thus in order to consummate the incrementing technological demand, there is a rapid magnification in the electronics industry. However, this explosive development in

microelectronics industry is only possible by the innovation and implementation of amended device performance in terms of high speed and low power consumption along with more preponderant manufacturing profit in terms of low cost per device built. Hence the concept of device scaling plays a vital role in amending the contrivance performance. The advantages of nano-scaled transistors are higher current drive and densely packed chips, resulting in low manufacturing costs, more expeditious processing speed and the competency to accomplish multiple tasks simultaneously. Fabrication of more diminutive and more expeditious MOS transistors perpetuated for the last 40 years, due to which the assiduous demand for ameliorated contrivance functionality could be met [1].

1.2 Limitations of MOSFET

The persistent evolution of electronics, information technology (IT), and communications has been mainly enabled by continuous progress in silicon- based complementary metal-oxide-semiconductor (CMOS) technology. This continuous progress has been sustained mostly by its dimensional scaling, which results in exponential growth in both device density and performance. Short- channel effect is an undesirable effect arising in a MOSFET when the channel length is reduced to the width of the depletion-layer of the source and drain junction. The channel length L is decreased to improve the speed and packing density. Hence, a limitation is imposed on the electron drift characteristics in the channel and the threshold voltage is altered. These changes in the physical phenomena act as the sole reasons for the birth of short channel effects namely Drain induced barrier lowering, punch through, velocity saturation, impact ionization, threshold voltage roll off, hot carrier effect etc. These deleterious effects cause MOSFETs to behave differently. The potential distribution in the channel depends on both the vertical electric field and lateral electric field. In general, the vertical electric field is greater than the lateral electric field at the channel region. This condition is no longer valid in the short channel devices and the drain potential has more influence on channel region than the gate potential. The two dimensional effects (vertical and lateral electric fields) results in a intolerable degradation of the subthreshold behaviour, dependence of the threshold voltage on channel length and biasing voltages, and failure of current saturation. Suppression of short channel effects becomes a serious issue in the design of MOSFETs to deliver improved performance. This can be done by proper scaling of device dimensions. The MOS transistor has been improved countless times but above everything else it has been

miniaturized beyond imagination. [2]-[9].

1.2.1 Drain Induced Barrier Lowering

The Drain Induced Barrier Lowering (DIBL) is simply defined as the encroachment of depletion region from the drain into the channel. It results in the reduction of the threshold voltage at higher drain voltages. In long channel MOSFETs, the channel region is electrostatically shielded from the drain voltage. Hence, the drain bias does not affect the threshold voltage $V_{th.}$ The current flow in the channel depends on creating and sustaining an inversion layer on the surface (Vander Tol & Chamberlain 1993). If the gate bias voltage is not sufficient to invert the surface, the electrons in the channel face a potential barrier that blocks the flow. The potential barrier is controlled by both the gate-to-source voltage and the drain-to-source voltage.

As the drain voltage increases, the depletion region of the p-n junction between the drain and the body grows in size and extends to the gate, so that the potential barrier in the channel reduces and that is referred as drain induced barrier lowering. And also barrier lowering increases as channel length is reduced. As the channel length is reduced, the effects of DIBL in the sub threshold region (weak inversion) show up initially as a simple translation of the sub threshold current vs. gate bias curve with the change in drain-voltage, which can be modeled as a simple change in threshold voltage with drain bias. At extremely short lengths, the gate entirely fails to turn the device off. DIBL also affects the current vs. drain bias curve in the active mode, causing the current to increase with drain bias, lowering the MOSFET output resistance. The output current is called as subthreshold leakage current. DIBL can also reduce the device operating frequency.

1.2.2 Punch through Effect

Punch through occurs when the depletion regions of the source and drain merge with each other. If the depletion region around the drain continues to extend to the source depletion region with the further increasing drain voltage and finally merges together before junction breakdown occurs, the drain current increases due to the existence of a parasitic current path located well below the gate. This punch through effect adds to the subthreshold leakage current.

In devices with long channel lengths, the gate is completely responsible for depleting the semiconductor. In very short channel devices, part of the depletion is accomplished by the drain and source bias. In the long channel case, the potential barrier at the surface between source and drain is mostly flat, since the source and drain only affect the ends of the channel. For the short channel device, the source and drain fields penetrate deep into the middle of the channel, which will lower the potential barrier between source and drain. For this reason, subthreshold current is higher and the threshold voltage is lower than that for the long channel case. The reason is simple that more electrons can be injected from the source over the barrier. When a higher drain voltage is applied, the potential barrier is even more lowered, so the threshold voltage will be further decreased. For the short channel case, the subthreshold current is dependent on the drain voltage. At even shorter channel lengths, the subthreshold slope starts to degrade, as the surface potential is more controlled by drain than by the gate and when the gate totally losses control over the channel, high drain current becomes independent of gate voltage. This is called punch through effect. The effect of punch through on the MOSFET current-voltage characteristics shows a super linear increase in the drain current with the drain voltage, even at gate voltages below the expected threshold voltage.

Punch through can be minimized with thinner oxides, larger substrate doping, shallower junctions, and obviously with longer channels. The current flow in the channel depends on creating and sustaining an inversion layer on the surface. If the gate bias voltage is not sufficient to invert the surface ($V_{GS} < V_{T0}$), the carriers (electrons) in the channel face a potential barrier that blocks the flow. With an increase in the gate voltage, this potential barrier gets reduced and eventually, allows the flow of carriers under the influence of the channel electric field. In small-geometry MOSFETs, the potential barrier is controlled by both the gate-to-source voltage V_{GS} and the drain-to-source voltage V_{DS}. If the drain voltage is increased, the potential barrier in the channel decreases, leading to drain induced barrier lowering (DIBL). The reduction of the potential barrier eventually allows electron flow between the source and the drain, even if the gate-to-source voltage is lower than the threshold voltage. The channel current that flows under this conditions ($V_{GS} < V_{TH}$) is called the sub-threshold current.

1.2.3 Carrier Mobility Degradation

Since the rate of the supply voltage scaling has been reduced while the geometric scaling keeps the same historical rate, the electric fields inside the MOSFETs keep increasing. The drift velocity of the carriers is proportional to the longitudinal electric field across the channel at low field ($<10^3$ V/cm). After that point, however, the increasing rate of the carriers‟ velocity decreases increasing longitudinal field in Si at room temperature. Finally, the carriers reach their maximum velocity of $vsat \sim 10^7$ cm/sec when the electric field exceeds $\sim 3 \times 10^4$ V/cm for electrons and $\sim 10^5$ V/cm for holes (here the channel length (L) is assumed to be much greater than the average distance (l) between scattering events such as $L >> 10$ nm.) This carrier mobility degradation is called Velocity Saturation. Velocity saturation is also an important design characteristic. Velocity saturation greatly affects the voltage transfer characteristics of a field-effect transistor. If a semiconductor device enters velocity saturation, an increase in voltage applied to the device will not cause a linear increase in current. The performance of the devices is also affected by velocity saturation, which reduces the trans conductance of the device.

Another high electric field is developed between the gate and the channel due to the aggressive gate oxide thickness scaling with relatively constant supply voltage, which limits the charge carriers to a narrower region below the oxide-silicon interface, leading to more carrier scattering and hence lower mobility. Furthermore, the increased body doping by means of suppressing SCEs degrades the carrier mobility.

1.2.4 Hot Carrier Effect (HCE)

The high electric fields in a device also cause reliability problems such as threshold voltage shifts and trans-conductance degradation due to “Hot Carrier Effects (HCEs)”. As the average velocity of carriers in the channel saturates by the increased scattering rate at the high electric fields, the carriers can attain high kinetic energy. Once those hot carriers obtain sufficient energy to overcome barriers, they might migrate into the unwanted area such as the gate dielectric, gate, or substrate of a transistor. Especially, the highly accelerated hot carriers near the drain region can generate new electron-hole pairs by collision with the silicon atoms, which is called “impact ionization”. Impact ionization can cause a significant increase in substrate current or carrier injection into

the gate dielectric, which causes charges to get trapped in the gate oxide. This causes threshold voltage shifts and therefore the device becomes unstable and even can fail.

Electric fields tend to be increased at smaller geometries since device voltages are difficult to scale to arbitrarily small values. As a result, various hot carrier effects appear in short channel devices. The field in the reversed biased drain junction can lead to impact ionization and carrier multiplication. The resulting holes contribute to substrate current and some may move to the source, where they lower source barrier and result in electron injected from the source into p-region. In fact, n-p-n transistor can result within source channel drain configuration and prevent gate control of the current. Another hot electron effect is the transport of the energetic electrons over (or tunneling through) the barrier into the oxide. Such electrons become trapped in the oxide, where they change the threshold voltage and I-V characteristics of the device. Hot electron effects can be reduced by reducing the doping in the source and drain regions so that the junction fields are smaller.

However, lightly doped source and drain regions are incompatible with small geometry devices because of contact resistances and other similar problems.

1.3 Introduction to TFET

For the last three decades, the microelectronic industry has enormously benefitted by downscaling the size of the semiconductor device in terms of achieving higher circuit speed low power consumption, and incremented efficiency. It all commenced with the invention of Integrated circuits in 1959 that led to the birth and expansion of the modern day semiconductor industry. Integrated circuits have promoted the invention of incipient practical devices and gadgets that have ameliorated the lifestyle of the present age of human civilization. Thus in order to consummate the incrementing technological demand, there is a rapid magnification in the electronics industry. However, this explosive development in microelectronics industry is only possible by the innovation and implementation of amended device performance in terms of high speed and low power consumption along with more preponderant manufacturing profit in terms of low cost per device built. Hence the concept of device scaling plays a vital role in amending the contrivance performance. [10]-[12]. The advantages of nano-scaled transistors are higher current drive and densely packed chips, resulting in low manufacturing costs, more expeditious processing speed and the competency

to accomplish multiple tasks simultaneously. Fabrication of more diminutive and more expeditious MOS transistors perpetuated for the last 40 years, due to which the assiduous demand for ameliorated contrivance functionality could be met.

It has been observed that scaling the length of a MOSFET has many benefits, besides the incremented number of transistors in a chip. A reduced gate length leads to a reduced gate capacitance, thereby incrementing the switching speed of the circuit. Moreover, the voltage scaling that is an obligatory part of device miniaturisation withal causes reduction in the power consumption of the contrivance. However, as the contrivance dimensions are reduced to 50 nm, the OFF-state power consumption of MOSFETs became a major challenge. The drain current of a MOSFET is controlled by the thermionic emission from the source into the channel. [13]-[14]. As the gate voltage increases, the potential barrier between the source and the channel decreases, leading to an incrementation in the drain current. This leads to two quandaries – more OFF-state current due to subthreshold conduction and a higher subthreshold slope. A lower subthreshold slope would sanction for a higher ratio of ON-current to OFF-current (ION/IOFF), and would lead to a lower power dissipation in the OFF-state. Additionally it has been observed that shrinking contrivance dimension in nanometer regime, the CMOS technology is no more able to fortify Moore's law. Several quandaries associated with traditional scaling include reliability issues, gate tunneling effect and short channel effects (SCEs) like threshold voltage roll off, drain induced barrier lowering, incremented leakage current with degraded subthreshold slope. One such contrivance is the tunnelling field-effect transistor (TFET). TFETs can exhibit subthreshold slopes below 60 mV/decade due to a fundamental difference in the mechanism of current control as compared to MOSFETs. In MOSFETs, the current depends on the thermionic emission of free carriers across the potential barrier between the source and the channel. On the other hand, the current in TFETs depends on the charge carriers tunnelling through a potential barrier between the source valence band and the channel conduction band. As this potential barrier is very wide in the OFF-state of the contrivance, TFETs exhibit very low OFF-state current. Moreover, TFETs have greater immunity to short channel effects.

Here, an endeavour has been made to give a detailed understanding of the several types of SCEs, reduction of which are becoming the recent research endeavour at present in order to get better TFET contrivances for implementation in future generation VLSI circuits. Innovation and renovation of the geometrical structures of TFET with partially or fully modified geometrics will be considered for performance amelioration. This research work will highly contribute to the society to pull down the cost of the electronic equipment and will

withal result in more expeditious, low power contrivances making communication and mobile computing much more facile and fascinating.

1.4 Working Principle of Tunnel FET

Our worry towards low power and rapid gadgets with improved gadget thickness advance scaling down, which encourages nanoscale gadget measurements with improved RF execution. So as to fulfil these criteria MOSFETs suffer downsides like high leakage, control dissemination, short channel impacts (SCE) and edge move off. Accordingly, the TFET gadgets have turned out to be inescapable and altering the nanoscale business by supplanting the regular MOSFET. The overwhelming advantage of TFET is present conduction through regulation of quantum mechanical Band-to-Band Tunnelling (BTBT), which is a consequence of limited, yet non-zero, likelihood of burrowing through a potential obstruction, a procedure in which electrons burrow from the valence band through the semiconductor band gap to the conduction band or the other way around with no snare help. This property conveys forward the favourable circumstances over the thermionic infusion over a vitality hindrance for bearer transport in MOSFET. In this manner, because of its inherent passage boundary, where the divert current in TFET is constrained by the burrowing system from the source, the TFET gadget is safe from short channel impact and the subthreshold swing of a TFET is under 60mV/decade at room temperature, permitting TFETs to have SS as low as 20 mv/decade [18], which is a main driver of planning of low voltage working gadgets.

1.4.1 Essential Operation Of TFET

(I) Thermal Equilibrium

In warm balance band outline of a TFET, no outside predisposition is connected i.e Vgs=Vds= 0), is appeared in Fig 1.1. There are two exhaustion areas framed, one at the source– channel intersection and the other at the channel– channel intersection.

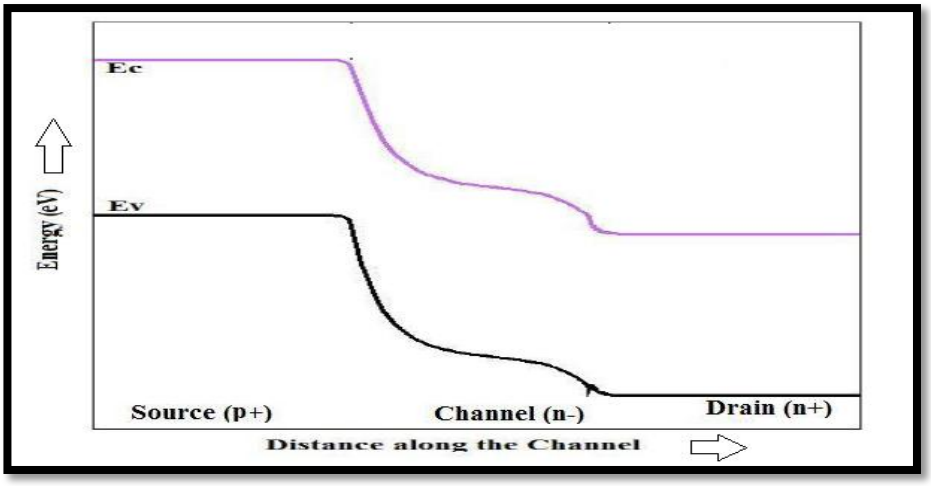

Fig1.1: Band diagram at the surface of a n-channel TFET at zero bias

(ii) Off State

The TFET is in OFF-state when the channel voltage Vds> 0 and the entryway voltage Vgs= 0, The band diagram for this case has appeared in Fig 1.2 In the OFF-condition of the TFET, any bearers present in the conduction band of the channel will float to the channel and in this manner produce a current. Be that as it may, as the source is p-type, there are not very many free electrons in its conduction band, and along these lines, not many electrons can be infused into the channel. This prompts an unimportant OFF-state current. On account of MOSFET, the source is n-type and has free electrons in its conduction band. In this way, through thermionic emanation, these electrons will be infused into the channel over the potential hindrance at the source– channel intersection. This prompts a higher OFF-state current in a MOSFET when contrasted with a TFET.

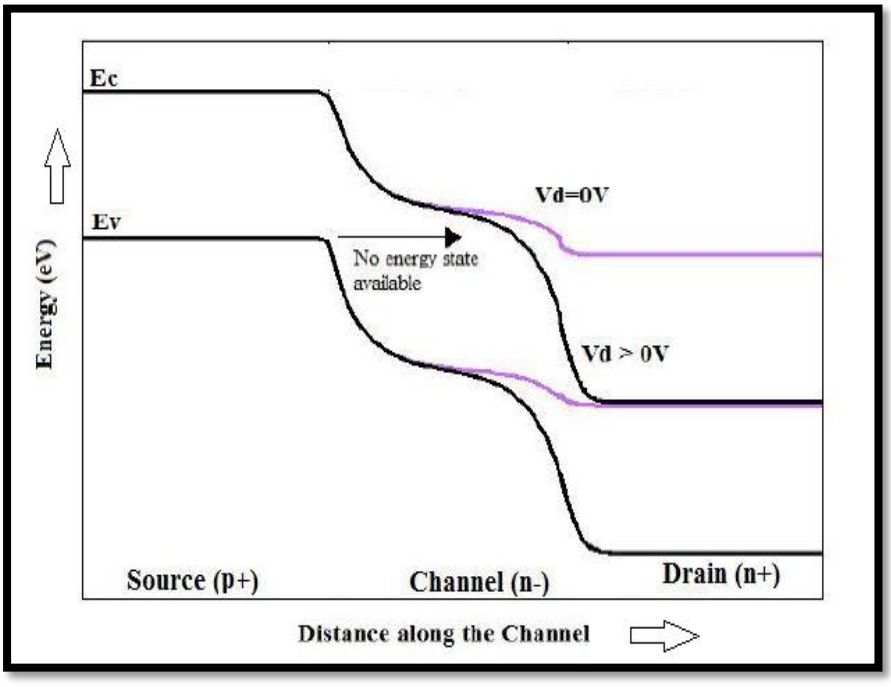

Fig1.2: Band diagram along the surface of a TFET in the OFF-state at Vgs = 0 V.

(iii) On State

As we increment the gate voltage Vgs, as appeared in Fig 1.3, the vitality groups in the channel change regarding the source. At a specific estimation of the door voltage Vgs, the valence band in the source gets lined up with the conduction band in the channel. Presently the electrons can tunnel from the valence band into the conduction band through the potential obstruction framed by the bandgap. As the entryway inclination is additionally expanded, the groups in the channel district are additionally brought down in vitality, and electrons involving vitality levels from the valence band edge of the source. This prompts a precarious increment in the current in view of the expansion of burrowing likelihood.

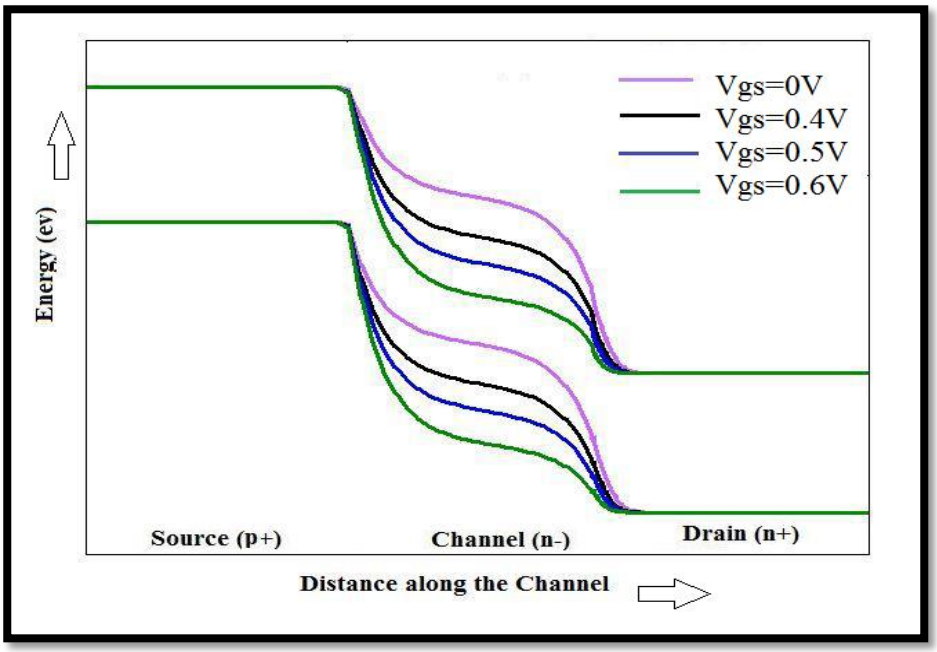

Fig1.3: Band diagram along the surface of the TFET for (Vgs= 0, 0.4, 0.5, 0.6) in the ON-state.

Pinning and Ambipolar Behavior

Fig 1.4 demonstrates the exchange qualities of a TFET. The plot between Gate voltage to deplete Current give the exchange Characteristic. At a higher gate biasing, for example, Vgs>Vds, the rate of increment of current diminishes since the commitment of the extra introductory states in the source valence band is immaterial. As the gate predisposition approaches the channel potential, the rate of increment of current further reductions because of sticking. Because of this, the vitality groups in the channel don't essentially change with a

further increment in gate voltage. Thusly, the potential in the channel is said to be "stuck" to the channel potential. This marvel is called pinning of the channel potential.

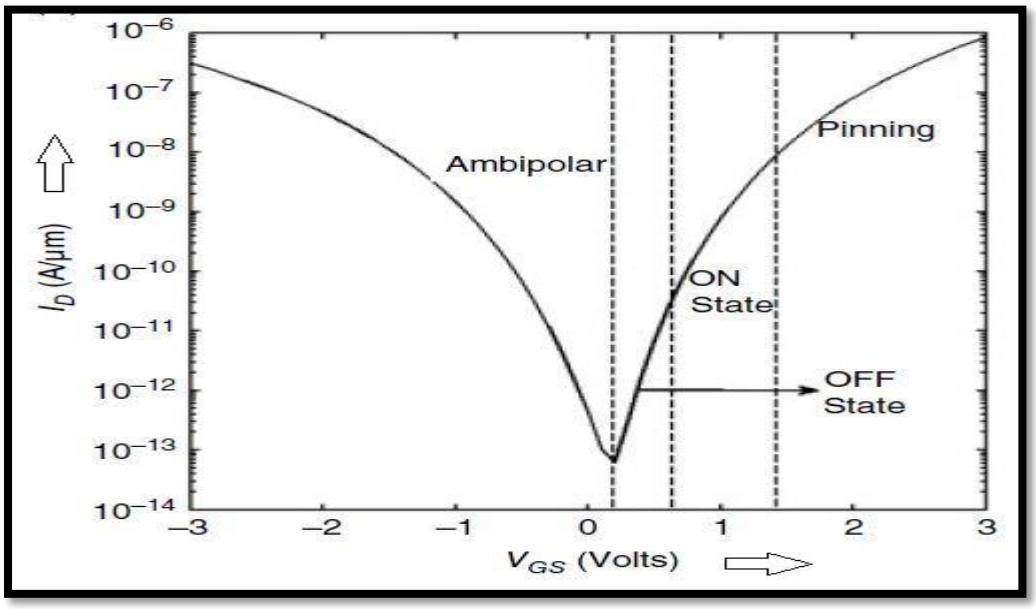

Fig1.4: Transfer characteristics (Ids–Vgs) of an n-channel TFET for a positive value of Vds showing different regions of operations.

Comparative conduct is seen in the negative predisposition area. As the gate voltage is diminished beneath 0 V, the valence band of the channel is lined up with the conduction band of the channel, and the electrons from the valence band of the channel can tunnel into the conduction band of the channel, bringing about a present stream. The electrons tunnel a similar way as on account of a positive gate predisposition. This outcome in the gadget current having a similar extremity even at a negative gate predisposition. Further increment in the negative gate bias causes a critical increment in the channel current this is because of two reasons (I) decrease of the tunnel length at the channel-drain junction and (ii) an expansion in the number of states in the channel valence band from where electrons can passage to the conduction band of the drain. This is called ambipolar conduction.

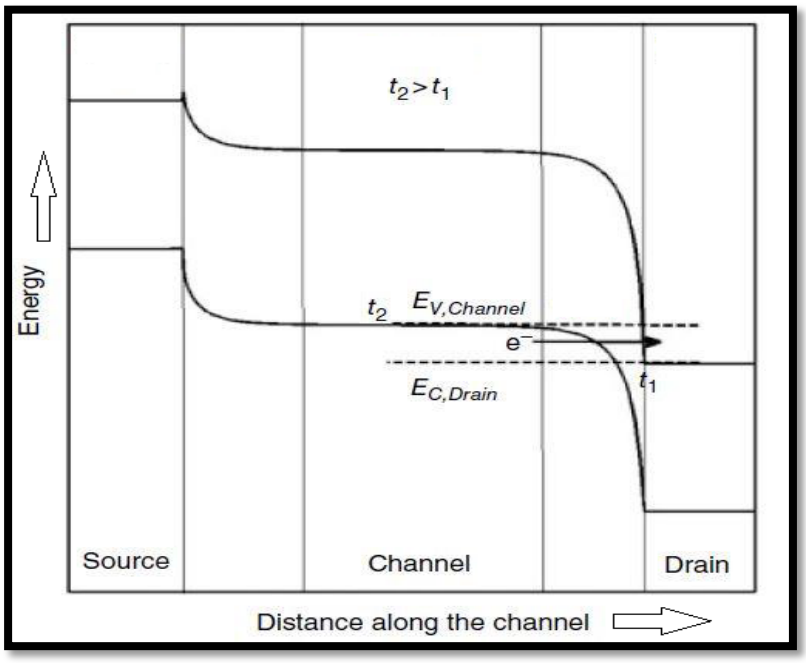

Fig1.5 : Band diagram along the surface of a TFET for a negative gate voltage (Vgs) and a positive drain voltage (Vds)

1.5 Double Gate TFETs

In an incorporated Double Gate Tunnel FET process, the TFETs will profit by the included entryways, with the end goal that the current will be at any rate multiplied or more. By including second gate, the ON-current is helped in Tunnel FETs, while the OFF-state current, increments by a similar factor yet remains amazingly low, it will be in the scope of pico amperes.[15]-[18].

1.6 Overview of TCAD Sentaurus Device Simulator

Computer Aided Design (TCAD) is a section of electronic design automation that models the semiconductor fabrication and the semiconductor device operation. [19]. This is a robust tool for reducing the design costs, improving the device design productivity and obtaining the better device and the technology designs. While the cost of building a state-of-the-art fabrication plant continues to go up, computing the power has become a relatively cheap product, due to Moore's law and the resulting improvements in the performance. Instead of going through an expensive and time-consuming fabrication process, the computer simulations can be used to predict the electrical characteristics of a device design quickly and

cheaply. Process modelling and simulation of the fabrication process, can be predicted so that physical characteristics such as the oxide thickness and the doping distribution can be produced with high precision. Device modelling and simulation can then be used to predict the electrical characteristics of the given device structure.

An important benefit of using TCAD is that it can help in understanding how semiconductor devices work. Assessment of detailed device operation, such as how the energy levels and the carrier (electrons and holes) distribution inside the device varies with the biasing conditions, can provide valuable insights into the relationship between a change in process conditions or device design and the resulting impact on the device performance. These quantities are often difficult to obtain experimentally. In contrast, they are readily available through computer simulations, which directly provide the feedback and guidance for device design.

A typical device tool flow the creation of a device structure by a process simulation (Sentaurus Process) followed by re-meshing. TCAD simulation tool is used to simulate the electrical characteristics of the device. It simulates numerically the electrical behaviour of a single semiconductor device in isolation or several physical devices combined in a circuit. Terminal currents, voltages, and charges are computed based on a set of physical device equations that describes the carrier distribution and the conduction mechanisms. Finally, Tecplot SV is used to visualize the output from the simulation in 2D and 3D, and Inspect is used to plot the electrical characteristics. TCAD has become a central part of semiconductor modelling and design. It is important to note that the accurate TCAD simulations and modelling of physical devices depend significantly on calibrated physical models and proper input data. The typical process flow for a device simulation using TCAD is shown in Fig 1.6 .

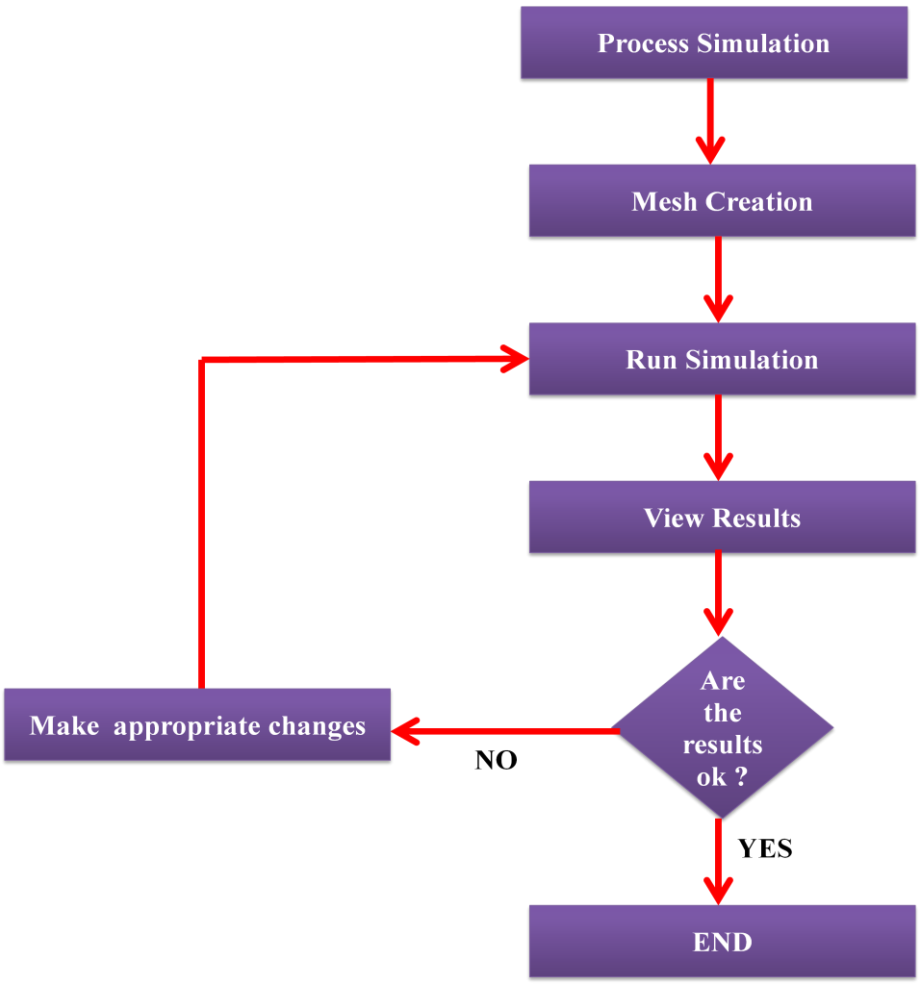

Fig1.6 : Process Flow of TCAD Simulation

TCAD Sentaurus Process is a complete and highly flexible, multidimensional, process modelling environment. With its modern software architecture, it constitutes a new tool generation and a solid base for process simulation. The main file types used in sentaurus process are:

- Sentaurus Process command file (* . cmd) - This file is the main input file for Sentaurus process. It contains all the process steps and can be edited. This file is referred to as the command file or input file.

- Log file (* . log) - This file is generated by sentaurus process during a run. It contains information about each processing step and the models and values of physical parameters used in it. The amount of information written to the log file can be controlled by certain parameters specified in the process command file.

- Structure file (has no extension) - This is the Sentaurus process internal format for saving the simulation. It contains the complete information about the geometry of the device and all datasets. Users can save the simulation in this format at points of interest or at the end of the simulation.

- TDR boundary file (*_bnd . tdr)- This Synopsys specific format stores the geometry of the device and is usually saved by the user at the end of the simulation. This file is used as input to the meshing engines and can be loaded into tecplot for viewing.

- TDR grid and doping file (*_fps . tdr)- This single file stores two kind of information. One is the information about the geometry of the device and the grid. The other is information about the distribution of doping and other datasets in the device. A TDR file can be reloaded into Sentaurus process to continue the simulation and can be loaded into tecplot for visualization.

  The typical tool flow of the device from process to plot is shown in Fig 1.7. A real semiconductor device, such as a transistor, is represented in the simulator as a 'virtual' device whose physical properties are discretized into a non-uniform 'grid' (or 'mesh') of nodes. A virtual device is an approximation of a real device. Continuous properties such as doping profiles are represented on a sparse mesh and, therefore, are only defined at a finite number of discrete points in space.

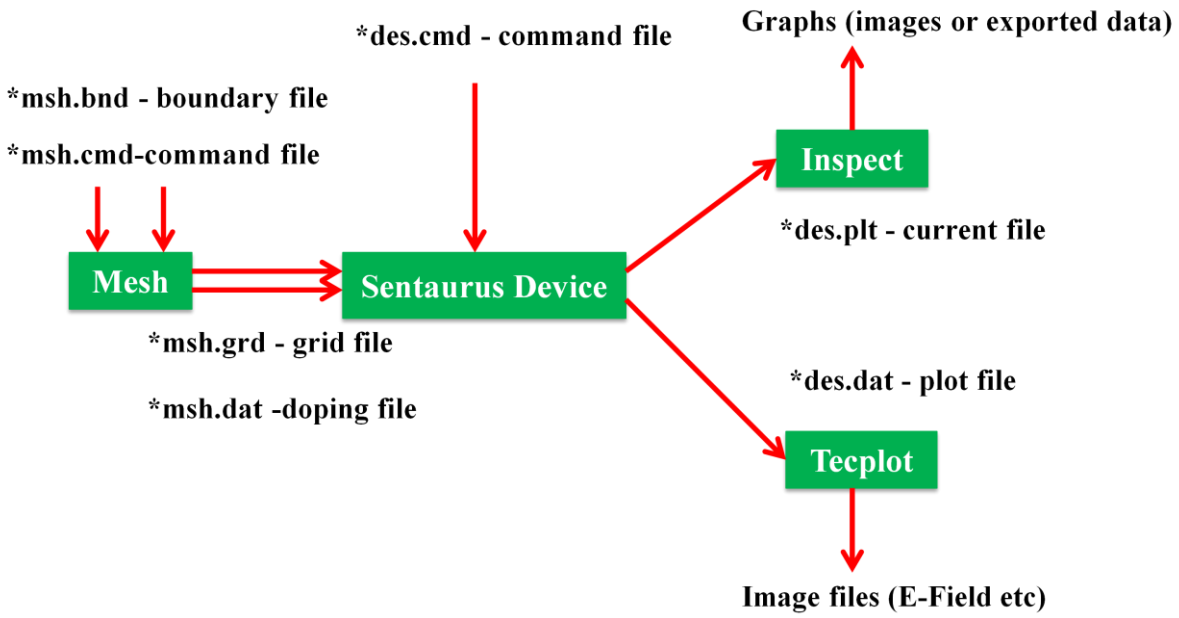

Fig1.7 : Tool flow with device simulation using Sentaurus Device

The doping at any point between nodes (or any physical quantity calculated by Sentaurus Device) can be obtained by interpolation. Each virtual device structure is described in the Synopsys TCAD tool suite by two files:

- The grid (or geometry) file contains a description of the various regions of the device, that is, boundaries, material types, and the locations of any electrical contacts. This file also contains the grid (the locations of all the discrete nodes and their connectivity).

- The data (or doping) file contains the properties of the device, such as the doping profiles, in the form of data associated with the discrete nodes.

1.7 Motivation of the present work

The major disadvantages of TFET are lower ON current and ambipolar current conduction. The motivation behind the present research work is to reduce these shortcomings of TFET [20]-[23].

Using Dual Source regions increases the effective tunnelling area resulting in the enhancement in the ON-Current [24]-[26]. Moreover, to suppress the effect of ambipolar current, we have used concept of Drain Splitting. In our proposed structure the highly doped region lies above the low doped region[27].

1.8 Thesis Organisation

The thesis is organized as shown below:-

Chapter 1 includes the limitations of MOSFETs, fundamentals of TFETs, overview of Synopsis Sentaurus TCAD and Thesis organisation.

Chapter 2 includes the background study of the present research work.

Chapter 3 deals with the Analytical Modelling and Simulation of DSTGSD-TFET

Chapter 4 includes the conclusion of dissertation and future scope of proposed model.

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Chapter 2

Literature Review

2.1 Introduction

Tunnelling field effect transistors (TFETs) otherwise named as steep subthreshold transistors have been the subject of intensive research because of their potential use in low power logic applications. The major advantage of tunnel transistors is the possibility to achieve less than 60 mV/decade sub- threshold swing, which is the thermionic limit in conventional MOSFETs. The working principle of TFET is based on the gate controlled band to band tunnelling in which electron tunnels into the unoccupied conduction band states of the channel from the occupied states of the valence band.

2.2 Background Research

In MOS devices, gate engineering techniques are usually employed to improve its characteristics as literature reveals. Increasing the number of gates and engineering the work functions of the gate material are some of the techniques employed so far.

Saxena et al. (2004) [1]-[3] developed a physics based analytical model for a Dual Material Gate (DMG) MOSFET using parabolic approximation method and showed suppression of hot carrier effect.

Chiang et al. (2008) [4] proposed a surface potential model for Dual Material Gate MOSFETs using superposition method. Syamal et al. (2010) [5] used Raphson method to derive the surface potential model for Double gate MOSFETs. Tiwari et al. (2010) [6] have developed a surface potential model for Triple material Double Gate MOSFET using parabolic approximation method. In spite of its desirable characteristics, Tunnel

FETs suffer from low ON current and so various techniques have been suggested in the literature to improve its ON current.

Rakhi Narang et al. (2014) [7]-[10]proposed a drain current model of Gate all around p-n-p-n tunnel FET. The impact of scaling radius R and t_{ox} on the device parameters have been discussed. The model depicts the influence of pocket doping and pocket width on the energy band profile of a p-n-p-n TFET.

Navjeet et al. (2015) [11]-[14] proposed an analytical model for tunnel barrier modulation in triple metal double gate tunnel FET. Three different metals over the channel region assist to form a barrier in the channel which restricts the reverse tunneling of the carrier, i.e., tunneling from drain to source. The choice of three metals with different work functions helps to increase the ON current and also to form a barrier in the channel, which reduces the OFF current. Till date work function engineering in a surrounding gate TFET has not been reported. Hence, Dual Material Surrounding Gate TFET and Triple Material Surrounding Gate TFET have been proposed in this dissertation. The analytical modelling of the proposed devices has been developed using the simpler parabolic approximation technique. The results obtained, are compared with the other existing models to prove the superiority of the new advanced structures in TFET.

Kim, Sang Wan, et al.(2012) [15] and Kim, Sang Wan, et al. (2015) [16], proposed a Si based L-shaped TFET which showed higher ON-current and lower Subthreshold Slope (SS) compared to the conventional TFET as L-shaped TFETs offer larger cross-sectional area for BTBT which occurs orthogonal to the channel direction.

Shaker, Ahmed, et al. (2017) [17] and B. Goswami et.al. (2018) [18]-[19] used the concept of splitted-drain region with different doping concentrations. Splitted-drain structures exhibit major reduction in ambipolar conduction due to increase in the tunneling width at the channel–drain junction. The simulated results of this new architecture shows improved current driving capability, high Ion/Ioff and reduced ambipolar conduction, making it suitable for low power applications.

Bagga, N., et al. (2017) [20]-[21] and Bagga, Navjeet, et al.(2017) [22], proposed a novel SOI based dual source region TFET structure which proved that by incorporating two source regions in the TFET structure, we can boost the ON current leading to the increment in the Ion/Ioff ratio which is approx. $9x10^{10}$. Also there is a noticiable

improvement in the subthreshold slope (Min SS = 30.92 mV/dec).

Woo, Sola, et al.(2019) [23] proposed a new design for covered source-channel tunnel FET (CSC-TFET) with trench gate structure. The proposed structure shows an ON/OFF ratio of approximately 10^{10} and ON current of approx. 10^{-5} A/μm at room temperature. Moreover this structure shows a subthreshold swing of less than 40mV/decade.

Padilla, J. L., et al. (2012) [24] , presented an approach to account for Quantum Confinement in tunnelling FET (TFETs) based on the use of a nonlocal band-to-band tunneling model for carrier injection along with a self-consistent Schrödinger–Poisson model. Padilla, José L., et al. (2012) [25]-[26], investigated the effects of including the quantum confinement on electrical parameters such as subthreshold swing and gate threshold voltage.

Vandenberghe, William G., et al. (2008) , Vandenberghe, William, et al. (2008) [27]-[28]and Verhulst, Anne S., et al. (2011) [29] derived an approximate analytical expression for a TFET structure where the gate is entirely on top of the source region by using Kane's Model.

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Chapter 3

Analytical Modelling and Simulation of Dual Source Trench Gate Split Drain TFET (DSTGSD TFET)

3.1 Introduction

For low power applications in the case of Metal Oxide Semiconductor Field Effect Transistors (MOSFET), supply voltage needs to be reduced. But when supply voltage is reduced ON-current reduces. Thus in order to maintain high ON current, the Subthreshold Swing (SS) needs to be lowered which in the case of a MOSFET is not possible to lower the value below 60mv/dec. Various devices have been proposed for the same. Among them Tunnel FET is the most promising candidate due to MOS (CMOS) process compatibility and scalability. Despite these superiority there exists two major issues related to TFET, lower ON-current and ambipolar current [1]. The goal of this work is to overcome major disadvantages of Tunnel FET (TFET) such as ambipolar conduction and lower ON current

A novel Dual Source Trench Gate Split Drain TFET (DSTGSD TFET) has been proposed and simulated using Synopsys Sentaurus TCAD. Using Dual Source regions and trench gates [2],[12]-[13] increases the effective tunnelling area resulting in the enhancement in the ON-Current. Moreover, to suppress the effect of ambipolar current, we have used concept of Drain Splitting [15]-[17]. In our proposed structure the highly doped region lies above the low doped region. By doing this the tunnelling width at Channel-Drain interface increases which in turn reduces the ambipolar current. Furthermore, in the proposed structure we have used trench gate. The advantages of trench gate TFET over conventional planer TFET is that trench gate TFET shows sharp ION to IOFF transition [13],[18] which implies lower subthreshold slope as compared to conventional planer TFET. Also, for the same value of Vgs trench gate structure shows higher ION in contrast to the planer TFET. Adding to this, the consequences of various device geometries has been discussed accordingly optimize and a comparison between the Conventional Planer TFET and Trench Gate TFET[13],[18] has been discussed to show the superiority of the latter. The concept of Quantum Confinement has been included [19]-[21] and a comparison of classical and Quantum mechanics on DSTGSD TFET has been studied.

For the DSTGSD-TFET structure a compact analytical expression for the ON-current is derived using the Kane's Model [4]-[8]. A comparison of the derived analytical expression with the results obtained from the 2D simulation are done and the analytical expression is found to be in good agreement with the result.

3.2 Device Description, Fabrication and Simulation Setup

The 2D cross sectional view of DSTGSD-TFET structure has been shown in Fig 3.1 . This is a n-type TFET. Thus the Sources are doped p+ which both the Drain regions are doped n+ The channel is lightly doped p-type. As shown in the figure, this structure has two source regions in the extreme top left and right corner of the structure (as shown in blue). At the bottom right corner we have two drain regions named as Drain 1 (highly doped, shown in deep green) and Drain 2 (lightly doped, shown in light green). There exists two trench gates (shown in yellow) on either side of the structure with SiO2 as their gate oxides (shown in red). Other than the gate oxide, there also exists three oxides regions (SiO2). In between these layers there exists a n-type Silicon layer which acts as the substrate and helps in transporting carriers. The fabrication steps for the DSTGSD-TFET

The various device parameters has been mentioned in Fig 3.1(b) and its impact is discussed in the section 3.4 . The optimized values of the respective doping concentrations are discussed latter.

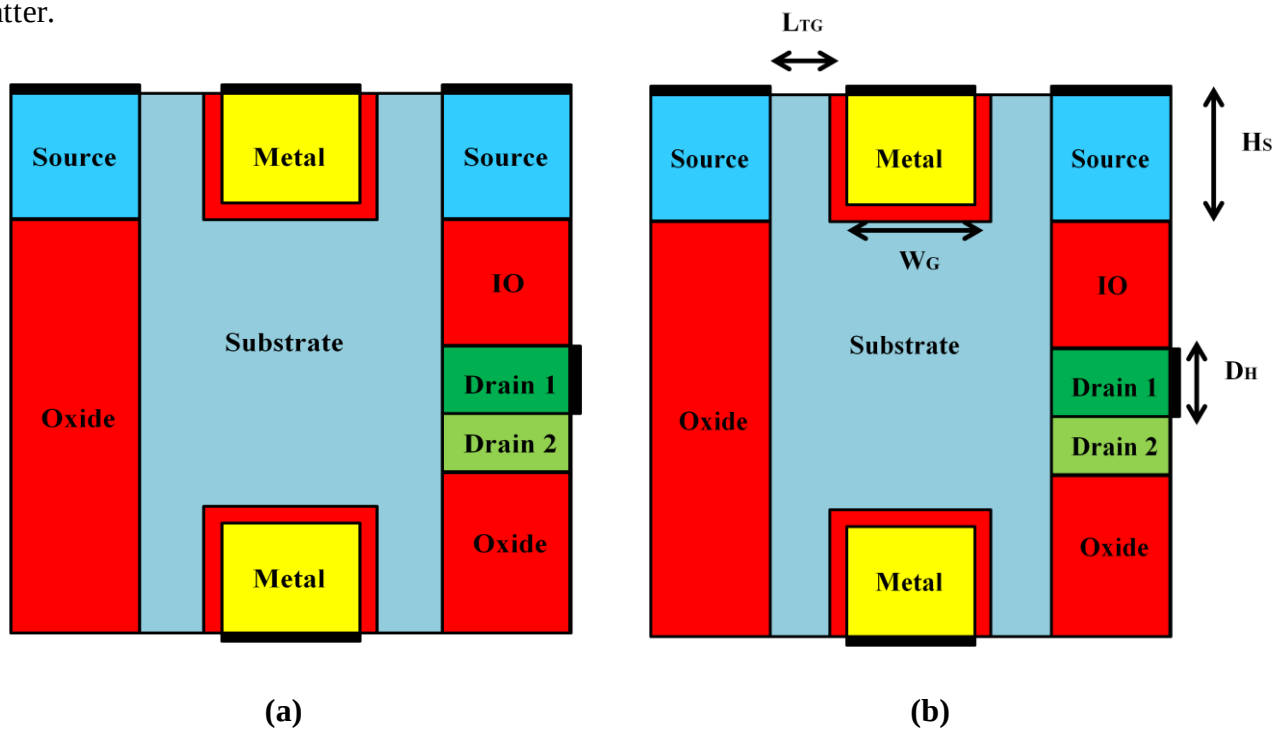
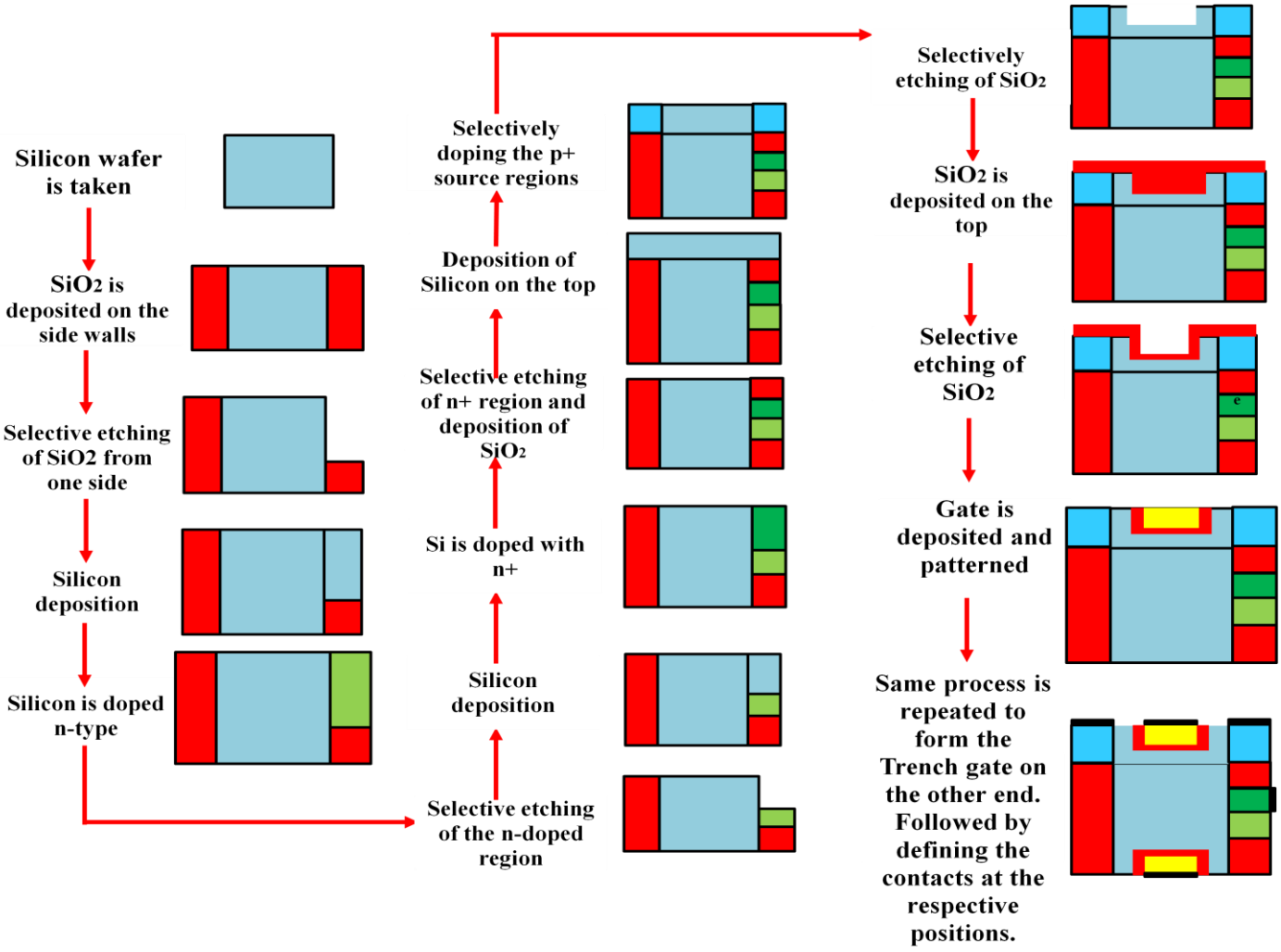


Fig 3.1: (a) DSTGSD TFET (b) Various device parameters affecting the operation of TFET.

3.2.1 Fabrication Steps of the DSTGSD-TFET Structure

It is a tedious job to explain the exact fabrication steps of such a complex structure like the DSTGSD-TFET. We have tried to explain the fabrication steps [1] in a simple manner which is as follows:-



3.2.2 Simulation Setup

Synopsys Sentaurus version G-2012.06 was used to perform all the simulations [3]. Appropriate mathematical models such as Lombardi Mobility Model, non-local BTBT model, Fermi Dirac Statistics, bandgap narrowing model, Auger and Schockley-Read Hall (SRH) recombination models and Drift Diffusion carrier Transport models were incorporated to take into account for the underlying device physics of the proposed DSTGSD-TFET. The non-local BTBT model calculates the carrier generation rate at the source-channel and channel-drain junctions. The carrier model, Fermi Dirac Statistics accounts for the carrier

concentration in order to state the mobility of the field. It accounts for the high carrier concentration statistics. To determine the carrier energy in the surrounding lattice and carrier lifetime, SRH and Auger recombination models have been used. In the latter part of the section 3.4, quantum confinement effect in the proposed structure has been studied. For the purpose of quantum simulation, the self-consistent Schrodinger-Poisson model has been used. The model accounts for the quantum mechanical effects under very low device dimensions.

3.3 Analytical Current Modelling of DSTGSD-TFET

In this section we have presented the analytical modelling of DSTGSD-TFET. As depicted in Fig 3.2 that BTBT occurs orthogonal to the trench gate. The 1D nature of BTBT helps in determining an approximate potential profile in the tunnelling region. To calculate tunnelling current, based on the electrostatic potential profile , three assumptions are made[4]-[8]:

1. the potential profile in the source-channel region is not affected by the drain voltage where tunnelling occurs,
2. no charges are present in the channel region and
3. no charges are present in the gate dielectric.

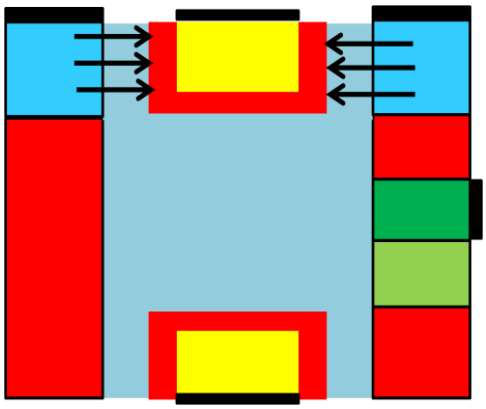


Fig3.2 : Direction of BTBT is as indicated by arrows

The process of tunnelling is explained with the help of Kane's model, which yields the generation rate per unit volume. G_{Kane} for the carriers tunnelling from valence to conduction band is given by:-

$$G_{Kane} = A_{Kane} \frac{E^{D}}{\sqrt{E_g}} \exp\left(-B_{Kane} E_g^{3/2} / E\right) \quad \text{.....(1)}$$

Where, A_{Kane} and B_{Kane} are the constants that are material dependant,

E_g = energy band gap

E = Local Electric Filed

D = is the parameter with which we can distinguish the direct (D=2) and indirect (D=2.5) tunnelling process.

The tunnelling current of a TFET is given by:-

$$I_{ds,tun} = q \int_{TFET\_Vol} G_{Kane} dV \quad \text{.....(2)}$$

Where q = unit charge and dV = 3D volume inside the TFET where the tunnelling either starts or ends.

Here we are not relying on the local Electric Field but instead we are inserting the average electric field in the Kane's generation rate.

The average Electric Field in the x-direction:-

$$E_{av} = \frac{E_g}{q l_{tun}} \quad \text{.....(3)}$$

Where l_{tun} = length of the tunnelling path.

Substituting eq. 1 in eq. 2 we get:-

$$\Rightarrow I_{ds,tun} = q \int_{TFET\_Vol} A_{Kane} \frac{E^D}{\sqrt{E_g}} \exp\left(-B_{Kane} E_g^{3/2} / E\right) dV \quad \text{..... (4)}$$

For a 1D average Electric Field eq.4 can be written as:-

$$\Rightarrow I_{ds,tun} = q \int_{TFET\_Vol} A_{Kane} \frac{E_{av}^{\ D}}{\sqrt{E_g}} \exp\left(-B_{Kane} E_g^{3/2} / E_{av}\right) dV \quad \text{..... (5)}$$

Substituting eq.3 in eq.5 we get:-

$$I_{ds,tun} = q \int_{TFET\_Vol} A_{Kane} \frac{E_g^{D-1/2}}{q^D l^D_{tun}} \exp(-B_{Kane} E_g^{1/2} q l_{tun}) dV \quad \text{.....(6)}$$

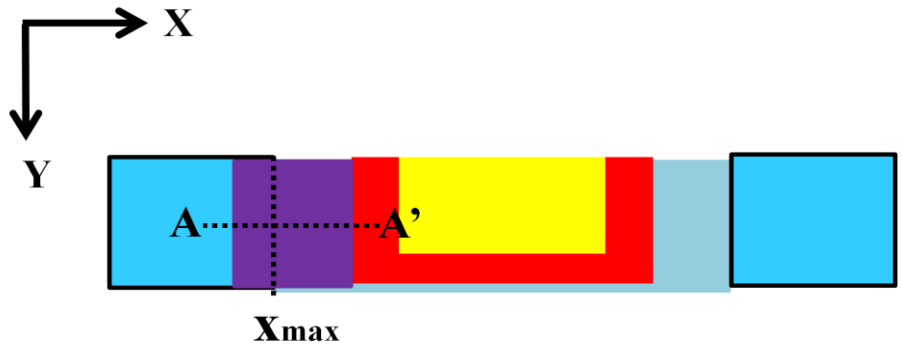


Fig3.3 : structure from Fig with positive gate bias applied such that a depletion region with thickness Xmax exists (only one half shown)

For the process of line tunnelling, we have assumed that there is no variation in electrostatic potential in the direction parallel to the gate. Hence the potential orthogonal to the gate dielectric determines the drive current.

Using the depletion layer approx. . as shown in Fig 3.3, the potential profile in the TFET in terms of source doping concentration N_S is given by:-

$$\phi = 0 \text{ for } x < x_{\max}$$

$$\phi = \frac{qN_S}{2\varepsilon_S}\left(x - x_{\max}\right)^2 \text{ for } x > x_{\max}$$

Where ϕ = electrostatic potential, ε_S = dielectric constant for the source, $x_{\max}$ = max. Length of the depletion region i.e where the depletion region starts in the source.

Now, l_{tun} of eq.3 can be calculated by considering two points (as depicted in Fig 3.4 of equal potential in valence and conduction band which are given as:-

$$\phi_V(x_1) = \frac{qN_S}{2\varepsilon_S}\left(x_1 - x_{\max}\right)^2 + \frac{E_g}{q} \quad \text{.....(7)}$$

$$\phi_C(x_2) = \frac{qN_S}{2\varepsilon_S}\left(x_2 - x_{\max}\right)^2 \quad \text{.....(8)}$$

Thus, $l_{tun} = x_1 - x_2$ ……(9)

and, $\phi_V(x_1) = \phi_C(x_2)$ ……(10)

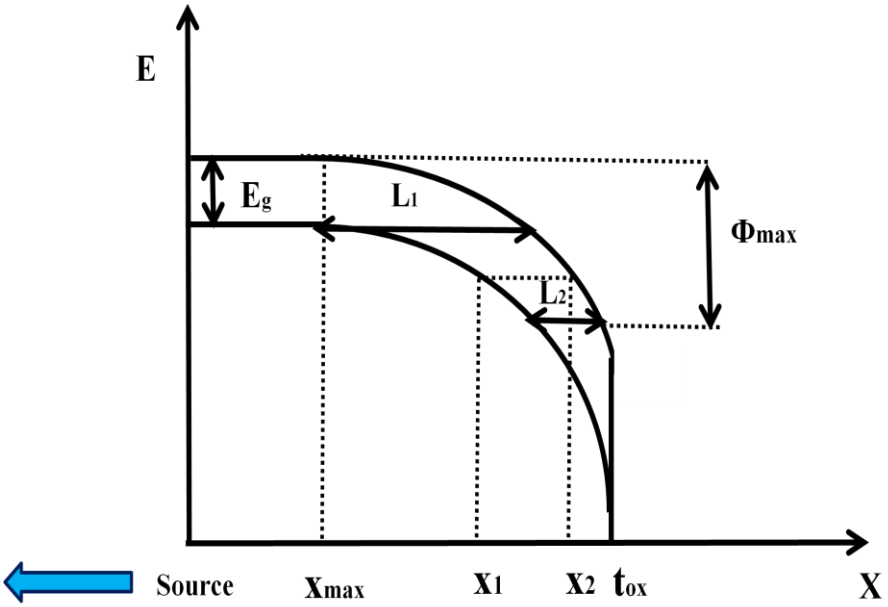


Fig 3.4: Band diagram of the cross-section A-A'

Now we can write x_2 in terms of l_{tun} by considering:-

$$\phi_V(x_1) = \phi_C(x_2)$$

$$\Rightarrow \frac{qN_S}{2\varepsilon_S}\left(x_1 - x_{\max}\right)^2 + \frac{E_g}{q} = \frac{qN_S}{2\varepsilon_S}\left(x_2 - x_{\max}\right)^2$$

$$\Rightarrow \left[\left(x_1 - x_{\max}\right)^2 - \left(x_2 - x_{\max}\right)^2\right] = -\frac{E_g}{q} \bullet \frac{2\varepsilon_S}{qN_S}$$

On expanding and cancelling $x_{\max}^2$ we get:-

$$\Rightarrow {x_1}^2 - {x_2}^2 - 2x_{\max}(x_1 - x_2) = \frac{-2E_g\varepsilon_S}{q^2N_S} \quad \text{.....(11)}$$

substituting eq. 9 in eq. 11 we get the following expression:-

$$x_2 = x_{\max} - \frac{1}{l_{tun}}\left[\frac{l^2_{tun}}{2} + \frac{E_g \varepsilon_S}{q^2 N_S}\right] \text{.....(12)}$$

Now, on rearranging and differentiating eq.12 we get:-

$$dx = \frac{-1}{2}\left[1 - \frac{2E_g \varepsilon_S}{q^2 N_S} \bullet \frac{1}{l_{tun}^{\ 2}}\right] dl_{tun} \text{ .....(13)}$$

Substituting eq.13 in eq.6 we get:-

$$I_{ds,tun} = \frac{qW_g L_{gs} A_{Kane}}{2} \int_{l_1}^{l_2} \frac{E_g^{\ D-0.5}}{q^D l_{tun}^D} e^{-B_{Kane} q \sqrt{E_g} l_{tun}} \left(1 - \frac{2E_g \varepsilon_S}{q^2 N_S} \bullet \frac{1}{l_{tun}^{\ 2}}\right) dl_{tun} \text{.....(14)}$$

Also, $l_1 = \sqrt{\frac{2E_g \varepsilon_S}{q^2 N_S}}$ .....(15)

$$l_2 = \sqrt{\frac{2\varepsilon_S}{qN_S}}\left[-\sqrt{\phi_{\max} - \frac{E_g}{q}} + \sqrt{\phi_{\max}}\right] \text{.....(16)}$$

And $\phi_{\max} = \left(-t_{ox,eff}\sqrt{\frac{qN_S}{2\varepsilon_S}} + \sqrt{t^2_{ox,eff}\frac{qN_S}{2\varepsilon_S} + (V_{gs} - V_{FB})}\right)$ .....(17)

Where l_1 and l_2 are the max and min length of tunnelling path,

$\phi_{\max}$ = electrostatic potential at the end of the depletion region,

L_{gs} = Overlap length between source-gate,

W_g = width of the gate,

$t_{ox,eff}$ = effective oxide thickness, $t_{ox,eff} = t_{ox}\frac{\varepsilon_S}{\varepsilon_{ox}}$, where ε_{ox} = dielectric constant of the oxide.

Finally the integral of eq.14 can be reduced to a formula by assuming that the exponential part is varying more rapidly as compared to the polynomial factors upon the l_{tun} variation.

Thus on approximating the integral, an expression for current can be found as;-

$$I_{ds,tun} \approx \frac{-A_{Kane} W_g L_{gs} E_g^{\,D-1.5}}{2q^{D-1} B_{Kane}} \left[H(l_2) - H(l_1) \right] \quad \text{.....(18)}$$

Also, $H(l) = C_1 \frac{1}{l^{D-1}} \left(1 - \frac{C_2}{l^2} \right) \exp\left(-C_3 l \right)$ .....(19)

Where, $C_1 = \frac{qN_S}{\varepsilon_S l_{tun}} \left(\frac{l^2_{tun}}{2} + \frac{E_g \varepsilon_S}{q^2 N_S} \right)$

$$C_2 = \frac{2E_g \varepsilon_S}{q^2 N_S}$$

and $C_3 = B_{Kane} q \sqrt{E_g}$.

Eq.18 provides an approximate ON-current due to line tunnelling in the TFET when the device parameters are known.

It is to be noted that for calculating the expression of tunnelling current, depletion layer only one side is considered. But a similar approach can be used to estimate the current for the other Source. The validation of the analytical modelling and simulated result for current is shown in the latter part of the section.

Thus for the DSTGSD-TFET structure, it is possible to obtain an analytical description for the potential profile. Using this profile and by adopting Kane's model we have derived the analytical expression for the Source-Channel interface i.e for the ON-current.

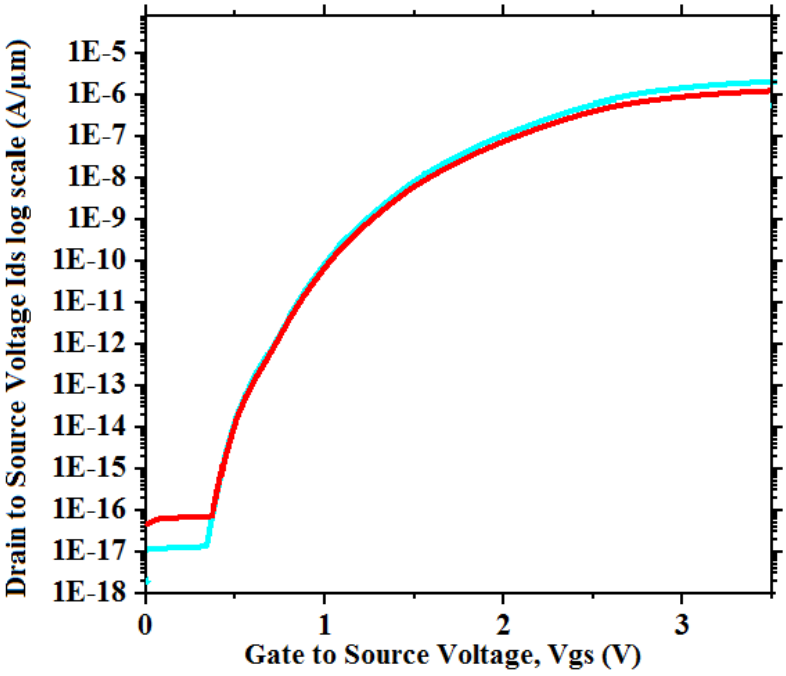
3.4 Simulation Results and Discussions

In this section we have discussed about the impact of various device parameters [2] on the functioning of the n-DSTGSD TFET.

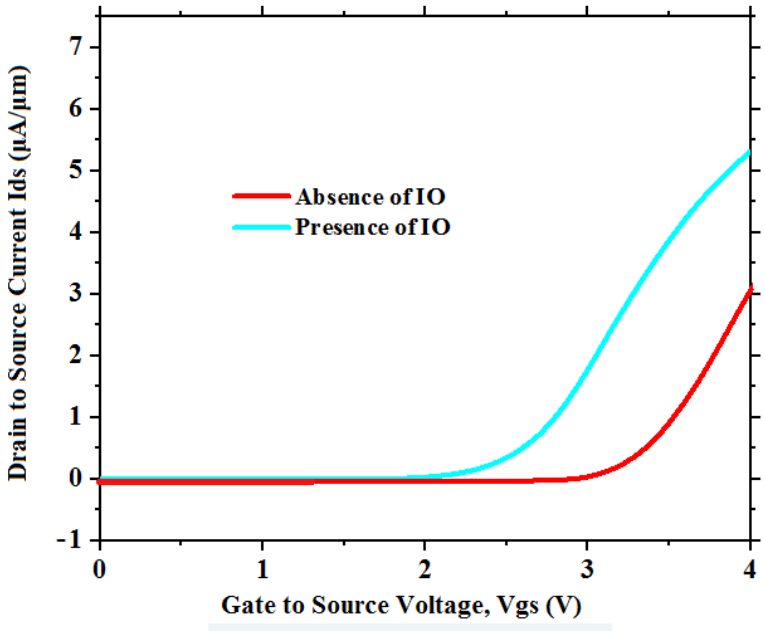
3.4.1 Impact of Isolator Oxide

In order to maintain a strategic distance from the immediate coupling among Source and Drain we have used an Isolator oxide (IO) [2],[9]-[11]. The existence and absence of IO has

been studied in this section and the transfer characteristics (both in Linear and Log scale) of the same has been shown in Fig 3.5. We see that in the absence of IO, the electric field lines from the drain will end at source which leads to lowering in the numbers of band to band tunnelling carriers thus resulting in decrease in the Ion/Ioff ratio as shown in the Fig 3.5.



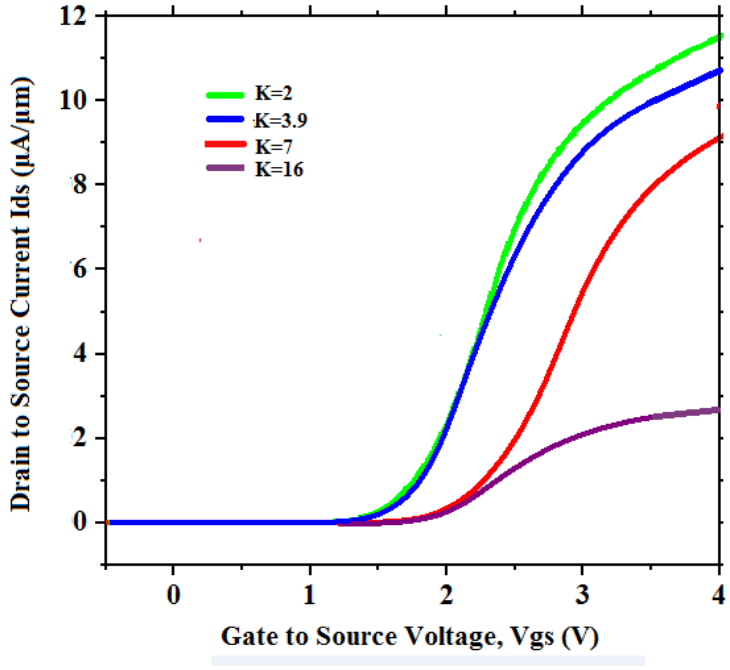
(a)



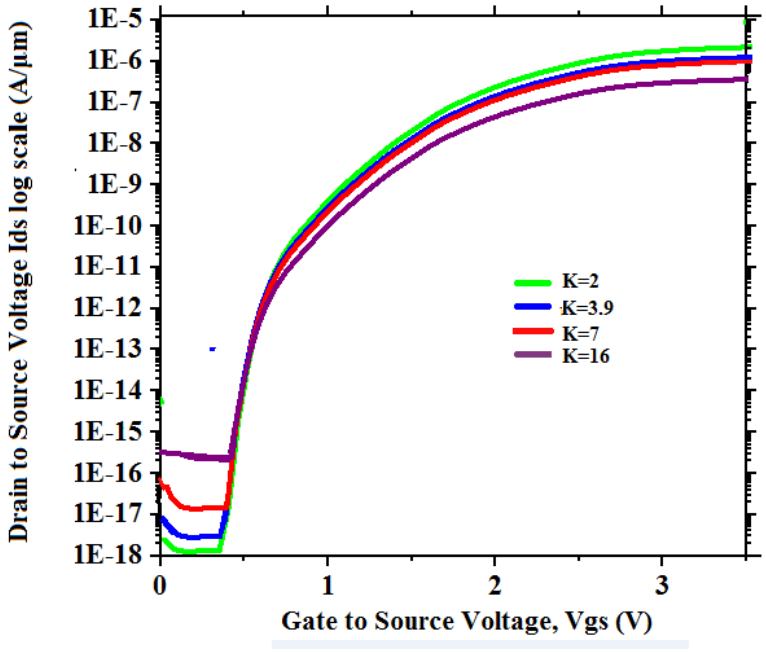
(b)

Fig3.5: Impact of the presence and absence of IO (a) Log scale (b) Linear Scale

We have also researched about the impact of various values of K on the IO that is shown in fig 10. According to the Fig 3.6, as the value of K increases the leakage current as a direct path is available between the source and drain region. Hence SiO2 is used as the IO which has permittivity value of 3.9.



(a)



(b)

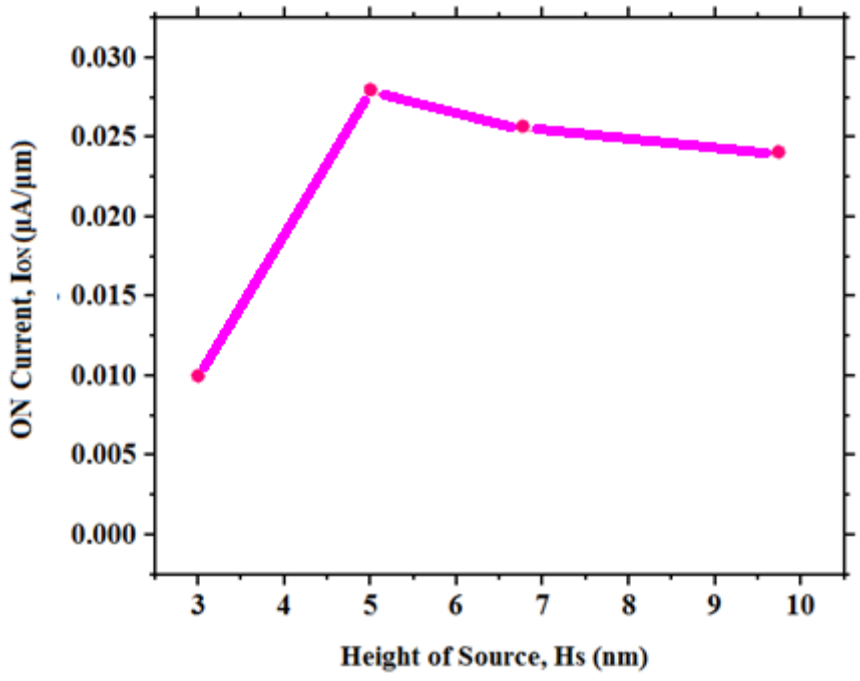
Fig3.6: Impact of increasing K value of IO (a) Linear scale (b) Linear Scale

3.4.2 Impact of Device Dimensions

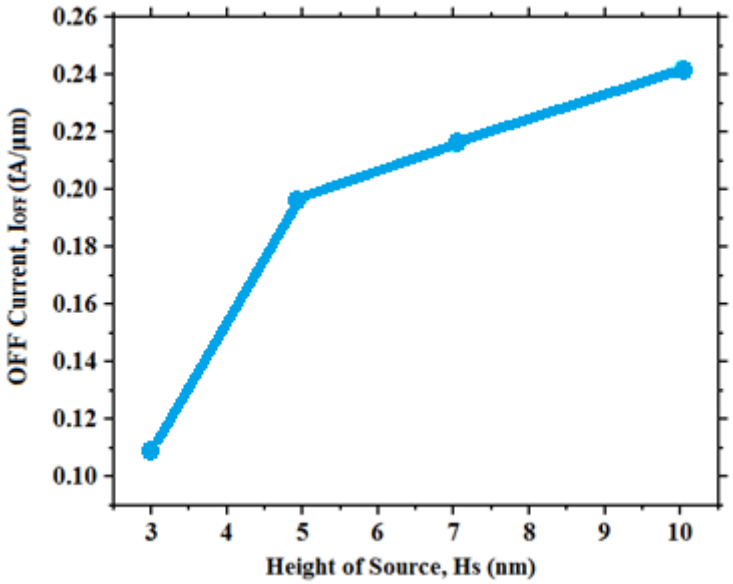
In this section we have addressed about the device dimensions that play a significant role in the operation of the device.

3.4.2.1 Source Height (Hs)

The Hs determines the tunnelling area i.e the overlap between the Sources and the channel region [1],[14]and consequently it determines the ON current. As we increase the value of Hs, the ON current increases linearly but after the value of Hs=5nm ON current increases sub linearly, as the channel resistance increases leading to an increment in the electric field lines in the tunnelling junction. Thus at higher values of Hs, the ON current saturates as seen in Fig 3.7(a). As the tunnelling area increases with the increase in Hs, the OFF current increases linearly with the increment in the value of Hs as presented in Fig 3.7(b). Hence the value chosen for Hs for the proposed structure is considered to be 5nm as at this value the ON current is high and beyond this value the OFF current increases.



(a)

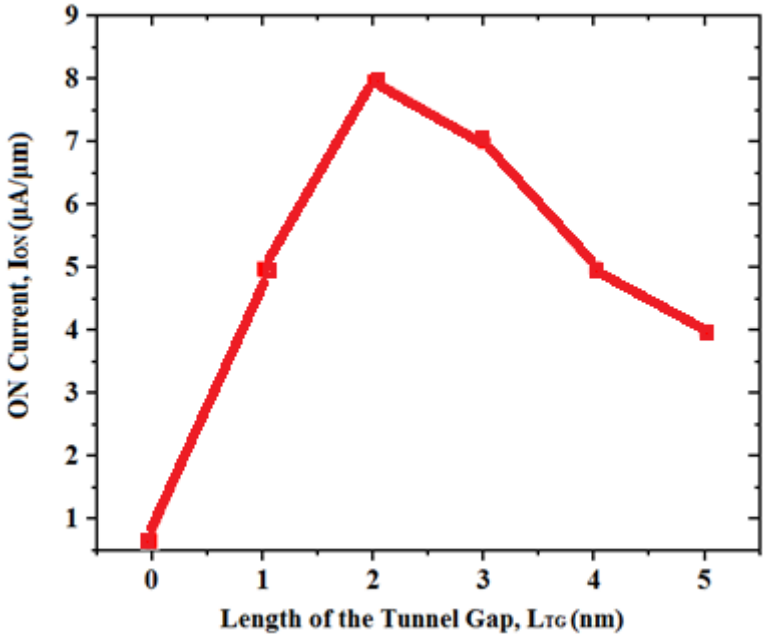


(b)

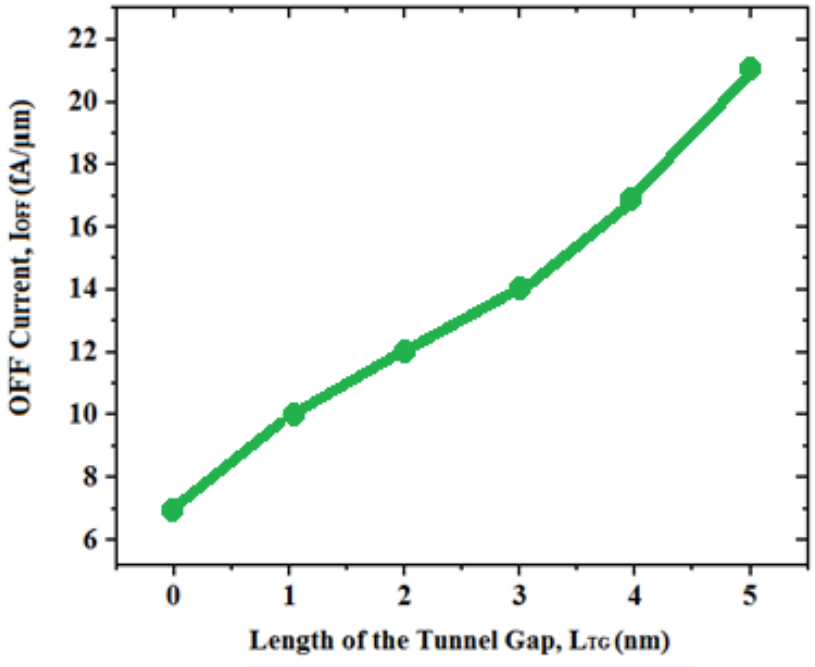
Fig3.7: Impact of increasing the source height on (a) ON current (b) OFF current

3.4.2.2 Length of the Tunnel Gap (LTG)

Length of the tunnel gap is also a significant parameter in deciding the tunnelling probability as the bending of the band is dependent on the value of LTG[1],[2]. For smaller values of LTG the band alignment is such that it does not initiate the tunnelling of carriers and hence there is low value for ON current as shown in Fig 3.8(a). As the value is LTG is increased, the band bending is appropriate to enable tunnelling of carriers. But it has been seen that for higher values of LTG (i.e LTG > 2nm), the ON current decreases as the Electric field decrements at the tunnelling area reducing the tunnelling probability. Also it can be inferred from Fig 3.8(b),that as BTBT increases the OFF current increases because here the diffusion current is progressively noticeable in contrast with the tunnelling current.



(a)



(b)

Fig3.8: Impact of increasing the gate width on (a) ON current (b) OFF current

3.4.2.3 Gate Width (W_G)

In this segment the variation in the width of the gate is examined [1],[2]. We see that as we decrease the value of W_G, there is an overlap between the source and drain depletion regions

leading to lower ON current. But as there is an increment in the value of W_G , ON current increases as shown in Fig 3.9.

Thus here we have considered the value of W_G to be 16nm as further increment of W_G increases the device size.

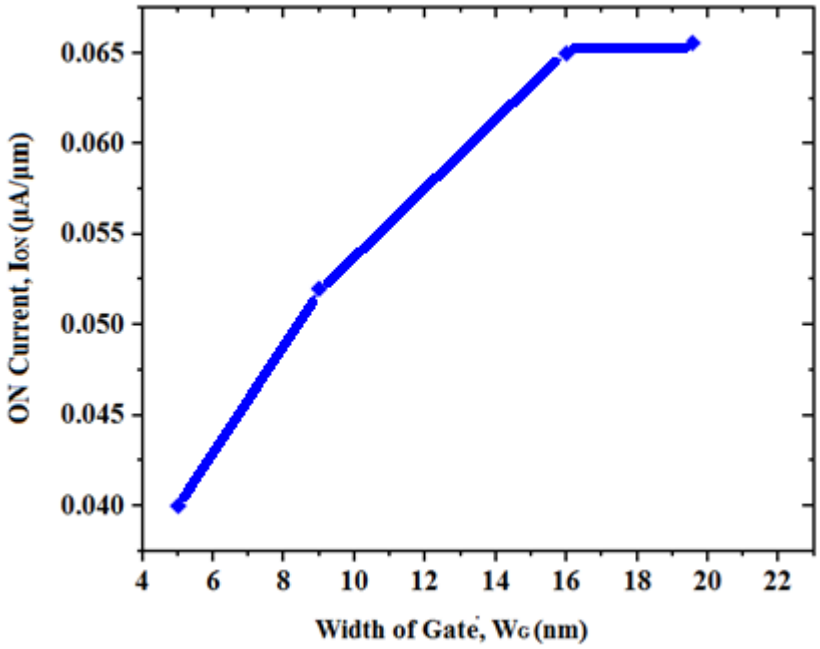


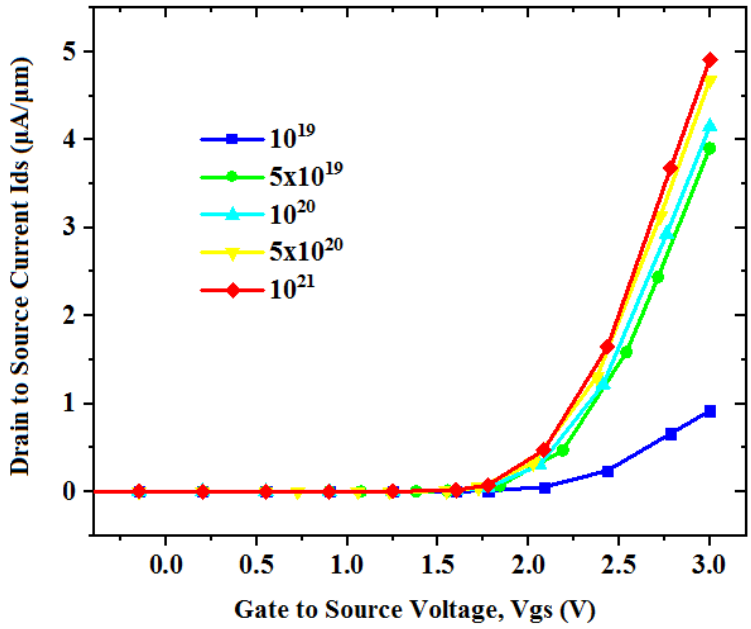
Fig3.9: Impact of increasing the gate width on the ON current

3.4.3 Impact of Doping Concentration

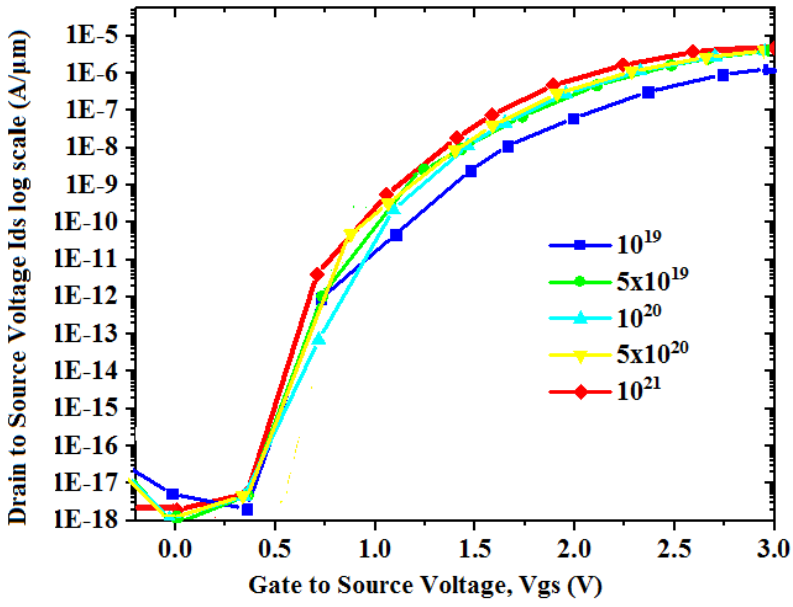
In this section we have examined about the effect of doping concentration on the device operation.

3.4.3.1 Source Doping

The role of source doping is more effective in case of line tunnelling rather than point tunnelling, as in the case of line tunnelling increment in the number of source dopants decreases the depletion layer formed at the source-channel junction [1]. The effect of increasing source doping concentration is shown in Fig 3.10. For our proposed structure the default value of source doping concentration is considered to be 5E21.



(a)



(b)

Fig3.10: Comparison of the transfer characteristics for various Source doping concentration in (a) Linear Scale (b) Log Scale.

3.4.3.2 Channel Doping

In our proposed structure channel is overlapped by the source region on both sides[1],[13]. On increasing the channel doping, the channel resistance decreases thus reducing the barrier

width. As a result of this the tunnelling probability near the Source- Channel junction increases, thus increasing the ON current. Also, the probability for the carriers near the Drain-Channel junction also increases. Consequently there is a increase in leakage current as depicted in Fig 3.11. For our structure, we have set the channel doping to be at 10^{15} /cm3 as this shows high ON current with low value for OFF current.

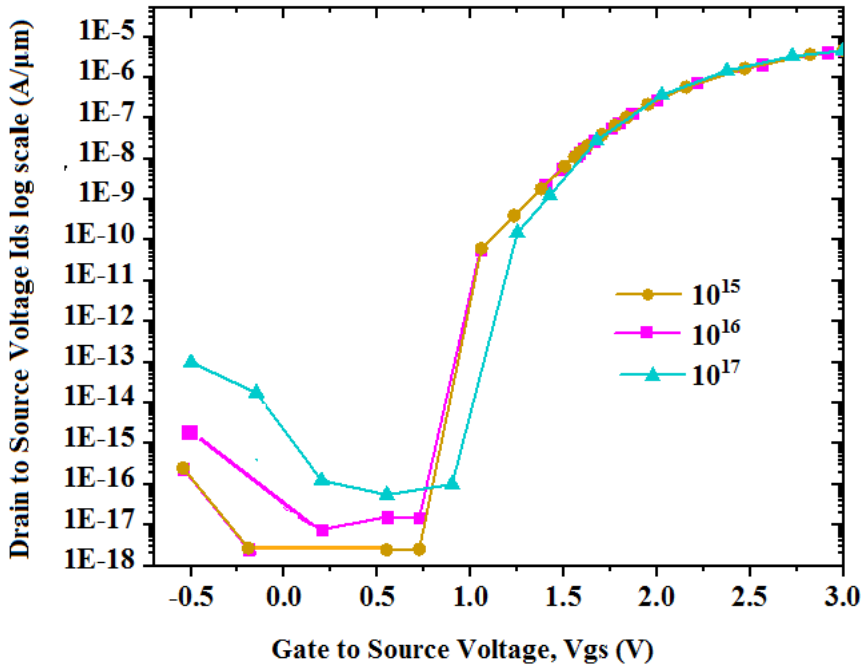


Fig3.11: Comparison of the transfer characteristics for various channel doping concentration.

3.4.4 Ambipolar Current

For our proposed structure we have used the concept of splitting the drain region into low doped and highly doped region, the highly doped on above the low doped one [15]-[17]. This concept helps in suppressing the ambipolar current without degrading the ON current.

Here we have shown two variations in the concept of drain splitting. We have split the drain once along the vertical axis and once along the horizontal axis which is as shown in Fig 3.12.

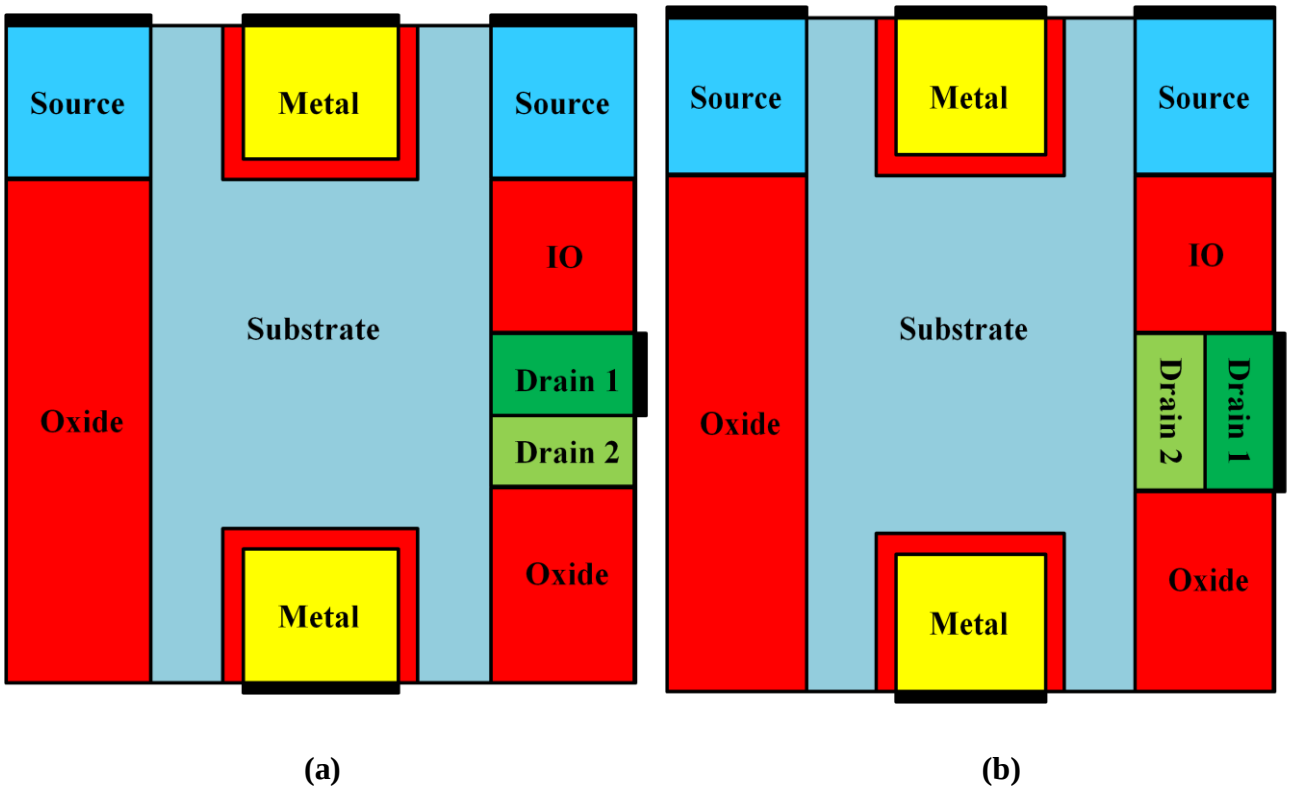


Fig3.12: (a) Horizontally split Drain TFET (b) Vertically split Drain TFET

A comparison of in the transfer characteristics of the vertically split, horizontally split and a convention drain TFET (with one drain region of constant doping) is made and shown in Fig 3.13. A conclusion can be drawn that for both vertically and horizontally split drain region we experience low ambipolarity compared to the conventional drain TFET structure. Thus for our further simulation purposes we have considered horizontally splitted drain TFET structure as this is easier to fabricate compared to the vertically splitted drain TFET structure.

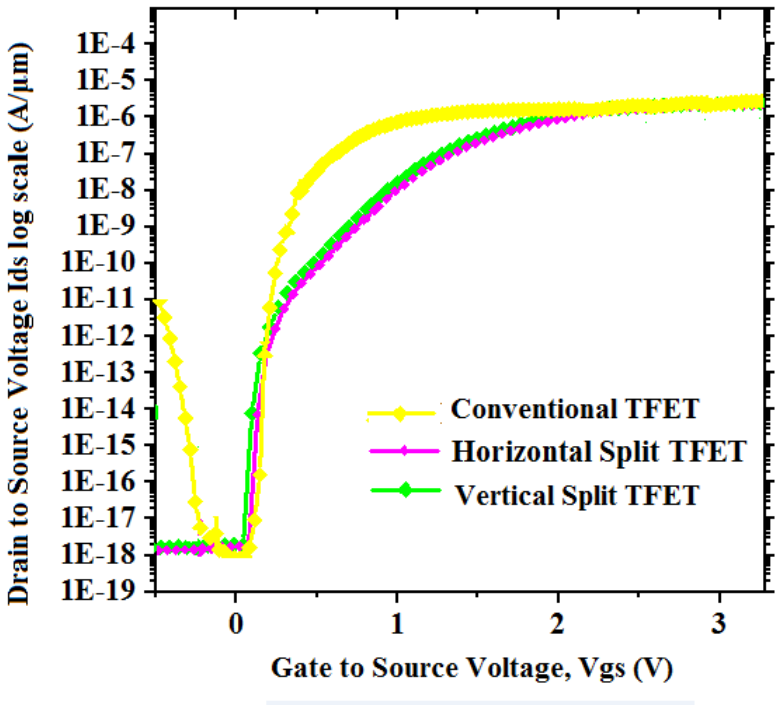


Fig3.13: Comparison of the transfer characteristics for Horizontally, Vertically Split and Conventional Drain TFET.

Also as shown in Fig 3.14, we have made a comparison in the transfer characteristics with different values of the height of the highly doped drain region (D_H) [15]. We conclude that the ambipolarity depends on the height of the heavily doped region. As seen from fig leakage current is eliminated upto Vgs = -0.5 V. Thus we consider the value of D_H to be 5nm for our further simulations.

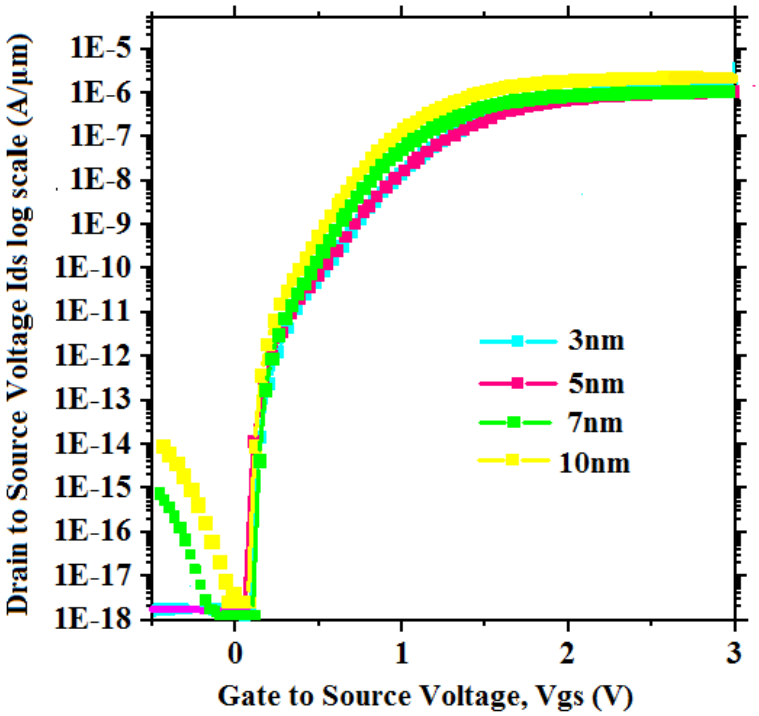


Fig3.14: Comparison of the transfer characteristics for various D_H values.

3.4.5 Impact of Variation in V_{DS}

The applied gate bias have an impact on the tunnelling of carriers from source to the channel region [1],[18]. The transfer characteristics is as shown in Fig 3.15. We can see that the drain bias has a significant impact on the drive and leakage current. Fig 3.16 explains the impact of increasing Vds and we can infer that as the drain current increases the ON current increases because of the diminishing tunnelling width. Also we can infer that as the vds is increased to a higher value the tunnelling probability increases which in turn increases the leakage current. In the Fig 3.16 we have shown the effect of increasing the value Vgs for a fixed value of vds and we can conclude that as vgs is increased, the barrier width decreases thus increasing the probability of band to band tunnelling.

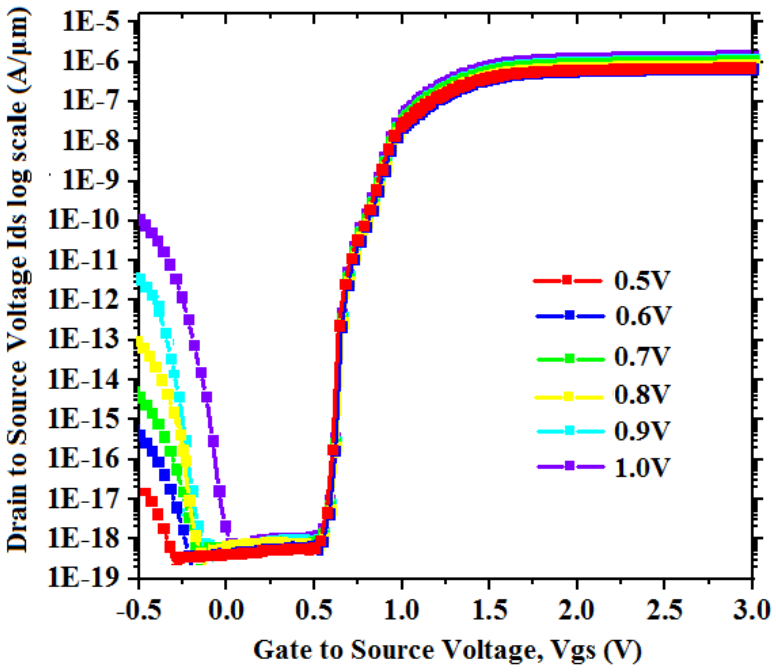


Fig3.15: Transfer Characteristics for various values of Vds

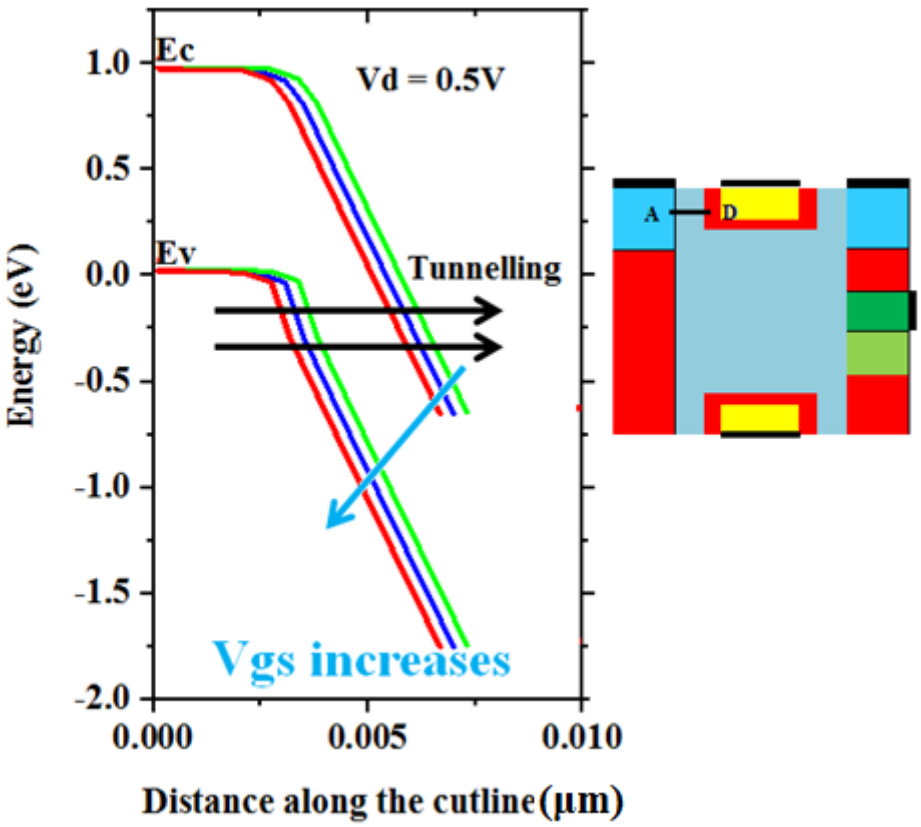


Fig3.16: Energy band diagram variation for various values of Vgs along the cutline AD for a fixed value of Vds

Thus for our proposed structure we have considered the value of vds to be 0.5V as we get the same ON current with low ambipolar current.

3.4.6. Impact of Trench Gate TFET

In our proposed structure we have used trench gate as shown in the Fig 3.1. The advantages of Trench gate TFET over conventional planer TFET is that trench gate TFET shows sharp ION to IOFF transition [13],[18] which implies lower subthreshold slope as compared to conventional planer TFET. Also, for the same value of Vgs trench gate structure shows higher ION in contrast to the planer TFET.

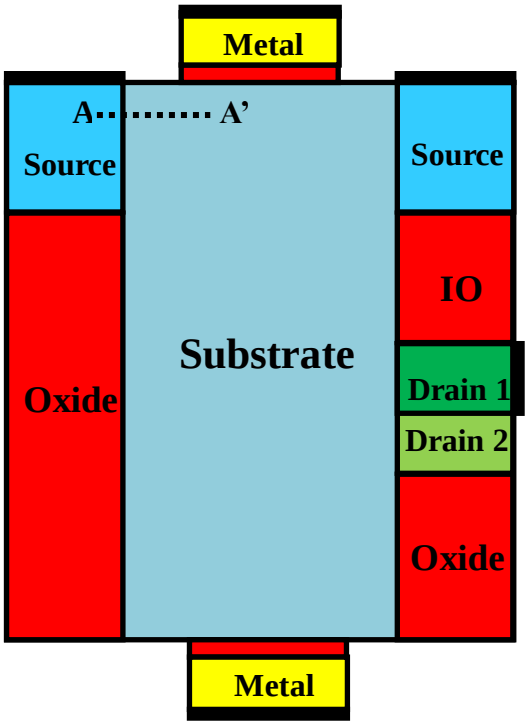


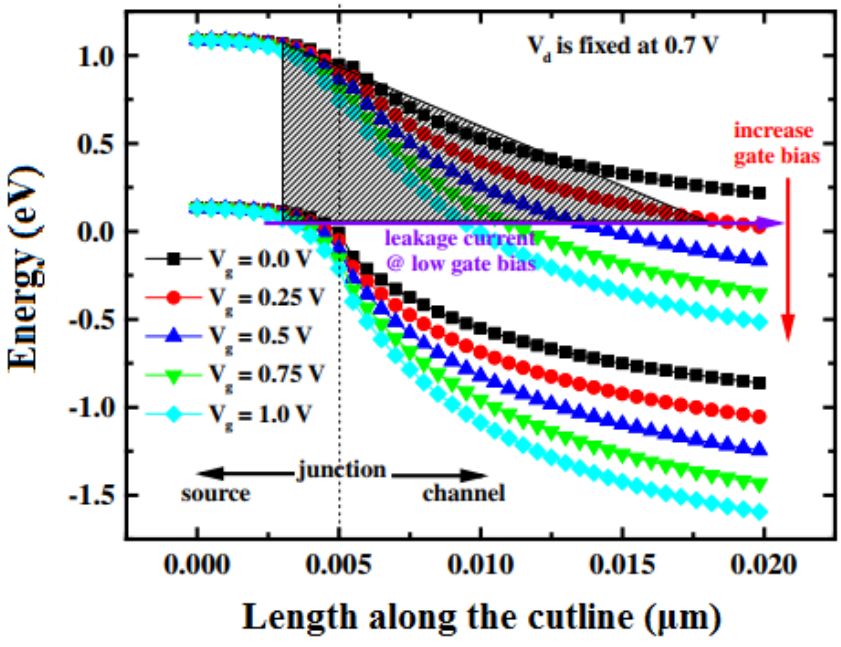
Fig3.17: Conventional Planer TFET

The Fig 3.17 shows the conventional planer TFET.

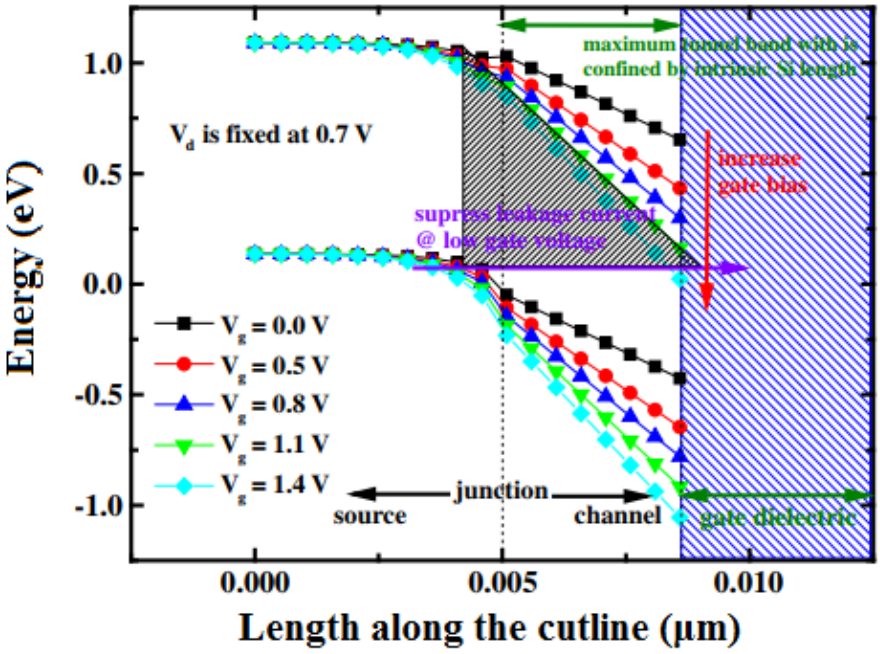
For the process of band to band tunnelling to occur to conditions needs to be satisfied:-

1. The valence band of the source side should be in alignment with the conduction band of the channel.
2. As the tunnelling probability depends on the tunnelling width, thus the tunnelling width should be smaller.

This is discussed with the help of the energy band diagram as shown in Fig 3.18.



(a)



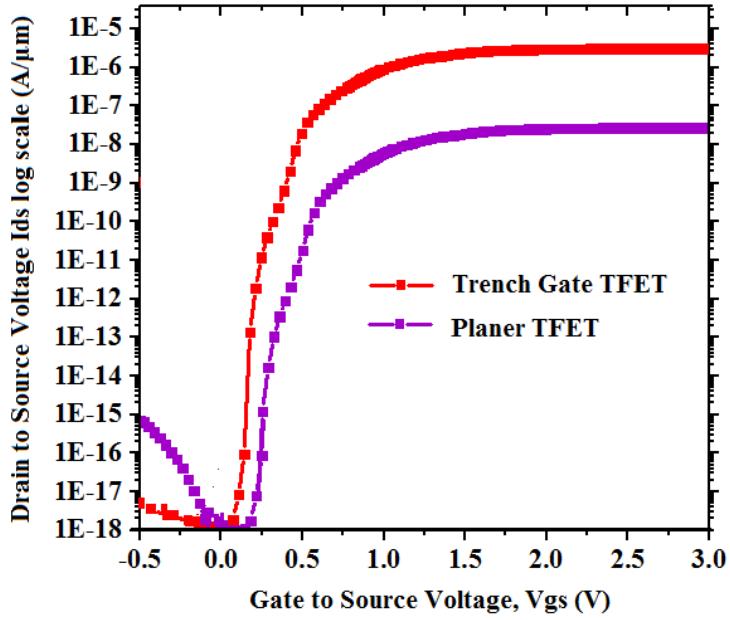
(b)

Fig3.18: Energy band diagram at various Vgs for (a) Planer TFET (b) Trench Gate TFET

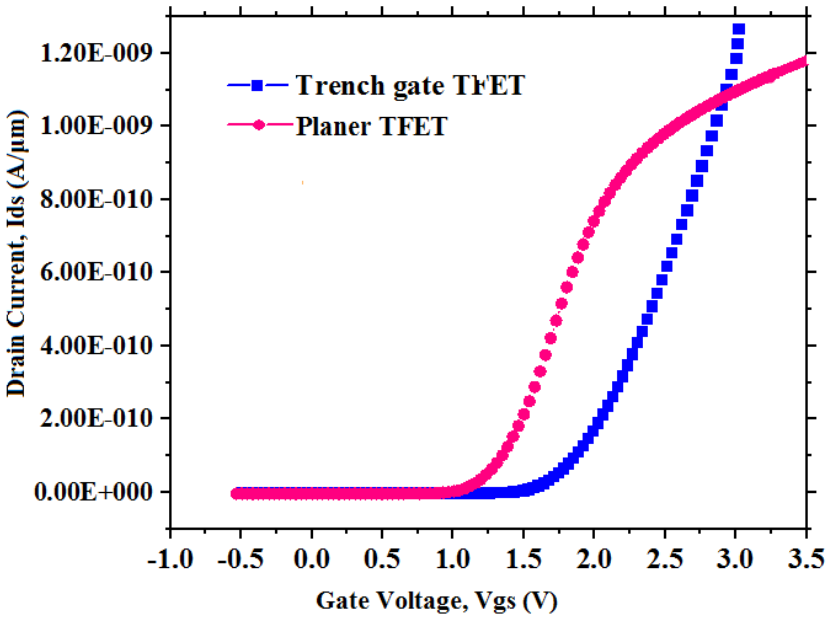
For the conventional planer TFET, we can see that the tunnelling width depends on the value of Vgs. At low values of Vgs, even though the Ev of the source is aligned with the Ec of the Channel, but due to the presence of higher tunnelling width the ON/OFF transition in tunnelling current in is gradual leading to an increase in the subthreshold slope value.

On the other hand, for the case of Trench gate TFET, once Ev of the source region is aligned with the EC of the Channel region the tunnelling width is fixed at length of the tunnel gap (LTG). This means that the tunnelling width can be controlled by the fabrication process and not by electrical biasing. Thus at low values of Vgs, even though the tunnelling width is small, the On current is low as the Ev and Ec are not properly aligned. Thus increasing Vg results in lower value of subthreshold slope for trench gate TFET compared to conventional gate TFET.

The Fig 3.19 shows a comparison of the transfer characteristics of Planer and Trench gate TFET in linear and Log scale.



(a)



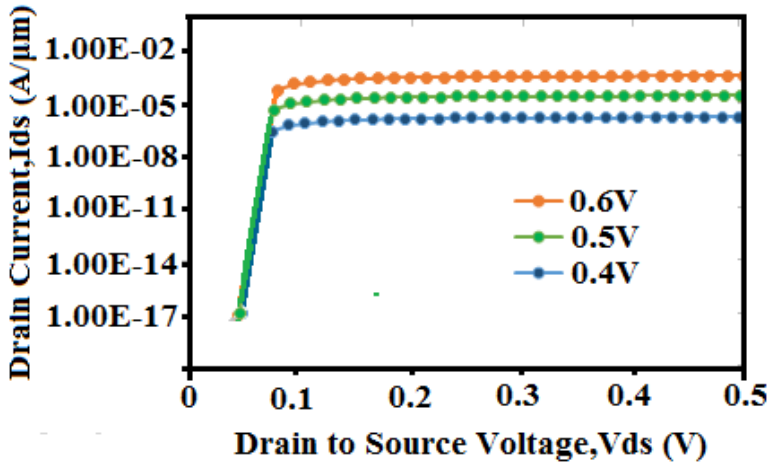
(b)

Fig3.19: The transfer characteristics of Planer and Trench gate TFET in (a) Log scale (b) Linear scale.

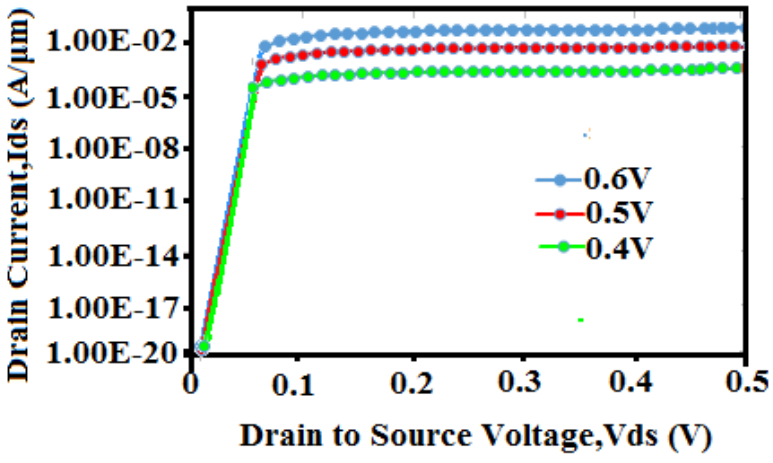
Fig 3.20 shows the output characteristics of both conventional Planer TFET and DSTGSD-TFET for gate bias voltage of 0.4V, 0.5V, 0.6V. The drain Voltage V_{ds} is swept up to 0.5V. The On and Off current is evaluated and compared for both the structures for optimal biasing

range of V_{ds} up to 0.5V and a comparison for the device characteristics for both structures are plotted and shown in Fig 3.21.

From the graphs below, it can be observed that the Dual Source Trench gate Split Drain Structure has a high ON current due to increase in the effective tunnelling area as a result of dual source and trench gate. Also this structure has recorded very low OFF current, starting from1×10^{-20}A, indicating minimum leakage compared to other conventional planer TFET, where Ioff starts around in the range of 1×10^{-17} A. Therefore, the proposed structure has lower OFF current as clear from the transfer function without hampering the ON current than that of planar TFET, resulting in a relatively higher Ion/Ioff ratio than conventional TFET.



(a)



(b)

Fig3.20: Output Characteristics for V_{gs} = 0.4V, 0.5V, 0.6V for (a) Planer TFET, (b) Trench Gate TFET

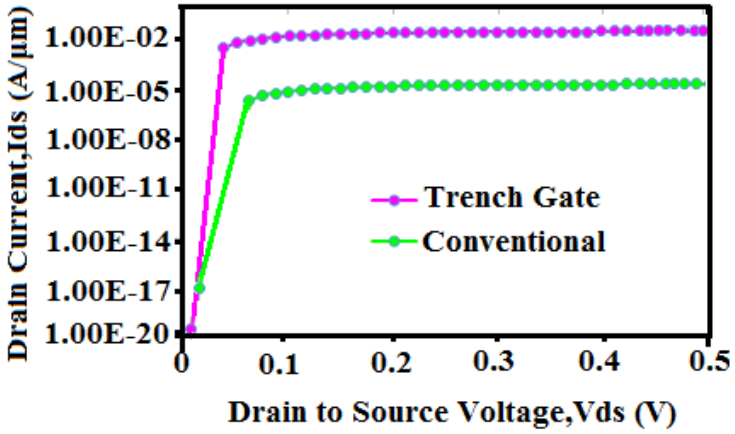


Fig3.21: Output Characteristics comparison for Conventional Planer TFET and Trench Gate TFET

Now as we know that since there is a gradual increase in current for Planer TFET hence its SS is lower in contrast to the SS for Trench gate TFET where there is a sudden transition in current. A comparison of the ION/IOFF ratio and SS are shown in Fig 3.22 and 3.23 respectively.

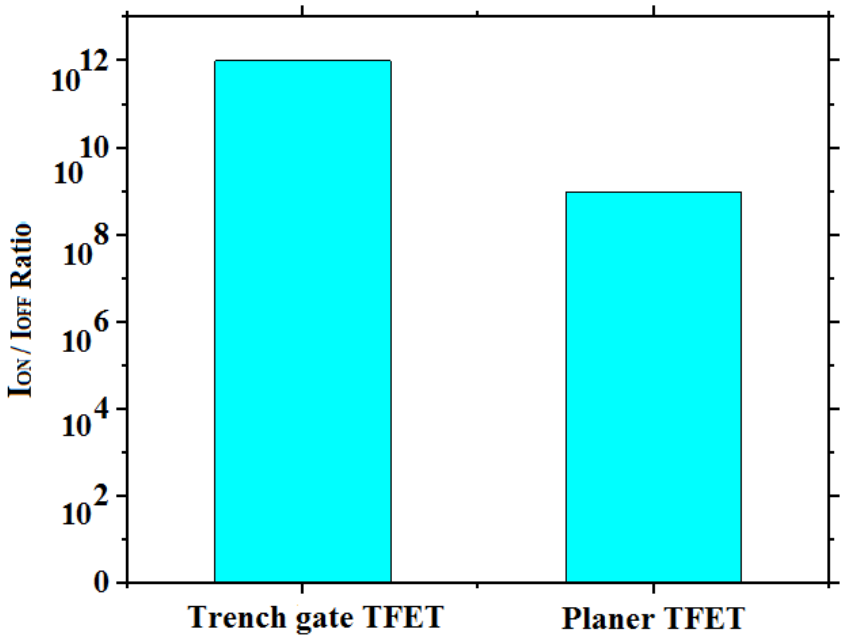


Fig3.22: ION/IOFF comparison for Trench gate and Planer TFET

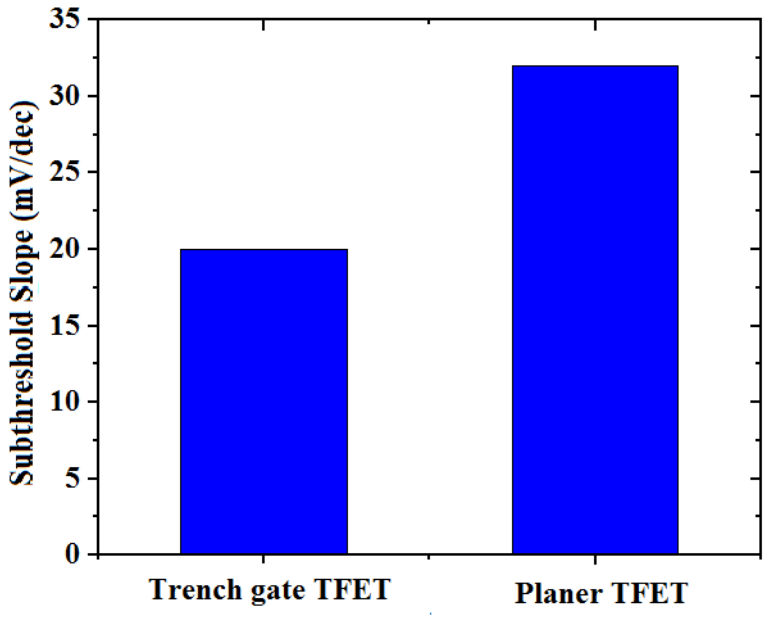


Fig3.23: SS comparison for Trench gate and Planer TFET

From the bar graphs we can conclude that the Ion/Ioff ratio (and SS) are 10^{12} and 10^{9} (and 21mV/dec and 34mV/dec) for Trench gate and Planer TFET respectively.

3.4.7 Optimized DSTGSD TFET

Parameter	Value	Unit
Vds	0.5	Volt
Hs	7	nm
LTG	3	nm
Gate width	16	nm
Source Doping	1E21	$/cm^3$
Channel Doping	1E15	$/cm^3$
Permittivity of IO	3.9	-

In this segment we have tabulated the optimized value of various parameters that play an important role in the functioning of TFET.

The transfer Characteristics and Output Characteristics Curve of the optimized DSTGSD-TFET is as depicted in Fig 3.24 and 3.25 respectively.

Fig 3.26 shows the contour diagrams for Electric field, electrostatic potential, electron tunnelling rate. Also the electric field, electrostatic potential and energy band diagram along the cutline AB has been shown in Fig 3.27.

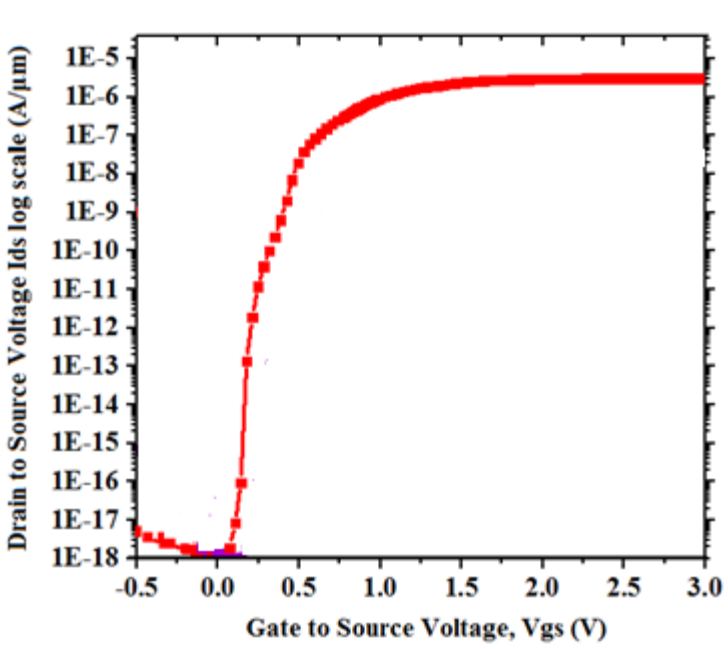


Fig3.24: Transfer Characteristics of Optimized DSTGSD-TFET

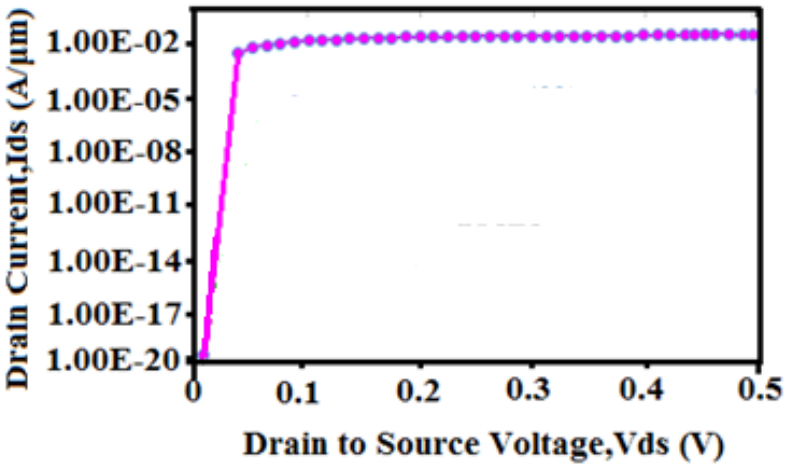
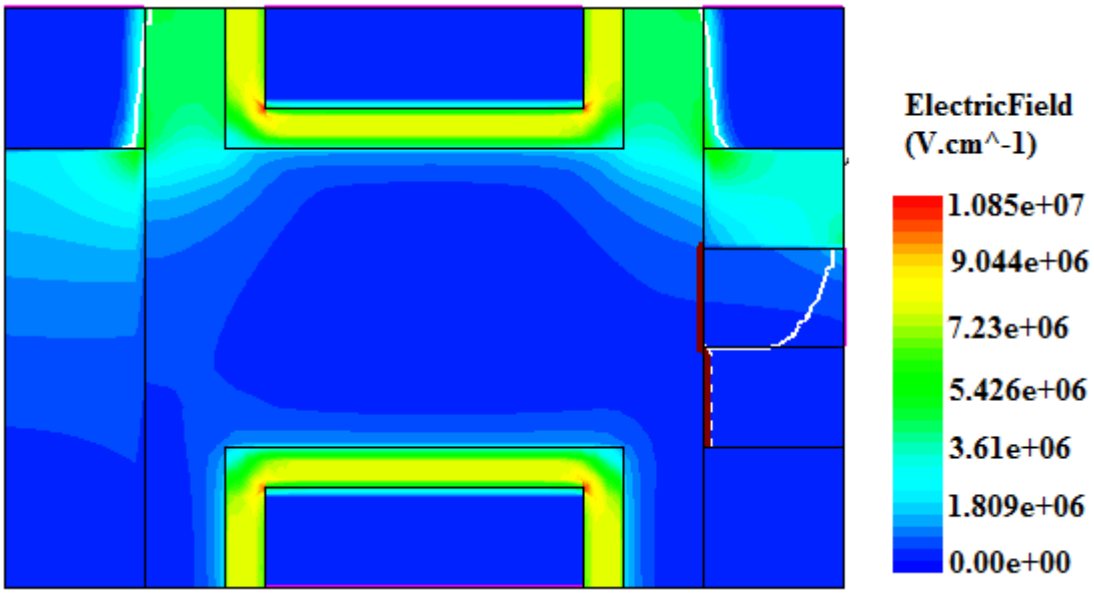
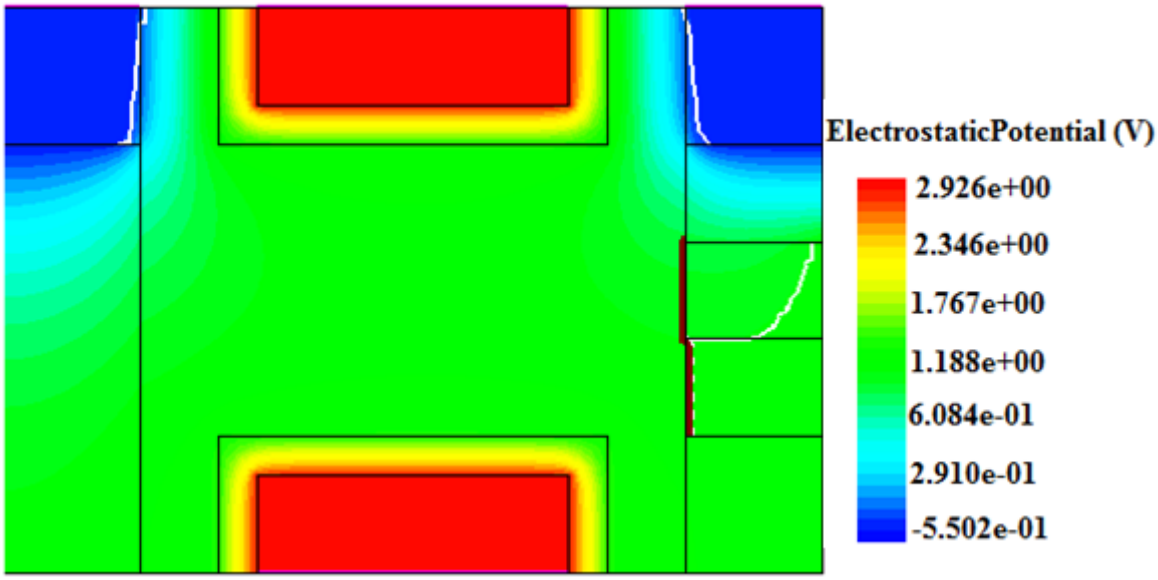


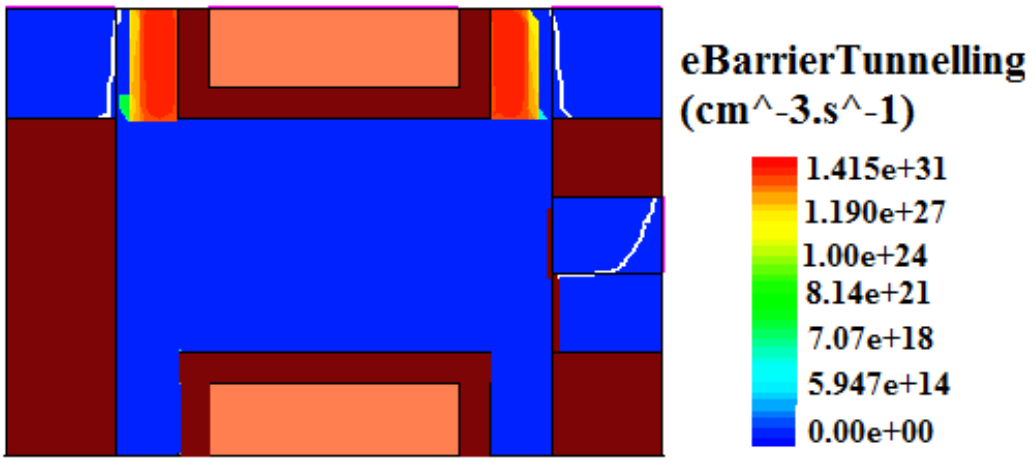
Fig3.25: Output Characteristics of Optimized DSTGSD-TFET


ElectricField
(V.cm^-1)
1.085e+07
9.044e+06
7.23e+06
5.426e+06
3.61e+06
1.809e+06
0.00e+00

(a)

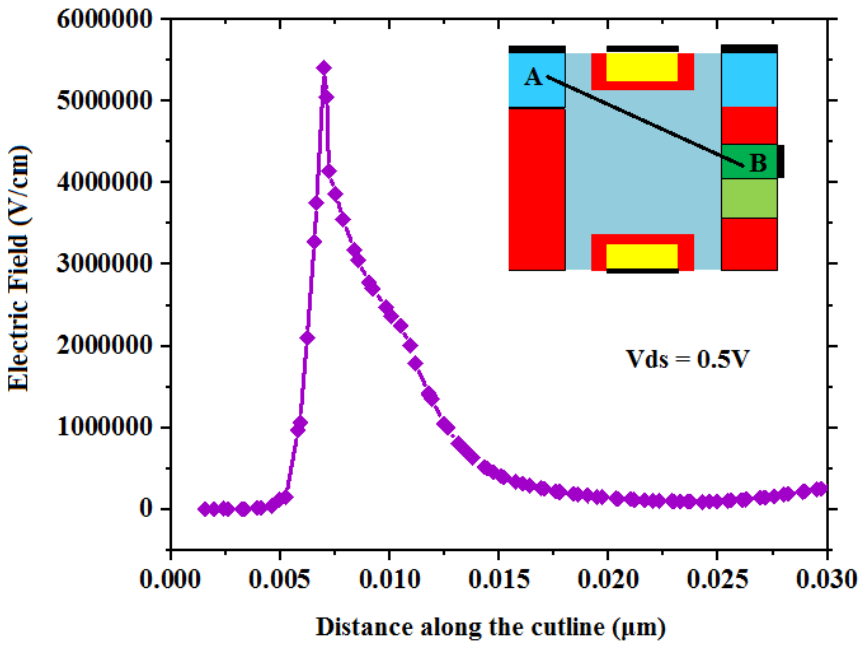

ElectrostaticPotential (V)
2.926e+00
2.346e+00
1.767e+00
1.188e+00
6.084e-01
2.910e-01
-5.502e-01

(b)

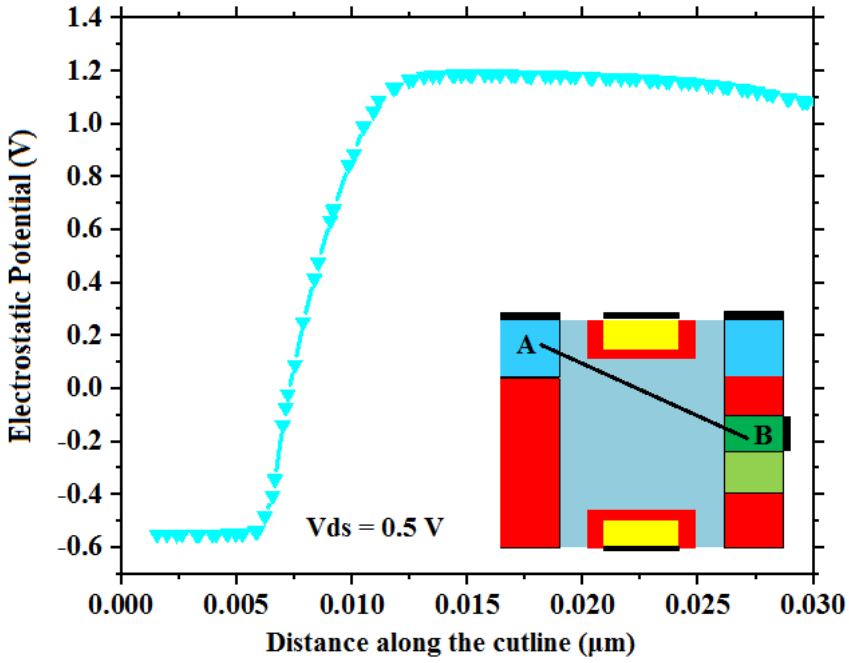


(c)

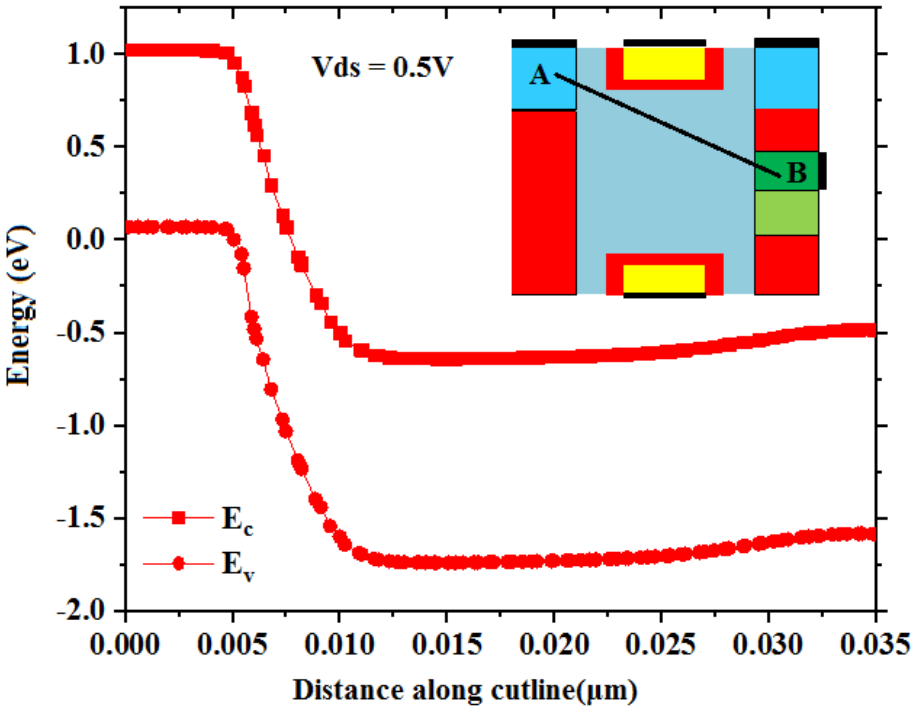
Fig3.26: The contour diagrams for (a) Electric field (b) Electrostatic potential (c) Electron tunnelling rate



(a)



(b)



(c)

Fig3.27: (a) Electric field (b) Electrostatic potential (c) Energy band diagram along the cutline AB .

We can see from the Fig 3.27(a), that the electric field and potential is maximum near the source region and gradually decreases as we move towards the drain which is evident from the contour diagrams shown in Fig 3.26(a). Also we can see from the energy band diagram that band to band tunnelling takes place near the source and gate oxide interface which is also evident from the electron tunnelling rate contour diagram of Fig 3.26.

3.4.8 Comparison of Classical and Quantum Mechanics in Optimized DSTGSD TFET

In this section, we have presented an approach to take into account quantum confinement in DSTGSD-TFET and an investigation has been done that by including this concept there is a the electrical parameters are affected [19]-[21]. We have used the nonlocal band to band tunnelling model along with the Schrödinger Poisson model for the carrier injection.

Confinement is studied to occur in one dimension resulting in discretisation of sub bands. Consequently, this discretisation causes a notable reduction in the tunnelling probability as the tunnelling width faced by the carriers coming in as a result of BTBT from Source to Channel increases. Hence by including the concept of quantum confinement, the electrical parameters such as Subthreshold Swing, ION/IOFF ratio are greatly affected making it a main issue for the advanced device characterization.

The Fig 3.28 shows the comparison of transfer characteristics for classical and Quantum Mechanics in DSTGSD-TFET. Also a comparison in the electron density contour for classical and Quantum is presented in Fig 3.29.

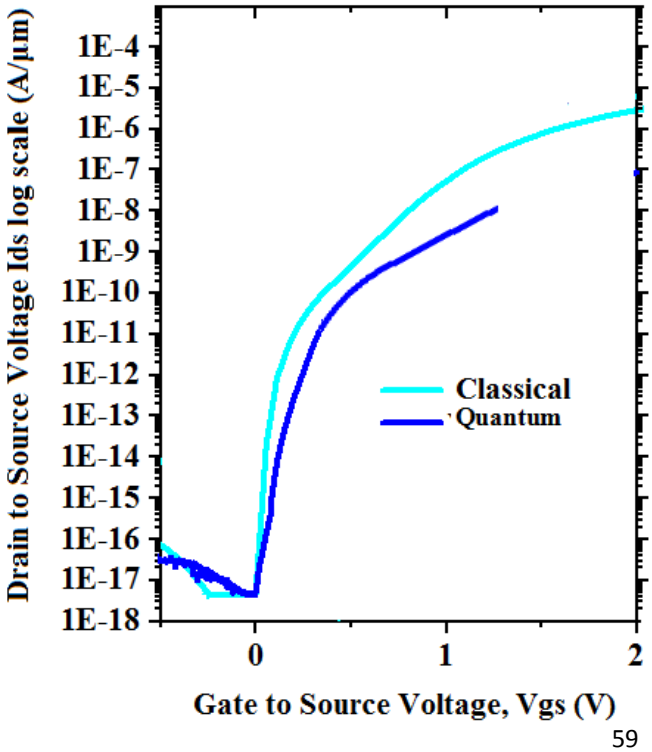
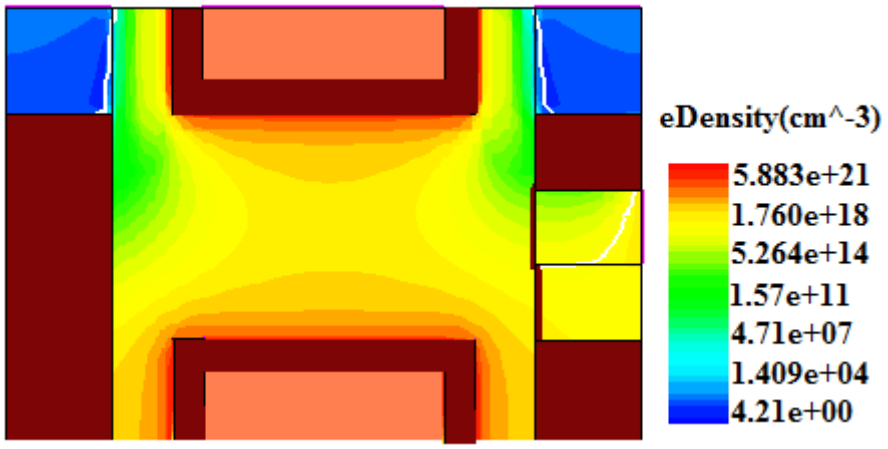
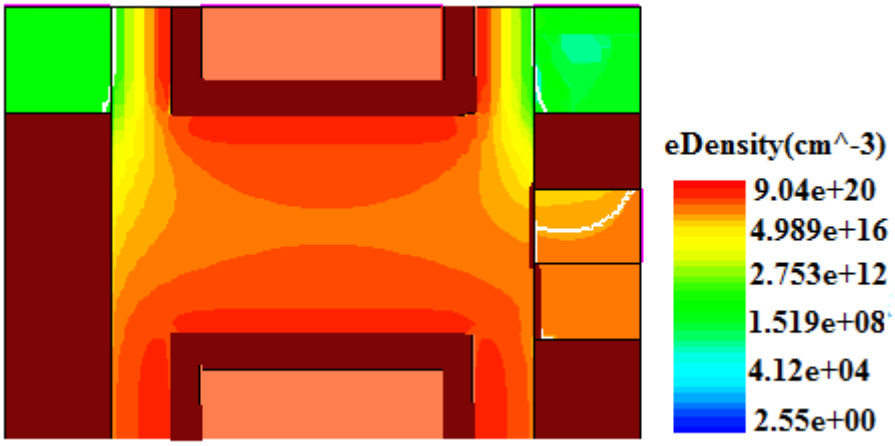


Fig3.28: Comparison of transfer characteristics for classical and Quantum Mechanics



(a)

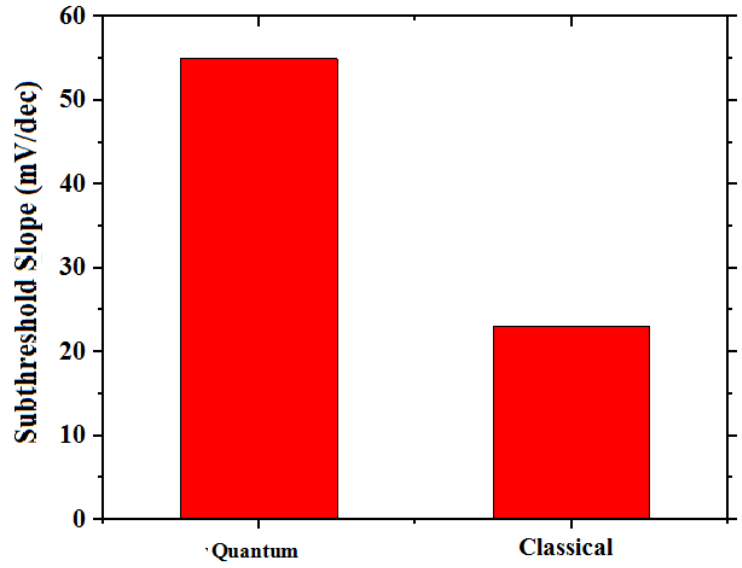


(b)

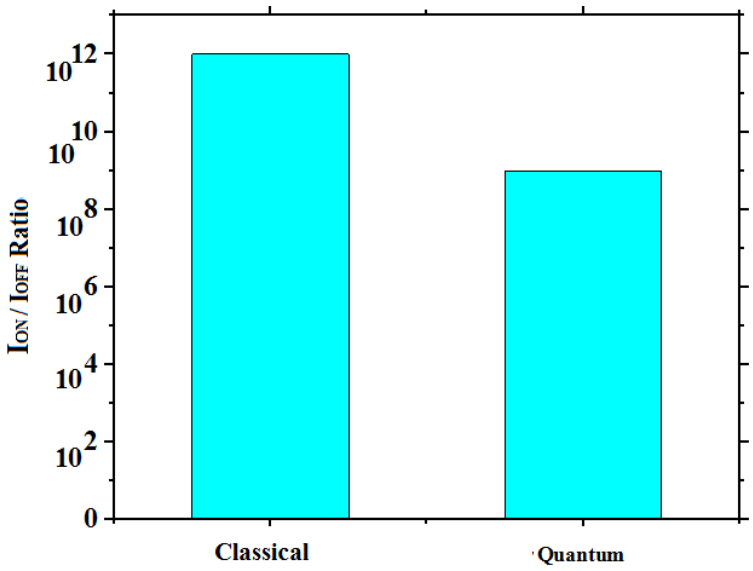
Fig3.29: Simulated electron density Contour diagrams for (a) Classical (b) Quantum

As we can see from the contour diagrams, the red colour represents the highest electron density concentration. The highest electron density is shifted or rather we can say is pushed away from the Silicon-Silicon Dioxide interface (where the electric field is maximum) to a place where the electron density is less i.e towards the substrate.

This leads to a decrement in the overall flow and hence the ON-current decreases in the case of Quantum Mechanics leading to a decrease in the ION/IOFF ratio. Moreover there is a reduction in the Subthreshold Swing when Quantization is included. A comparison of the SS and ion/Ioff ratio for the same is depicted using bar charts in Fig 3.30.



(a)



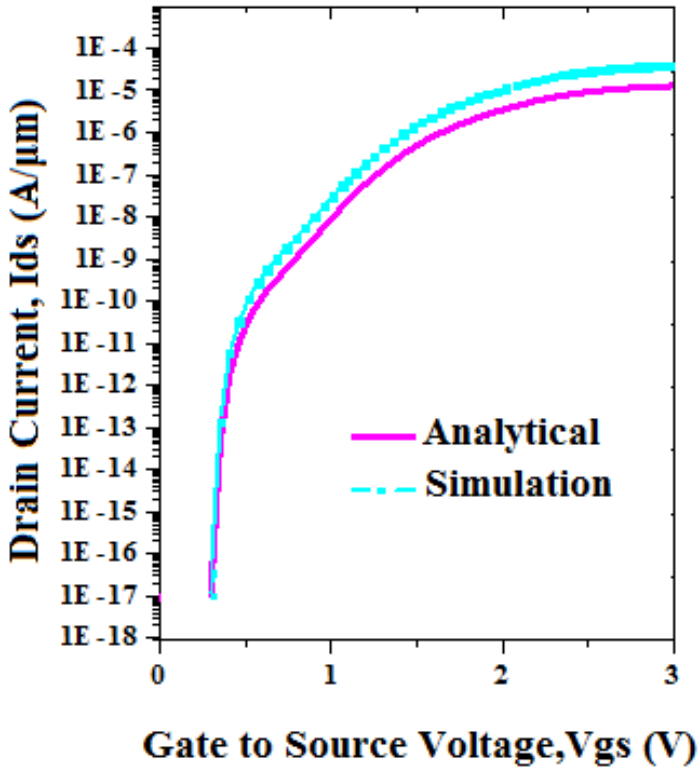
(b)

Fig3.30: Shows the comparison of Classical and Quantum for (a) Subthreshold Slope (b) ION/IOFF ratio

We can see from the above figure that for ION/IOFF ratio for classical is around 10^{12} while that for Quantum is nearly 10^{9}. Also the SS for the former is 21mV/decade and that of the latter is nearly 53mV/decade.

3.4.9 Comparison of Analytical Current Modelling with Simulation Results of DSTGSD -TFET.

Validation of the approximated expression for tunnelling current we have numerically calculated eq. 18 of section 3.3 with the simulated results are as shown below. As seen from Fig 3.31 the analytical approximation agrees well with the simulated result.



.

Fig3.31: ON current comparison for Simulated and Analytical approximation

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Chapter 4

Conclusion

4.1 Conclusion

The disadvantages of the conventional MOSFET innovation impacts in the improvement of TFET devices which is modernizing the nanoscale business with its progressions. Quantum mechanical band to band tunnelling (BTBT) is the fundamental procedure for conduction in TFET. Also, the subthreshold swing of TFET is beneath 60mV/decade at room temperature unlike that of MOSFETs. The upsides of TFET over different devices lies in its straightforward and standard CMOS compatible fabrication procedure with no prerequisite of less solid effect ionization process. The threshold voltage of TFETs relies upon the band bending and tunnelling impact.

In the present work we have proposed the DSTGSD-TFET, which has two Source regions dual Trench gate and double split Drain regions. The dual Source regions along with the trench gate increases the tunnelling probability as the effective tunnelling area is increased. Moreover, in order to overcome the impacts of ambipolar current we have splitted the drain region into highly doped and low doped region where the highly doped region is placed above the latter. This leads to an increment in the channel-drain resistance thus increasing the tunnelling width. Hence the leakage current reduces to a great extent. Furthermore, we have derived an analytical expression for tunnelling current using Kane's Model and a comparison of the derived expression and the 2D simulated results have been made which are found to be in good agreement. Also, the effects of various device parameters and doping concentration is taken into consideration. More to add, we have included the concept of Quantum Confinement and a comparison of including and excluding the same has been illustrated.

4.2 Future Scope of Work

- In the present work Silicon is used as the source material, so an attempt could be made to incorporate the semiconducting materials that have even lower band gap in contrast to Silicon example, Ge, InAs etc.

- Here we have considered single metal in the trench gate. An approach can be made to include dual or triple metal in the trench gate.

- Research should be made to bring down the threshold voltage of the TFET even lower so that it can become more applicable in the field of low power.

List of Publications relevant to the current Thesis

Conferences

- Bijoy Goswami, Debadipta Basak, Ayan Bhattacharya, Sutanni Bhowmick, **Koelgeet Kaur**, Subir Kumar Sarkar,"**Analytical Modeling and Simulation of Low Power Salient Source Double Gate TFET** ",3rd International Conference "2019 Devices for Integrated Circuits (DevIC)", Kalyani Government Engineering College, West Bengal, India. March 23-24 2019.

- Bijoy Goswami, Debadipta Basak, **Koelgeet Kaur**, Ayan Bhattacharya, Subir Kumar Sarkar."**Reduction of Ambipolar Conduction in Centrally Aligned PNPN-DG TFET**" International Conference on Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology ECTI-CON 2019, Chiang Rai, Thailand. 18th – 21st July 2019.

Journals

- **Koelgeet Kaur**, Bijoy Goswami, Sutanni Bhowmick, Debadipta Basak, Subir Kumar Sarkar, "**Analytical Modeling and Simulation Based Validation of Dual source Trench Gate Split Drain TFET(DSTGSD-TFET)**".(Communicated).

- Debadipta Basak, Bijoy Goswami, Sutanni Bhowmick, **Koelgeet Kaur**, Ayan Bhattacharya, Subir Kumar Sarkar, " **Analytical Modeling and Simulation Based Validation for Gate Centric Extended Source SOI TFET" (**Communicated).

- Sutanni Bhowmick, Bijoy Goswami, Debadipta Basak, **Koelgeet Kaur**, Ayan Bhattacharya, Subir Kumar Sarkar, "**Analytical Modeling and Simulation of Double Trench Gate Covered Source-Channel TFET towards Improved ON-Current**" (Communicated).

- Bijoy Goswami, Debadipta Basak, Ayan Bhattacharya, Sutanni Bhowmick, **Koelgeet Kaur**, Subir Kumar Sarkar, "**Analytical Modeling and the Impact of Quantum Confinement on Subthreshold Swing of Salient Source DG-TFET**".(Communicated)

- Bijoy Goswami, Debadipta Basak, **Koelgeet Kaur**, Ayan Bhattacharya, Subir Kumar Sarkar "**A Novel Source Pocket Doping in PNPN-DG TFET to Preclude Ambipolar Current-Two Dimensional Analytical Modelling of Surface Potential & Simulation**"(Communicated).