A COMPREHENSIVE CHARACTERIZATION AND PERFORMANCE ANALYSIS OF NANO SCALE HETEROJUNCTION TFET

Thesis Submitted
In Partial Fulfillment of the Requirement
For The Award of the Degree Of

MASTER OF TECHNOLOGY
IN

VLSI DESIGN AND MICROELECTRONICS TECHNOLOGY
Of

JADAVPUR UNIVERSITY
By

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ACKNOWLEDGEMENT

This wonderful journey of experience has come to an end with completion of this thesis. First and foremost, I feel myself fortunate in having the privilege to express my deep sense of gratitude and indebtedness to my project guide **Prof. Subir Kumar Sarkar**, Department of Electronics & Tele-Communication Engineering, Jadavpur University, Kolkata for providing me the opportunity to carry out thesis under his guidance and developing the concepts related to my thesis topic. His constant discussion and encouragement conducts my intellectual and personal growth, not only in my subjects and thesis topic but also in comprehensive attitude towards relevant issue. I also want to thank him for giving me the opportunity to access all the amenities whenever necessary and for introducing me to the methodology of technical skills and approach towards difficult problems. His technical and ethical contributions in my work and life are invaluable and will be treasured for rest of my life. His involvement paved the way for the successful completion of my exertion and thesis.

I would also like to express sincere gratitude to all my professors of Jadavpur University for their consent and providing necessary information whenever required. I am grateful to **Mr. Bijoy Goswami, Mr. Dinesh Kumar Dash, Mr. Anup Dey, Ms Pritha Banerjee, Ms. Priyanka Saha** for their suggestions & enormous encouragement. I would like to offer my sincere gratitude to them for sharing the ups and downs during the development and bearing inconvenience. The words of thanks are only a token of my true appreciation for all they have done to make my project in the present shape.

I would like to thank H.O.D Department of Electronics & Telecommunication Engineering, Jadavpur University for providing me all the facilities for carrying out the entire project work. I would like to express my sincere appreciation to all the teaching and non-teaching staff of the department for providing necessary support and aids.

Finally I would like to dedicate this work to my parents and thank them from the bottom of my heart for their unconditional lone support and blessing. They are the strength I absorbed for performing all the work, now and in future.

THANK YOU

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ABSTRACT

This dissertation discusses about an alternative choice of CMOS technology which encounters various limitations due to miniaturization of device dimensions.

A conventional TFET device is worked in the basis of the quantum band to band tunneling near source (p-type)-channel (intrinsic) interface by the transition of electron carriers from source valence to channel conduction band and provides better electrical behavior than conventional and advanced MOSFET devices. But low on current is a limitation of conventional TFET devices.

To reduce this limitation, Heterojunction TFET can be the best alternative with implementing new material in the source region. This Heterostructure provides high ON current by several orders of magnitude and can be attained at a low electric field. Compared to the conventional double gate TFET this hetero double gate TFET is considered a promising candidate in providing high ON current due to efficient tunneling in source channel interface, and also taking depletion region in both interface region provides more accurate result over conventional.

Further, this thesis work investigates about quantum confinement effects as an integral part of the device parameters when the channel length is shrunk about less than the 20-nanometer regime. In dual metal gate TFET structure, vertical electric field is modified by incorporating different work function in the gate and resulting enhancement of the performance of device structure.

The simulation process has been carried out using SILVACO Atlas software for conventional single metal TFET and afterwards double metal dual gate Heterostructure TFET with quantum confinement model. Structures implementing new metals and also a gate, source engineering will be done for optimization further benefits in low power applications. And also for non ambipolar conduction effect, drain engineering attain good result Analytical model has been performed for surface potential and electric field in our proposed work.

CHAPTER 1

Introduction & Organization of Thesis

1.1: Introduction

1.2: Motivation of proposed work

1.3: Introduction to TFET

1.4: Organization of Thesis

References

1.1: Introduction

There is a revolution in electronics industry after the invention of the transistor which is closely followed by the discovery of monolithic integrated circuit. Since 1960s new industries have been created to manufacture semiconductor devices ranging from small diodes to complex microprocessor chips.

Based on the growth of semiconductor technology in recent and an advent nature of continuous downscaling of integrated circuit provides an era of the semiconductor industry in higher packing density and better performance. These key observations were enunciated by Gordon Moore, founder of INTEL at late 1965, which projected doubling of transistor count in a chip every two or three years and the performance will also be double.

Progress in the field of CMOS technology, miniaturization of MOSFET has largely benefited microelectronic industry in the last few decades. Hundreds of millions of transistors can be placed in an integrated circuit due to shrinking of the size of MOSFET below 100nm. As CMOS technologies are downscaled, there are advantages over speed and power due to small capacitance and the smaller supply voltage. The continuous improvisations in device size reduction and continuous increase in device density and circuit complexity on a single chip have

realized the tremendous boost in the computing capability leading the consumers to expect ever better products at reduced cost thus emphasizing on scaling.

This chapter gives motivation for this thesis and also presents reason behind the power crises faced by conventional MOSFET due to their ever-increasing static power consumption after rigorous downscaling of chip size to integrate more functionality on-chip which is operating at a higher speed.

Continuously MOSFET scaling results higher packing density, increased circuit speed and reduced cost per function for both in fabrication and power consumption, as density is increasing in a chip, low operating voltage to be needed to keep constant power consumption.

1.2: Motivation of proposed work

In our proposed research work TFET has been in response to the severe challenges faced in scaling down the MOSFET, There are still some limitations in the TFET, such as low ON current and high saturation drain voltage, which can be surmounted by the Heterojunction and dual material gate. The consequent degradation of off-current can also be improved by using dual metal gate. High-k material as gate dielectric is used here providing significantly SS characteristics even below 50mV/decade. We have also considered source/channel and drain/channel depletion region to improve ON current and also degrade the effect of ambipolar behavior at drain-channel interface. Analytical model for surface potential and electric fields are also provided in this work

1.3: Organization of Thesis

This dissertation is divided into six chapters and its outline is described below:

Chapter 1: This chapter is contained about organization of overall thesis and also gives a brief overview of TFET technology as an alternative technological outcome and replacement of MOSFET. Motivation of the proposed work is given at the end of this thesis.

Chapter 2: In this chapter TFET is come to a part of interest as an alternative solution for limitation of CMOS, It outlines usage of various models to estimate tunneling mechanism and current of TFET device. It introduces basic operation and its electrical characteristics along with sub-threshold swing. And finally some literature has been studied regarding various techniques of device parameter engineering.

Chapter 3: H-Shaped Double Gate TFET for Low power Applications**,** in this chapter an h-shaped double gate TFET is proposed for the first time which provides high on current at low threshold voltage also it has been presented 32 mV/decade sub threshold swing.

Chapter 4: Electrical Characteristics of 2D Dual Material Double Gate Heterojunction Tunnel Field Effect Transistor with heterodielectric gate oxide. In this chapter Heterojunction TFET with dielectric engineered is proposed. Also here we consider depletion and accumulation/inversion layer and consider the both conditions estimated electrical characteristics of the device. Analytical model has been worked for the proposed structure.

Chapter 5: Efficient Quantum Mechanical Simulation for 2D Heterojunction Double Gate TFET for Low Power Applications. In this section quantum confinement is added as channel width below 10nm of proposed device and also study about the model which is used for confinement

Chapter 6: Concluding remarks and Future work. This chapter summarizes the material presented in the thesis, and gives suggestions for areas which need more study and investigation in the future. Perspectives are given, both related directly to this thesis work, and more generally.

1.4: Introduction to TFET

The tunnel field-effect transistor (TFET) has structure almost similar to that of MOSFET. However, the switching mechanism of this transistor is different from that of conventional MOSFET, making this device candidate for low power electronics. In this case, the basic principle is that of quantum tunneling through a potential barrier, unlike in case of conventional MOSFET, where thermionic emission over the potential barrier is the driving force behind electron transmission.

As a result, subthreshold swing of TFETs goes below 60 mV/decade at room temperature. Joerg Appenzeller in 2004 reported that a TFET with channel made of carbon nano tube can give subthreshold swing as low as 40 mV per decade. It is also observed that use of low power TFETs can lead to considerable saving of power when compared to conventional MOSFETs. The basic structure of TFET is that the source and drain regions are oppositely doped. The gate terminal controls the flow of electrons. The higher the on-current, the more is the speed of transistor. The lowering of threshold voltage is very important for constant field scaling. For constant voltage scaling, the supply voltage cannot be scaled down with lowering of device dimensions. This leads to reduction of processor speed with scaling.

However, TFET with a slope far below 63 mV/decade permits scaling of device dimensions with increase in processor frequency. In TFETs with increase in voltage, accumulation of electron occurs in the intrinsic region of the device. When the valence band of source and the conduction band of the channel get aligned due to the band tunneling effect in TFET, electrons flow from the valence band of p-region to the conduction band, leading to flow of current in the device.

When the gate voltage is reduced, the two bands become misaligned and current cannot flow through the device. Recently double gate TFET structures have been proposed by researchers to overcome the limitations of lateral TFET structures like requirement of very sharp doping profile, large gate leakage, etc.

In the last few years there has been a rising demand for the TFET (Tunnel field effect transistor) and researchers are doing a wide study on this transistor. Absolutely there must be a component with the TFET due to which it has involved huge attention of everyone. And here we will give you an overview of the transistor.

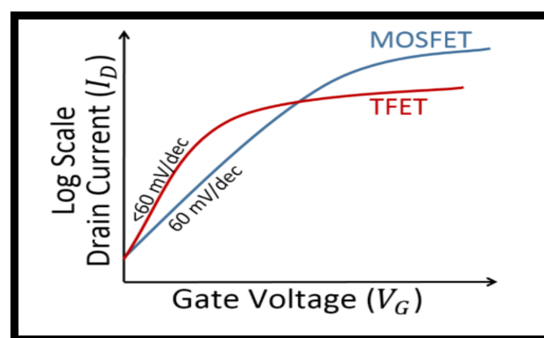

Figure 1.1 *Transfer Characteristics of TFET*

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CHAPTER 2

Overview of scaling theory, alternative replacement of MOSFETs and Literature Survey of TFETs

2.1: Introduction

2.2: Scaling Theory

2.3: Limitation of CMOS Technology

2.4: Short Channel Effects

2.5: Solution to the Limitations of CMOS

2.6: Tunneling Mechanism

2.7: Device Structure and Working Principle

2.8: TFET Literature Review

References

2.1.: Introduction

Scaling the length of a MOSFET has many benefits, besides the increased number of transistors in a chip. A reduced gate length leads to a reduced gate capacitance, thereby increasing the switching speed of the circuit. Moreover, the voltage scaling that is a necessary part of device miniaturization also causes reduction in the power consumption of the device. However, as the device dimensions were reduced to 50 nm and the power supply to 0.5 V, the OFF-state power consumption of MOSFETs became a major challenge. The drain current of a MOSFET is controlled by the thermionic emission from the source into the channel. As the gate voltage is increased, the potential barrier between source and channel is decreased, leading to an increase in the drain current. This leads to two problems – a larger OFF-state current due to subthreshold conduction and a higher subthreshold slope. The subthreshold slope (SS) of a MOSFET is thevariation in gate voltage required to increase the I_{DS} by a factor of 10. A lower subthreshold

slope would allow for a higher ratio of ON-current to OFF-current (ION/IOFF), and would lead to a lower power dissipation in the OFF-state. One such device is the tunneling field-effect transistor (TFET).TFETs can exhibit subthreshold slope below 60 mV/decade due to a fundamental difference in the mechanism of current control as compared to MOSFETs. In MOSFETs, the current depends on the thermionic emission of free carriers across the potential barrier between the source and the channel. On the other hand, the current in TFETs depends on the charge carriers tunneling through a potential barrier between the valence band of source and conduction band of the channel. As this potential barrier is very wide in the OFF-state of the device, TFETs exhibit very low OFF-state current.

Apart from the limitation imposed by the subthreshold slope, MOSFETs in the sub-50 nm channel regime also suffer from various short channel effects, such as drain-induced barrier lowering, threshold voltage roll-off, charge sharing between gate and drain, etc. As we shall study later in the chapter, TFETs have a greater immunity to these short channel effects. It may be pointed out that TFETs differ from the MOSFET only in the type of source doping. Therefore, the integration of the TFET fabrication process with the current MOSFET fabrication process would be easy.

2.2: Scaling Theory

The reduction of the dimensions of a MOSFET has been dramatic during the last three decades. Downscaling of the depletion layer widths also produces scaling of the substrate doping density. Scaling theory is developed for shrinking device sizes to increase device density & frequency and reduce the power dissipation & gate delays. Figure 2.1 shows average L (Gate length of device) of MOSFET vs. over years.

When all of the voltages and dimensions are reduced by the same scaling factor, the configuration inside the FET remains the same as it was in the original device. This is called constant field scaling, which results in increase in circuit speed proportion to the factor Sand circuit density proportional to S^2. Constant field scaling yields the largest reduction in the power-delay product of a single transistor. However, it requires a reduction in the power supply voltage as one decreases the minimum feature size.

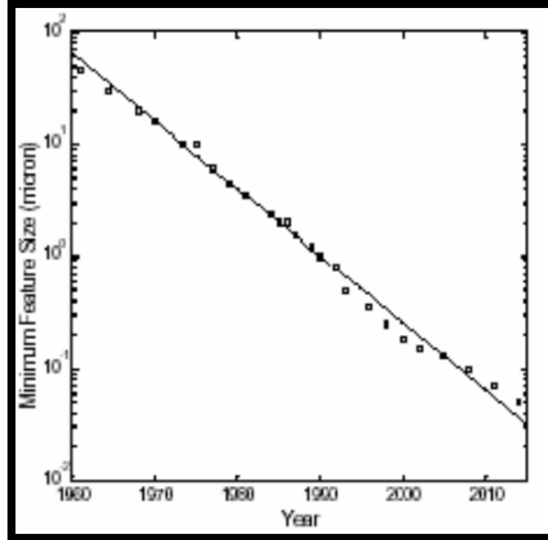
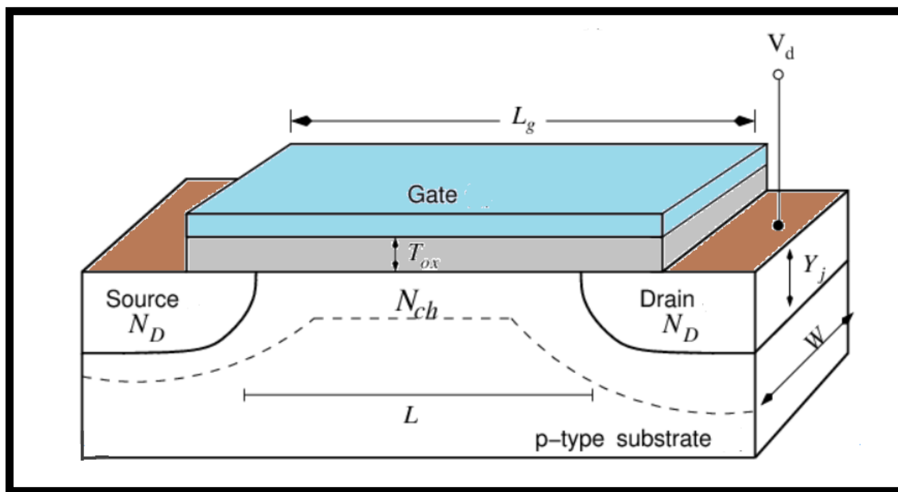
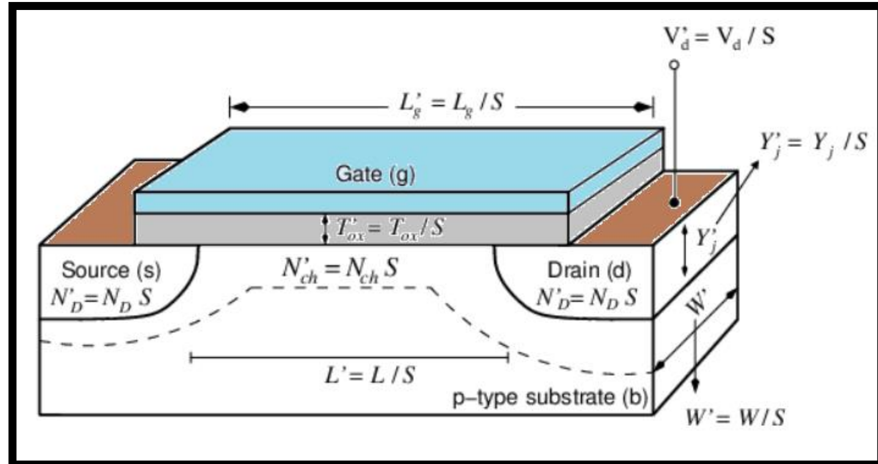


Figure 2.1 ***Average device lengths vs. time***

Constant voltage scaling provides voltage compatibility with older circuit technologies. The disadvantage of constant voltage scaling is that the electric field increases as the minimum feature length is reduced. This leads to velocity saturation, mobility degradation, increased leakage currents and lower breakdown voltages.



Original Device



Scaled Device

Figure2.2. Original device and after scaling device parameters

It can be seen from the Figure 2.2 that when we have applied scaling theory on conventional MOSFET device, it has been observed that the voltages could not be scaled at the same rate as the length. The scaling rule of some physical parameters of device are listed on

Table 2.1

Parameter	Constant Field Scaling	Generalized Scaling
Device Dimension (L_g,W,t_{ox})	1/S	1/S
Doping Concentration	S	αS
Voltage	1/S	α/S
Electric Field (F)	1	α
Carrier Velocity (v)	1	1
Depletion layer width (W_D)	1/S	1/S
Capacitance (C=εA/t_{ox})	1/S	1/S

Current (I)	1/S	α/S
Circuit Delay Time (τ=CV/I)	1/S	1/S
Power Dissipation per circuit (P~VI)	$1/S^2$	α/S
Power delay product per circuit(Pτ)	$1/S^3$	α/S
Circuit Density (∝1/A)	S^2	S^2
Power Density (P/A)	1	α^2

2.3: Limitation of CMOS Technology

This Dissertation is about Tunnel FET, mechanism of carrier transport through the band to band tunneling. It needs to understand why Tunnel FET is an alternative instead of conventional MOSFET technology, In order to understand it is necessarily to elaborate first Dennard's Scaling Rule.

In 1974, R. Dennard published an article which has become very famous in the semiconductor device community, about how to scale a MOSFET while keeping the electric fields inside the device unchanged He recommended that all device dimensions be scaled by 1/κ, while the doping ofthe source and drain regions should increase by a factor of κ. Applied voltages should also be scaledby 1/κ. These rules have been roughly followed ever since, until rather recently.
The reason for which Dennard’s scaling rules no longer work as well as they did in the past can beseen in Fig. 1.3, which shows the scaling trend from the 1.4 μm node to the 65 nm node. While thesupply voltage V_{DD} decreased to about 20% of its original value, the threshold voltage V_T only wentdown to approximately half of its starting value. That threshold voltage decrease did not happen as anatural result of Dennard scaling. It had to come about in other ways, such as changing the doping ofthe channel region under the gate. Since the electric fields inside a MOSFET stay nearly constantwhen the scaling rules are followed correctly, the threshold voltage stays nearly constant as well,unless other changes are made.

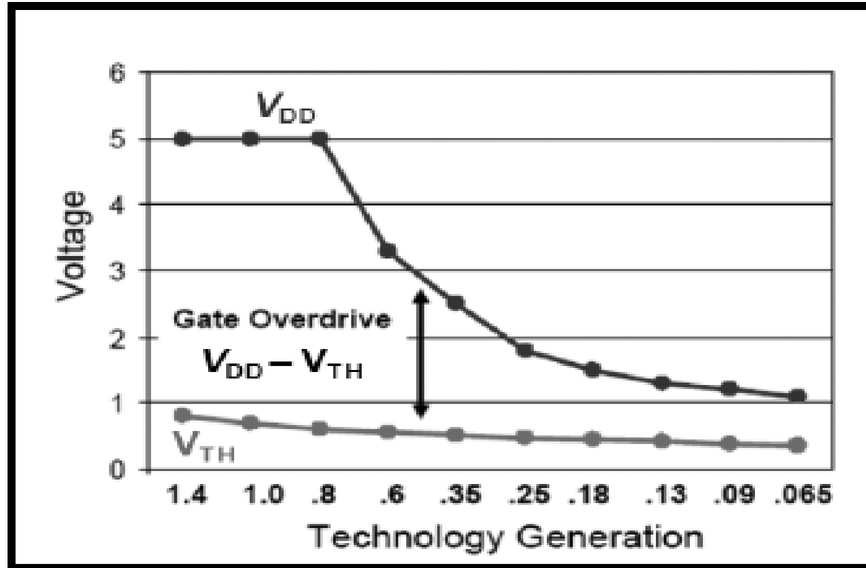


Figure 2.3 *The trend of supply voltage and threshold voltage scaling vs. technology generation. V_{DD} decreases with device dimensions, but V_T does not.*

The most important consequence of V_{DD} reducing during device scaling while V_T reduces significantly less, is that the gate overdrive, also shown in Fig. 2.3, goes down. When gate overdrive decreases, on-current decreases, which negatively affects device performance, the Ion/Ioff ratio, and dynamic speed (CgV_{DD}/Ion). There are two possible solutions to this problem of needing a high gate overdrive: either V_{DD} can stay higher than it should with constant field scaling, or V_T can be scaled down more aggressively.

Fig. 2.4 shows that the formerly-followed scaling trends of $1/\kappa = 0.7$ every 2 or 3 years (bold and dashed lines at the top of the figure, for reference) no longer hold true for V_{DD}. In order to maintain acceptable levels of gate overdrive, V_{DD} scaling has slowed down drastically. When the supply voltage decreases along with device dimensions, then the power density $IonV_{DD}/A$ (on-current times supply voltage divided by surface area) remains constant, which means that the energy needed to drive the chip, and the heat produced by the chip, remain constant. This assumes that when devices scale down, we don't see chip size decreasing, but rather, more complexity and functionality is added with each generation, and chip size remains more or less constant.

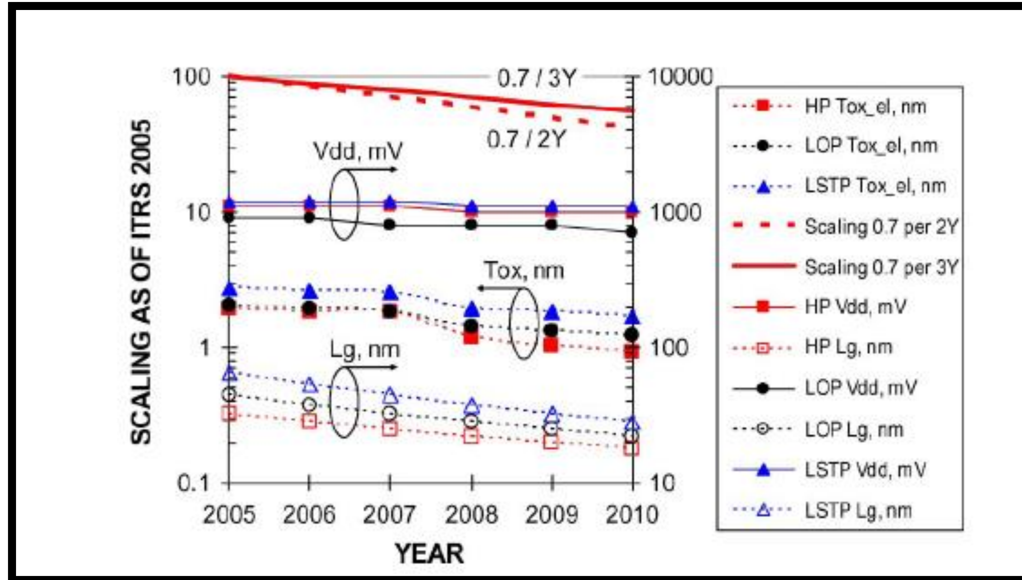


Figure 2.4 *Scaling trends showing the decreases in tox and Lg, while V_{DD} stays almost unchanged*

When VDD doesn't scale down, power density increases instead. For each MOSFET, the dynamicand static power consumption can be expressed as

$$P_{Dynamic} = fC_L V_{DD}^2$$

Where f is the frequency and C_L is the total switched capacitive load, and

$$P_{Static} = I_{leak} V_{DD}$$

Where I_{leak} is the sum of the leakage currents in the device when the MOSFET is in the off-state. If V_{DD} does not decrease, and yet device dimensions decrease, and more devices are added to a chip such that chip size is not significantly reduced, then it can be expected that power consumption will rise considerably. The current trend of increasing power is illustrated in Fig. 2.5. The discussion up until now has not explained why static power would be increasing much faster than dynamic power, and that comes back to the second option for keeping a high gate overdrive: scaling down V_T.

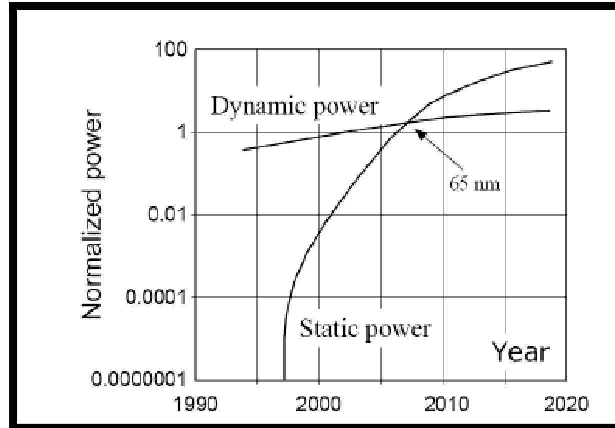


Figure 2.5 *Trends of dynamic and static CMOS power, showing that static power consumption has become a greater problem than dynamic power consumption*

One characteristic of conventional MOSFETs is their fixed slope in subthreshold, when I_{DS}-V_{GS} is plotted on a log-linear scale. This fixed slope means that once the device has been fully optimized in order to have the most abrupt possible turn-on with gate voltage, and the subthreshold swing $S = dV_{GS}/d(\log I_{DS})$ has hit its limit of 60 mV/decade at room temperature, then the only way to lower the threshold voltage further is to shift the I_{DS}-V_{GS} characteristic horizontally on the x-axis, as illustrated in Fig.2.6. If we want to shift V_T by 60 mV, then the price to pay is an increase of onedecade of off-current, and in turn, of static power.

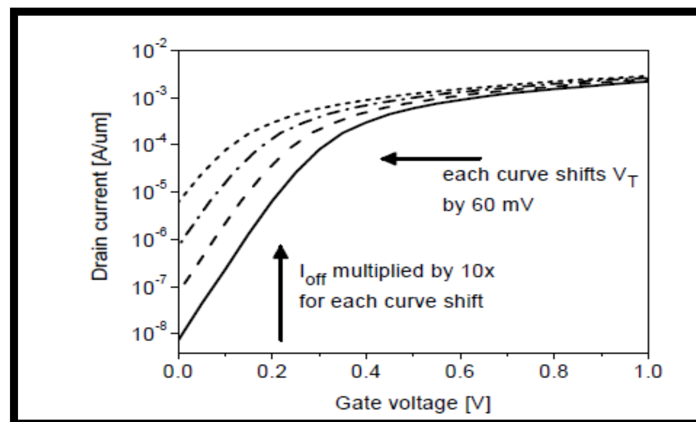


Figure 2.6 *A typical I_{DS}-V_{GS} curve for a highly-optimized conventional MOSFET, showing the subthreshold swing limited to 60 mV/decade at room temperature. If we want to decrease V_T by shifting the curve left, we pay a price in leakage current. Solid curve's data is from an*

optimized asymmetrical double-gate conventional MOSFET, which is then shifted three times. Such a shift could come from engineering the gate work function.

Why is power dissipation such a problem? There are quite a few reasons for which circuits should use less energy, some of which will be mentioned here. The first can be seen on a global scale. We would like our computers, appliances, and gadgets to use less power because it's better for the environment. On a more personal level, it's less expensive to use less electricity. On a practical level, it's more convenient for battery-operated gadgets because their batteries will last longer before needing to be charged. And on a comfort level, it is better when laptops and hand-held gadgets have a lower power density and therefore produce less heat. Looking at Fig. 2.7, the trend of increasing power for Intel computer chips is shown.

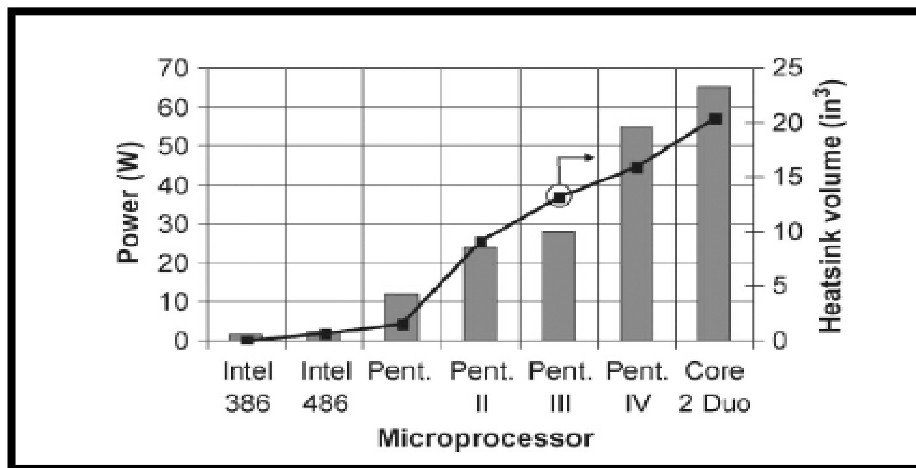


Figure 2.7 *Computer chip power trends, along with the accompanying increase in heat sink volume.*

If we assume that chips tend to be on the order of 1 to 2 cm2, we can get a rough idea of the power density as well. According to published in 2010, current power density is around 60-80 W/cm2. An ITRS presentation predicted that the power density for the 14 nm node would be greater than 100 W/cm2 Fig. 1.7 also shows on its right axis that in order to cope with the increasing power density, the heat sink must grow in volume. This too has a limit, since we would like our appliances, computers, and gadgets to stay the same size or shrink, not get larger in order to accommodate a large heat sink required by the power-hungry chip inside.

2.4: Short Channel Effects Limitation of MOSFET

The current use of power supply much higher than predicted by Dennard shows that the industry as a whole is not interested in maintaining constant field. More realistic motivations for scaling device parameters are performance and reliability. Therefore, to predict the scaling of future technologies we should scale each parameter to provide the highest performance device possible while satisfying certain basic electrical and reliability requirements. These fundamental limitations together are termed as short channel effects.

2.4.1 Drain-Induced Barrier Lowering (DIBL)

For long-channel devices, the source-channel potential barrier is determined primarily by the voltage applied to the gate. Increasing the gate voltage causes the barrier height to reduce, resulting in injection of electrons from the source into the channel. At a particular gate voltage – the threshold voltage – the barrier has reduced sufficiently to allow a significant amount of injection, and flow of current, to take place.

In a short-channel device, the drain junction is now quite close to the source junction. As a consequence, the potential at the source-channel region is determined not only by the gate voltage, but also the drain voltage. The drain voltage can cause a lowering of the barrier at the source end of the channel, causing current to flow for a lower value of gate voltage. This effect is called DIBL (pronounced “dibble”)

The height of this barrier is provided by the balance between drift and diffusion current. If a high drain voltage is applied, the barrier height is decreased, as indicated in Fig. 1.8, show an increased drain current. Thus VGS control drain current. For device modeling this parasitic effect can be accounted for by a threshold voltage in reduction of dependent on the drain voltage. The DIBL effect becomes obvious when looking at the transfer curves of a MOS transistor for the linear and saturated cases (Fig. 1.9). If there was no DIBL, the two curves would coincide in the subthreshold regime. The DIBL effect can be measured by the lateral shift of the transfer curves in the subthreshold regime ΔV_{th} divided by the drain voltage difference of the two curves

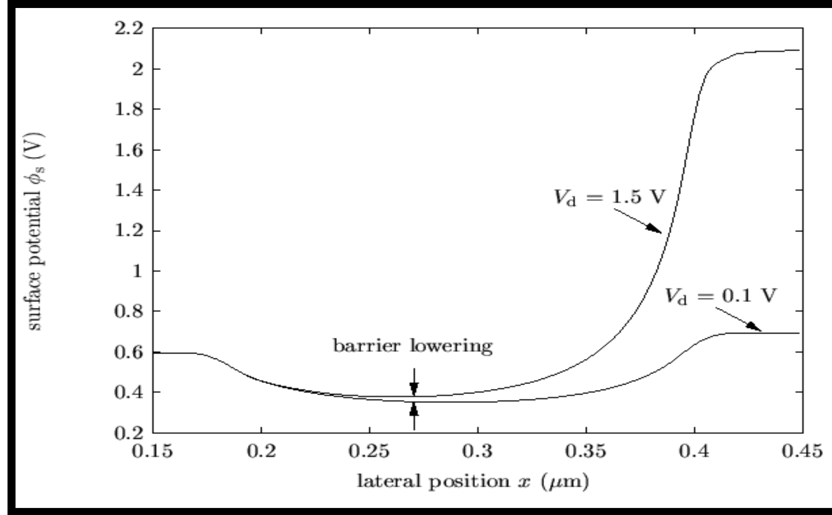


Figure 2.8 *Surface potential of Device β for 0.1 V and 1.5 V drain voltages (linear and saturated case).*

and is given in units (mV/V) $DIBL = \frac{\Delta V_{th}}{\Delta V_D}$

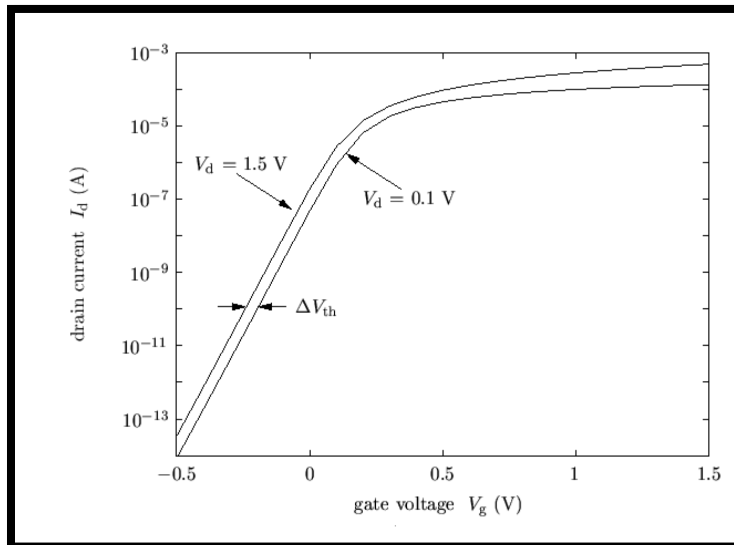


Figure 2.9 *Transfer curves of Device β for 0.1 V and 1.5 V drain voltage (linear and saturated case)*

The magnitude of DIBL obviously depends on the channel length L, but also on the doping NA. Higher doping's would mean that electric field from the drain is more effectively screened, resulting in lower DIBL. Another way to interpret DIBL is that the potential lowering is due to merging of the edges of the depletion regions emanating from the source and drain junctions.

Higher doping's reduce the depletion widths, and consequently delay their merging, reducing the DIBL effect. Thus, increasing the bulk doping is a good strategy to minimize DIBL.

2.4.1.1 Effect on threshold voltage

One consequence of DIBL is an apparent reduction of the threshold voltage. This is clear physically, because with DIBL present, a smaller bias at the gate (threshold voltage) is reduce the barrier sufficiently to allow current to flow. Since larger drain voltages result in increased barrier lowering, the threshold voltage keeps decreasing with increasing V_{DS}, that is, V_T is now a function of V_{DS}, which was not the case for long channel devices.

An approximate empirical relationship used for ΔV_{th} due to DIBL is

$$\Delta V_T^{DIBL} = -\sigma V_{DS}$$

Where σ is called the DIBL factor, and is usually expressed in units of mV/V. typical values of σ for a modern transistor fall in the range of 10-100mV/V. The DIBL factor is, of course, a strong function of L, and is often modeled empirically as $\sigma = \sigma_0 \exp(-L / L_0)$

Where L_0 is a characteristic length. Equation implies that the effect of DIBL is present for $VDS \neq 0$ where as in fact the barrier and threshold voltage are lowered.

2.4.1.2 Effect on subthreshold region

The coupling of the drain field to the source-channel junction affects how current flows in the subthreshold region for a short-channel device. As drain voltage increases, the barrier reduces due to DIBL, and larger drain current flows. This behavior is very different from what is seen for the long channel device, where the subthreshold current is independent of drain voltage.

Parameters affecting sub-threshold regime

$$I_D = I_{pf} \exp[\frac{\beta(V_{GS} - V_T)}{\eta}]$$

Where I_{pf} is the pre exponential factor and $\eta = [1 + (C_D / C_{OX})]$. The first point to be noted that I_D is larger for short channel case than the long channel case because VT is former for both DIBL and charge-sharing. Secondly VDS dependence of ID in the case of short channel arises because VT is now dependent on VDS through above equation. How eve the effect of DIBL not only translates into a charge of VT, but also change in subthreshold slope. The reason is for that due to proximity of the drain, the gate is less control of current flow compared to the long channel case. The gate has ceded some of the control of the drain. As a consequence changing the gate voltage does not affect the current flow as strongly as it does for the long channel device and the subthreshold fall off is not as tight.

2.4.2 Velocity Saturation

As the MOS device is scaled down, electric fields in the device become large. This creates a significant problem. It is true that the voltages used have also scaled down from 5 V to about 1 V in an attempt to keep the field within limits, but with the corresponding channel lengths decreasing from 5 μm to 70 nm, and gate oxide thickness from 100 nm to 1.5 nm, it is clear that the electric fields, both horizontal and vertical, have increased significantly in short channel MOSFETs. There are several consequences of the high electric fields. One of the most important is velocity saturation experienced by the carriers as they move along the channel in the presence of a high lateral electric field. It is well-known that the drift velocity of carriers in a semiconductor does not continue to increase linearly with electric field at higher fields. On the contrary, the velocity, plotted as a function of field, starts to level off, and finally saturates at a value v_{sat}. For electrons and holes in silicon, the value of v_{sat} is about $1x10^7$ cm/sec at room temperature. Several models have been used for drift velocity v as a function of electric field E. One of the most common is

$$v = \frac{\mu_n E_y}{\{1 + (E_y / E_c)^n\}^{1/n}}$$

In the above equation, μ_n is the low-field electron mobility, Ec ($=v_{sat}/\mu_n$) is the critical field determining velocity saturation, and Ey is the electric field in the direction of motion of the electrons (the lateral y direction in case of the MOSFET). The above equation yields $v=\mu_n E_y$ for

low fields, v=vsat for high fields. The value of n typical lies between 1 and 2, and is chosen is so as to match experimentally data most closely.For very small values of L, the value of V_{Dsat} is almost zero, this is understandable since it says that the velocity is saturated in the channel even for small drain voltages. The drain current ID is then always saturated, and is given, from equation approximated by $I_{Dsat} = WC_{OX} v_{sat} [V_{GS} - V_T]$ The drain current is independent of L, that is, no matter how small L is made, the current does not increase beyond a point as velocity saturation finally limits the current. This implies that decreasing L will not improve performance (higher currents and speeds) in future technologies as it has done so dramatically in the past(see in figure 1.10). Further, note that the drain current is linearly, not quadratically, dependent on (V_{GS}-V_T) in saturation for the ultra-short channel transistor

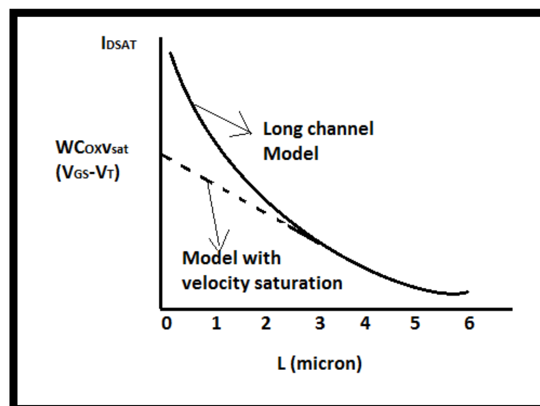


Figure 2.10 *Plot of Id versus channel length L. Note that, unlike the ling channel model which predicts ever-increasing I_{DSAT} as L reduces the model with velocity saturation shows only finite increases.*

2.4.3.Mobility Degradation

Velocity saturation, which we explored in the previous section, is equivalent to a reduction of mobility at high electric fields in the direction of motion of the carriers. In addition to this mobility degradation, there also exists a reduction of mobility due to transverse electric fields, that is, due to the field emanating from the gate. This is a “short-channel” effect only in as much the vertical fields increase significantly as the oxide thickness scales down together with channel lengths.

Physically, the reason that the transverse fields affect lateral current flow is as follows. Carriers in a MOSFET flow in the thin inversion layer near the surface of the silicon. They undergo frequent scattering events with the surface (particularly when it is microscopically “rough”), as well as additional columbic scattering due to interface states and charges in the insulator close to the interface. These effects conspire to make the so-called “inversion-layer” or surface mobility less than the bulk semiconductor mobility (typically about half). Now as the device scales down, the increased vertical fields pull the carriers towards the surface more strongly, where they undergo more frequent scattering. This increased scattering reduces the mobility of carriers further, and the larger the transverse field the lower is the mobility.

It has been found experimentally that the mobility for electrons as well as holes in silicon can be written as

$$\mu = \frac{\mu_0}{1 + (\theta E_{eff})^v}$$

Where E_{eff} is an effective transverse electric field describes below, $\mu 0$ is the mobility without the transverse field effect, and v is a factor between 1 and 2. The above form of the equation was first proposed by Sabnis and Clemens and this or similar forms have been observed by many researchers since. Note that the above form of the equation has a physical origin, and can be derived using Mathiessen’s rule. Let $\mu 0$ be the mobility of channel carriers for low transverse fields, and let μt be the mobility due to extra scattering caused by vertical fields. Assuming that the latter scattering increase with effective field as E_{eff}^v, we can write

$$\frac{1}{\mu} = \frac{1}{\mu_0} + \frac{1}{\mu_T} = \frac{1}{\mu_0} + KE_{eff}^v$$

Which gives the desired equation for μ.

A plot of ID versus VGS (on a linear scale) for small values of VDS, which is often used to find the threshold voltage, is now affected by the mobility degradation. Instead of a straight line with intercept VT and slope μn, we now see a curve gently drooping downwards for increasing VGS due to mobility degradation see in Figure 1.11. This is very commonly seen in measurements,

and the variation of slope with VGS can be used to estimate μ_{eff}as afunction of(V_{GS}-V_T). The measurement of threshold voltage is usually done by finding the intercept of the tangent at the point of highest slope.

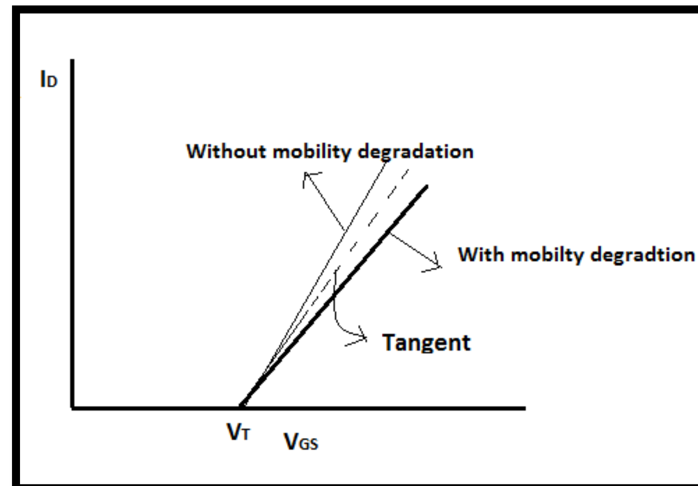


Figure 2.11 *Degradation of transfer characteristics due to mobility degradation*

2.4.4 Hot Carrier Effects and Impact Ionization

As channel lengths reduce, the lateral electric field increases, if applied voltages remain the same. This causes carriers flowing along the channel to gain energy and become "hot". The hot carriers can cause impact ionization, which produces extra hole electron pairs. This produces extra drain current, and also a substrate current consisting of the ionization-generated holes which flow towards the substrate, the most negative point in the transistor. The hot carriers may also gain sufficient energy to surmount the potential barrier at the silicon-insulator interface, and get injected into the insulator.

Due to the high electric field in the channel, electrons, which constitute the drain current in n-channel transistors, can get hot. If some of these electrons get sufficiently heated up – more than the 3.1 eV barrier Φox between silicon and silicon dioxide conduction bands – and also have their momentum directed (through an elastic collision) towards the interface, then these electrons can get injected into the insulator.

Furthermore, some of the holes created by impact ionization may also get heated up and be injected into insulator (though this process is more difficult for holes than for electrons, given the larger 4.9 eV barrier for holes at the Si/SiO2 interface). The holes and electrons flowing into the insulator cause several problems, including electron and hole trapping, interface state generation, and generation of bulk and "border" traps in the insulator.

2.4.5 Avalanche breakdown and parasitic bipolar action

As the electric field in the channel is increased, due to high energetic hot electrons, the avalanche breakdown occurs in the channel at the drain. This avalanche breakdown increases the current as in a p-n diode. The electrons are attracted by the drain, while the holes enter the substrate to form part of the parasitic substrate current.

In addition, there is parasitic bipolar action taking place. The region between the source and the drain can act like the base of an n-p-n transistor, with the source playing the role of the emitter and the drain that of the collector. The positive feedback between the avalanche breakdown and the parasitic bipolar action results in breakdown at lower drain voltage. The substrate current resulting from electron–hole pair generation may overload substrate- bias generators, introduce snapback breakdown, cause CMOS latch-up, and generate a significant increase in the subthreshold drain current.

2.4.6 Gate oxide charging

With the gradual scaling down of device dimension, breakdown of oxides and oxide reliability becomes two major concerns. High electric field in the channel becomes sufficient to heat up the channel electrons to a high kinetic energy such that they can transfer from the semiconductor channel into the gate oxide. These carriers slowly degrade the quality of the oxide and significantly alter the device threshold voltage and may lead over time to failure of the oxide. This type of short-channel effect in low dimensional devices is termed to as time dependent destructive breakdown (TDDB) or hot electron aging. Oxides other than silicon dioxide having larger dielectric constants have been considered as alternate oxides and are typically referred to as high-k dielectrics. Due to the larger dielectric constant of these high-k dielectrics, the same gate capacitance can be obtained with a thicker oxide. However, the challenge in using these

alternate oxides lies in obtaining the same stability, reliability and breakdown voltage as silicon dioxide. Oxides of interest include Al2O3, ZrO, TiO and HfO2.

Channel-length modulation

The channel-length modulation (CLM) is caused in a short channel MOSFET due to the shortening of the effective channel length of the transistor because of the increase in the drain depletion region with the increase in drain voltage. The resulting channel length is approximately equal to the metallurgical channel length minus the source and drain depletion region width. This result in an output conductance defined as the nonzero slope of the drain-current versus drain-voltage for the device.

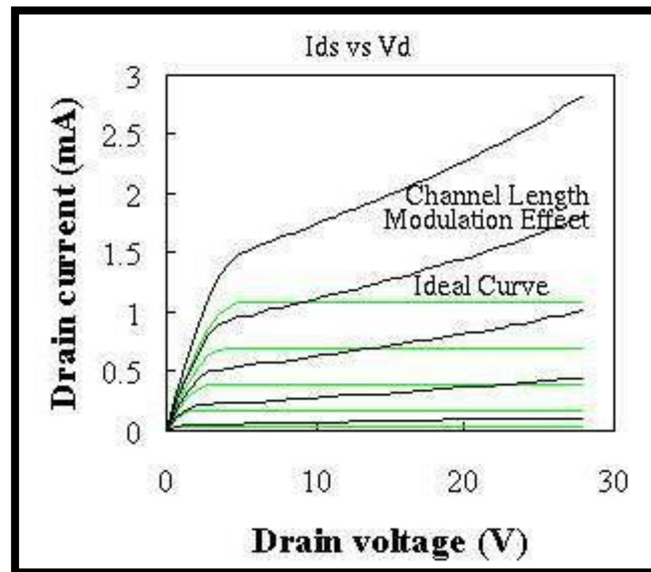


Figure 2.12 *Actual vs Ideal IDS-VDS graph*

The observed current I_{DS} does not saturate, but has a small finite slope as shown in fig 2.12. This is attributed as channel length modulation. This in MOSFET is caused by the increase in depletion layer width at the drain as the drain voltage is increased. This leads to a shorter channel length (reduced by ΔL) and increased drain current. When the channel length of MOSFET is decreased and MOSFET is operated beyond channel pinch-off, the relative importance of pinch-off length ΔL with respect to physical length is increased.

2.5: Solutions to Limitations of CMOS

Importance of Subthreshold Slope in Low Power Operation

Threshold voltage reduction increases the transistor leakage since a significant subthreshold current occurs during the off state of the transistor. This current has impact at the circuit level, since it is a fixed current contributing from all the devices in the off state. A subthreshold current of 10 nA at V_{GS}= 0 is insignificant for a single device, but in a 100 million transistor IC the impact on the overall power consumption is significant. Some technologies have MOSFETs with two different V_{Th}'s to solve the problem. The high speed devices with lower V_{Th} contribute significant higher leakage and are used in critical path where speed is important. Circuits where speed is not important are designed with higher V_{Th} transistors, reducing the overall power leakage.

Thus the no scalability of subthreshold slope of MOSFET to reduce , so that supply voltage could be scaled down as per Dennard's scaling Rule enabling less power dissipation has lead to think of alternative to MOSFET.

So why not design conventional MOSFETs with S < 60 mV/decade at room temperature? The answer to that question comes down to the way in which conventional MOSFETs produce their current in the subthreshold region. First, it is necessary to understand the Fermi-Dirac distribution function, which describes the probability of the occupation of energy levels byelectrons. This function is presented in Figure 1.16, plotted against E-EF, so that the probability of energy level occupation is 50% at E-EF = 0 eV, or in other words, where the electron energyis equal to the Fermi level. At absolute zero, the Fermi-Dirac distribution function would be 100% for energies less than the Fermi level, and 0% for energies more than the Fermi level, and the function would be perfectly abrupt.

The Fermi-Dirac distribution function can be represented mathematically as

$$f(E) = \frac{1}{1 + e^{(E - E_F)/KT}}$$

For conventional MOSFETs operating in the subthreshold region, as the gate voltage increases, the rate of increase of carriers in the channel is determined by this function, which is limited by kT/q. The Fermi-Dirac probability can be seen in the MOSFET subthreshold current equation

$$I_d \alpha e^{\frac{V_{GS}-V_T}{m(kT/q}\,)}$$

Where the term limits the rate of increase of the current with applied gate voltage. Solving for the swing, the term coming from the Fermi-Dirac distribution once again appears, and here serves as the determining factor for the well-known limit of 60 mV/decade at room temperature for conventional MOSFETs.

$$S = \frac{dV_g}{d(\log I_d)} = \ln(10)\frac{mkT}{q}$$

Where *m* is the body-effect coefficient, whose value is close to 1 for a well-optimized device. To be more precise, $m = 1 + C_{dm}/C_{ox}$ where $C_{dm}$is the bulk depletion capacitance at threshold, whenϕ_S =2ϕ_F. In an optimized MOSFET with very good gate control, $C_{ox} >> C_{dm}$, and *m* is slightly greater than 1. Then the above equation becomes S = ln(10) X 26 mV, or about 60 mV/decade. Since the subthreshold swing is inherently tied to the physical mechanism by which current is generated inside the device in subthreshold, in order to change this limit for swing, it is necessary to change the physical mechanism of the device. In the next section, A new type of devices will be introduced that do not generate their subthreshold current in the same way, and that therefore are not confined by this limit on subthreshold swing. This is Tunnel Field Effect Transistor.

Nowadays, there is a renewed interest in exploring devices that use tunneling for their on-current. In particular, there is a focus on devices which act as FETs, where a change of gate voltage turns the current on and off, but which use BTBT in their on state, as well as in the transition between off and on states. These devices have the potential for extremely low off

current and present the possibility to lower the subthreshold swing beyond the 60 mV/decade limit of conventional MOSFETs.

2.6. Tunneling Mechanism

Tunneling mechanism is a quantum mechanical process where electrons move through potential energy barriers. Band-to-band tunneling is the effect when electrons travel from the vb to the cb (or vice versa) across the energy band gap. This inter band tunneling mechanism has been used in P-I-N structure TFETs and shown to have a steeper slope . In spite of this steep slope, the on state current of the TFET is much lower than conventional MOSFETs. In order to achieve an increase in the on current a careful study of the tunneling mechanism is required.

Understanding the nature of band-to-band tunneling which is important for determination of the approximations made in different simulation models. This understanding is also useful when optimizing design parameters of TFETs for maximum performance.

2.6.1 Advanced tunneling models

In semiconductors, two different models are used to calculate the current resulted from tunneling – local and non-local models. In non-local models, tunneling treat as a process that occurs in spatial coordinates, where electrons tunnel from one point to another, as shown in Figure 2.13 Therefore, the WKB approximation and Landauer's tunneling formula that we have considered earlier can be classified as non-local models. Local models, treat tunneling as a phenomenon existing from band to band in the *E–k* space of the material.

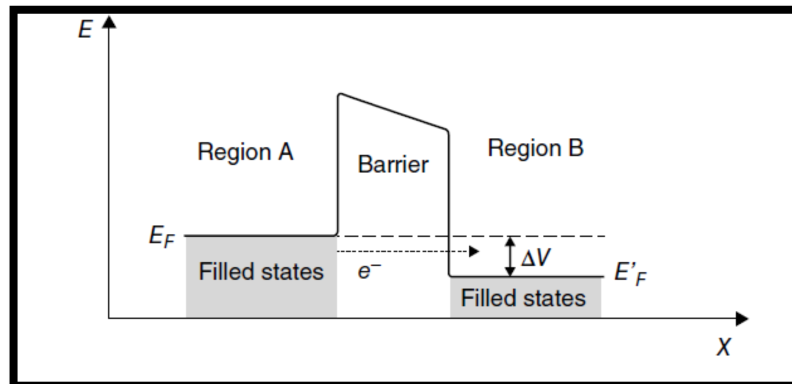


Figure 2.13 *Regions divided by a potential barrier with external bias. Empty states exist in Region B, to which electrons can now tunnel.*

2.6.1.1Non-local tunneling models

Since the non-local models approach tunneling from a spatial perspective, we need to know the spatial dependence of all the parameters in Schrodinger's equation to obtain the tunneling probability. If an external bias is applied to a semiconductor, the shape of the potential barrier $V(x)$ is complicated. The band structure of the semiconductor also needs to be incorporated into the potential $V(x)$ in Schrodinger's equation. Moreover, the potential in the semiconductor depends on the current (Ohm's law), while the current in turn depends on the shape of the potential barrier (Schrodinger's equation). All these complicated spatial dependencies make it difficult to solve Schrodinger's equation analytically.

Therefore, numerical approaches need to be applied to obtain a solution for calculating the tunneling probability. However, because all these complex dependencies are incorporated, non-local models provide an accurate estimation of the current in the device although they are difficult to solve analytically. As non-local models cannot be used to obtain analytical models, they are used in device simulation. on the other side, analytical models are essential for use in circuit simulation and to understand the functioning of devices. To develop analytical models, we use local tunneling models.

2.6.1.2 Local tunneling models

To understand local models, let us consider the problem from an energy band perspective. Semiconductors have various energy bands, which result from the interaction of the individual fields created by the atoms in its lattice. These energy bands are usually represented in an E–k diagram, which shows the allowed values of energy E that the electron can take. The E–k diagram of an intrinsic direct bandgap semiconductor. We can observe the presence of a valence band and a conduction band, separated by the bandgap – a potential barrier.

Since we have considered an intrinsic material, there are very few electrons in the conduction band. In the presence of an external electric field, these few electrons will flow to generate a very low current. However, if this electric field is sufficiently large, it is possible for electrons to tunnel from the VB to the CB without a change in energy, as shown in Figure 2.2. In other words, the electric field causes the bands in the semiconductor to be modified in such a way that the electrons in the valence band can tunnel through the potential barrier (the bandgap) and reach

the conduction band. Now that there are plentiful electrons in conduction band due to tunneling, an appreciable current can flow in the material.

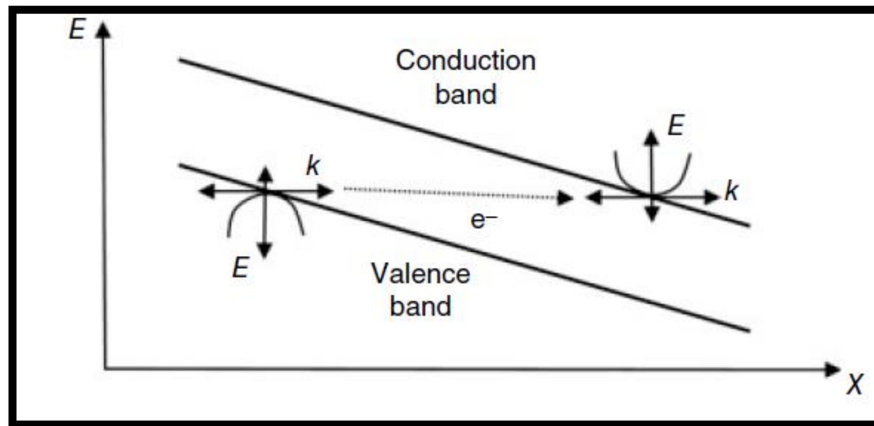


Figure 2.14 *Energy bands of a semiconductor with an electric field, with inset E–k diagrams. Non-local occurs, with the electron transitioning from the valence band maxima to the conduction band minima in the E–k diagram. Band to Band tunneling.*

An important approximation made while deriving local models is that where electric field is assumed to be constant, which is rarely true in a real device. Because of the assumption of a constant electric field, local models predict a single tunneling rate throughout the device. In case the electric field is position-dependent, we estimate the tunneling rate using the local electric field at every point in the device.

The tunneling rate at each point is then integrated throughout the device to give the total number of electrons that have tunneled from the source's valence band to the conduction band of channel. Since no generation or recombination is assumed, the total current is dependent only on the rate at which the electrons tunnel from the unoccupied valence band to the occupied conduction band. Therefore, in local models, it is assumed that each electron that reaches the conduction band is swept away to form a part of the total current.

Local models are broadly used in analytical modeling of TFETs as they give an analytical expression for the tunneling rate at each point.

2.5.2 Kane's model

This model is innovated by E.O. Kane in 1959 , this is one of the oldest and most widely used models for calculating the BTBT tunneling rate in TFET models.

The derivation of Kane's model is very complicated. However, a brief summary of the procedure followed in the paper is presented below.

As mentioned in the preceding section, we will be approaching tunneling as a Phenomenon occurring in the *E–k* diagram rather than in the spatial coordinates. We would, therefore, need to reframe Schrodinger's equation accordingly. In this new representation of the Schrodinger equation, there must be no spatial terms.

The terms that depend on space in Schrodinger's equation are: (i) the derivatives

That are with respect to spatial coordinates and (ii) the spatial dependence of the External potential $V(x)$. These spatial terms must now be reframed as functions of Either energy E or momentum k. This reformulation of Schrodinger's equation is done by using Bloch functions. Therefore, let us go through a brief introduction to Bloch functions. Semiconductors are crystalline solids, having a periodic structure. Due to such a structure, the atoms of the crystal produce a periodic potential *Vper* with the same periodicity as the crystal. When this potential *Vper*is substituted into the time-independent Schrodinger equation, we get

$$-\frac{\hbar^2}{2m}\frac{\partial^2\psi}{\partial x^2}+V_{per}\psi = E_n\psi \quad \text{.........(2.1)}$$

Note that we have added a subscript n to the energy, since different energy bands in the crystal correspond to different energies. In solid state physics, the solutions to the above Equation (2.1) are known as Bloch functions $\psi_{n,k}$. With this brief idea of Bloch functions, let us proceed with the derivation of Kane's model.

First we will consider the familiar Schrodinger equation in spatial coordinates for our particular physical situation, which is a crystal lattice (the semiconductor) to which an external bias is applied. The potential term $V(x)$ in Schrodinger's equation will, therefore, be a sum of the contribution due to the crystal lattice (*Vper*) and the contribution due to the external bias (*Vext*). It is assumed that the external bias *Vext* leads to a uniform electric field *Eext*in the crystal lattice.

Since the potential due to a uniform electric field is linear ($Vext= -qEextx$), we can write the time-independent Schrodinger equation as

$$-\frac{\hbar^2}{2m}\frac{\partial^2\psi}{\partial x^2}+(V_{per}-qE_{ext}x)\psi = E\psi \quad \text{.......(2.2)}$$

We will now use the Bloch functions to convert Schrodinger's equation from this spatial form to what is known as the crystal momentum representation. The crystal momentum representation is simply another form of Schrodinger's equation without any spatial dependence. In this representation, every operator and wave function in Schrodinger's equation is written as a linear combination of the Bloch functions. For decomposing the wave function ψ into a linear combination of Bloch functions, we only need to substitute the equation for a general wave function (2.2) into Schrodinger's equation, which will give

$$\Sigma a_n(k)\left(\frac{\hbar^2}{2m}\frac{\partial^2\psi_{n,k}}{\partial x^2}+V_{per}\psi_{n,k}\right)-\Sigma a_n(k)qE_{ext}x\psi_{n,k}=\Sigma a_n(k)E\psi_{n,k}$$

.......(2.3)

By comparing with Equation (2.1), we can observe that the term in the brackets is the energy of the *n*th band *En*. Making this substitution, and writing the equation for a single band, i.e. a single *an*(*k*), we get,

$$a_n(k)E_n - a_n(k)qE_{ext}x = a_n(k)E \quad \text{..............(2.4)}$$

Note that there are two terms corresponding to energy in the above equation –*En* corresponding to the energy solely due to the crystal and *E* corresponding to the total energy of the electron. We have now decomposed the wave function interms of Bloch functions, leaving the position operator *x* as the only spatially dependent operator in Equation (2.4). Therefore, to make Schrodinger's equation completely spatially independent, we now need to decompose this operator *x* in terms of energy *E* and momentum *k*.

2.7: TFET: Basic structure and operation

An essential area of focus in semiconductor technology, and devices in particular, is the continuous scaling down of the device dimensions. We have come a long way in this pursuit – from gigantic vacuum tubes that led to computers the size of large rooms, to the first MOSFET with a gate length of 300 μm, to transistors with gate lengths of14 nm or less. This has led to integrated circuits containing billions of transistors.As the device dimensions were reduced to 50 nm and the power supply to 0.5 V, the OFF-state power consumption of MOSFETs became a major challenge. The drain current of a MOSFET is controlled by the thermionic emission from the source into the channel. As the gate voltage increases, the potential barrier between the source and the channel decreases, leading to an increase in the drain current. This leads to two problems – a larger OFF-state current due to subthreshold conduction and a higher subthreshold slope. The subthreshold slope(*SS*) of a MOSFET is the change in gate voltage V_G required to increase the drain current I_{DS} by a factor of 10. A lower subthreshold slope would allow for a higher ratio of ON-current to OFF-current (I_{ON}/I_{OFF}), and would lead to a lower power dissipation in the OFF-state.

Basic operation

Figure 2.15 shows the basic structure of an p-channel-TFET and n-channel -TFET. The device has three regions – the source, the channel and the drain. Comparing the structure of an n-channel TFET with that of an n-channel MOSFET, the source doping in a TFET is p-type, whereas it is n-type in the MOSFET. This is the only major difference between a TFET and a MOSFET. The channel region in the TFET is usually intrinsic, or very lightly doped.

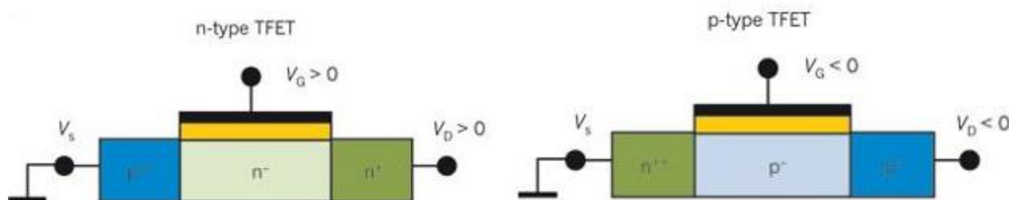


Figure 2.15 *n-Type TFET and p-Type TFET*

Operation

The TFET device is functioned by applying gate bias so that electron buildup occurs in the intrinsic section. At ample gate bias, BTBT (band-to-band tunneling) happens when the conduction band of the intrinsic region brings into line with the valence band of the P-region. In valance band, the flow of electrons In the p type region channel into the conduction band of the intrinsic region and the flow of current across the device. As the gate terminal bias is reduced, the bands develop misaligned and the flow of current is no longer flow.

Off State

The TFET is in OFF-state when the drain voltage $V_{ds} > 0$ and the gate voltage $V_{gs} = 0$, which is similar to the OFF-state of a MOSFET. In the OFF-state of the TFET, any charge carriers present in the conduction band of the channel would have a tendency to drift to the drain and thus generate a current. However, as the source is p-type, there are very few free electrons in its conduction band, and therefore very few electrons can be injected into the channel. This leads to a negligible OFF-state current. However, in the case of a MOSFET, the source is n-type and has free electrons in its conduction band. Through thermionic emission, a few of these electrons will be injected into the channel over the potential barrier at the source–channel junction. This leads to a higher OFF-state current in a MOSFET as compared to a TFET.

On State

As we increase the gate voltage V_{gs}, the energy bands in the channel change with respect to the source . At a certain value of the gate voltage V_{gs}, the valence band in the source gets aligned with the conduction band in the channel. In the OFF state of the device, the electrons in the valence band of the source did not have any available energy state in the channel into which they could tunnel. Now that the valence band of the source is aligned with the conduction band of the channel, electrons can tunnel from the former into the latter through the potential barrier formed by the bandgap E_g

As the gate bias is further increased, the bands in the channel region are further lowered in energy, and electrons occupying energy levels from the valence band edge of the source , Source to the conduction band edge of the channel , Channel can tunnel to the conduction band in the channel. This leads to a steep increase in the current. In addition, an increase in the gate voltage

not only increases the number of electrons that are able to tunnel but also increases their tunneling probability due to reduced tunneling length. Therefore, the current would vary significantly with a changing gate voltage.

Transfer characteristics

Figure 2.16 shows the transfer characteristics of a TFET in which the source and drain dopings are equal and opposite. The regions of operation discussed in the previous section have been marked on the figure. As we can observe, there is a very low current in the OFF-state of the device, when the conduction band of the channel is not aligned with the valence band of the source. As the gate bias is increased, the current rapidly increases due to reduction of the tunneling width and an increase in the number of initial states in the source from where tunneling can occur. At a higher gate bias, the rate of increase of current reduces since the contribution of the additional initial states in the source valence band is negligible. As the gate bias approaches the drain potential, the rate of increase of current further decreases due to pinning. A similar behavior is observed in the negative bias region.

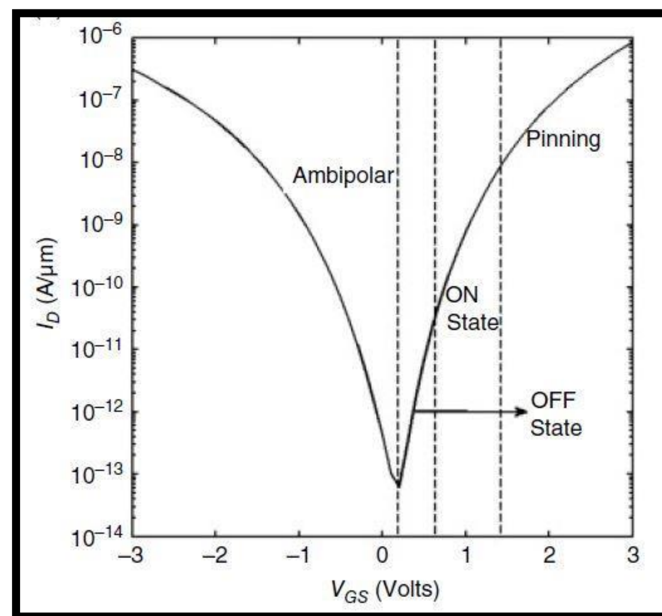


Figure 2.16 *Transfer characteristics of TFET*

Output Characteristics

Initially the gate potential is greater than the drain potential, due to which the channel potential is pinned at the drain potential. Therefore, as the drain potential is increased, the channel potential increases, leading to a significant increase in the current. As the drain potential approaches the gate potential, the channel potential is no longer dependent on the drain potential. Therefore, the current remains nearly constant with increasing drain bias. In this case, the output characteristics are saturated.

The output resistance in the saturation region is much higher in the case of the TFET as compared to MOSFET. Since channel length modulation has a negligible effect on the drain current of a TFET. Moreover, in the saturation region (*Vds>Vgs*), changing the drain voltage has a negligible effect on the channel potential, due to which the drain current due to source–channel tunnelling remains constant.

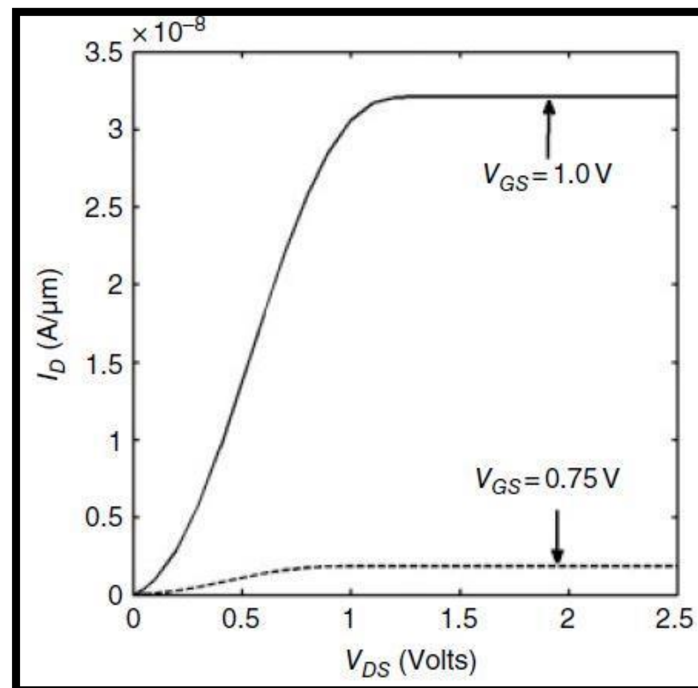


Figure 1.17 *Output Characteristics of TFET*

2.8: Literature review of TFET

The downscaling of conventional MOSFET possess various drawbacks in technological era. To overcome all the bottlenecks in the field of low power,Tunneling mechanism hence come to the subject to be interested. When gate overdrive voltage is decreased, the oncurrent becomelower, which negatively effectson device performances such as lower ION/IOFF ratio and reduce dynamic speed (CV_{DD}/Ion).

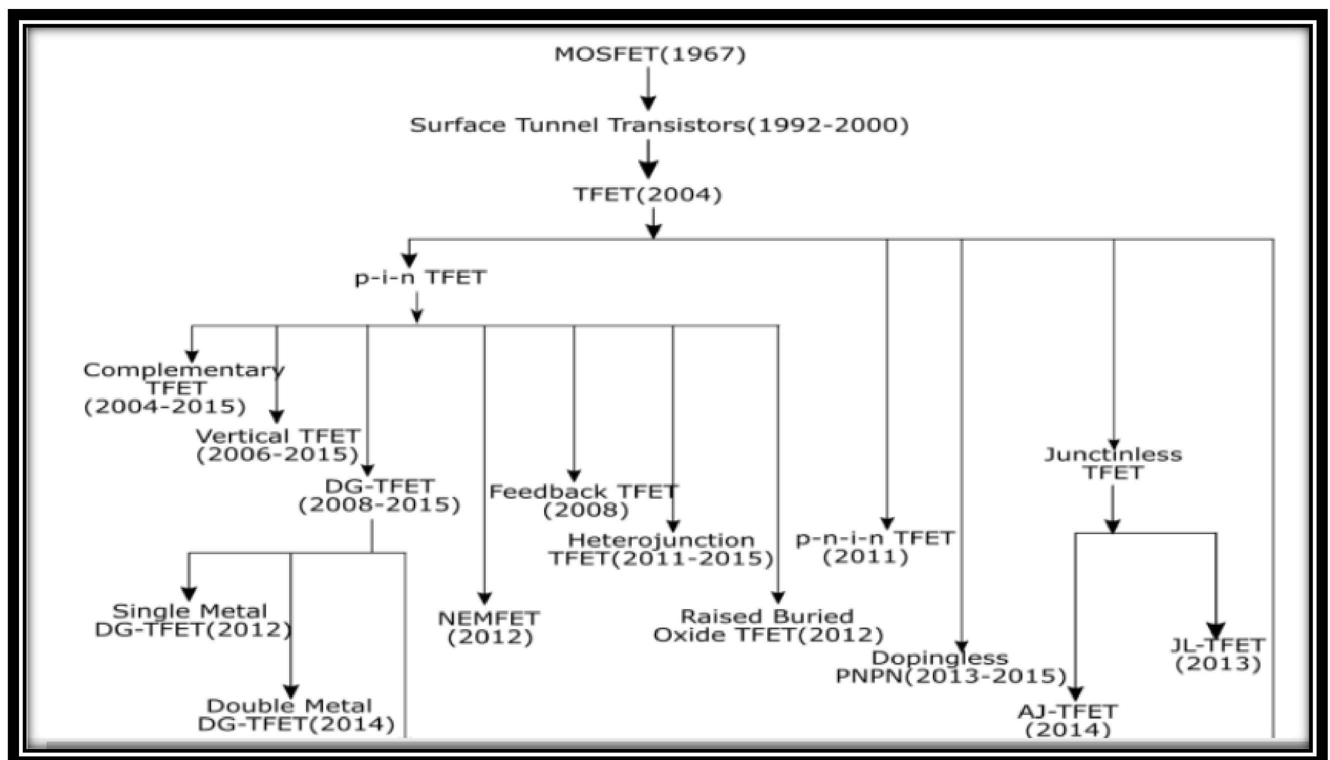


Figure2.18 *Evolution of TFET*

Surface Tunnel Transistors (1992-2000)

T Baba developed this surface tunnel transistor (STT) which is operated for low device length less than 0.1 micron with n+i-p+ doping in source-channel-drain. In this structure drain had a high doping profile in low doped substrate which makes a tunnel junction as carrier

transportation region.The STTs were fabricated by Heterojunction profile like GaAs/AlGaAs. These characteristics of STTs were accounted by inter band tunneling.

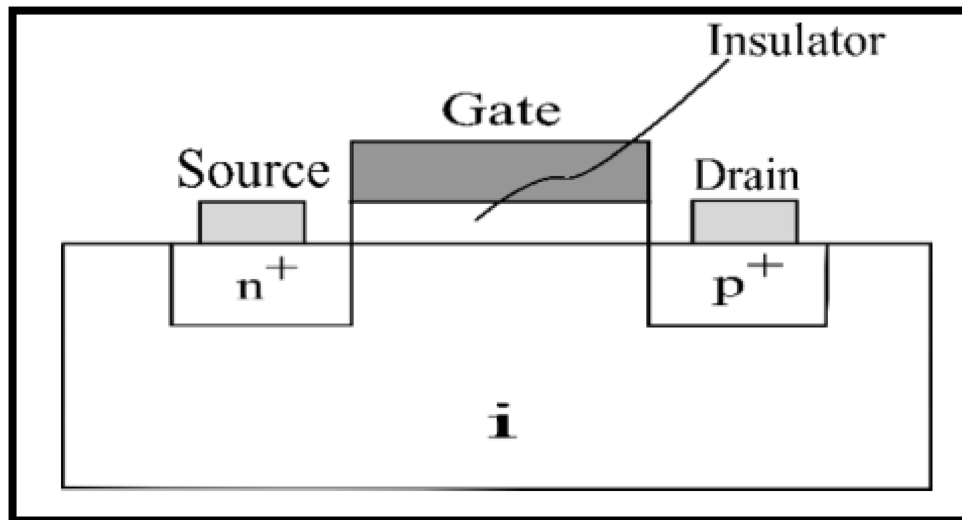


Figure 2.19 *Schematic of Surface Tunnel Transistors*

Gate Engineered TFET:

(i) Single Gate

The tunnelling occurs in this device between the intrinsic and p+ regions. To operate these devices, the p-i-n diode is reverse biased—the source is grounded, and a positive voltage is applied to the drain—and a voltage is applied to the gate. Without a gate voltage, the width of the energy barrier between the intrinsic region and the p+ region is much wider than 10 nm (the approximate minimum for significant tunneling probability), and the device is in the OFF-state. As the positive gate voltage increases, the bands in the intrinsic region are pushed down in energy, narrowing the tunneling barrier and allowing tunneling current to flow.

In order to be consistent with MOSFET technology, the names of the device terminals are chosen such that voltages areapplied in a similar way for Tunnel FET operation. Since a reverse bias is needed across the p-i-n structure in order to create tunneling and since an NMOS operates when positive voltages are applied to the drain and gate, the n-region is referred to as the drain and the p+ region as the source.

(ii) **Gate all around**

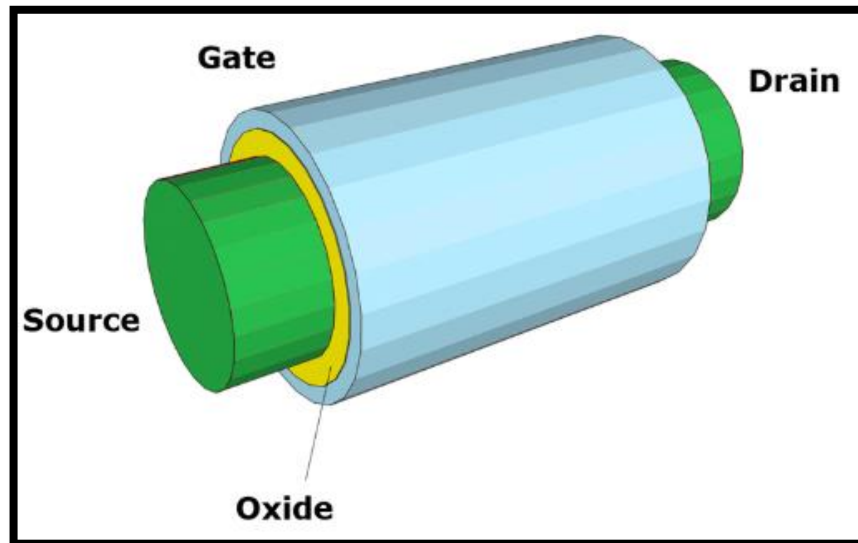


Figure 2.20*Schematic of GAA*

The increased gate control observed in a double gate TFET is further improved in a gate all around (GAA) TFET. Figure 2.8 shows the structure of a gate all around nanowire TFET. It consists of a silicon nano wire of radius 10 nm, surrounded by a gate oxide of thickness 2 nm, covered all around by the gate metal.

Such a structure can achieve a high level of electrostatic control of the gate, as all the field lines originating from the drain can terminate at the gate, without significant penetration into the channel. This leads to a steeper subthreshold slope and diminished short channel effects such as DIBL and threshold voltage roll-off. It also enhances the ON-state current, as this geometry provides a large area for the current to flow as compared to a planar device.

p-n-i-n TFET

Wei Cao discovered a new structure with a narrow n-layer at the tunneling junction. From conventional TFET it has better subthreshold swing and low on current It provides reliability assurance. Reliability issue can be occurred due to tunneling problem at the channel-dielectric interface, where strong electric field in held in parallel and anti parallel directions.

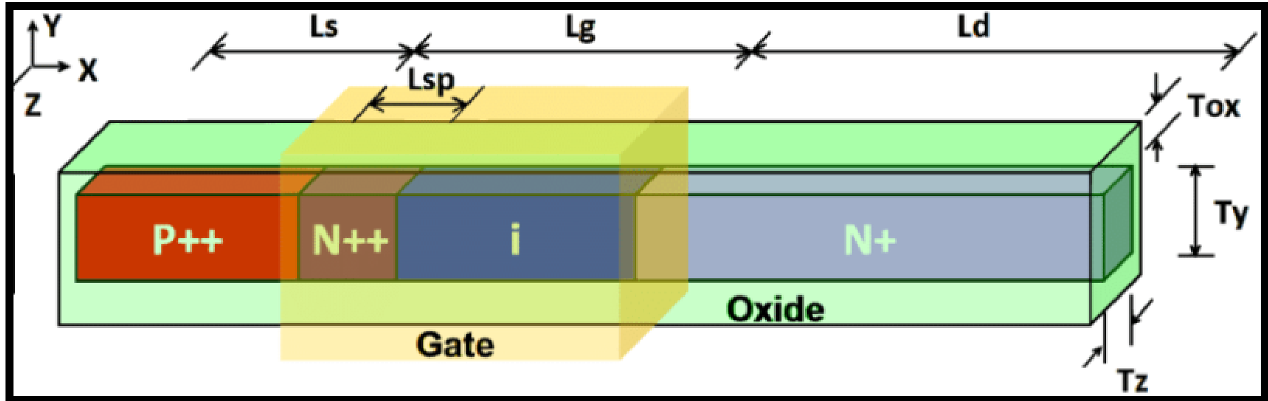


Figure 2.21 *Schematic of p-n-i-n TTFET*

Buried Oxide TFET

TFET has some drawbacks in providing low ON current and high OFF current which can be overcome by adding buried oxide on SOI layer. A hetero gate oxide and SOI structure with Raised Buried Oxide in drain is proposed to achieve ITRS requirement and reduced Miller capacitances.

The following advantages are:

- Increase on current
- Decrease off current
- Increase ION/IOFF
- Decrease miller capacitances

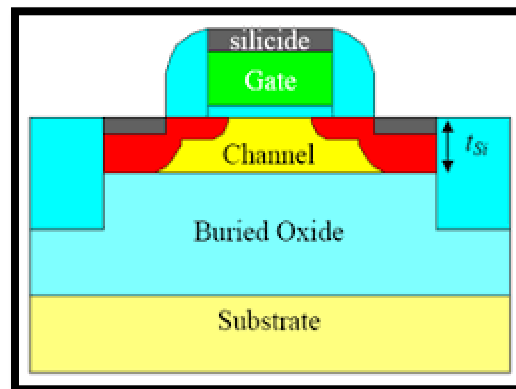


Figure 2.22 *Schematic of Buried oxide TFET*

Double Gate TFET

Figure 2.11 shows schematic diagram of Double Gate TFET. It consists of two gates, one at the top (called the front gate) and the other at the bottom (called the back gate). This configuration improves the electrostatic control of the gate on the channel since now the field lines from the gate terminate at the back gate rather than terminating in the channel. The ON-state current is also increased as compared to a single gate TFET, since there are two channels in which current can flow in the device.

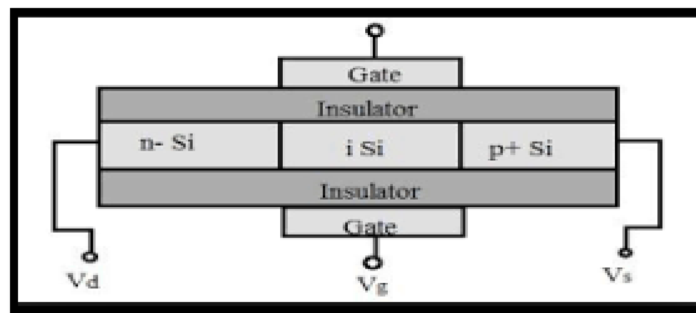


Figure 2.23 *schematic of Double Gate TFET*

Heterojunction TFET

Another TFET structure proposed for achieving a higher ON-current is the Heterojunction TFET made up of III–V materials. Figure 2.12 shows the structure of a heterojunction TFET. It consists of GaAs0.35Sb0.65 as the source material and In0.7Ga0.3As as the channel and drain material, giving us a heteromaterial junction at the source– channel interface. The band diagram of such a device at the surface. As the band diagram of a heterojunction is staggered at the source–channel junction. This leads to a shorter tunneling width, thus leading to an increased ON-current. Also, III–V materials are direct bandgap materials and have a bandgap smaller than Si. This also contributes to the increased ON-state current in heterojunction TFETs.

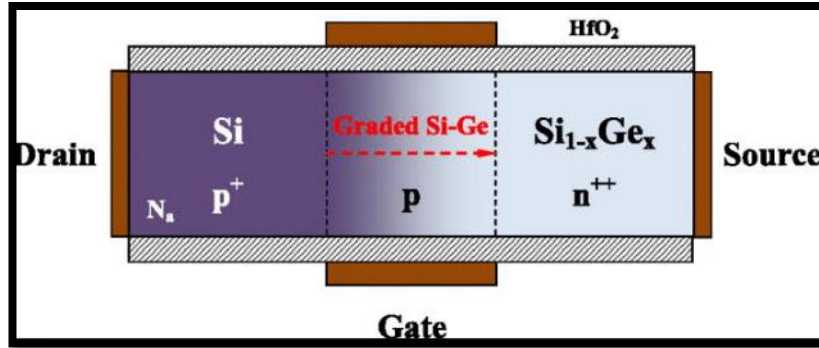


Figure 2.24 *schematic of heterojunction TFET*

Heterodielectric TFET

The device has reduced value of short channel effects and channel length modulation. There are three capacitances in tunnel FET, the capacitance between gate and source (), between gate and drain () and channel. capacitance. Capacitance component results in variable electron concentration, which is a direct function of the dielectric permittivity, and will have a higher capacitance near high-k and a lower capacitance value near low-k material while having a smooth transition. A schematic is shown in Figure 2.13.In ON state, the value of gate to source capacitance is less for double gate TFET and due less potential between drain and channel is gs Cgd having high value. Hetro gate oxides are used to fulfil ITRS requirements.

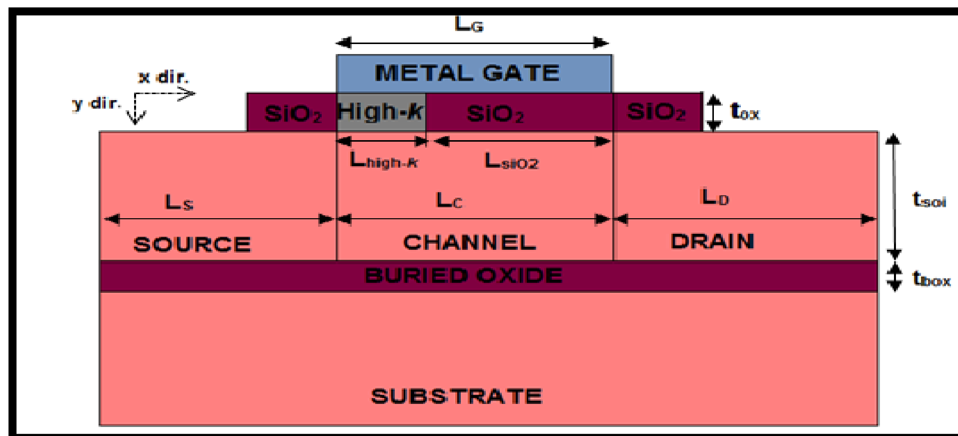


Figure 2.25 *Schematic of Heterodielectric TFET*

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CHAPTER 3

H-Shaped Double Gate Tunnel FET for Low Power Applications

3.1: Introduction

3.2: Device Structure

3.3: Device operation and simulation result

3.4: Surface potential

3.5: Electric field

References

In this chapter, we have proposed a novel H- Shaped Double Gate Tunnel Field Effect Transistor (HDGTFET), which has been analytically modeled and simulated for the first time using SILVACO Atlas. The proposed structure is symmetrical with highly doped p-type source (10^{21}/cm3), n-type drain (10^{16}/cm3), intrinsic channel and same metal work function in the double gates. All the fundamental device parameters such as Electric Field, Surface Potential and Transfer characteristics have been analyzed to demonstrate the tunneling phenomena in the channel region of the HDGTFET structure under various biasing conditions, channel length (L) and oxide thickness (tox).The proposed device exhibits excellent sub-threshold slope of 32mV/decade when the channel length is 30nm along with high ION/IOFF ratio. Reverse band bending is observed from the Electric Field simulations at the channel-drain interface implying suppressed ambipolarity and reduced leakage currents. The low ON-voltage of the proposed device, which is approximately 0.8 V, makes HDGTFET suitable for low power applications. Optimum results were obtained for reduced channel lengths.

3.1: Introduction

CMOS technology has been introduced us with its large application property from several years after its invention. Various devices has been designed and implemented by scaling the size of transistors. But reduced the size of transistor caused some issues which create an adverse effect on device characteristics. So a new technique of electron flow has been come that is Band to Band Tunneling of electron flow near source-channel interface region which provides sub-threshold swing below 60mV/decade and high ON current which is applicable for low power applications. Our proposed device is based on this electron flow mechanism and provides high ON-state current since a large tunneling (BTBT) mechanism is occurred in source to drain region. Various techniques have been developed to improve ON-State current but in this paper double gate H-shaped TFET has delivered relatively high On-State current. Further modification of device is done by varying device parameters which give better SS and ON-State and OFF-State current ratio.

3.2: Device Structure

Our proposed Double gate single metal TFET structure is illustrated in a two dimensional view in the Figure-3.2 in this paper Silicon area (Figure 3.1) provides H-Shape to this proposed structure. SiO2 (Silicon dioxide) is deposited on both side of channel region in this silicon wafer after that metal is deposited on oxide layers. The structure enacted as a symmetric TFET. Both gates have equivalent metal gate electrode include same work function. Gates with work function 4.8 eV is used here.

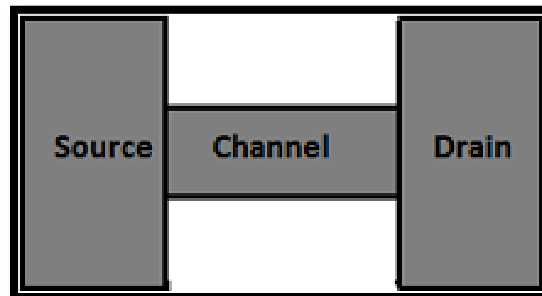

Figure 3.1 *H-Shaped Silicon area*

The channel is taken here as intrinsic or uniformly lightly doped p-type whereas source is highly doped p-type and drain is n- type. 't_{fox}' is front gate oxide thickness, and 't_{box}' is back gate oxide thickness. 'L' is represented as channel length in this schematic figure (Figure 3.2) of this structure. 'tsi' is channel width.

The Electronic Design Automation based software SILVACO simulation has been performed by using 2D ATLAS device simulator. This Silicon Oxide Insulator (SOI) TFET has initial channel length (L) 40nm and oxide thickness for both t_{fox} and t_{box} is 2nm (shown in Figure 1(b)) and 1nm between channel and metal. Initial channel width is 10nm. The source is doped at p-type 10^{21}/cm3 and drain is doped with n-type 10^{16}/cm3 respectively.

3.3 Device Operation and Simulation Analysis

Figure 3.3 and 3.4 shows the tunneling condition at off- state and as well as on state condition respectively. For getting device operation we have performed Simulation of our proposed device structure by Silvaco 2D modeling. We can see from the following figure (Figure 2(a)) that at off state condition there is no tunneling occurred at the source-channel region which implies that no operation is placed implies that device is switched off.

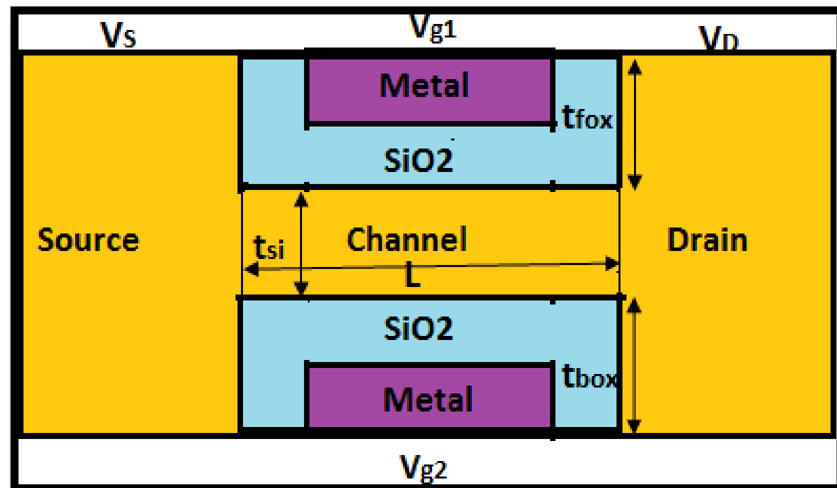

Figure 3.2*Two dimensional view of proposed TFET*

After the device is ON negative ions i.e. electron is started tunneling from source to channel region through BTBT tunneling mechanism. Source is highly doped than drain to reduce ambipolar nature for negative gate bias.

We can observe that the electron and hole concentration is 1021/cm3 and 1016/cm3 respectively in ON condition at VGS=0.8 V. The above device has intrinsic channel region which represents a p+ -i- +n TFET structure. Electrons as carriers are tunneling from valence band of p+ region i.e. source to conduction band of channel due to low barrier near source channel junction and create an abrupt p-n junction near source channel interface. Enhanced positive gate voltage cause more tunneling which cause more band bending at source channel junction that means more energy (electron) transfer from valence to conduction band which caused more current flow from drain region to source region. The advantage of this device is high ON current which is 10-3 A at low ON voltage which provides low power dissipation.

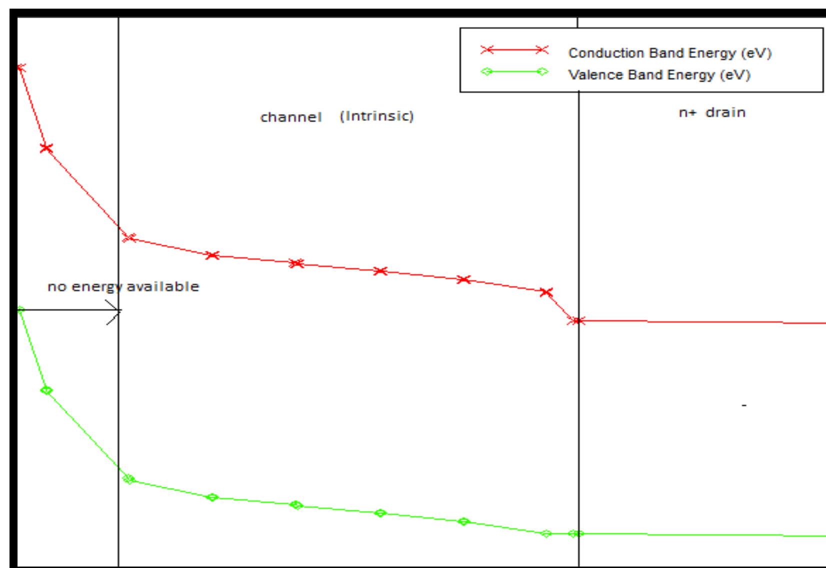

Figure 3.3 *Energy band diagram at off-state condition*

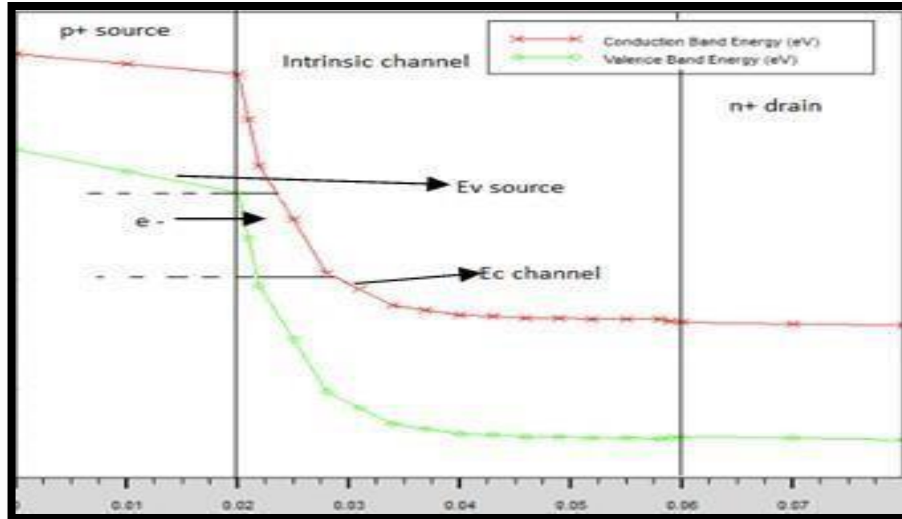

Figure 3.4 *Energy band diagram at on-state condition*

Figure 3.5 shows electric field analysis of our simulation result. Generation of electrons is more at source-channel region. SiO2 is low dielectric material through which some electron flow is occurred near source-channel region.

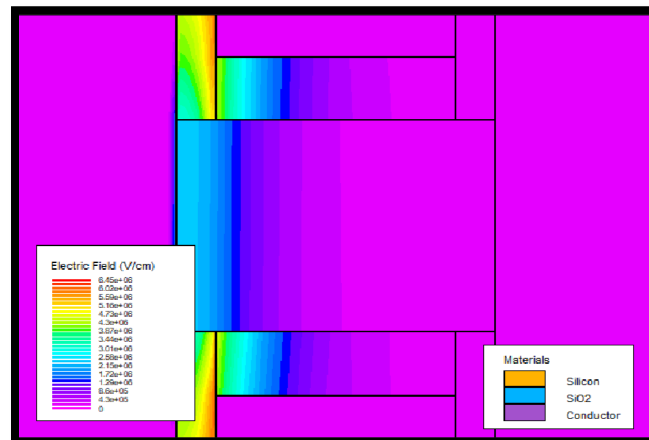

Figure 3.5 *Electric field profile of proposed device under V_{GS}=-2.0V to V_{GS}=2.0 gate bias voltage*

As gate voltage is much greater than drain voltage, the enhance of inversion layer in n+ drain region leads to channel potential which is approx to drain potential, as shown in Figure 4.The Advantage of using double gate is getting more current density at drain-channel region as tunneling effect is more which cause more current flow from drain to source. High work function metal is used in both sides to provide better operation in electron tunneling.

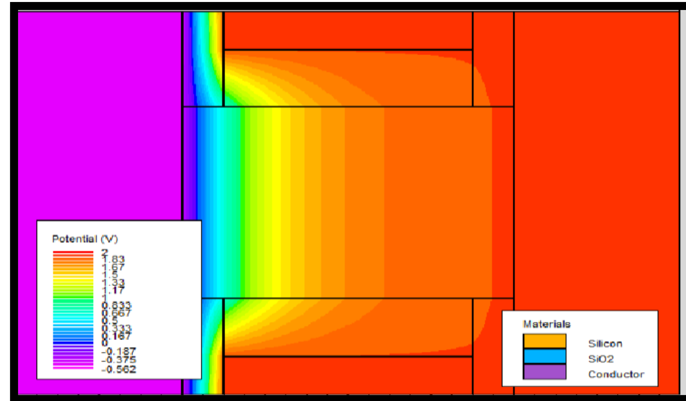

Figure 3.6 *potential profiles towards drain*

The proposed device is optimized by varying channel length and oxide thickness. Initially oxide thickness is 1nm in metal-channel interface, now it is enhanced to 3nm, Which causes to reduce the rate of current flow as electron tunneling rate at source channel region, is reduced due to increase of oxide layer and channel width is also reduced , since device is ON after applying much higher voltage that require more operating power consumption.

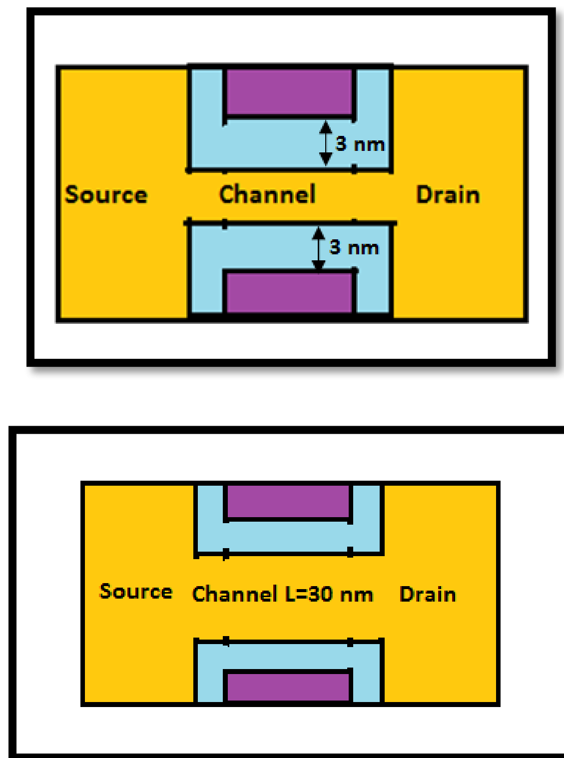

Figure 3.7 *2D view of further modification of proposed device*

Again, if we reduce the channel length (L) from 40nm to 30nm we obtain better ION/IOFF and SS .It can be analyzed from figure 6(a) that at initial condition when channel length=40 nm ON current is 10-3 and after further improvised the channel length i.e. L=30nm ON current is 10^{-2}. Sub threshold swing (SS) is reduced to 32mV/decade which is better than initial condition.

Transfer characteristics and DC performance of modulated proposed device is also analyzed in this section. The resulted Id-Vg graphs are shown in this section. It can be observed that ON current is 10^{-3}A/micron and OFF current = 10^{-17} at the initial condition due to the lower oxide thickness. Sub threshold swing (SS) is 38mV/decade, after reducing channel length we observed better ION/IOFF =1016 which produces more suitable TFET structure. That means more BTBT in source channel region and more current flow.

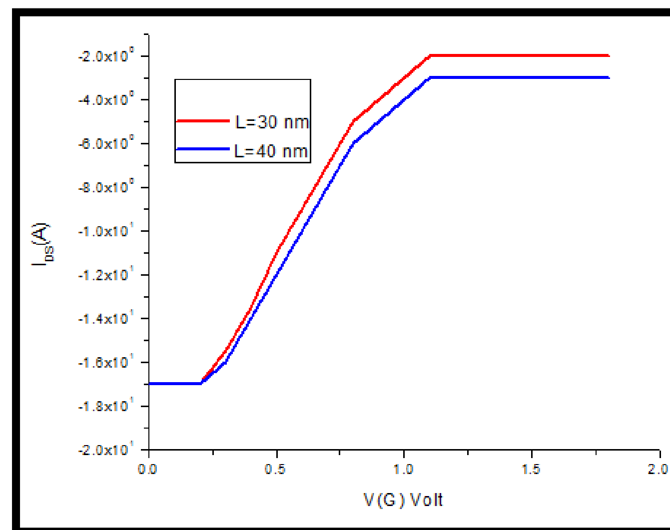

Figure 3.8 *Transfer characteristic for different channel length*

The device is ON at very low voltage (VGS=0.8 V) which is an advantage in applications for low operating power devices. At very low operating voltage BTBT tunneling rate is higher enough to provide high flow of current from drain to source which gives steep switching characteristics to this device.

3.4 Surface Potential

Surface potential profile along channel gate region of HDGTFET is made of double metal of same work functions. Due to variation of the oxide layer for both top and bottom of the gate metal, surface potential is optimized and it is shown in figure 3.10

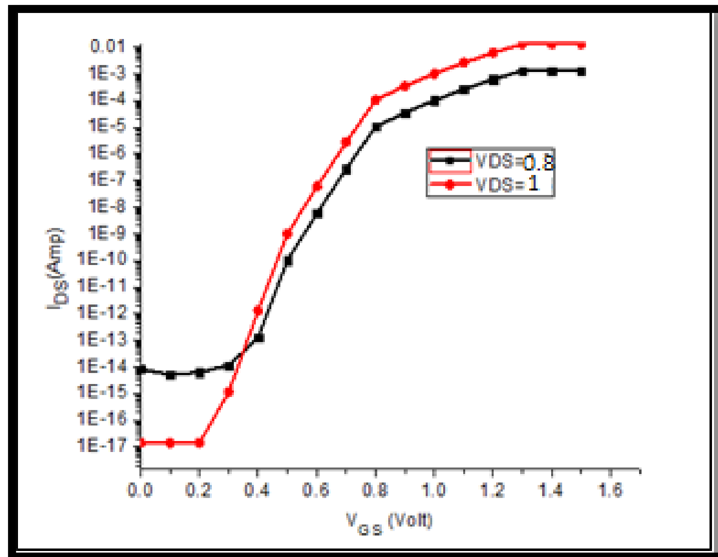

Figure 3.9 *Transfer characteristic for different drain voltages*

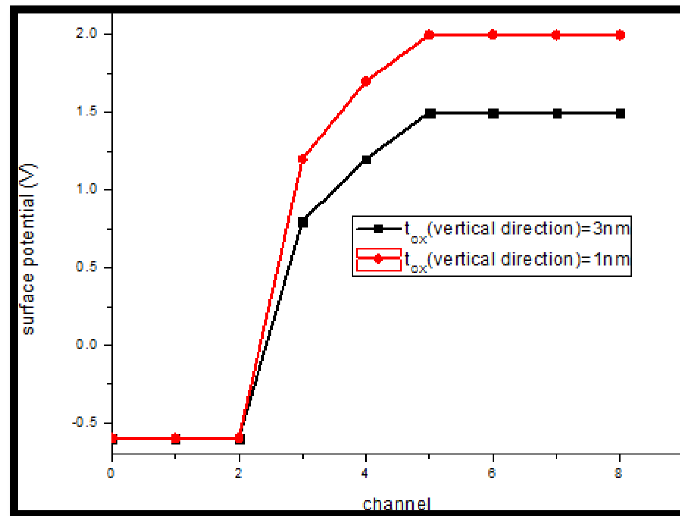

Figure 3.10 *Surface potential for various oxide thickness*

In this device channel length is also further modulated and thus surface potential is also varied.

3.5 Electric Field

Electric field is compared with modulated vertical oxide thickness, and different channel length in the following Figure 3.11 and 3.12.

The electric field for modulated device which has 1nm vertical oxide layer from both metal surfaces is compared with 3nm oxide layers for this H-shaped device. It can be observed that electric field is higher for lower oxide thickness, since the tunneling in source-channel junction is decreased and less band bending is occurred. Thus tunneling probability is decreased, which is not good for device operation. And also it can be elaborated that reduced reverse tunneling for both oxide layers provide suppressed ambipolarity and reduce leakage current. But it also can be observed that after certain increasing of oxide layer may increase leakage current and hence ambipolar conduction can be occurred.

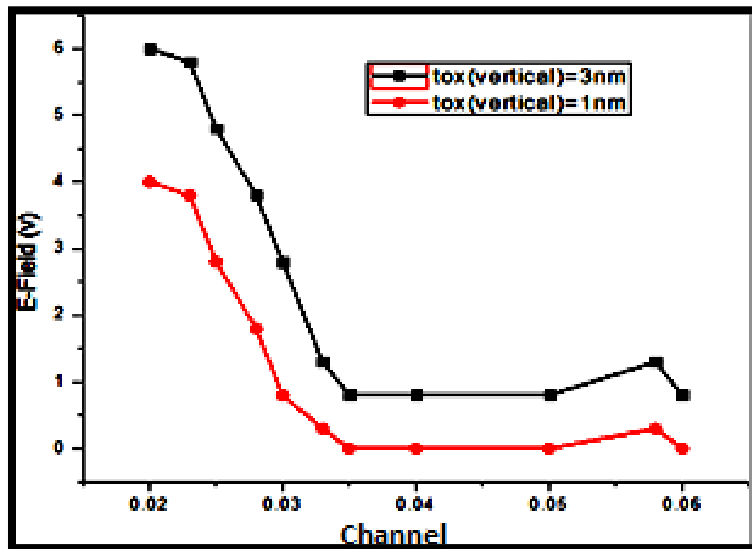

Figure3.11 *electric field profiles along channel length for different oxide thickness*

Electric field is compared in following figure 3.13 with the modulated channel length. As the channel length further reduced to 30 nm electric field is enhanced near source.

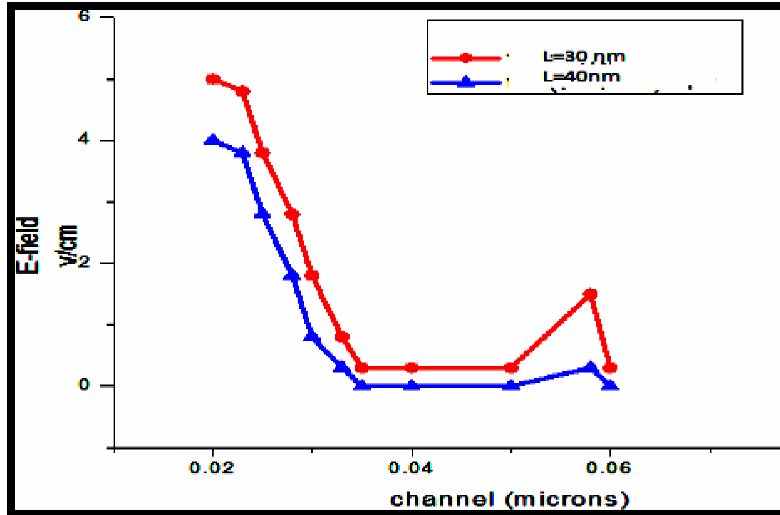

Figure3.12 *Electric field along various channel length*

The present work focuses on DC characteristics, mainly drains characteristics of H-shaped double gate Tunnel Field Effect Transistor to accept this for low power applications and also described the dependencies of ON current, on gate bias, channel length and oxide thickness. This work also features the extraction of device characteristics like electric field along with surface potential for modulated channel length and oxide thickness. This device displays in terms of preferable quality of power efficiencies.

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CHAPTER 4

Electrical Characteristics of 2D Dual Material Double Gate Heterojunction Tunnel Field Effect Transistor with heterodielectric gate oxide

4.1: Introduction

4.2: Device Structure

4.3: Analytical Model

4.4: Result and Discussion

References

4.1: Introduction

For low power applications and improve functionality on chip, scaling of conventional MOSFET device below submicron level posses various short channel effects along with low on current and higher subthreshold swing i.e. greater than 60mV/decade in room temperature. To reduce these limitations of MOSFET an alternative carrier transportation mechanism has been approached and developed a device TFET, as an attractive and alternative replacement of MOSFET in semiconductor industry.

TFETs are promising candidature than conventional MOSFET for providing extremely low off current characteristic. The physics behind operating principle of TFET is based upon tunneling mechanism which is caused by transfer of charged carriers from highly doped source-valence band to channel-conduction band. It helps electrons to across the smaller potential barrier near source channel interface region. Band-to-band tunneling of charged electrons allows low steep switching at low threshold voltage. It is also observable that TFET has some major drawbacks which include low ON current and ambipolar conduction. The low on current is due to low band to band tunneling due to large band gap of source and channel materials, or indirect band gap

nature. Various technological modifications has been approached to reduce this condition among these using Hetero materials in source channel region provides better result to increase on current due to higher tunneling probability at source-channel region. It also improves ambipolar condition at the drain channel region. In this proposed structure hetero dielectric material i.e. high dielectric HfO_2 and low dielectric SiO_2 at near source and drain region respectively has been used. This improves electrical characteristics of the device by reducing oxide capacitances which addresses threshold voltage roll-off related to downscaling of device dimensions and also improves SS below 60mV/decade.

Double gate structure improves switching speed by producing higher drain current over single gate structure. Here we consider depletion region in both source/ channel and drain-channel region to improve on current to improve accuracy of device characteristics. Other electrical characteristics like surface potential, electric field profile and tunneling effect has been estimated from simulated result by varying high-k dielectric oxide length below tunneling gate.

4.2 Device Structure

The proposed is demonstrated in figure 4.1which is a two-dimensional view of heterostructure double gate dual material device having lateral hetero dielectric material. The device has both 10 nm source and drain length along with following parameters including channel length L=40nm, the thickness of both oxides is 1nm,

Figure 4.1 *Two dimensional schematic view of proposed device*

Channel (silicon) thickness is 12nm which is greater than require thickness for quantum confinement model. So quantum mechanical effect can be ignored. The source is heavily doped with p-type 10^{21}/cm3 and drain is doped with n-type 10^{18}/cm3. Doping profile in the channel region is a p-i-n-type with uniform doping provides efficient tunneling of electrons. Top dual gate work functions are 5.3eV for tunneling gate and 5.1eV for the auxiliary gate and bottom gate work functions are 4.5eV, Tunneling gate length is 8nm and auxiliary gate length is 25 nm , In this proposed device Germanium is used as source material which has less bandgap 0.67eV, much lesser than silicon (1.14eV) providing a high rate of the band to band tunneling of charge carriers. Source channel depletion region is taken 2nm where drain channel depletion region has been taken 3nm for reducing reverse tunneling at drain/channel side.

Using Silvaco Atlas simulation software transfer characteristics and other electric parameters have been estimated.

4.3 Analytical model

In this section we have discussed about the analytical model for our proposed device considering uniform doping along the channel region, here we have considered depletion region at the source/drain channel interface.

A. *Surface potential*

Surface potential model can be obtained by solving 2D Poisson's equation.

$$\frac{\partial^2 \psi_i(x,y)}{\partial x^2} + \frac{\partial^2 \psi_i(x,y)}{\partial y^2} = -\frac{qN_i}{\varepsilon_{si}}$$ where i=1,2,3,4 region………..(1)

$$for(0 \le x \le L, 0 \le y \le t_{si})$$

Where L=L1+L2+L3+L4 for different region in channel, L1 and L4 are depletion region length whereas L2 and L3 are lengths under two dissimilar metal in channel region. ε_{si} is the dielectric constant of silicon. $\psi_i(x,y)$ is the potential distribution in 2D device.

Using the parabolic approximation method the potential in the channel region is

$\psi(x,y) = C_{i0} + C_{i1}(x)y + C_{i2}(x)y^2$ …………..(2)

Under two different metals surface potential along channel region with considering depletion region in both source/drain side is

$\psi(x,y) = \psi_s(x) + C_{i1}(x)y + C_{i2}(x)y^2$ …………………(3)

Where C_{i1} and C_{i2} are arbitrary constants and $\psi_s(x)$ is assumed as front and back surface potentials for different regions i=1, 2, 3, 4;

Due to different metal having different work functions, flat band voltages are different which are

$\phi_{MS1} = \phi_{M2} - \phi_{si} = V_{FBM1}$

$\phi_{si} = \chi + \frac{E_g}{2} + \phi_{bi} = V_T \ln(N/n_i)$ $\phi_{MS2} = \phi_{M2} - \phi_{si} = V_{FBM2}$,

Where ϕ_{M1} and ϕ_{M2} are the work functions of M1 and M2 and $\phi_{si} = \chi + \frac{E_g}{2} + \phi_{bi}$ where $\phi_{bi} = V_T \ln(N/n_i)$ is the built in potential, E_g is bandgap of silicon, χ is the electron affinity.

Boundary Conditions

1. Derivative of surface potential at the both front and back gate oxide for dual material is continuous, so we have

Region: L1<x<L2

$$\left.\frac{d\psi_1(x,y)}{dy}\right|_{y=0} = \frac{(\varepsilon_{ox}+\varepsilon_k)}{\varepsilon_{si}}\frac{\psi_{s1}(x) - V_{GS1}}{t_f}$$

$$\left.\frac{d\psi_1(x,y)}{dy}\right|_{y=t_{si}} = -\frac{(\varepsilon_{ox}+\varepsilon_k)}{\varepsilon_{si}}\frac{\psi_{s1}(x) - V_{GS1}}{t_b}$$

Region: L2<x<L3

$$\left.\frac{d\psi_2(x,y)}{dy}\right|_{y=0} = \frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{\psi_{S2} - V_{GS2}}{t_f}$$

$$\left.\frac{d\psi_2(x,y)}{dy}\right|_{y=t_{si}} = \frac{-\varepsilon_{ox}}{\varepsilon_{si}}\frac{\psi_{S2}-V_{GS2}}{t_b}$$

Where t_f and t_b are front and back gate oxide thickness

2. Surface potential is continuous at the interface of two metals.

$$\psi_0 = \psi_0(x_0,0) = -V_T \ln(N_1/n) = \psi_1(x_0,0)$$
$$\psi_1 = \psi_1(x_1,0) = \psi_2(x_1,0)$$
$$\psi_2 = \psi_2(x_2,0) = \psi_3(x_2,0)$$
$$\psi_3 = \psi_3(x_3,0) = \psi_4(x_3,0)$$
$$\psi_4 = \psi_4(x_3,0) = V_T \ln(N_3/n) + V_{DS}$$

Where ψ_0 source end potential near channel interface and ψ_4 is drain end potential and N3 is the doping concentration of drain region

$$x_0 = 0$$
$$x_1 = L_1$$
$$x_2 = L_1 + L_2$$
$$x_3 = L_1 + L_2 + L_3$$
$$x_4 = L_1 + L_2 + L_3 + L_4$$

3. Electric flux along the channel is continuous at the metal interface

$$\left.\frac{d\psi_j(x)}{dx}\right|_{x=x_j} = \left.\frac{d\psi_{j+1}(x)}{dx}\right|_{x=x_j}$$ Where j=1,2,3

Solving the boundary conditions 1 we obtain the value of arbitrary constants C_{i1} and C_{i2} and put those values in (1) and using (2) we get,

$$\frac{d^2\psi}{dx^2} - \alpha^2\psi_i(x) = -\alpha^2\beta_i$$
$$\beta_i = V_{GS} + \frac{qN_i}{\varepsilon_{si}\alpha^2}$$

And $\alpha = \sqrt{2\lambda / t_{si}^2}$

Where λ is is the ratio of gate oxide and silicon thin body capacitance i.e. $\lambda = \frac{C_{total}}{C_{si}}$

$C_{total} = \frac{\varepsilon_{ox} + \varepsilon_k}{t_{ox}}$ under metal 1 and $C_{total} = \frac{\varepsilon_{ox}}{t_{ox}}$ under metal 2 for the channel region R_2 and R_3

Silicon body capacitance is $C_{si} = \frac{\varepsilon_{si}}{t_{si}}$

The parameters α and β have different values for different regions along the channel Characteristics length for surface potential in each region is η=1/α.

The solution for equation (4) for different i[th] region (R_1, R_2, R_3, R_4) can be obtained individually

$$\psi_{dep}(x_0) = V_{bias} - \frac{kT}{q}\ln(\frac{N_a N_c}{n^2_i})$$

$$\psi_1(x_1) = ae^{(\frac{x-L_1}{\eta})} + be^{-(\frac{x-L_1}{\eta})} + \beta_i$$

$$\psi_2(x_2) = ce^{(\frac{x-L_1-L_2}{\eta})} + de^{-(\frac{x-L_1-L_2}{\eta})} + \beta_i$$

$$\psi_3(x_3) = le^{(\frac{x-L_1-L_2-L_3}{\eta})} + me^{-(\frac{x-L_1-L_2-L_3}{\eta})} + \beta_i$$

$$\psi_{dep}(x_4) = V_{DS} + \frac{kT}{q}\ln(\frac{N_d N_c}{n^2_i})$$

Six unknown parameters a, b, c, d, l, m are solved by using surface potential and continuity equation at the depletion/metal and two metal interfaces.

B. *Electric Field*

The vertical and lateral electric field $E_{iy}(x,y)$ and $E_{ix}(x,y)$ can be computed for any region along channel from surface potential as

$$E_{ix}(x,y) = -\frac{d\psi_i(x,y)}{dx} = -\frac{A}{\eta}\exp(\frac{x-x_{i-1}}{\eta}) + \frac{B}{\eta}\exp(\frac{x-x_{i-1}}{\eta})$$

$$E_{iy}(x,y) = -\frac{d\psi_i(x,y)}{dy} = -(C_{i1} + 2yC_{i2})$$

C. *Length of depletion region*

$$L_1 = \sqrt{2\varepsilon_{si}(\beta_2 - \psi_0)/(qN_1)}$$

$$L_1 = \sqrt{2\varepsilon_{si}(\beta_2 - \psi_0)/(qN_1)}$$

Where L1 and L4 are the source and drain depletion region length respectively

4.4 Result and Discussion

In this section, simulation data has been presented for optimization of our proposed device. For fixed minority carrier life time Scholdey-Read-hall recombination model, BTBT Kane model, concentration dependent model, parallel electric field dependent model and bandgap narrowing model has been selected for simulation. Here quantum confinement model is ignored due to 12nm silicon channel thickness Figure 4.2 shows energy band diagram for length variation of high-k dielectric oxide (HfO2). It has been shown that doping profile is same for all. Minimum band energy can be shown for 6nm HfO2 length. All the results have been observed for V_{DS}=1V and V_{GS}=-2V and V_{GS}=2V

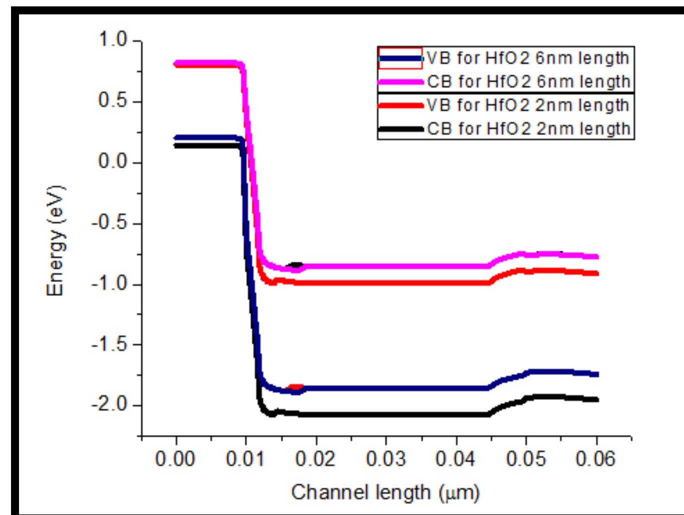

Figure 4.2*Energy Band Diagram along the surface for different HfO2 length at on state condition for biasing at VGS=-2 V and VGS=2 V and VDS=1V*

Figure 4.3 and 4.4 shows lateral electric field for constant gate bias voltage against various drain voltage.

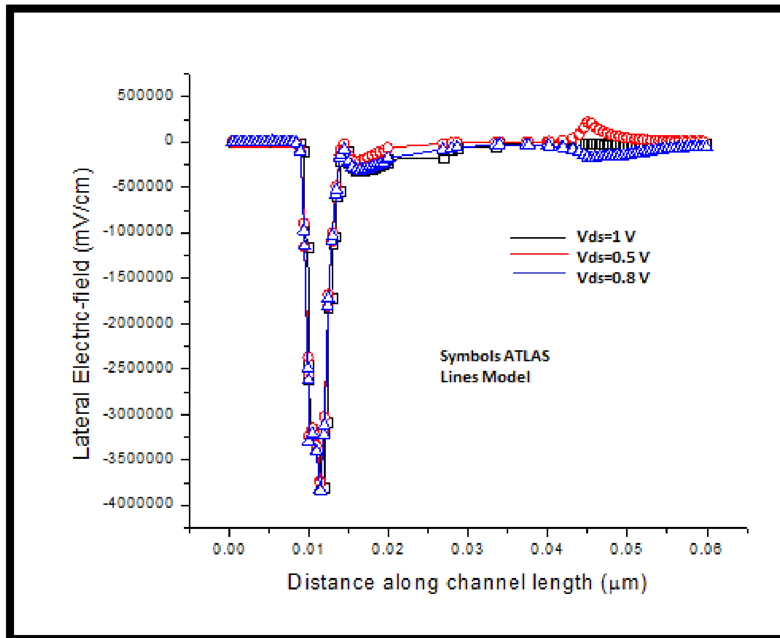

Figure 2.3 *Lateral Electric field profiles along channel length for different drain voltages*

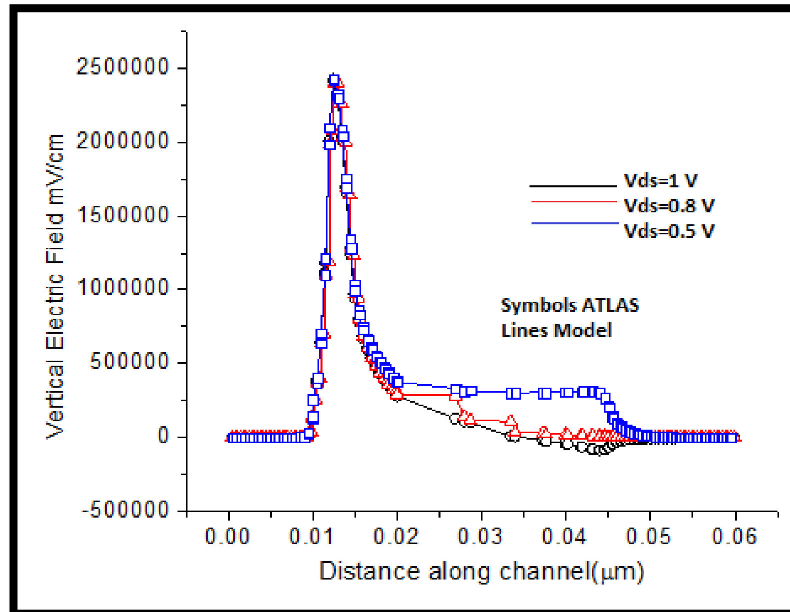

Figure 3.4 *Vertical Electric field profiles along channel length for different drain voltages*

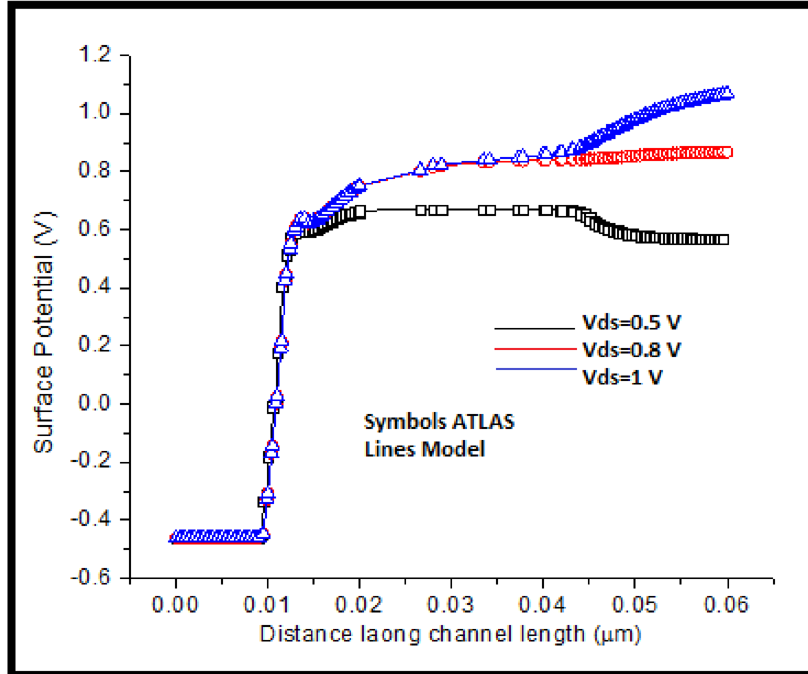

Figure 4.5*Variation of surface potential against V_{GS} for different V_{DS} of proposed device*

I t is also can be observed that operation at depletion or accumulation inversion layer depend on drain voltages. For increasing the gate bias voltage potential is constrained due to depletion, inversion or accumulation region in channel.

Figure 4.6 shows potential in depletion mode that when channel is fully depleted for low gate voltage and high drain voltage and compare it with inversion/accumulation mode of channel when gate bias applied is higher than drain voltage.

The simulated band to band tunneling energy for homo i.e. silicon in source region and heterostructure for VDS=0.8 V has been shown in the figure 4.7. It is shown that small tunneling length is for Heterojunction DGTFET device compare to homojunction DGTFET because of small bandgap energy that help to decrease potential barrier

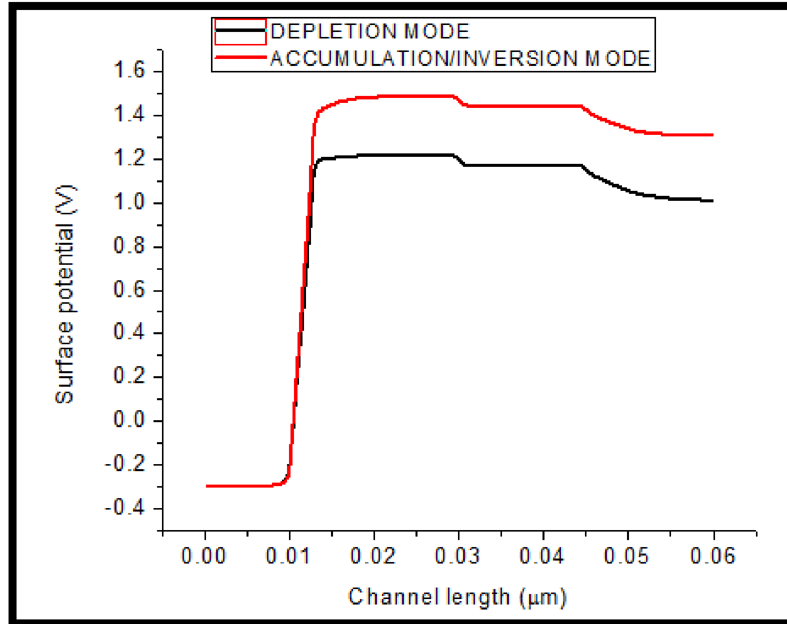

Figure4.6 *surface potential along different mode of channel*

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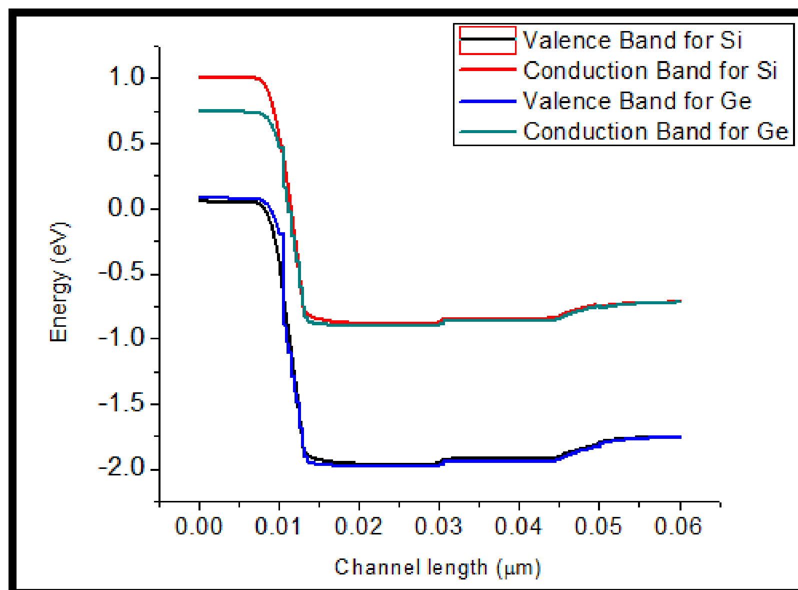

Figure 4.7 *comparison of band diagram of homo(si) and Heterojunction (Ge-Si) DGTFET* V_{GS} *bias voltage and* $V_{DS}=0.8$ *V*

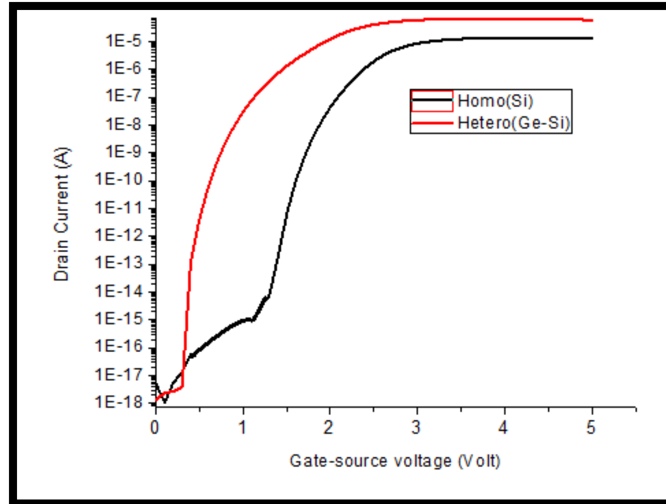

Figure4.8 *Variation of drain current against VGS for different DGTDFET at V_{DS}=0.8 V*

In the figure 4.6 compares drain current variation for homo (Si) and Heterojunction (Ge-Si) DGTFET without considering subthreshold region that means not in weak inversion layer when gate to source voltage is less than threshold voltage. For Heterojunction threshold voltage is 0.4 V where in case of homojunction Vth=1 V for V_{DS}=0.8 V

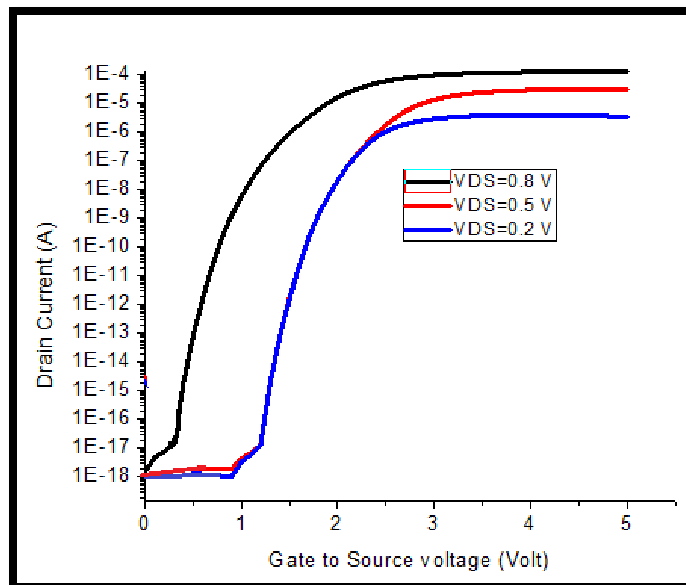

Figure 4.9*Transfer characteristics for different drain to source voltage*

Figure 4.7 demonstrates drain current against constant gate bias voltage for various drain to voltage. It has been shown from the graph that higher drain voltage reduce the tunneling barrier and increase the on current and hence on/off ratio has been increased.

Simulation result of surface potential of a two dimensional hetero junction TFET with lateral high-k HfO2/ SiO2 has been developed with and without consider depletion layer in channel region. The atlas model is developed for both Heterojunction and homojunction TFET. Electrical characteristics like transfer characteristics, energy band diagram for various length of high-k oxide, surface potential for different drain voltages of our proposed device has been estimated.

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CHAPTER 5

Efficient Quantum Mechanical Simulation for 2D Heterojunction Double Gate TFET for Low Power Applications

5.1 Introduction

5.2 Device Structure

5.3 Model description

5.4 Result and discussion

References

5.1 Introduction

For high performances at low voltages and high packing density along with higher operating speed, scaling technology over conventional MOSFET generate various limits both in the fabrication process and device characteristics mainly fundamental subthreshold swing 60 mV/decade in room temperature. To overcome these limitations of MOSFET an alternative choice has been implicated in the silicon industry. TFET is that one solution whose carrier transportation mechanism depends upon the band to band tunneling. TFET provides low off state current that makes that device more convenient in low power applications.

The tunneling width between conduction and valence band seems to be important parameter as minimum tunneling width of TFET makes tunneling probability more efficient to across potential barrier. Tunneling probability exponentially depends upon the potential barrier width. Inversion layer formation is one of these mechanisms to increase tunneling by reducing tunneling width by increasing gate voltage.

Except the formation of inversion layer there is another mechanism come to this chapter is appearance of quantum efficient which effects on tunneling width. Due to appearance of

quantum confinement, in sub band condition the energy bands which are conduction and valence band turns into discrete spectrum of energy that make the tunneling take place at the first bound state for charged carriers as shown in figure 5.2. That increases the band gap energy and reducing BTBT tunneling effect which results significant low current profile for device.

5.2 Device structure

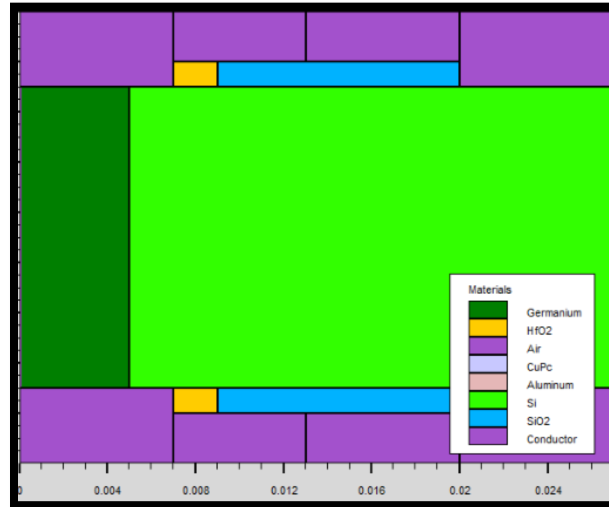

Figure 5.1 *2D schematic diagram of proposed device*

Our proposed device is double gate dual material Heterojunction TFET as shown in figure 5.1. Germanium-silicon body thickness is taken 10nm for our device. Source is highly doped with $10^{21}/cm^3$ doping concentration whereas drain is n+ doped with $10^{18}/cm^3$. Intermediate channel region is low doped p-n with uniform doping concentration. Source/ drain lengths are same i.e. 5nm and channel length is below 20nm for quantum analysis. Dual material double gate work functions are 4.5 eV. We have taken 1nm thick gate oxide (HfO_2/SiO_2) layer for each gate.

5.3 Model Description

Here we use self-consistent Schrodinger-Poisson model for quantum confinement of our proposed device. Quantum analysis is done in simulation with Silvaco Atlas software. The model name is so because of self consistently solve Poisson equation for potential and Schrödinger model is used for bound state energy in energy band spectrum for valence and conduction band.

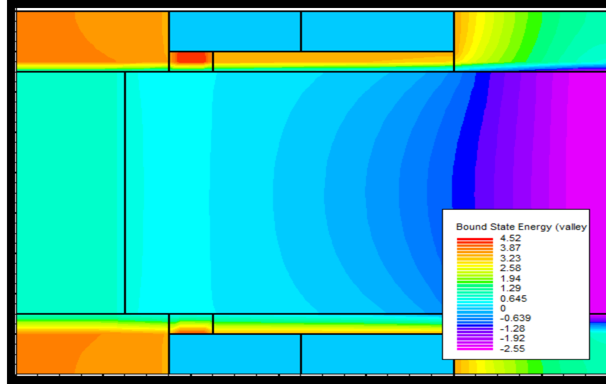

Figure 5.2*First Bound State energy for electron-hole carriers in quantum confinement*

We can assume confinement take in one direction so that quantum analysis can be done by one dimensional Schrödinger Poisson equation. The calculation of the quantized density of states relies upon a solution of Schrodinger's Equation.

$$-\frac{\hbar}{2}\frac{\partial}{\partial x}\left(\frac{1}{ml}\frac{\partial\psi_{il}}{\partial x}\right)+E_C(x)\partial\psi_{il}=E_{il}\psi_{il}\;\ldots\ldots\ldots\ldots(5.1)$$

$$-\frac{\hbar}{2}\frac{\partial}{\partial x}\left(\frac{1}{mt}\frac{\partial\psi_{it}}{\partial x}\right)+E_C(x)\partial\psi_{it}=E_{it}\psi_{it}\;\ldots\ldots\ldots\ldots(5.2)$$

where E_{it} is the ith bound state energy for transverse mass, E_{il} is longitudinal, Ψ_{it} is the transverse wavefunction, Ψ_{il} is the longitudinal wavefunction, and E_C is the is the band edge energy. This expression is for electrons but an equivalent expression exists for holes.

For quantum analysis both equation have to be solve by dividing each step.

In addition Schokley Read Hall model has been used for recombination. Bandgap narrowing and parallel electric field transportation model have been used.

5.4 Result and Discussion

Figure 5.3 has shown the electron concentration profile for classical and quantum confinement for V_{DS}=0.5 V and gate bias voltage. Here confine the motion of moving electron particles to restrict some energy levels and make the energy levels discrete.

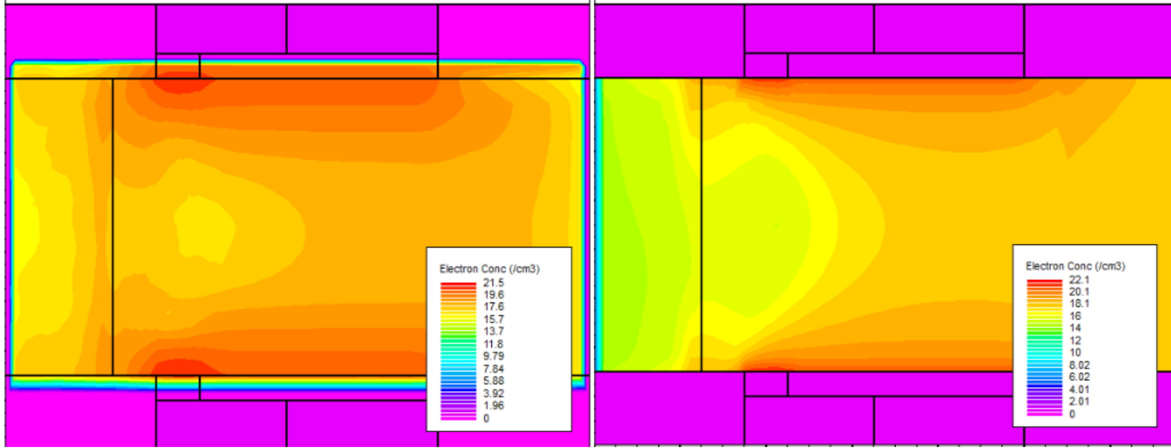

Figure 5.3 *Shows Electron concentration for VGS=0.5 V with and without quantum confinement*

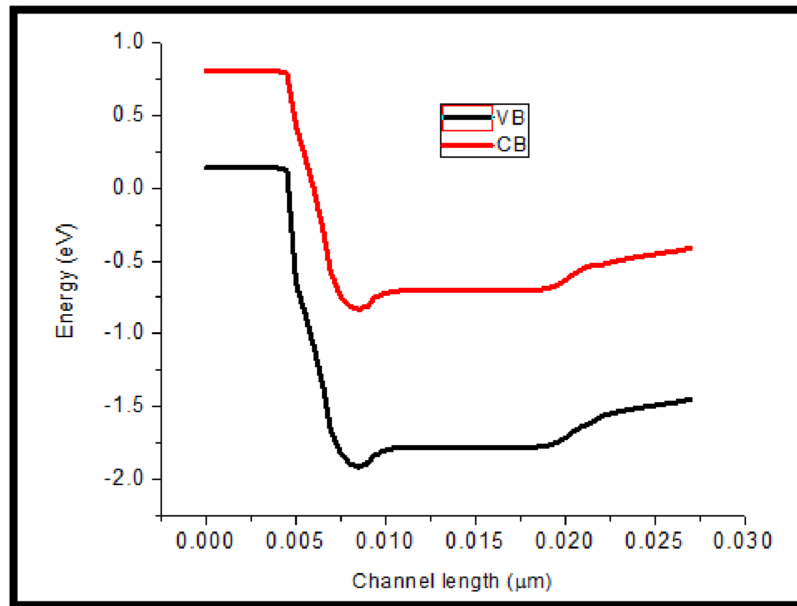

Figure 5.4 (a) *Energy Band diagram with quantum confinement*

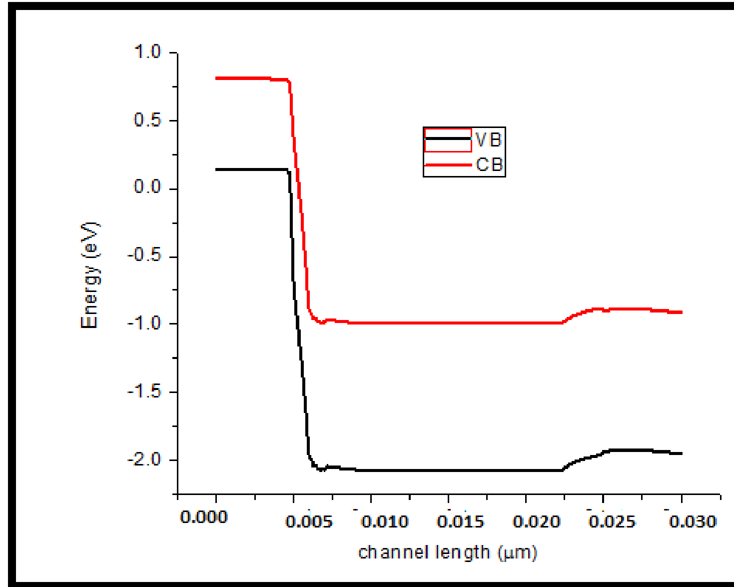

Figure 5.4(b) *classical energy band diagram*

From figure5.4(a) and 5.4(b) it has been shown that due to quantum confinement band gap energy has been increased at V_D=1 V and hence on current is reduced.

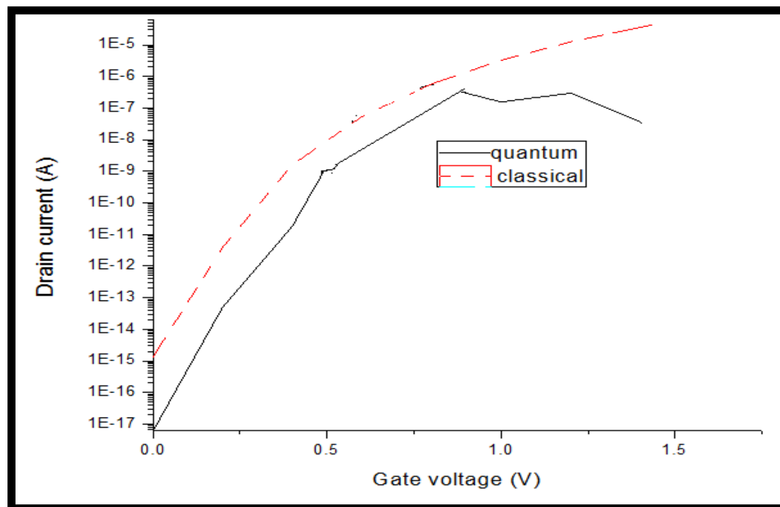

Figure 5.5 *Comparison of Transfer characteristics at V_D=0.3 V*

Figure 5.5 shows the transfer characteristics for different mode of operation one is classical and other is with quantum confinement mode for V_{DS}=0.3 V. It has been see that on current in case

of quantum has been decreased due to formation of discrete energy band in sub band region and makes movement of carriers discontinuous from conduction to valence band.

I_D-V_{GS} curve can be more accurate at high drain voltages as in low voltages dependence on gate voltage making it stiff bending in case of quantum confinement. Due to confinement pinning is stronger to increase energy band gap and hence increasing the gate voltage making BTBT lower.

In our proposed device we have been implemented quantum confinement as an advance technology towards quantum analysis. All the results have been done in Atlas simulation software. At low drain voltage device posses low on current for high gate voltage. This reduction can be further improvised by increasing the drain voltage.

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CHAPTER 6

Concluding Remarks and Future Work

Conclusion:

We have reported the first systematic simulation-based study of the static characteristics of optimized silicon Tunnel FETs to parameter fluctuations. We predict a much reduced Ambipolarity and high on current due to taking source/drain depletion region and high-k oxide length scaling compared to conventional Sio2 gate oxide. A trade-off will need to be made when choosing the desired alignment of the gate dielectric at the source end. Quantum confinement effect for this proposed device having below 10nm channel thickness also improved sub threshold swing from conventional. This study also suggests that the control of the high-k gate process, depletion region formation width at the tunnel junction, and film thickness in TFET with less parameter fluctuation than that required by conventional is crucial for future high-performance Tunnel FETs with reproducible characteristics. In chapter 3: An h-shaped double gate TFET with SiO2 as front gate and bottom gate dielectric has been proposed. The low vth (Fig.3.8 and Fig. 3.9 page no.50-51) give steeper switching to this device and hence it is an advantage over conventional MOSFET.In chapter 4: A Double metal double gate Heterojunction TFET has been proposed which shows superior tunneling probability due to small band gap of Germanium which is used as source material. In terms of ON current due to both depletion and inversion layer in channel region has been estimated as shown in Figure 4.4 (page no 64). Also dielectric engineering has an effect on tunneling probability. This proposed structure also reduced ambipolar conduction due to consider near depletion region in drain channel interface as shown in Figure 4.5 (page no 64) In Chapter 5, A double material heterodielectric TFET has been proposed with quantum confinement model whose principal includes boundary state energy in which energy bands are discrete in energy band spectrum also compare the confinement result with classical mode and estimated transfer characteristics at low drain voltages where it can be seen in Figure 5.5 (page no 72) that on current has been reduced due to higher band gap in quantum confinement.

Future work:

- ❖ We have studied the electrostatic characteristics of the proposed devices. However, there is lot of scope to explore the analog characteristics and digital applications of TFET.
- ❖ Analysis of quantum mathematical model of TFET can be included as future work
- ❖ All the simulations have been done in 2 Dimension. There is a need and scope for further analysis in 3 Dimension for a natural insight into the device.
- ❖ The work in this thesis is based on simulation. There lies a lot of research scope in fabrication of the proposed device and calibration of the simulated results with the experimental work.

Publications relevant to the current Thesis

- Goutika Paul, Bijoy Goswami, Subir Kumar Sarkar "H-Shaped Double Gate Tunnel FET for low power Applications", on International Conference on Recent Trends in Electronics and Computer Science (ICRTES-2019)
- Mandira Biswas, Goutika Paul, Bijoy Goswami, Subir Kumar Sarkar "PPV Based Bottom Gate Organic Field Effect Transistor (BGOFET)", on International Conference on Recent Trends in Electronics and Computer Science (ICRTES-2019)
- Bijoy Goswami, Goutika Paul, Debadipta Basak, Sutanni Bhowmick, Arindam Haldar, Subir Kumar Sarkar"Implementation of L-shaped Dielectric Double Metal Dual Gate TFET towards Improved Performance Characteristics and Reduced Ambipolarity"on 2nd National Conference on Information, Photonics &Communication (IPC'19)