Measurement based Small Signal Model Extraction of GaN HEMT

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This is to certify that the thesis entitled "***Measurement based Small Signal Model Extraction of GaN HEMT***" has been carried out by **ANURADHA RUDRA (Roll No: 001610703011, Examination Roll No: M6VLS19018 and Registration No: 137283 of 2016-17)** under my guidance and supervision and can be accepted in partial fulfilment for the degree of Master of Technology in VLSI Design and Microelectronics Technology. In my opinion the work fulfils the requirement for which it is submitted. To the best of my knowledge, the matter embodied in the thesis has not been submitted to any other organization.

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This is to certify that the Master Thesis entitled "**Measurement based Small Signal Model Extraction of GaN HEMT"** is hereby approved as a creditable study of an engineering subject carried out and presented in a manner satisfactory to warrant its acceptance as pre-requisite to the degree for which it has been submitted. It is understood that by this approval the undersigned do not necessarily endorse or accept every statement made, opinion expressed, or conclusion drawn therein but approve the thesis only for the purpose for which it has been submitted.

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ABSTRACT

Small signal models are indispensable for many practical reasons. Accurate model is the demand of the hour as modelling paves way for the betterment of existing technology while helping the circuit designers to cut down time and cost of development.

This thesis mainly deals with the development of small signal model, which is the first step in the modelling and also a gateway for large signal modelling. We performed the parameter extraction procedure of a GaN-on-SiC device. The thesis ends with a comparison between the behaviour of the measured and that of the modelled circuit. This study will provide useful information that one aspects in the performance of a designed model.

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Chapter 1

Introduction

Semiconductor device modelling creates models for the performance of the electrical devices based on primary physics, such as the doping profiles of the devices[1]. It may also comprise the formation of compact models(such as the well known SPICE transistor models), which try to arrest the electrical behaviour of such devices but do not generally derive them from the original physics. Normally it starts from the output of semiconductor process simulation[2].

The power scaling which is now a chief driving force in the industry is a crucial parameter along with capacitance, power supply and clocking frequency. Key parameters that narrate device behaviour and system performance include threshold voltage, driving current and sub-threshold characteristics[1].It is the convergence of system performance issues with the core technology and device design variables that grades in the ongoing scaling laws that we now codify as Moore's law[3].

Compact Modeling includes mostly the material that after several years of IC design applications has been found both theoretically sound and practically significant [4].Models of circuit elements which are sufficiently simple to be incorporated in circuit simulators and are sufficiently accurate to make the outcome useful to circuit designers are called compact. Continued down-scaling of semiconductor devices has made it necessary to incorporate new physical phenomena, while extended applications have led to the inclusion of the secondary and ternary effects in order to achieve the required model accuracy[5].At the same time, the increased size of the integrated circuits, that can now be subjected to the full SPICE analysis[8][9], disallowed proportional increase in the model execution time. Hence considerable time went into compact model reformulation in such a way that noticeably improved correctness and model superiority are gifted without exorbitant decrease in the computational efficiency. Moore's law is the observation that the number of transistors

in a dense integrated circuit doubles about every two years[6]. The surveillance is named after Gordon Moore, the co-founder of Fairchild Semiconductor and CEO of Intel, whose 1965 paper described a doubling every year in the number of components per integrated circuit and proposed this rate of growth would persist for at least another decade[3]. In 1975, looking overconfidently to the next decade, he revised the prediction to doubling every two years. The period is often quoted as 18 months because of a prediction by Intel executive David House[6].

1.1 Choosing Compact Modeling

Compact Models of circuit elements are models that are sufficiently simple to be included in circuit simulators and are adequately true to make the outcome of the simulators useful to circuit designers[4]. The conflicting objectives of model simplicity and accuracy make the compact modelling eld an exciting and challenging research area for device physicists, modelling engineers and circuit designers. Design engineers use those transistors build logic circuits that perform specific functions. Computationally efficient description of the terminal properties of a device as a function of terminal voltages.[7]

1.2 Problems with non-physical models

A model(which is not physical) for any of the physical quantities makes the other quantities non-physical also[10].For instance in the equation shown here: I = QuE. If Q is modelled incorrectly with respect to the bias then mobility has to become non-physical to match the measured current. Regional models are other reasons models become non-physical and they need smoothing functions between regions [10].Severe over-design or under-design when predictions due to process variations are incorrect, then they yield to Excessive costs and Poor yield.

1.3 Requirements of Compact models

Every foundry / company makes MOSFET transistors that are different. Even within a foundry or company there are dierent types of transistors: thick gate oxide, thin gate oxide process etc. A compact model must not be technology dependent[7].The necessities of Compact modelling have been listed below:
(1)Speed of evaluation Circuit simulation speed and accuracy is critical for timely design.
(2)Avoid expensive math functions.
(3)Avoid Internal nodes, if possible If internal nodes are used, then let the circuit simulator solve for the quantities on the node.
(4)Reuse computed quantities and intermediate variables.
(5)Accurate modelling of temperature dependence.

1.4 GaN HEMT and its versatile usage in RF Applications

Gallium Nitride (GaN) based high electron mobility transistors (HEMTs) outperform Gallium Arsenide (GaAs) and silicon based transistors for radio frequency (RF) applications in terms of output power and efficiency due to its large band-gap (3.4 eV@300K) and elevated carrier mobility possessions[11]. These rewards have made GaN technology a talented candidate for upcoming high-power microwave and potential millimeter-wave applications. Current GaN HEMT models used by the industry, such as Angelov Model, EEHEMT Model and DynaFET (Dynamic FET) model, are pragmatic or semi-empirical. Lacking the physical description of the device operations, these empirical models are not directly scalable[13]. Circuit design that utilises the models requires multiple iterations between the device and circuit levels, becoming a lengthy and costly process.

The existing physics based models, such as surface potential model, are computationally intensive and thus impractical for full scale circuit simulation and optimization[18]. To enable efficient GaN-based RF circuit design, computationally efficient physics based compact models are required.

1.5 Background

The emerging GaN technology is promising for high power and high frequency power ampliers design due to its competitive material properties, such as high band-gap, superior electron mobility and carrier velocity. The wide band-gap (3.5 eV@300 K) allows for up to 100 V drain to source voltage without device breakdown, which enables GaN HEMTs having more than an order of power density than Si-based power devices and GaAs HEMTs [11]. The superior electron mobility (2300 cm^2 /(V_s) @ 300 K) and carrier velocity (2.1107 cm/s) makes it capable to operate even in W-band 2 (75 – 110 GHz) while delivering watt level power without significant power-combining circuitry [12]. In addition to process technologies, device models play a significant role in high-performance RF circuit design [13,14].

Currently, due to the sustainable development of electromagnetic (EM) CAD software, general passive devices used in RF circuits are well modelled with simple and precise descriptions [15,16]. However, the models for active devices, such as diodes and transistors, are modelled with less satisfaction for circuit design in terms of both accuracy and computation efficiency due to the nature of multi-physics-dependent device non-linear behavior. Therefore, the limitations and trade-os of the existing models are discussed. Compact models refer to device models used for integrated circuit design in circuit simulation[17].

Based on the model formation, the existing compact models for RF transistors can be divided into two categories, the empirical models and the physics based models. The empirical models for GaN HEMTs, such as Angelov model, EEHEMT model and DynaFET (Dynamic FET) model, use analytical functions with tting parameters or artificial neural networks (ANNs) [18 - 20] to empirically describe the current and charge behaviours at each terminal. These empirical models usually have simple parameter extraction routine and are easy to implement in circuit simulators.

Furthermore, due to the close-form property of empirical functions and ANNs, these models are computational efficient, making them widely used in commercial CAD software for circuit design [19]. However, the equations in empirical models do not represent the operating principles of the device and do not allow direct linkage between device parameters and circuit level performance. Moreover, the empirical models are usually fitted to measurement data with non-physical tting parameters, which are not scalable with geometry, biasing and/or temperature. This often means only very limited device dimensions are available with each technology library with reasonable accuracy for circuit design. To adopt other device dimensions beyond the default dimensions requires lengthy recalibration. Furthermore, different characteristics in the empirical models are usually modelled using independent equations and different sets of parameters which are fitted through different sets of measurement data, leading to inconsistency of model behaviours.

1.6 Motivation

The high frequency and high power application scenarios require the transistor model to be accurate.Again the goal for modern transistor modelling is not only to accurately model the behavior of the transistor, but also enable the best performance of the entire system. Achieving this goal requires physics based compact models. Physics based models provide designers circuit-level element representation of the device, which enables device optimization, such as layout parasitic optimization for the optimum device performance. Furthermore, physics based models potentially support device circuit interactive design, which optimizes the RF circuit and device as a holistic system. Therefore, it is important and necessary to implement physics-based description of transistor behaviour in modern transistor modelling techniques. Designer requirements on the accuracy and flexibility of the device models are always increasing. This is directly linked to the increasing complexity of the targeted applications and signals. In the same time the effects highlighted on semiconductor technologies in maturation (eg. GaN) brings new challenges to the modelling engineers.
Chapter 2 lists the literature where all the previous work in the different domains of the thesis are listed.
Chapter 3 introduces the subject of modelling where different types of modelling techniques have been discussed.
Chapter 4 discusses the small signal parameter extraction procedure. We shall look at the HEMT device,its features and the current flow mechanism. Algorithms for extracting the extrinsic and intrinsic parameter have been given.

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Chapter 2

Literature Review

2.1 Introduction

Metal semiconductor field effect transistors (MESFET) are compatible with group III-V compounds. Schottky (metal-semiconductor) junction is used instead of using a p-n junction for gate. MESFETs are used in microwave receivers as low noise amplifier, satellite communication, military communication and many other high frequency operations. To maintain a high transconductance in a MESFET, the channel conductivity must be very high. By introducing the impurities in the crystal structure, the conduction property of a semiconductor material can be modified. Semiconductor material is needed to be doped with huge dopant to increase the carriers in it. The immobile ion concentration increases with the increasing doping concentration. Due to high electric field interaction, the carriers start scattering and results to effective mobility degradation. It is necessary to have a high carrier density but without affecting mobility degradation and without directly introducing the dopant in material. The concept of HEMTs meets all these requirements. Between two materials a junction with different band gaps is used as channel instead of a doped region. The wide band element (AlGaN) has excess electron in its conduction band as it is doped with donor atoms. The electrons from the doped layer drops to the not so doped layer (GaN) due to availability of lower energy states and forms a depleted AlGaN layer. This is due to the reason that the heterojunction created by different band gap materials forms a quantum well in the conduction band on GaN side.The electron velocity in this region is very high and there is less probability of collision between two electrons as the layer is undoped. The electrons cannot escape this region due to high potential barrier between two different band gap materials and as a result it forms a thin layer of elevated mobile conducting electrons known as 2-D electron gas. Thus the scattering effect is reduced and a high mobility is achieved.

The reward of a HEMT are its capacity to find a large electron density ($1012cm^2$)in a very thin layer(less than 100A thick) very close to the gate while concurrently eliminating ionized impurity scattering. The AlGaN layer in a HEMT is fully depleted under normal operating conditions and since the electrons are confined to the heterojunction, device behaviour closely resembles that of a MOSFET. The compensation of the HEMT over the Si MOSFET are the higher mobility and maximum electron velocity in GaN compared with Si, and the smoother interfaces achievable with an AlGaN/GaN heterojunction compared with the Si/SiO2 interface. The superior feat of the HEMT translates into an extremely high cuto frequency, and devices with fast access times.

To have a clear understanding of the device physics and to have an accurate prediction of the device performance at high frequency, different small signal analysis had been demonstrated. Analysis of small signal model includes the proper determination of the intrinsic and the extrinsic elements, where the intrinsic elements are assumed to be bias dependent and extrinsic elements to be bias independent. The accurate extraction of parameter values, is very necessary for perfect device modelling.

2.2 Review on Extraction of intrinsic parameters

The work on field-eect transistors started in the year 1952 and considered the performance of the device when operated with electric fields in the channel below the critical eld, where the mobility of carriers depended on the electric eld. This work was reviewed by Dacey and Ross who showed that, in this range of operation[electric fields in the channel below the critical eld], the frequency cuto, and transconductance ,g_m, of the device boosts with increasing values of electric eld. The rst frequently used FET lumped element circuit models were presented by Dacey and Ross in 1955 and Hower and Bechtel in 1973 [1], [2]. In particular the eect of non-constant mobility at high electric fields is analysed in some detail and shown to be a governing consideration for some designs.

The basic SSEC extraction method was presented by Minasian [3] for GaAs MESFETs in 1977. This paper presented a simplified design oriented equivalent circuit for the GaAs MESFET.The element values were easily determined from the measurements. Moreover a simple model has been presented in this paper which shows a good agreement of the modelled parameters with measured parameters to 10 GHz for 1 micrometer-gate MESFETs.

This paper did not help us determine the model parameters separately.

This work eventually was extended to determine the extrinsic resistances and inductances from S-parameter data in a cold-FET condition (V_{ds} =0) by Diamant and Laviron in 1982 [4].A MESFET with an unbiased drain was considered. Diamant and Laviron explained that for zero drain voltage, the region under the gate can be described by a distributed, uniform, R-C transmission line , which eventually leads to a simple analytical model which they expected to be of good accuracy. It was shown that this model, combined with the lumped circuit model of the extrinsic part of the MESFET, is very suitable for comparison with experiment and lead to a straightforward measurement method of several device parameters, in particular the parasitic source, gate, and drain resistances and reactance.Few discrepancies were there in the method. The independent measure of the extrinsic model could have resulted in increased accuracy for the parameters and by reducing the number of unknown parameters; the discrepancies could have been avoided.

IIn 1984, Curtice and Camisa [5] reported a procedure for generating the equivalent circuit models for carrier-mounted GaAs FETs .The problem was that there were too many variables and the requirement was to create a unique solution based only upon a set of broad-band S-parameter measurements. Before this attempts were already made to construct FET models based only on S-parameter measurements. But unfortunately Vaitus has exposed that the errors associated with measuring and de-embedding device scattering parameters leads to major errors in the equivalent circuit element values for GaAs FET's. Some of these errors can be reduced with enhanced S-parameter measurement techniques. However, GaAs power FET's are carrier-mounted and therefore are surrounded by more parasitic circuit elements and require additional de-embedding. Although there was a good agreement for S-parameters results, still the method did not assure agreement for the values of stability factor and MAG. It was found that any loss in the FET carrier would have affected the values determined for the circuit elements which modelled the FET chip.

Information regarding the small-circuit equivalent circuit of a eld eect transistor is very functional for the device presentation investigation (gain, noise, etc.)in scheming of microwave circuits and characterizing the device technical process. By optimizing the element values to closely t the small-signal microwave scattering parameters calculated on the device usually, the small-signal equivalent circuit is obtained. However, this equivalent circuit

determination has several drawbacks:

- A correct broad-band S-parameter dimension is required.
- For small differences in the error function, the most favourable element values can vary depending upon the optimization method and the preliminary values.
- To have a physical implication, the equivalent circuit requires a preface determination of certain parameters (gate resistance or inductances, for example)

In order to defeat these difficulties Dambrine's paper developed a new method to determine the FET small-signal equivalent circuit. This method consists in a undeviating, fast, and truthful measurement of the different elements performed at moderately low frequency. This new method for finding the parasitic capacitances values is very useful for two main reasons. This new method for finding the parasitic capacitances values is very useful for two main reasons.
This new method for finding the parasitic capacitances values is very useful for two main reasons:

- A FET design can be characterized through way of parasitic capacitances.
- The intrinsic gate-to-source capacitance can be perfectly defined if C_{pg} is known.

In Dambrine's method a physically based determination of the extrinsic parameters was carried out and an analytical set of equations were provided for the direct calculation of the seven intrinsic SSEC elements as a function of the measurement frequency. The frequency independence of each SSEC element was checked which provided a fast and reliable method to affirm the coherency of extracted element. Further work on the parasitic capacitance and SSEC parameter extraction was carried out [7], which explained the inception of parasitic capacitances and demonstrated how they should be modelled. The work presented here showed that, in an active FET, the field lines both in the semiconductor and on top of the semiconductor terminate at the periphery of the gate, so that C_{gs} and C_{gd}, are independent of the electrode separations. This method did not show much light to the

determination of C_{ds}.

Latter the work in [8] emphasized the bias independent nature of cold-FET extrinsic parameters. With the objective of extraction of the parasitic resistances and inductances all the characterization methods relied on 2 strong forward biased gate Schottky junctions. The forward bias condition 4 eliminates the control of the intrinsic R-C parallel networks and allows the extraction of the extrinsic SSEC elements. The cold-FET method allows the extraction of FET parasitic resistances and inductances at forward bias.

A analytical direct extraction method for the determination of MESFET and HEMT parasitic elements was described in a narrative and precise way in [9]. This procedure differs from the previously described "cold FET" technique by terminating the requirement of forward biasing of the Schottky gate junction. This method allowed the extraction of parasitic inductance and resistance element without large forward gate currents which most of the times leads to irreversible degradation of the gate electrode.

The small-signal equivalent circuit of a heterojunction field-effect transistor (HFET) is used in the design of high speed circuits and characterization of fabrication processes. The small-signal circuit also helps in accepting device physics. Speedy and correct parameter extraction for HFET modelling is hence needed to devise, build up, and construct high-yield, low-cost, high-performance monolithic circuits.

In [10] a new cold-FET extrinsic SSEC model is demonstrated together with a Schottky series resistance which enables the extraction of the parasitic resistances and inductances. To extend the model validity to high frequencies pads were modelled as a -network. This work highlighted the importance of addition of R_{gd} to accurately model the maximum stable gain (MSG), maximum available gain (MAG), current gain (h_{21}), and stability factor (k) and exhibited the exact equations for the calculation of the intrinsic element values versus frequency.

Reuter [11] published an extensive intrinsic SSEC adding the capacity of modelling impact ionization. A new small-signal-model was offered, which permitted an accurate modelling of S-parameters over a wide frequency range. In contrast to predictable RF and noise models, the agreement between measured and modelled scattering shown in this paper allowed successful prediction and modelling of small-signal parameters of various monolithic microwave integrated circuits (MMIC's).

By making extensive use of regression analysis, Miras and Legros [12] presented interesting approaches for extracting the extrinsic elements of short gate InP HEMTs without strongly forward biasing the gate Schottky junction and achieved excellent agreement between measured and modelled data. However, their work included some intrinsic SSEC elements as frequency dependent quantities, at the cost of increased complexity and reduced physical interpretation.

Besides the aforementioned contributions, further model extensions and methods were proposed, to find suitable SSEC element values fitting the measured device data [13]–[22]. The well-known drawback of these approaches is that they often make extensive use of additional circuit elements and can occasionally result in inadmissible SSEC values. In [17] the extrinsic parameters extraction part is done first, expert starting values for the extrinsic elements were generated using cold-parameter measurements. In the intrinsic parameter extraction part, an efficient technique was proposed for optimal extraction. The properties of GaN HEMT that were considered through the predened approaches are as follows:

- High two-dimensional electron gas (DEG) densities.
- Large conduction band discontinuity.
- Piezoelectric and spontaneous polarization effects.

Due to the lack of native GaN substrates, GaN HEMTs for RF and high-power applications are now predominantly fabricated on silicon carbide (SiC) or silicon (Si) substrates. While Si offers a somewhat lower thermal conductivity, it is available in commercial volumes and large wafer sizes at economically competitive prices. However, GaN HEMTs grown on Si-substrates can exhibit parasitic buffer effects originating from the [23]:

- Nitrification of Si in the initial stages of nitride growth.
- Unintentional contamination from the substrate during growth.

In 1996, Goto [24] proposed the use of a simple gate and drain extrinsic series R-C-network in order to model the reduced isolation in their proposed

extrinsic circuit model. In this paper the GaAs-Si interface, influences of the pads, and the Si substrate on the microwave characteristics are included and the pads are expressed by series connections of resistors and capacitors in the circuit. The novel equivalent circuit describes the microwave characteristics of HEMTs-on-Si. It also has a immense benefit in that it can independently analyse the intrinsic device characteristics and influences of Si substrate and GaAs-Si interface.

The rst AlGaN/GaN HEMT on Si substrates presented in [23] showed good static output characteristics when biased at +1 V on the gate.The approach was extended to two R-C-pairs at the gate, and three R-C-pairs at the drain, by Chumbes in [23] who reported an accurate model for GaN on leaky Si(111) substrates in 1999.

Another key consideration for GaN HEMTs is associated with the high-contact resistances originating from the large conduction band discontinuity, as pointed out by Gaska [25] in 1997. This paper reported analysis based on a high positive turn-on voltage of the gate-source leakage current in AlGaN/GaN high electron mobility transistors (HEMTs).

In the same year, Burm [26] showed that highly resistive contacts can be modelled as transmission lines. This work mainly included the metalsemiconductor ohmic contacts modelled as a transmission line, as parasitic Z-elements cannot be modelled as an uncomplicated resistor/inductor distinct circuit due to high contact resistances. The model described the remarkably resistive contacts with a good exactness

In 2000, Chigaeva [27] demonstrated good agreement between simulation and measurements when driving sufficiently high current through the gate in order to diminish the influence of the gate capacitance and therefore decrease the differential resistance. Because high gate currents often lead to irreversible device degradation, significant trouble was taken on developing low gate bias model extraction techniques for GaN HEMTs.

Initially developed for Al-GaAs/ GaAs HEMTs in 1999, Jeon [28] reported the first extraction method able to extract the extrinsic elements in cold-FET mode below pinch-off. By describing the Schottky barrier and channel region by means of a distributed R-C-network, this method allows one to determine the parasitics without forward biasing of the gate and thus avoids any possible device degradation.

Based on this approach and simplifying the equations obtained by neglecting the drain-source capacitance C_{ds}, Guang [29] extracted the extrinsic elements using only a small forward bias applied to the gate of the AlGaN/GaN HEMT device.

Also in 2006, work from Crupi [30] treated the existence of the channel capacitance in their approach, requiring an iterative procedure to determine a suitable forward bias condition, which is high enough to restrain the channel resistance and low enough to not cause significant current flow through the gate. A detailed analytical extraction procedure also taking the drain source capacitance Cds into account is reported by Brady in [31] from 2008.

Their approach is also based on the cold-FET technique of Jeon 4 [28], in combination with the modified distributed channel model. Despite the good fitness of the modelled and simulated Z-parameters, some of the extracted results e.g. the extracted channel resistance is tenfold overestimated compared to the specified sheet resistance of 300 /square and reflects the difficulty of optimizer-driven extraction procedures.

A series of extraction algorithms have been presented in [17]–[22], beginning with the report of a 15-element small-signal FET model in 1992, which evolved to a 22-element distributed model for GaN HEMTs on Si, which was later extended to a large signal model in 2011. The core of their approaches is a hybrid optimization technique which determines the starting values either from measurements or from a genetic algorithm based procedure and then uses a local optimization technique, to find the optimal value of each element. For the development of analog and digital integrated circuits, an accurate device model is a valuable tool.Especially for high-speed digital applications,for the active device to operate over the entire operating range from dc to over 10 GHz, a large signal model has to be used. The most suitable method to examine a FET at high frequencies involves S-parameter measurements.

Measurements have to be performed at many bias settings over the frequency range of curiosity, for the classification of the broad-band manners of a device as the electrical properties of an FET powerfully depend on the applied gate- and drain-to-source voltages. The S-parameter data (in a vast amount) of a single FET can be condensed .By using an equivalent circuit of physically meaningful elements which is reported in [32], this set can be condensed to a set of 15 frequency independent variables.

Several commercially available programs exist which can optimize some

or all of these parameters.Although in general the carefully calculated S-parameter data are approximated in an acceptable manner by these methods, the resulting element values depend on the starting values and may vary considerably from 8 their physical values. A number of authors [33], [34] have shown that a so-called cold modelling, when the FET is calculated at 0 V drain-to source voltage, can be used to decrease the unknown set of parameters to seven or eight variables, which results in better convergence and reduced computation time. But as stated in [33], there are still problems concerning the unequivocal determination of the best possible values of the equivalent circuit using these general optimizing programs.

The parasitic circuit elements are pre-extracted from three to ve sets of zero drain-to-source bias S-parameters measured at the preferred gate to-source and drain-to-source biases. In the second step, the S-parameters are fitted to the equivalent circuit of an FET in the common-source, common-drain, and common-gate configurations to improve the accuracy and consistency of the modelling. A brilliant harmony between modelled and measured S-parameters, stability factor, and maximum stable (available) gain was obtained.

A new method 5 has been proposed in [35] and extended in [36] to determine the seven internal device elements analytically at frequencies below 5 GHz. An excellent fitness up to 5 GHz but significant errors at higher frequencies has been observed in this work and verified. As a result an improvement is done to this method to settle on the internal device parameters analytically with no frequency limitations. At any frequency over the range of S-parameter measurements which was limited to 26 GHz, now it is likely to evaluate the small-signal equivalent circuit.Additionally, due to the absence of any iteration loops the procedure described here is very fast, and crucial. An improved method to determine the broad-band small-signal equivalent circuit of FET's is thus presented. If desired, the equivalent circuit elements can be uniquely determined at any frequency describing exactly the measured S parameters, which is not possible with conventional fitting programs. Also, any frequency interval of interest can be used for averaging the analytically determined values of the small-signal elements. The validity of the equivalent circuit can be verified by plotting the determined parameters versus frequency. This improved method can also be used for devices showing low frequency effects as well as for devices with applications far beyond 5 GHz.

A method for the optimization of small signal equivalent circuits of microwave and millimeter-wave FET's based on a genetic algorithm coupled 9

with a semi heuristic local search procedure is presented in [13].The algorithm has been successfully applied to both measured and synthetic data in a wide frequency range, and it is shown that it is able to:

- consistently provide excellent model fitting and
- once the non uniqueness of solutions has been overcome by preliminary de-embedding of the device parasitics,extract unique, physically meaningful values for the equivalent circuit elements even in the presence of significant experimental errors.

One of the most interesting features of the proposed genetic algorithm is that it requires practically no a priori knowledge of the equivalent circuit parameter values. In the optimization experiments described in this paper it has been shown that even though these values are allowed to span over two orders of magnitude, convergence to a very good fitness can consistently be achieved. This means that the initial-guess bias of conventional non-linear programming techniques is not an issue for our algorithm, which is an important result of this paper. With straightforward modification, like a change of the routine that calculates the model S-parameters, the algorithm can be used to optimize small-signal equivalent circuits of different topologies, such as those used for bipolar transistors; in principle, it may also be applied to 6 a wide range of large-signal modelling problems, whenever an efficient and initial-guess insensitive optimization tool is required. A complete extraction process of all equivalent-circuit elements in a GaN HEMT device is presented in [36].

The obligation to hold back the channel resistance by forward biasing the gate terminal is avoided. Clear-cut expressions are introduced to guess these parasitic quantities and consequently recover the effectiveness of the systematic optimization method. A time dependency in the output conductance has been introduced into the equivalent-circuit topology. For the observed increase in phase delay at higher frequencies it efficiently represents a time delay at the output.

The analytical expression values of intrinsic equivalent circuit elements are determined by using an optimization procedure that is straightforward.All extrinsic parasitic elements are evaluated under cold FET condition without forward biasing gate terminal as there is no requirement 10 for the channel

resistance to be small. A time dependency in the output conductance has been introduced into the equivalent circuit topology. It represents a time delay at higher frequency. A new method for determining the small-signal equivalent circuit components of FET(s) has been described in [37].

2.3 Review on Extraction of extrinsic parameters

In [38] a new small signal equivalent circuit (SSEC) is introduced which consists of both extrinsic and intrinsic circuit element. Small-signal equivalent circuit (SSEC) models demonstrate being compulsory to a broad range of activities, ranging from the considerate studies of device physics, the study of device presentation, the characterization and contrast of fabrication processes, the bottom-up assembly of large-signal models, the extraction of intrinsic noise parameters, and the design of monolithic microwave integrated circuits (MMICs). Because the SSEC model links the physical structure of the device to its circuit behavior, it allows investigation of the microwave performance as a function of the device geometry. A physically representative model can therefore be used for frequencies extending beyond those of the measurement setup. In the course of this work, specific investigation is made to demonstrate the differences brought about by diverse materials for devices implemented with a given mask set.

The extrinsic SSEC is introduced to clearly describe the pad capacitances on various substrates and buffer materials, regardless of their residual conductivity.

An enhanced equivalent circuit for the pinched-off FET at Vds = 0 has been anticipated in [39] which preserves the symmetry of the device when viewed from gate and drain. Parasitic drain capacitances have been evaluated from low-frequency Y parameters.

In 2009, a new scalable modelling approach has been presented in [40]. It is based on the explanation of a lumped module explanation of the extrinsic parasitic network, which is verified to be flawlessly scalable with the number of gate fingers and the corresponding finger width. The device scalable parasitic elements are recognized by using only EM simulation data of just one reference device. This means that neither device dimensions in expedient conditions of passivity (i.e., pinched-off or forward-gate cold FET conditions), nor different-in-size device measurements are required for the extrinsic element mining.

The model is then compared to the classic methods of Dambrine [37] and White and Healy [39] under cold FET pinch off condition and its advantages are pointed out.A robust and accurate method for determining the remaining extrinsic elements is also presented in the paper. Also an assessment has been provided for the error caused while neglecting the cold-FET channel capacitance. The SSEC model extraction has been described at typical bias points for $2m^2$ AlInAs/GaInAs HEMT and GaN HEMTs on Si(111).There are a huge number of model extraction methods that uses the forward gate bias but how much forward gate bias is appropriate is not properly mentioned.Further the S-parameter measurement for intrinsic elements have been reported in many paper but the S-parameter measurement with the intrinsic and extrinsic elements together are still under progress.

Despite White and Healy's improvements, extracting the extrinsic capacitances in a cold-FET pinch-off condition still involves three notable drawbacks:

- It requires a well pinched-off device with low gate leakage levels.
- Large negative gate voltages must be applied to reduce extraction dependence on gate voltage.
- Conductive or imperfectly insulating buffer/substrates cannot be taken into account.

In order to avoid the aforementioned drawbacks, a passive open dummy structure can be used to determine the extrinsic capacitance elements. This can either be done through full-wave electromagnetic simulations, as reported by Resca in 2009 [40] or by measurement as proposed by Goto [32] and Chumbes [31] in 1996 and 1999, respectively. Imperfections of the buffer and the substrate can on the other hand only be determined by actual measurements.

In [41] a small signal model is proposed for pseudomorphic high electron mobility transistor (PHEMT). Using particle swarm population-based search method as a global search and optimization tool both the extrinsic and intrinsic circuit elements of a small-signal model are determined. On a 200 m gate width AlGaAs/InGaAs PHEMT the parameters extraction of the small-signal model is performed. From the measured S-parameters the equivalent circuit elements for a proposed 18 elements model are determined directly. The method described in this paper has been used to extract the

parameters of the proposed small-signal model from 0.5 up to 18 GHz. The verification of the validity of the proposed method is done by comparing the simulated small S-parameters with the measured data of a $0.25m$ by $200m$ gate PHEMT.

In the present work both intrinsic and extrinsic circuit elements are considered for the analysis in order to accurately model all the parasitic effects in the high frequency ranges. The extrinsic SSEC is introduced to clearly describe the pad capacitances on various substrates and buffer materials, regardless of their residual conductivity.

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Chapter 3

FET Small Signal Modeling

3.1 Overview of GaAs MESFET

The Gallium Arsenide metal semiconductor field effect transistor (GaAs MESFET) influences as one of the mostly used devices, in modern MIC/MMIC applications such as switches, power ampliers, low noise ampliers, oscillator, etc. Reliable modelling methodology and accurate device models of GaAs MESFET are currently extremely useful and in demand.

Today,the gallium arsenide metal semiconductor eld effect transistor (GaAs MESFET) has served as the driving force behind the technological advancements of microwave and millimeter-wave integrated circuits.Due to its relatively simple geometry with great proficiency and outstanding performance,the GaAs MESFET has become one of the most important semiconductor devices in MMIC technology and digital GaAs ICs.

3.1.1 History of GaAs MESFET

The primary development of a gallium arsenide eld eect transistor using a Schottky gate was undertaken by Mead in 1966 [1].In 1967,a GaAs MESFET was fabricated by Hopper and Lehrer [2].A prominent step was made by Turner et al in 1971 [3], when 1 m gate length GaAs MESFET was fabricated, giving f_{max} equal to 50GHz and useful gain up to 18GHz.With the development of the quality of GaAs materials and basic FET prototype technology,rapid development was achieved for GaAs MESFET devices in the direction of both low noise and high power applications.The rst low noise GaAs MESFET was reported by Leichti et al.[4] in 1972.And later in 1973,the rst high power GaAs MESFET was reported by Fukuta et al. in Fujitsu [5].With the early progress of GaAs MESFET technology, a simple

logic circuit consisting of MESFETs and Schottky diodes was monolithically integrated on a semi insulating GaAs substrate.The feasibility of using GaAs metal-semiconductor field-effect transistors (GaAs MESFET's) in fast switching and high-speed digital integrated circuit applications was demonstrated in 1974 [6].

In the late 70s and the 80s, reports on a process for the medium-scale integration of MESFET digital circuits on GaAs will be offered.Gate propagation delays less than 100 ps with fanout of two and binary division from DC to 2 GHz had been achieved[7].The manufacturing technology was not mature enough to support the cost and volume requirement for the consumer mass market.By the early 1990s,GaAs MESFET manufacturing technology was developing rapidly,and the cost was cut down.

As a result of which GaAs technology became more competitive compared to other process technologies. Since then,the GaAs MESFET device and GaAs integrated circuits have found a wide range of applications, such as in wireless systems.The demand for mobile and personal communication systems has increased the use of GaAs MESFET for high-speed digital and analog integrated circuits.GaAs based heterojunction devices including high electron mobility transistor (HEMT) and heterojunction bipolar transistor (HBT) provide a range of performance advantages.In the case of HEMT technology,it has the advantage of higher frequency performance and lower noise figure than that achievable by MESFET of similar gate length.

GaAs HBT technology has high transconductance, high power density, and excellent matching of a bipolar transistor. Also, the HBT transistor can operate from a single power supply.GaAs HBTs are commonly used for high power amplification applications.InP transistors (HBTs, HEMTs) would dominate at extremely high frequency.

However, the market share of MESFET is small because SiC substrate is costly, and SiC and GaN technology is still in an embryonic stage compared to GaAs. Despite the superior performance of these technologies mentioned above, GaAs MESFET technology remains competitive for various applications. Its performance is satisfactory for many areas, and has a lower cost. In current years, GaAs MESFET technology is also facing serious competition from silicon and silicon-germanium technologies in RF and microwave applications.

A MESFET (metal–semiconductor eld-eect transistor) is a eld-eect transistor semiconductor device similar to a JFET with a Schottky (metalsemiconductor) junction instead of a p-n junction for a gate.

F_t and F_{max} are the figures of merit used to benchmark the high frequency performance of RF transistors.F_t is the frequency at which current gain equals unity and output is AC shorted.F_t is also known as cut-off frequency.F_{max} is the frequency at which maximum unilateral power gain equals unity.F_{max} is also known as maximum frequency of oscillation. "Unilateral" means the 2-port network is one directional,i.e. S12 = 0.Both parameters can be measured and derived using network analyzer and S-parameters.

The key advantage of the MESFET is the higher mobility of the carriers in the channel as compared to the MOSFET. Since the carriers located in the inversion layer of a MOSFET have a wavefunction, which extends into the oxide, their mobility - also referred to as surface mobility - is less than half of the mobility of bulk material. As the depletion region separates the carriers from the surface their mobility is close to that of bulk material. The higher mobility leads to a higher current, transconductance and transit frequency of the device.

The disadvantage of the MESFET structure is the presence of the Schottky metal gate. It limits the forward bias voltage on the gate to the turn-on voltage of the Schottky diode. This turn-on voltage is typically 0.7 V for GaAs Schottky diodes. The threshold voltage therefore must be lower than this turn-on voltage. As a result it is more difficult to fabricate circuits containing a large number of enhancement-mode MESFET.

The higher transit frequency of the MESFET makes it particularly of interest for microwave circuits. While the advantage of the MESFET provides a superior microwave amplifier or circuit, the limitation by the diode turn-on is easily tolerated.Typically depletion-mode devices are used since they provide a larger current and larger transconductance and the circuits contain only a few transistors, so that threshold control is not a limiting factor. The buried channel also yields a better noise performance as trapping and release of carriers into and from surface states and defects is eliminated.

CMOS continues to advance to smaller geometries.Compared to silicon, GaAs has a higher electron mobility and peak drift velocity[8].The electron velocity at low eld is sufficiently high so that high switching speed and therefore high cuto frequency can be achieved.The primary advantages for using GaAs

over silicon are large transconductance, low ON resistance, and fast switching speed. Unlike Silicon, a semi-insulting GaAs substrate can be formed. This contributes to the simple structure of the GaAs MESFET, and the high resistivity of the GaAs substrate results in very small parasitic capacitance.

The drawback of MESFET technology is a limitation related to the voltage swing limited by the gate-leakage current; this reduces the noise margin of the circuit. On the other hand, silicon technologies have been more acceptable, and provide a dominant level of integration. Silicon technologies also have the advantage of integrating analog design with digital design[9]. This makes it possible to design single chip ICs for mixed signal systems. For SiGe devices, the low breakdown voltage limits their usage in power applications. Compared to SiGe devices, the GaAs FET gives more efficient power amplification.

GaAs devices normally dominate when higher frequency and increased power requirement are addressed. GaAs MESFET is the workhorse of GaAs Technology. To sum up, GaAs MESFET has wide applications even though it is facing strong competition from other device technologies[10].

3.1.2 Overview of Device Model

In the early days, microwave circuit design was based upon a low volume cut-and-try approach in which a preliminary design was built, tested and optimized until the desired performance is obtained. The circuit was then redesigned and fabricated. This approach was engineering labour intensive and not compatible with low production costs. The computer-aided design (CAD) then emerged to permit the circuit design to be completed, simulated and fully tested in the computer before its fabrication.It is very important to accurately simulate the circuit during the design stage, so as to closely correlate the design result with its practical performance.

Commercially available CAD software such as ADS and Cadence are widely employed in microwave system design. The accuracy of simulation results of these CAD tools is largely based on an accurate prediction of the device involved in the circuit.As a result, accurate models for both active and passive devices and elements are greatly needed.Specially, since GaAs MESFETs are the main building blocks of a large number of microwave applications, it is absolutely necessary to develop accurate GaAs FET models to improve the circuit performance prediction. Currently a good number of GaAs MESFET models exist, and each of them can be classified into special categories.For

example, the FET models can be grouped into physically based model, empirical model and experimental model based on their derivation. Among these three, the empirical model can be easily implemented into circuit simulators. Thus, they are most widely used by circuit designers and in device libraries. Moreover, according to different types of their prediction performance, these FET models can also be grouped into small-signal model and large-signal model. Small-signal model mainly focuses on the scattering-parameter of the device whilst the large-signal model is important for non-linear MESFET modelling.Although much work has been done in the modelling of GaAs MESFET, accurate linear and non-linear models of this active device are still in great demand.

Numerous MESFET fabrication possibilities have been explored for a wide variety of semiconductor systems. Some of the main application areas are military communications, as front end low noise amplifier of microwave receivers in both military radar devices and communication, commercial optoelectronics, satellite communication, as power amplifier for output stage of microwave links, and as a power oscillator.

3.1.3 History

The evolution of technology computer-aided design (TCAD),the synergistic combination of process,device and circuit simulation and modeling tools finds its roots in bipolar technology,starting in the late 1960s,and the challenges of junction isolated,double-and triple-diffused transistors.These devices and technology were the basis of the first integrated circuits;nonetheless,many of the scaling issues and underlying physical effects are integral to IC design,even after four decades of IC development.With these early generations of IC,process variability and parametric yield were an issue,a theme that will re-emerge as a controlling factor in future IC technology as well.
Process control issues,both for the intrinsic devices and all the associated parasitics presented formidable challenges and mandated the development of a range of advanced physical models for process and device simulation.Starting in the late 1960s and into the 1970s,the modeling approaches exploited were dominantly one and two-dimensional simulators.While TCAD in these early generations showed exciting promise in addressing the physics-oriented challenges of bipolar technology, the superior scalability and power consumption of MOS technology revolutionized the IC industry.By the mid-1980s,CMOS became the dominant driver for integrated electronics.Nonetheless, these early TCAD developments [4][5] set the stage for their growth and broad

deployment as an essential tool set that has leveraged technology development through the VLSI and ULSI eras which are now the mainstream.
IC development for more than a quarter-century has been dominated by the MOS technology.In the 1970s and 1980s NMOS was favoured owing to speed and area advantages,coupled with technology limitations and concerns related to isolation, parasitic effects and process complexity.During that era of NMOS dominated LSI and the emergence of VLSI,the fundamental scaling laws of MOS technology were codified and broadly applied[6].It was also during this period that TCAD reached maturity in terms of realizing robust process modeling (primarily one-dimensional) which then became an integral technology design tool,used universally across the industry[7].At the same time device simulation,dominantly two-dimensional owing to the nature of MOS devices,became the work-horse of technologists in the design and scaling of devices[8][9].The transition from NMOS to CMOS technology resulted in the necessity of tightly coupled and fully 2D simulators for process and device simulations.This third generation of TCAD tools became critical to address the full complexity of twin-well CMOS technology including issues of design rules and parasitic effects such as latch-up[10][11]. An abbreviated perspective of this period,through the mid-1980s,is given in [12] and from the point of view of how TCAD tools were used in the design process[13].

3.2 Introduction to modeling

Engineers are interested in designing devices and processes and systems. That is, beyond observing how the world works, engineers are interested in creating artifacts that have not yet come to life. We begin this section with a dictionary definition of the word model: model(n): a miniature representation of something; a pattern of something to be made; an example for imitation or emulation; a description or analogy used to help visualize something (e.g.,an atom) that cannot be directly observed; a system of postulates, data and inferences presented as a mathematical description of an entity or state of affairs.The appearance of Very Large Scale Integration caused a pronounced interest in concentrating on device modeling.

It was in the early 1960's when the first integrated circuits which just contained a few devices became commercially available.Since then an evolution has taken place so that the manufacture of integrated circuits with about 500.000 transistors per single chip is possible nowadays.This upcoming Very-Large-Scale-Integration (VLSI) certainly revealed the need of a better understanding of the basic device physics.The miniaturization of the single transistor, which is one of the inseparable preconditions of VLSI, brought about

a collapse of the classical device models, because completely new phenomena emerged and even dominated the device behavior. One consequence of this evidence led to an unimaginable number of suggestions of how to modify the classical models to incorporate several of the new phenomena. Additionally new activities have been initiated to explore the physical principles which make a device operational. The number of scientific publications which utilize the terms *device analysis, device simulation and device modeling*[1,2,3] The characteristic feature of early modeling was the separation of the interior of the device into different regions, the treatment of which could be simplified by various assumptions like special doping profiles, complete depletion and quasi-neutrality. These separately treated regions were simply connected to produce the overall solution. If analytic results are intended, any other approach is prohibitive.

Fully numerical modeling based on partial differential equations [4] which describe all different regions of semiconductor devices in one unified manner was first suggested by Gummel [5] for the one dimensional bipolar transistor. This approach was further developed and applied to pn-junction theory by DeMari [6,7]and to IMPAXT diodes by Scharfetter and Gummel [8].The first two dimensional numerical analysis of a semiconductor device was carried out by Kennedy and O'Brien [9] for the junction field effect transistor. Since then two dimensional modeling has been applied to fairly all important semiconductor devices.

Device Model
A model means a set of mathematical formulas, circuit representations, tables and reference standards.
CMOS Device Modeling for Circuit Design

Before a circuit is designed, to be integrated by CMOS VLSI technology, a model must be adopted which will describe behavior of all components successfully

3.2 Significance of Modeling

Transistors are simple devices with complicated behavior. In order to ensure the reliable operation of circuits employing transistors, it is necessary to scientifically model the physical phenomena observed in their operation using transistor models.There exists a variety of different models that range in

complexity and in purpose. Transistor models divide into two major groups: models for device design and models for circuit design.
The modern transistor has an internal structure that exploits complex physical mechanisms.Device design requires a detailed understanding of how device manufacturing processes such as ion implantation,impurity diffusion,oxide growth, annealing,and etching affect device behavior.Process models simulate the manufacturing steps and provide a microscopic description of device "geometry" to the device simulator."Geometry" does not mean readily identified geometrical features such as a planar or wrap-around gate structure, or raised or recessed forms of source and drain.It also refers to details inside the structure,such as the doping profiles after completion of device processing.

With this information about what the device looks like,the device simulator models the physical processes taking place in the device to determine its electrical behavior in a variety of circumstances: DC current-voltage behavior, transient behavior (both large-signal and small-signal),dependence on device layout (long and narrow versus short and wide, or interdigitated versus rectangular,or isolated versus proximate to other devices).These simulations tell the device designer whether the device process will produce devices with the electrical behavior needed by the circuit designer, and is used to inform the process designer about any necessary process improvements.Once the process gets close to manufacture, the predicted device characteristics are compared with measurement on test devices to check that the process and device models are working adequately.

Although long ago the device behavior modeled in this way was very simple – mainly drift plus diffusion in simple geometries – today many more processes must be modeled at a microscopic level;for example,leakage currents in junctions and oxides,complex transport of carriers including velocity saturation and ballistic transport,quantum mechanical effects,use of multiple materials (for example, Si-SiGe devices,and stacks of different dielectrics) and even the statistical effects due to the probabilistic nature of ion placement and carrier transport inside the device.Several times a year the technology changes and simulations have to be repeated.The models may require change to reflect new physical effects,or to provide greater accuracy.The maintenance and improvement of these models is a business in itself.

These models are very computer intensive,involving detailed spatial and temporal solutions of coupled partial differential equations on three-dimensional grids inside the device[1][2][3][4][5].Such models are slow to run and provide detail not needed for circuit design. Therefore, faster transistor models ori-

ented toward circuit parameters are used for circuit design.

Transistor models are used for almost all modern electronic design work.Analog circuit simulators such as SPICE use models to predict the behavior of a design.Most design work is related to integrated circuit designs which have a very large tooling cost, primarily for the photo masks used to create the devices, and there is a large economic incentive to get the design working without any iterations.Complete and accurate models allow a large percentage of designs to work the first time.

Modern circuits are usually very complex.The performance of such circuits is difficult to predict without accurate computer models, including but not limited to models of the devices used.The device models include effects of transistor layout: width,length,inter-digitation,proximity to other devices;transient and DC current-voltage characteristics; parasitic device capacitance,resistance, and inductance;time delays;and temperature effects;to name a few items[6].

Physical models
These are models based upon device physics,based upon approximate modeling of physical phenomena within a transistor. Parameters within these models are based upon physical properties such as oxide thicknesses,substrate doping concentrations, carrier mobility,etc.In the past these models were used extensively,but the complexity of modern devices makes them inadequate for quantitative design.Nonetheless,they find a place in hand analysis(that is, at the conceptual stage of circuit design),for example,for simplified estimates of signal-swing limitations.

Empirical models
This type of model is entirely based upon curve fitting, using whatever functions and parameter values most adequately fit measured data to enable simulation of transistor operation.Unlike a physical model,the parameters in an empirical model need have no fundamental basis, and will depend on the fitting procedure used to find them.The fitting procedure is key to success of these models if they are to be used to extrapolate to designs lying outside the range of data to which the models were originally fitted.Such extrapolation is a hope of such models,but is not fully realized so far.

Small-signal linear models Small-signal or linear models are used to evaluate stability, gain, noise and bandwidth, both in the conceptual stages of circuit design (to decide between alternative design ideas before computer simulation is warranted) and using computers. A small-signal model is gen-

erated by taking derivatives of the current-voltage curves about a bias point or Q-point.As long as the signal is small relative to the non-linearity of the device,the derivatives do not vary significantly,and can be treated as standard linear circuit elements. A big advantage of small signal models is they can be solved directly, while large signal non-linear models are generally solved iteratively, with possible convergence or stability issues.By simplification to a linear model,the whole apparatus for solving linear equations becomes available,for example, simultaneous equations, determinants,and matrix theory (often studied as part of linear algebra), especially Cramer's rule.Another advantage is that a linear model is easier to think about,and helps to organize thought.

Small-signal parameters
A transistor's parameters represent its electrical properties.Engineers employ transistor parameters in production-line testing and in circuit design.A group of a transistor's parameters sufficient to predict circuit gain, input impedance, and output impedance are components in its small-signal model.A number of different two-port network parameter sets may be used to model a transistor.These include:

- Transmission parameters (T-parameters)
- Hybrid-parameters (h-parameters)
- Impedance parameters (z-parameters)
- Admittance parameters (y-parameters)
- Scattering parameters (S-parameters)

Scattering parameters,or S parameters,can be measured for a transistor at a given bias point with a vector network analyser.S parameters can be converted to another parameter set using standard matrix algebra operations.

Rapid progress of IC technology in recent years has led to reduction of device dimensions and development of sophisticated process steps.With increase in complexity in fabrication of VLSI chips,need for device modelling and process simulation has become increasingly important.In device modelling, with the help of an appropriate model of a device, one can design a device of chosen specifications based on a set of device parameters.The performance of VLSI devices in turn are closely determined by process conditions.It is, therefore, necessary to understand,characterise and optimize the

process steps involved in device fabrication.This can be achieved by simulation of each process through formulation of an accurate model of the basic physical mechanism involved.Once the models are developed and coded in a comprehensive computer program,the device and process parameters can be correctly predicted without going through the actual process and fabrication steps.

3.3 Different types of modeling:

The three most common types of models used in industry today are: physical models ,compact models and behavioural models.The schematic diagram of the various techniques have been depicted in Figure 3.

3.3.1 PHYSICAL MODELING:

Physical modeling is a way of modeling and simulating systems that consist of real physical components.It employs a physical network approach, where the blocks correspond to physical elements.We join these blocks by lines corresponding to the physical connections that transmit power.This approach lets us describe the physical structure of a system, rather than the underlying mathematics.These models support all phases of Model-Based Design.
An example of process modeling applied to MESFET has been shown in Figure 1. Physical modeling tools bring accuracy and efficiency to this effort by enabling us to:

- Assemble system-level models that span multiple physical domains and include the control system in a single environment
- Create reusable models of our physical system with physical ports, in addition to input and output signals
- Model custom physical components using a physical modeling language.

These models include all forms of diagrams, drawings graphs and charts,most of which are designed to deal with specific types of problems.By presenting significant factors and inter-relationships in pictorial term, physical models are able to a problem in a manner that facilitates analysis.Physical models, as the name suggests, are based on the physics of the device technology.
Due to the nature of the physical model, complex model equations have to be used, which can lead to time-consuming simulations. The advantage of the physical model is that it can be successfully used over the largest operating range, compared to alternate methods, since equations are used to describe

complex physical rules rather than actual measurement results.

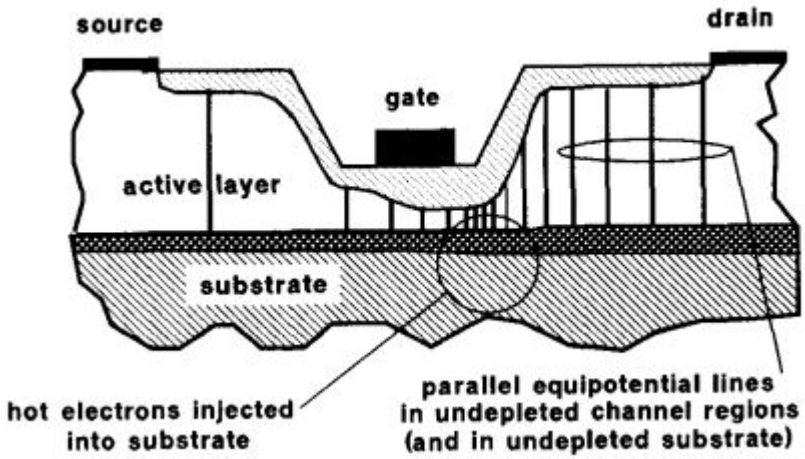


Figure 1: Example of process modeling applied to MESFET

In contrast to equivalent circuit models which can be used to reverse-model devices using measured data, physical models are essentially predictive, producing results based on the physical geometry and description of the device and circuit. This type of model is not obtained by fitting model parameters to measured electrical data as in equivalent circuits and semi-empirical physics-based models, and hence the quality of agreement between measured and simulated results is mainly a function of the quality and accuracy of process data supplied to the model, assuming that the physics and parasitic are adequately described.Flow diagram of an integrated CAD tool for the simulation of MESFET devices from the technological stage to circuit performance has been beautifully depicted in Figure 2. In the case of sub-micron gate length MESFET's this implies that a model capable of representing hot electron effects is required. There have been many contributions of full two-dimensional modelling of GaAs MESFET's, the more recent of which address the issue of CAD and optimization [10],[11].
However, these comprehensive two-dimensional models are too computationally intensive for present resources, preventing interactive design and analysis. Quasi-two-dimensional models [12], [14], [15], [16], [17] retain the essential physical description, but allow several orders of magnitude improvement in speed [12],[13].
Physical simulation allows the internal behavior of the device to be completely known, thereby leading to both better understanding of device oper-

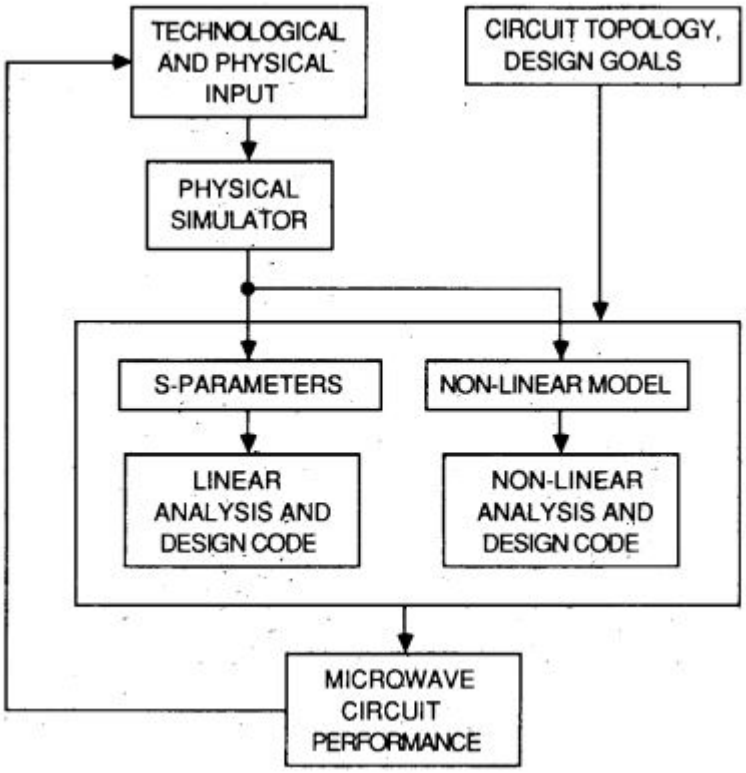


Figure 2: Flow diagram of an integrated CAD tool for the simulation of MESFET devices from the technological stage to circuit performance

ation and easier and more accurate identification of equivalent circuits.

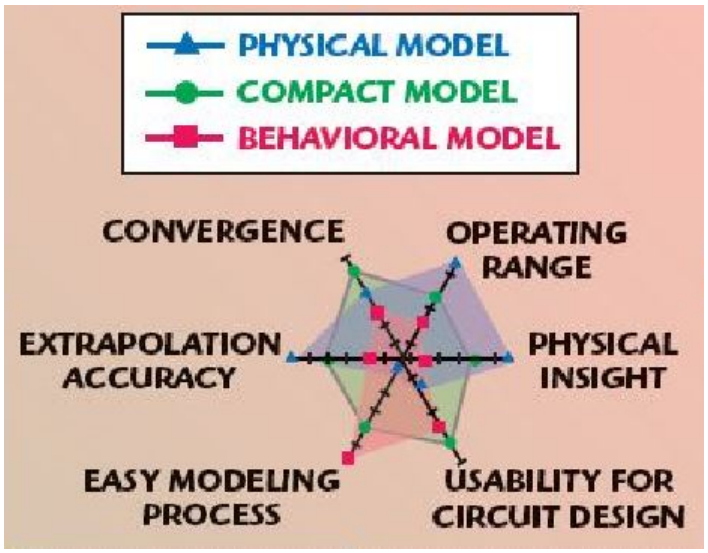


Figure 3: Different types of modeling techniques

3.3.2 MATHEMATICAL MODELING:

Mathematical model(n);a representation in mathematical terms of the behavior of real devices and objects.Mathematical modeling is beyond doubt much more than just taking a situation, usually one from the real world, and using variables and one or more elementary functions that fit the phenomena under consideration to arrive at a conclusion that can then be interpreted in light of the original situation.The general steps to perform this type of mathematical modeling is presented in figure 4.Mathematical modeling can be defined as a mathematical process that involves observing a phenomenon, conjecturing relationships, applying mathematical analyses (equations, symbolic structures,etc.),obtaining mathematical results.

While the goal of mathematical modeling in cognitive psychology is to select one model from a set of competing models that best captures the underlying mental process, the researcher often chooses the model that best fits a particular set of data.Presumably, the justification for this procedure is that the model providing the best fit (e.g., the one that accounts for the most variance) is the one that most closely approximates the underlying mental process.In fact, this justification is unwarranted, for a highly complex model

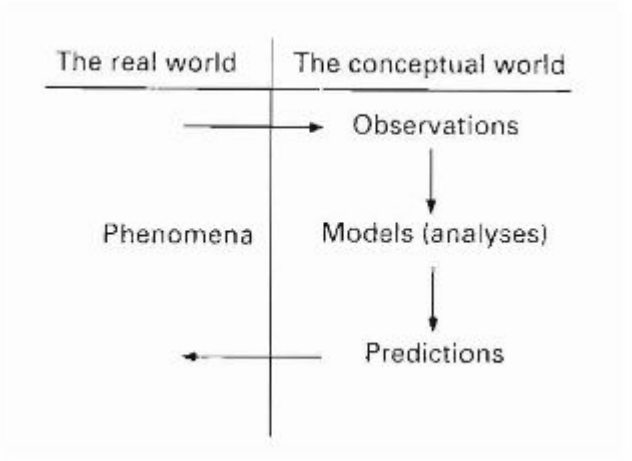


Figure 4: Steps in Mathematical Modeling

can provide a good fit without necessarily bearing any interpretable relationship with the underlying process.The purpose of this paper is to support this claim and, in so doing, demonstrate the importance of complexity in model selection.Specifically,it is shown that model selection based solely on the fit to a particular set of data will result in the choice of an unnecessarily complex model that overfits the data and thus generalizes poorly to other data generated by the same underlying process.

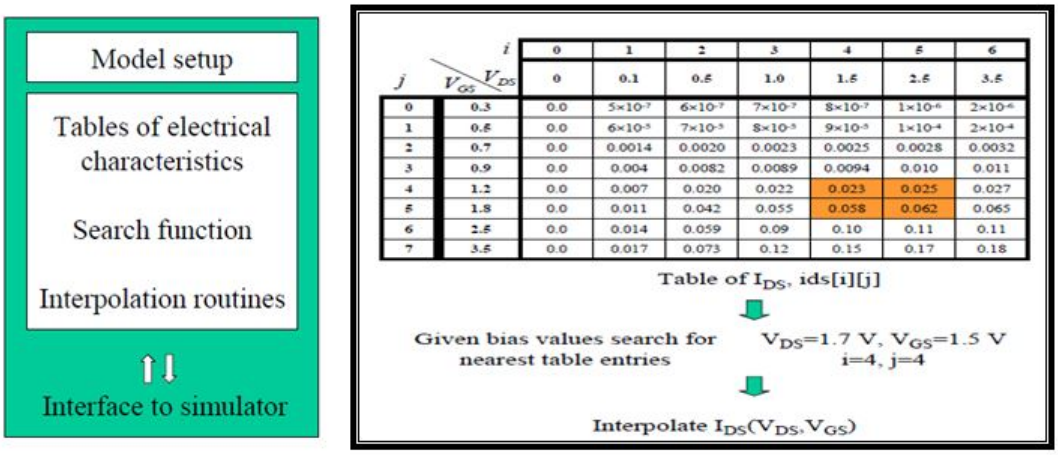
3.3.3 TABLE BASED MODELING

Matlab/Simulink is a very useful tool to design accurate mathematical model of physical system and to analyze its performance.Later on model based on lookup table block was implemented which provides less computational complexities [10 -13].
In computer science, a lookup table is an array that replaces runtime computation with a simpler array indexing operation. A lookup table block uses an array of data to map input values to output values. Simulink performs a "lookup" operation for a given input values, to retrieve the corresponding output values from the table. If input values are not defined, lookup table block estimates the output values based on nearby values [14]. This method uses the experimental data for the modeling of a system which is imported from the excel file to the Matlab/Simulink. It provides a curve fitting tool to develop a three-dimensional surface from the data points of an array.
The behavior of actual physical systems often varies with time due to wear, environmental conditions, and manufacturing tolerances. Use adaptive lookup

tables to model the time-varying behavior of physical plants. Adaptive lookup table values update dynamically with incoming input-output data as the model is simulated [15-21].

3.3.3.1 Table look-up models

An example to show the table-based model is shown in figure 5, where V_{GS} and V_{DS} are presented in the form of a Look up table.



j	V_{GS} \ V_{DS}	0	0.1	0.5	1.0	1.5	2.5	3.5
	i	0	1	2	3	4	5	6
0	0.3	0.0	5×10^{-7}	6×10^{-7}	7×10^{-7}	8×10^{-7}	1×10^{-6}	2×10^{-6}
1	0.5	0.0	6×10^{-5}	7×10^{-5}	8×10^{-5}	9×10^{-5}	1×10^{-4}	2×10^{-4}
2	0.7	0.0	0.0014	0.0020	0.0023	0.0025	0.0028	0.0032
3	0.9	0.0	0.004	0.0082	0.0089	0.0094	0.010	0.011
4	1.2	0.0	0.007	0.020	0.022	0.023	0.025	0.027
5	1.8	0.0	0.011	0.042	0.055	0.058	0.062	0.065
6	2.5	0.0	0.014	0.059	0.09	0.10	0.11	0.11
7	3.5	0.0	0.017	0.073	0.12	0.15	0.17	0.18

Figure 5: Table based models

3.3.3.2 The good points of Table based models

- Models for new devices can be implemented quickly
- Less time-consuming parameter extraction
- Fewer errors in implementation
- Controllable accuracy– Density of table data and interpolation method
- Measurement-based model– no need to change model equations

3.3.3.3 Table Models: The not so good points

- Limited predictive capabilities

- Large "model files" – storage and distribution issues
- Larger memory requirements
- "Black-box" not suitable for every purposes

In recent years, table-based models have become important tools for rapid accurate device modeling. Several groups in the U.S. and Europe [22]–[25] developed and put these models into practical use. The models are highly accurate and device independent and they expedite simulations because they are based directly on the measured data. Performance between measured points is interpolated with spline functions and these functions should be differentiable to a high order of derivatives in order to ensure a correct description of harmonics and convergence within harmonic balance (HB) simulations. Specific software and equipment is needed to extract and use these types of models, and technology-related changes in the device characteristics require repeating the extraction procedure. Care should be taken to extract data carefully because the model can give unexpected results when operated out of the specified range.

3.3.4 GLOBAL MODELING

In the most comprehensive book on the topic [26], global modeling is defined as: Computer modeling done to investigate social questions or problems of global scale. Global Modeling of Microwave and millimeter-wave circuits and systems means developing a comprehensive analysis and design tool that incorporates several physical aspects of the problem.

When semiconductor devices are operated at high frequencies, the inherent coupling between fluctuations in charge distributions and EM fields (and the resulting effect it has on carrier transport) must be included into the simulation model. As the device operating frequency increases, the period of the EM waves begins to approach the relaxation time of carriers in the semiconductor material.The necessities of global modeling is prominently presented in figure 6.Thus, a finite amount of time is physically required for carriers to react to the field and to change their velocities. This means that the resulting transport is directly affected by the EM wave propagation in the device.Static simulators (i.e. Poisson solvers) are unable to directly capture this carrier-wave interaction.Furthermore,they do not properly account for the existing magnetic fields present in a real device. Therefore, accurate simulation of high-frequency devices requires tools that account for both particle dynamics and EM wave interaction with the carriers.

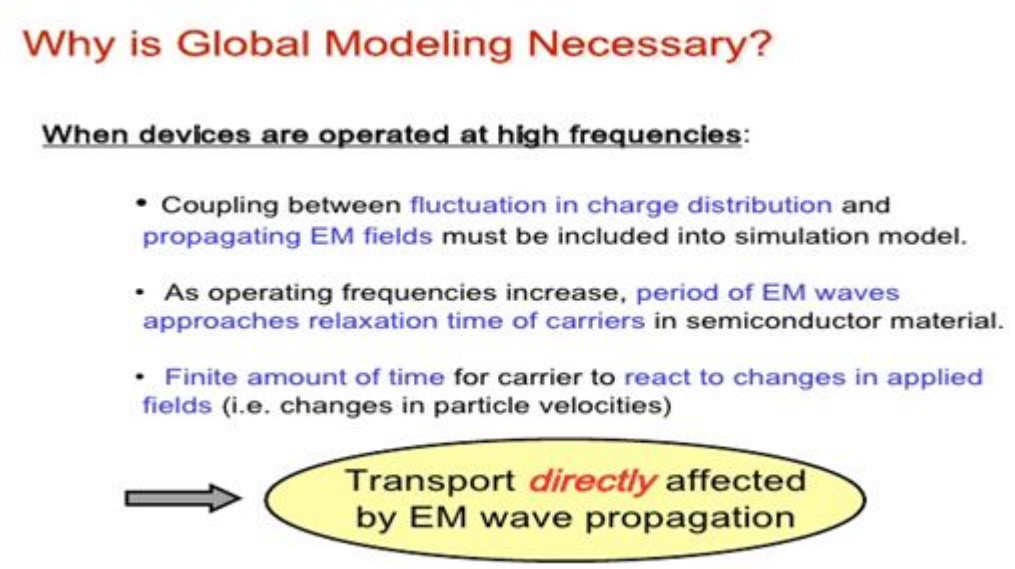


Figure 6: Golabl Modeling

3.3.5 BEHAVIORAL MODELING:

Behavioral modeling is the highest level of abstraction in the Verilog HDL. All that a designer need is the algorithm of the design, which is the basic information for any design. This level simulates the behavioral level of the circuits and development rate in this level is highest. Although the development rate in this abstraction level is high there are some drawbacks such as the delay modeling is not possible. In practice any circuit is first implemented in this level to understand the theoretical possibility of the circuit and then it is implemented in at a lower level to analyze the practical aspects. This level of Verilog has blocking and non-blocking assignment. Blocking assignment is sequential nature and using the combination of both assignments, complex sequential can be modeled with ease.
Behavioural Modeling using Procedural Blocks and Statements :

- describes what the circuit does at a functional and algorithmic level
- encourages designers to rapidly create a prototype
- can be verified easily with a simulator

3.3.6 CHARGE BASED MODELING

Let us cite this type of model with an example.Conventional transistor models for the transient simulation of MOS circuits were formulated in terms of non-linear capacitors.A charge-based model was developed to overcome errors and to account for the bulk charge.It was shown that the capacitances between any pair of terminals are non-reciprocal.Bulk-source,bulk-drain,and drain-source couplings were modeled, as were the gate-to-bulk capacitances in saturation.The drain-source capacitances were found to be negative.The capacitance characteristics of the model was verified experimentally.The impact of the charge-based model on simulation of practical circuits was considered.Although the model was particularly useful in simulating silicon-on-insulator circuits,it gave improved simulation of bulk MOS technologies as well.

3.3.7 COMPACT MODELING:

Models of circuit elements which are sufficiently simple to be incorporated in circuit simulators and are sufficiently accurate to make the outcome useful to circuit designers are called compact. The conflicting objectives of model simplicity and accuracy make the compact modeling field an exciting and challenging research area for device physicists, electronic engineers and applied mathematicians.The priority of the test measurements utilised for building a Compact Model is shown in figure 7.Continued down-scaling of semiconductor devices has made it necessary to incorporate new physical phenomena, while extended applications have led to the inclusion of the secondary and ternary effects in order to achieve the required model accuracy.In addition several rigid requirements in terms of model continuity and qualitative behavior have been imposed over the years.At the same time, the increased size of the integrated circuits that can now be subjected to the full SPICE analysis disallowed proportional increase in the model execution time.Hence considerable effort went into compact model reformulation in such a way that dramatically increased accuracy and model sophistication are accomplished without prohibitive decrease in the computational efficiency.

The models of MOS transistors underwent revolutionary change in the last few years and are now based on new principles.The recent models of diodes, passive elements,noise sources and bipolar transistors were developed along the more traditional lines.Following this evolutionary development they became highly sophisticated and much more capable to reflect the increased

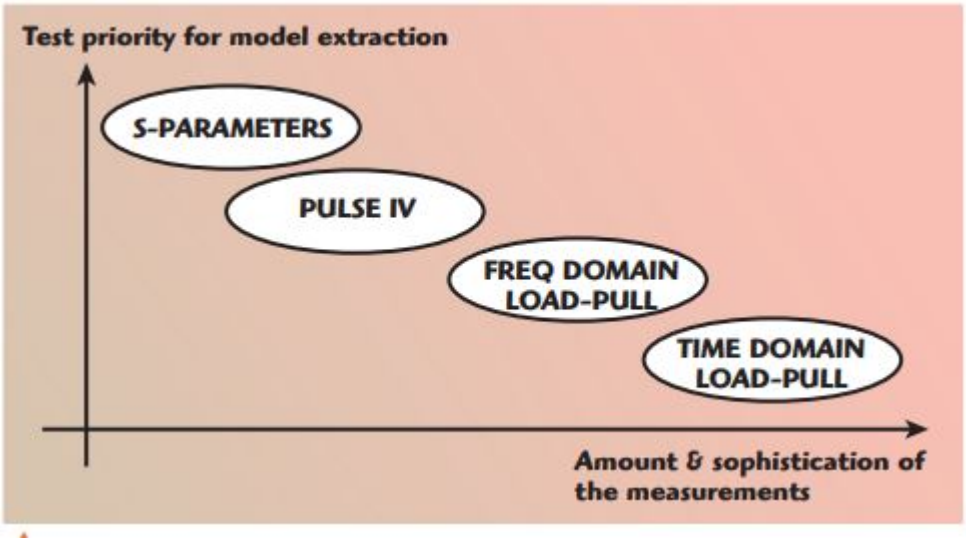


Figure 7: Measurements for Compact Model

demands of the advanced integrated circuit technology.The latter depends on the compact models for the shortening of the design cycle and eliminating the elements of over-design which is often undesirable in today's competitive environment.At the same time, statistical modeling of semiconductor devices received new significance following the dramatic reduction of the device dimensions and of the power supply voltage.
Finally, despite the complexity of the fabrication process,the multi-gate MOS transistors are now seriously considered for the purpose of controlling the small geometry effects.To evaluate the potential impact of these devices on the IC design, compact models of these devices,preferably based on the same principles as the models of traditional MOSFETs, are becoming important.The last comprehensive description of the compact models of various semiconductor devices reflects the state of the art in late 1980s [18].While remaining an influential and valuable source of information, it can no longer serve the needs of the compact modeling community in the 21st century.

3.3.7.1 Choosing Compact Modeling over other types of medeling techniques:

Compact transistor models,based on measured IV and S-parameters, allow designers to shift focus from transistor designs to circuit designs.Extracted

from quasi-isothermal pulsed IV and pulsed S-parameter data and validated with load-pull characterization,compact transistor models contain a reduced set of parameters.Unlike other model types,compact models take into account complex phenomena,such as electro-thermal and trapping effects.For simulations under nonlinear operating conditions,responses to complex modulated signals(such as EVM or ACPR) are accurately predicted as low-frequency and high-frequency memory effects are taken into account.A schematic diagram of a compact model of FET has been cited in figure 8.Compact transistor models are ideal for die-level applications,as developing such a model from IV and S-parameters are straightforward and relatively quick.
Packaged-transistor models need to include a die-level model as well as a bonding model and package model,and consequently can be time consuming and costly.

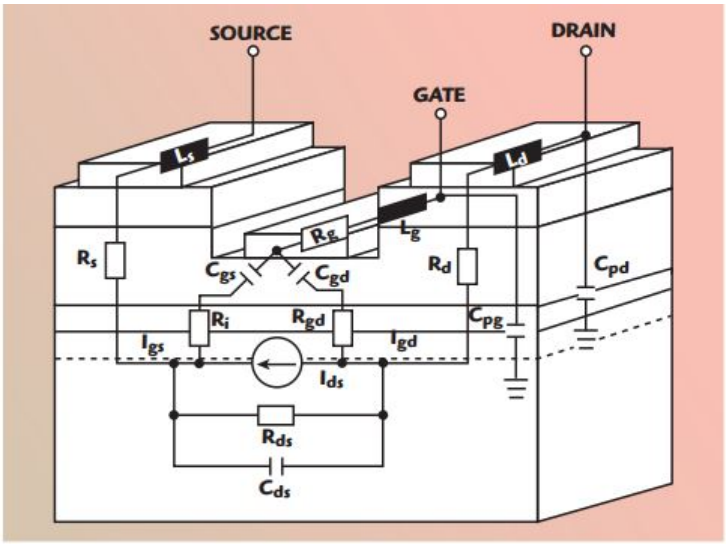


Figure 8: Compact FET model schematic

Behavioral models, based on frequency domain measurements, are far less flexible than physical or compact transistor models, but can be easily developed for any type of component(including die-level or packaged transistors). Behavioral models are considered black-box models, where only the responses of the component to some controlled stimuli are known, and are consequently only valid under the operating conditions measured.This model type is actively under development and has been recently improved to take into account memory effects [19, 20] however, as a table-based model;it cannot be as complete as a formula-based model.It is clear that each model type,

physical,compact and behavioural,has unique advantages and disadvantages, as illustrated in the above figure.

While there is no one-size-fits-all model, compact transistor models offer the shortest development time for maximum flexibility with regards to die-level transistors. Research and development of compact transistor models has been, and continues to be, an important topic for universities and institutes across the globe.[21-26] As such, an abundance of literature and documentation exists on the background RD of compact models.

The design flow of a GaN FET compact transistor model, shown in figure consists of:

- Linear model extraction through small-signal S-parameters
- Nonlinear model extractionthrough pulsed IV measurements
- Nonlinear capacitance modeling through synchronized pulsed IV/RF
- Electro-thermal modeling through temperature control
- Trapping effect modeling.
- Additionally, the compact transistor model can be validated through load-pull measurements.

3.3.8 Goals of Device Modeling

The fundamental goal in device modelling is to obtain the functional relationship among the terminal electrical variables of the device that is to be modelled. These electrical characteristics depend upon a set of parameters including both geometric variables and variables dependent upon the device physics. The circuit designer has control of the design parameters and judiciously sets these parameters during the design. The process parameters are characteristic of the semiconductor process itself and are not at the control of the circuit designer once the process has been specified. The circuit designer may, however, interact with the process engineer to help specify the process that will be used for a particular design.

For most physical devices,at best only a good approximation to the actual relationship of the variables can be obtained. Trade-offs are often made between the quality of the approximation and its complexity.The required

accuracy and the intended use of the model are factors the engineer considers when making these trade-offs.

Modeling plays a significant role in the efficient simulation of VLSI circuits. By simplifying the models used to analyze these circuits, it is possible to perform transient analyses with reasonable accuracy at speeds of one or two orders of magnitude faster than in conventional circuit simulation programs. The necessity of modeling lies in the nature of technology and its advancement. The modeling minimizes time and cost of the process involved. The mathematical model provides an insight into the behavior of the physical system that reduces the problem to its essential characteristics. Modeling means study of processes and objects in another physical environment as models that duplicate the behavior of the systems under observations. electronic engineers need to continuously improve the methods that are used for mathematical description, numerical analysis and computer-aided design of electronic devices and systems. Modeling is the only effective approach that responds to the current marketplace which demands fast and inexpensive design and production.

3.3.9 Small signal Models

Most circuits perform their task for which they are intended only over a limited excitation range.This range is typically specified in terms of a maximum input signal excursion about some nominal point.Internal to the circuit,these input variations typically cause excursions around some nonzero dc operating point.Often these inputs are sinusoids of small amplitude compared to the supply voltages providing power to the circuit.An analysis of how these small sinusoids propagate through the circuit is termed small signal analysis or ac analysis. The points(nodal voltages and branch currents) about which the circuit operates are termed as the bias points or quiescent points(Q-points).Although it might be desirable to have all Q-points at either zero volts or zero amps,it is not practical and generally not possible to do this.
Small-signal modeling is a common analysis technique in electronics engineering which is used to approximate the behavior of electronic circuits containing nonlinear devices with linear equations.It is applicable to electronic circuits in which the AC signals,the time-varying currents and voltages in the circuit,have a small magnitude compared to the DC bias currents and voltages. A small-signal model is an AC equivalent circuit in which the nonlinear circuit elements are replaced by linear elements whose values are given by the

first-order (linear) approximation of their characteristic curve near the bias point.
Many of the electrical components used in simple electric circuits, such as resistors,inductors,and capacitors are linear, which means the current in them is proportional to the applied voltage.Circuits made with these components, called linear circuits, are governed by linear differential equations,and can be solved easily with powerful mathematical methods such as the Laplace transform.
In contrast, many of the components that make up electronic circuits, such as diodes, transistors, integrated circuits, and vacuum tubes are non-linear;that is the current through them is not proportional to the voltage,and the output of two-port devices like transistors is not proportional to their input.The relationship between current and voltage in them is given by a curved line on a graph, their characteristic curve (I-V curve).In general these circuits don't have simple mathematical solutions.To calculate the current and voltage in them generally requires either graphical methods or simulation on computers using electronic circuit simulation programs like SPICE.

However in some electronic circuits such as radio receivers,telecommunications, sensors,instrumentation and signal processing circuits,the AC signals are small compared to the DC voltages and currents in the circuit.In these, approximate AC equivalent circuit can be derives, which is linear,allowing the AC behavior of the circuit to be calculated easily.In these circuits a steady DC current or voltage from the power supply,called a bias,is applied to each non-linear component such as a transistor and vacuum tube to set its operating point,and the time-varying AC current or voltage which represents the signal to be processed is added to it.The point on the graph representing the bias current and voltage is called the quiescent point (Q point).
In the above circuits the AC signal is small compared to the bias,representing a small perturbation of the DC voltage or current in the circuit about the Q point.If the characteristic curve of the device is sufficiently flat over the region occupied by the signal,using a Taylor series expansion the non-linear function can be approximated near the bias point by its first order partial derivative (this is equivalent to approximating the characteristic curve by a straight line tangent to it at the bias point).These partial derivatives represent the incremental capacitance, resistance, inductance and gain seen by the signal,and can be used to create a linear equivalent circuit giving the response of the real circuit to a small AC signal.This is called the *small-signal model*.

The small signal model is dependent on the DC bias currents and voltages

in the circuit (the Q point).Changing the bias moves the operating point up or down on the curves,thus changing the equivalent small-signal AC resistance,gain,etc. seen by the signal.
Any non-linear component whose characteristics are given by a continuous, single-valued, smooth (differentiable) curve can be approximated by a linear small-signal model.Small-signal models exist for electron tubes, diodes, field-effect transistors (FET) and bipolar transistors,notably the hybrid-pi model and various two-port networks.Manufacturers often list the small-signal characteristics of such components at typical bias values on their data sheets.

3.3.10 Large-signal analysis

Large-signal analysis pertains to setting up the bias conditions and deals with the non-linear behavior of the transistor.Small-signal analysis assumes that the transistor is correctly biased and concentrates on the linear behavior for small signals,ignoring the messy non-linear stuff.

3.3.11 Differences between small signal analysis and Large signal analysis:

A small signal model takes a circuit and based on an operating point (bias) and linearises all the components.A small signal model ignores simultaneous variations in the gain and supply values.

3.3.12 Semiconductor device modeling

Semiconductor device modeling creates models for the behavior of the electrical devices based on fundamental physics, such as the doping profiles of the devices.It may also include the creation of compact models (such as the well known SPICE transistor models),which try to capture the electrical behavior of such devices but do not generally derive them from the underlying physics.Normally it starts from the output of a semiconductor process simulation.
The power scaling which is now a major driving force in the industry are critical parameters are capacitance,power supply and clocking frequency.Key parameters that relate device behavior to system performance include the threshold voltage, driving current and sub-threshold characteristics.

It is the confluence of system performance issues with the underlying technology and device design variables that results in the ongoing scaling laws that we now codify as Moore's law.

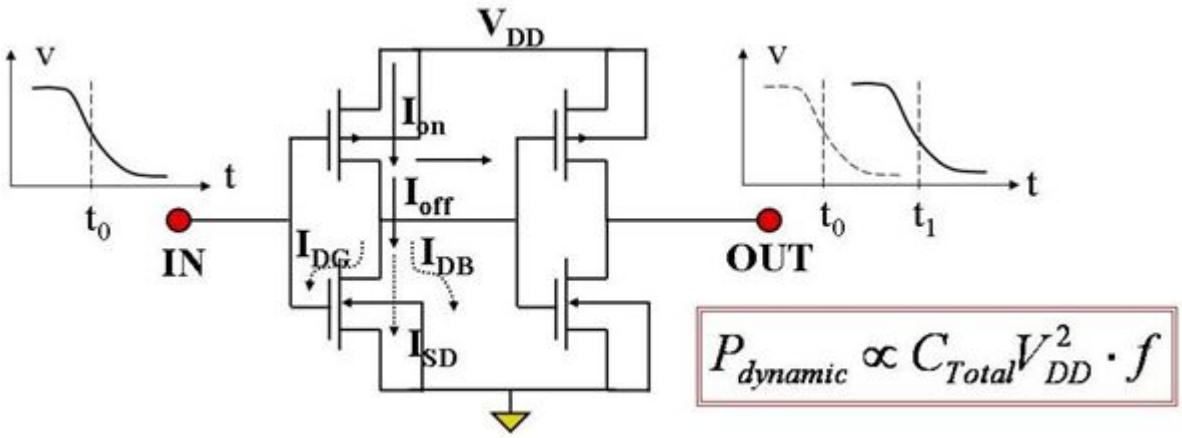


Figure 9: Schematic of two stages of CMOS inverter, showing input and output voltage-time plots.Ion and Ioff (along with IDG, ISD and IDB components)indicate technologically controlled factors. Credit: Prof. Robert Dutton in CRC Electronic Design Automation for IC Handbook, Vol II, Chapter 25

The physics and modeling of devices in integrated circuits is dominated by MOS and bipolar transistor modeling.However, other devices are important, such as memory devices, that have rather different modeling requirements.There are of course also issues of reliability engineering for example, electro-static discharge ESD) protection circuits and devices,where substrate and parasitic devices are of pivotal importance.These effects and modeling are not considered by most device modeling programs.

Physics driven versus compact models:
Physics driven device modeling is intended to be accurate,but it is not fast enough for higher level tools, including circuit simulators such as SPICE. Therefore, circuit simulators normally use more empirical models (often called compact models) that do not directly model the underlying physics.For example, inversion-layer mobility modeling, or the modeling of mobility and its dependence on physical parameters,ambient and operating conditions is an important topic both for TCAD (technology computer aided design) physi-

cal models and for circuit-level compact models.However, it is not accurately modeled from first principles, and so resort is taken to fitting experimental data.For mobility modeling at the physical level the electrical variables are the various scattering mechanisms, carrier densities,and local potentials and fields, including their technology and ambient dependencies.Figure 9 shows how a model of a two-stage CMOS inverter has been constructed based upon the technologically controlled factors. By contrast,at the circuit-level, models parametrize the effects in terms of terminal voltages and empirical scattering parameters.The two representations can be compared,but it is unclear in many cases how the experimental data is to be interpreted in terms of more microscopic behavior.

3.3.13 Importance of device modelling and process simulation:

Rapid progress of IC technology in recent years has led to reduction of device dimensions and development of sophisticated process steps.With increase in complexity in fabrication of VLSI chips,need for device modelling and process simulation has become increasingly important.In device modelling, with the help of an appropriate model of a device, one can design a device of chosen specifications based on a set of device parameters.The performance of VLSI devices in turn are closely determined by process conditions.It is, therefore, necessary to understand,characterise and optimize the process steps involved in device fabrication.This can be achieved by simulation of each process through formulation of an accurate model of the basic physical mechanism involved.Once the models are developed and coded in a comprehensive computer program,the device and process parameters can be correctly predicted without going through the actual process and fabrication steps.

3.4 Device Description

A cross-section view of a GaAs MESFET is shown in Figure 10 below, which illustrates its basic structure. Three metal electrode contacts are shown to be formed onto a thin semiconductor active channel layer.Source and drain are ohmic contacts,while gate is a Schottky contact.The gate metal forms a Schottky barrier diode,which gives a depletion region between the source and the drain.The gate depletion region and the semi-insulating substrate form the boundary of the conducting channel.A potential applied to the drain causes electrons to flow from the source to the drain.Any potential applied on the gate causes a change in the shape of depletion region,and a subsequent

change in current flow.

For microwave operations, the most critical dimension is the "length" of the gate along the carrier path.The shorter the gate length, the higher becomes the signal frequency.If the FET is to handle a large amount of signal current, the gate width must be increased appropriately.

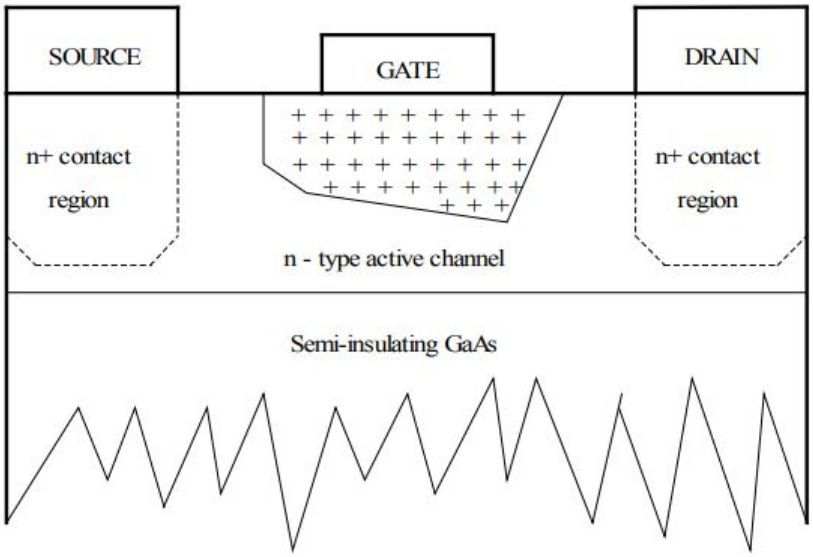


Figure 10: Cross-sectional view of a GaAs MESFET

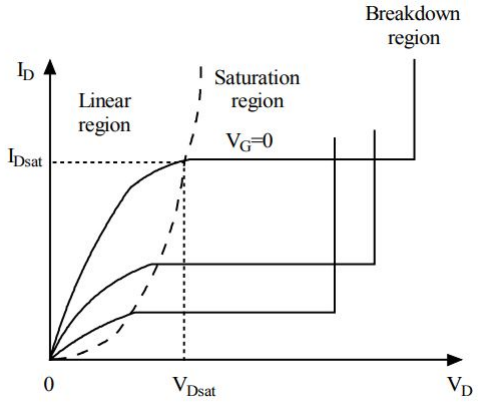


Figure 11: Basic current-voltage characteristics of a MESFET

The current-voltage relationships of a MESFET are illustrated in the figure 2.The channel current is plotted as a function of applied drain-source potential for different gate-source voltage levels. Three regions of operation can be identified from the figure 2.They are the linear region, the saturation region and the breakdown region.In the linear region, current flow is approximately linear with drain voltage. As drain potential increases, the depletion region at the drain end of the gate becomes larger than at the source end. Since the electrical field increases with the drain-source potential, a related increase in electron velocity occurs; this simultaneously makes a linear increasing current through the channel region.Increasing the drain voltage results in the electrons reaching their maximum limiting velocity at the drain end of the gate.At this point,the current no longer increases with increasing drain bias, the device is said to be saturated, and its operation enters saturation region. Finally, when gate and drain bias become very large, the device enters the breakdown region, where the drain current increases sharply.Basic current-voltage characteristics of a MESFET can be seen in figure 11.

The Schottky barrier of the gate contact creates a layer beneath the gate that is completely depleted of free charge carriers. No current can flow through this region since there are no free carriers exist in it. Moreover, the existence of the depletion layer reduces the available cross-section area for current flow between the source and drain. The depletion layer penetrates deeper into the active channel when reverse bias is applied to the gate. If the gate is made sufficiently negative, the depletion region will extend across the entire active channel and the conduction channel is closed. This essentially allows no current to flow. The gate potential to accomplish this phenomenon is known as the pinch-off voltage Vpinch-off. And at this point, the device operates in pinch-off region.

3.5 Physical Meaning of Small-Signal Equivalent Circuit Elements

The gure shows a commonly used MESFET small-signal equivalent circuit topology. This equivalent circuit has served as an accurate small-signal model for virtually all GaAs MESFETs [11]. It has been shown to provide an accurate match to measured S-parameters at least through 25GHz [12], and could be used at higher frequency by adding some parasitic elements in the equivalent circuit. This huge amount of S-parameter data of a single GaAs

MESFET can be reduced to a set of 15 frequency-independent variables as shown in this equivalent circuit. Basically, all these 15 unknowns can be divided into two parts:
(i) The intrinsic elements $g_m, g_{ds}, C_{gs}, C_{gd}$ includes, in fact, the drain-gate parasitic C_{ds}, R_i, tau, whose values are function of the bias conditions.

(ii)The extrinsic elements $L_g, C_{pg}, R_g, L_s, R_s, R_d, C_{pd}, and, L_d$
which are independent of the biasing conditions.

The same equivalent circuit is shown in Figure 12, superimposed on a GaAs MESFET device cross section, indicating the physical origin of each equivalent circuit element. From this figure, it is easy to recognize that each lumped element in the equivalent circuit of a GaAs MESFET is related with a corresponding physical part of the transistor.

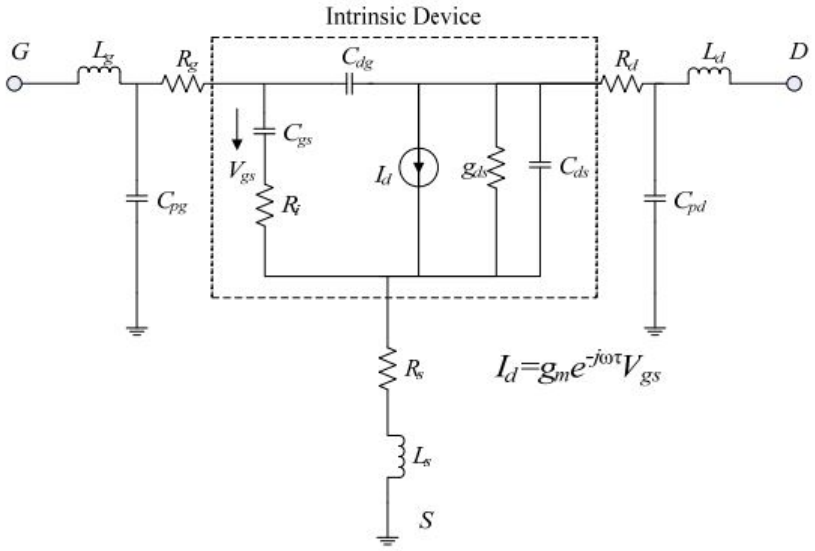


Figure 12: Small-signal Equivalent Circuit of a Field Effect Transistor

3.5.1 Parasitic Inductances $L_g, L_d,$ and L_s

These parasitic elements are introduced to account for the inductances arising from metal contact pads deposited on the device surface and bonding wires on the package.Parasitic inductances have an important impact on device performance especially at high frequency.They must be accurately

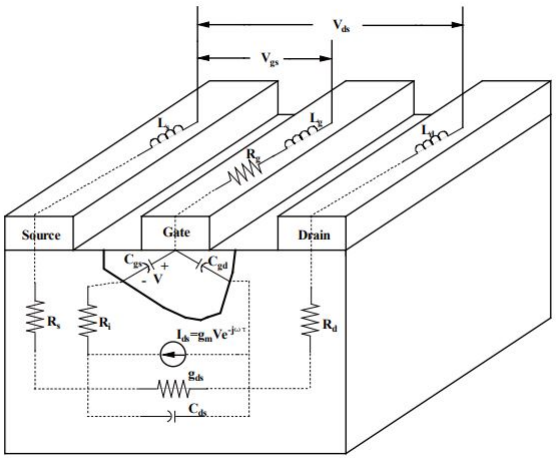


Figure 13: Physical origin of the GaAs MESFET small signal model

characterized. Among L_g, L_d,and, L_s,the inductance,L_g is usually the largest. The typical values of L_g and L_d are on the order of 10 to 100pH, source inductance L_s is often small, around 10pH for on wafer and chip devices.Bond wire and package will add additional parasitic inductances that in many cases dominate the device parasitics,and they must be accounted for in the circuit model.

3.5.2 Parasitic Resistances $R_s, R_d,$ and R_g

Gate resistance R_g physically arises from the metallization resistance of the gate Schottky contact. Resistances R_s ,and, R_d are introduced to represent the contact resistances of drain and source ohm contacts as well as any bulk resistance leading to the active channel.Investigation and measurements show a slight bias dependent behavior of these resistances. However, they are normally considered to be constant in commonly used large-signal models.

3.5.3 Parasitic Capacitances C_{pg}, C_{pd}

Parasitic capacitances arise primarily from metal contact deposited on the device surface and bonding wires on the package. Like parasitic inductances, parasitic capacitances are related to the device structure. For some devices on wafer, C_{pg} and C_{pd} could be ignored in the low frequency region without introducing significant error to the equivalent circuit due to their small values (on the order of 1pF).

3.5.4 Intrinsic Capacitances C_{gs}, C_{gd}, C_{ds}

The behavior of the depletion region beneath the gate of a MESFET is determined by the bias applied to the device terminals. The variation of the space charge region is caused by both gate-to-source potential and gate-to-drain potential. Gate charge Q_g is considered to be the space charge beneath the gate that varies with gate bias and drain bias.The gate-source capacitance C_{gs} is the derivative of the space charge with respect to the gate-source bias V_{gs}, when the gate-drain voltage is constant:
$\mathrm{C}_{gs} = \frac{\delta Q_g}{\delta V_{gs}}$
The gate-drain capacitance C_{gd} is the derivative of the space charge with respect to the gate-drain bias V_{gd}, when V_{gs} is constant:
$\mathrm{C}_{gd} = \frac{\delta Q_g}{\delta V_{gd}}$

3.5.5 Transconductance gm

Transconductance basically governs the current driving capability and is extremely important for estimating the microwave performance of the device
The incremental change in the output current Ids of a MESFET for a given change in input voltage V_{gs} is measured by the device transconductance g_m.Transconductance g_m provides the intrinsic gain mechanism of the device. Mathematically,it is defined as the derivative of drain current with respect to gate-source biasing voltage: $\mathrm{g}_m = \frac{\delta I_{ds}}{\delta V_{gs}}$

The value of transconductance shifts at low frequency, and the frequency at which this shift occurs varies. Both the gate length and the gate width of MESFET affect the transconductance values. The g_m value changes directly with gate width and inversely with gate length.

3.5.6 Charging Resistance R_i

R_i is the charging resistance.

3.5.7 Transconductance Delay τ

When gate biasing voltage changes, the drain current I_{ds} needs some time to respond to this change. The transconductance delay τ represents the inherent delay to this process.The physically meaning of the transconductance delay is the time it takes for the charge to redistribute itself after a changing in gate voltage.

3.6 Sub-threshold Effect

When a MESFET is biased near pinch-off, the physical phenomena that dominate device performance are different from those that govern device behavior under normal operating conditions. The threshold voltage is defined as the applied gate voltage under which the channel is completely depleted of free carriers. The classical depletion model is derived based on the abrupt depletion approximation. The model assumes that the expulsion of free carriers within the depletion region is total and that the substrate is a perfect insulator. In reality, however, the transition from depleted to neutral region takes place over a few Debye lengths due to the presence of mobile carriers at the depletion boundary. Consequently, when the gate-channel and channel-substrate depletion regions approach each other within this distance, the channel mobile carrier density will decline less rapidly than predicted by the abrupt depletion approximation. Using the abrupt depletion approximation leads to significant underestimation of the channel mobile carrier density, particularly in the sub- and near threshold regions. The noticeable effect of the sub-threshold region is the exponential dependence of the drain current on the gate bias.

3.7 HEMT Structure and Construction

The HEMT or High Electron Mobility Transistor is a form of Field Eect Transistor, that is used to provide very high levels o performance at microwave frequencies.The most imporatant element in HEMT is the specialised PN junction. The most common materials used to make a HEMT structure are: Aluminium Gallium Arsenide (AlGaAs) and Gallium Arsenide(GaAs). The usage of GaAs is due to its high level of basic electron mobility which is crucial to operation of the device.Silicon is never used in a HEMT as it has lower level of electron mobility.The basic operation of a HEMT is very much dierent than other types of FET as a result of which it is able to give a very much improved performance, particularly in microwave radio applications.

The HEMT is a heterojunction device with superior performance to its homojunction counterpart, the MESFET.However,a HEMT relies on the formation of a two dimensional electron gas at the heterojunction interface. A typical cross-sectional schematic of AlGaN/GaN HEMT device is shown in Figure 14.The device is usually grown on a semi-insulating substrate which has a high thermal stability and close lattice matching with GaN.A buffer layer is grown on top of the substrate to act as an isolation layer between the

substrate and channel.Any lattice mismatching or crystal defects from the substrate are minimised using this GaN buffer layer.The device usually uses a schottky gate contact and ohmic source and drain contact. The channel in a HEMT is formed at the heterojunction interface of the AlGaN barrier and GaN channel layer.The following section describes more about the operation of HEMT.

The manufacture of an HEMT as follows procedure,first an intrinsic layer of Gallium Arsenide is set down on the semi-insulating Gallium Arsenide layer.This is only about 1μ thick.After that,a very thin layer between 30 and 60 Angstroms of intrinsic Aluminium Gallium Arsenide is set down on top of this layer.The main purpose of this layer is to ensure the separation of the Hetero-junction interface from the doped Aluminium Gallium Arsenide region.

This is very critical if the high electron mobility is to be achieved. The doped layer of Aluminium Gallium Arsenide about 500 Angstroms thick is set down above this as shown in the diagrams below. The exact thickness of this layer is required and special techniques are required for the control of the thickness of this layer.

There are two main structures that are the self-aligned ion implanted structure and the recess gate structure. In self-aligned ion implanted structure the Gate, Drain and Source are set down and they are generally metallic contacts, although the source and drain contacts may sometimes be made from germanium. The gate is generally made of titanium, and it forms a minute reverse biased junction similar to that of the GaAs-FET. For the recess gate structure, another layer of n-type Gallium Arsenide is set down to enable the drain and source contacts to be made. Areas are etched as shown in the diagram below.

The thickness under the gate is also very critical since the threshold voltage of the FET is determined by the thickness only. The size of the gate, and hence the channel is very small. To maintain a high-frequency performance the size of the gate should be typically 0.25 microns or less.

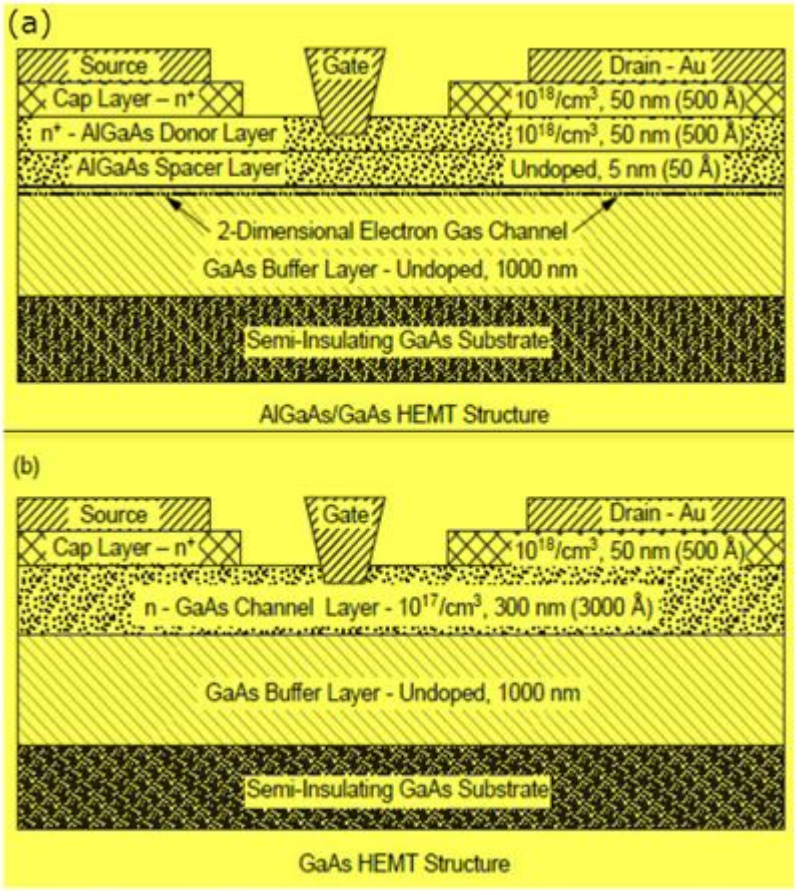


Figure 14: Cross-Sectional diagrams comparing structure of an AlGaAs or GaAs HEMT and a GaAs

3.8 HEMT Operation

In the most common HEMT structures, the wide bandgap barrier is doped n-type while the narrow bandgap channel remains undoped.As a result, electrons diffuse from the wide bandgap material into the narrow bandgap material to minimise their energy.This process continues until a balanced Fermi level is formed in the two materials and equilibrium is established. Because of the resulting electrostatics,a new triangular well forms on the narrow bandgap side of the heterojunction. Which we call it as two dimensional quantum well and the electrons confined inside the well is called Two Dimensional Electron Gas (2DEG).A schematic cross-section of HEMT has been

presented in figure 15.The n-doped barrier in the device supplies electrons to the undoped channel, thus spatially separating the channel charge carriers from their ionised donors.In this manner, the heterostructure channel is capable of delivering high carrier concentration with high mobility as impurity scattering is minimised in the undoped channel. As an added advantage, surface scattering is also reduced by moving the current-carrying region below the barrier. To understand the principle of operation and techniques,the formation of 2DEG and different effects involved in the HEMT are explained in the following sections.The HEMT or High Electron Mobility Transistor is a type of field effect transistor (FET),that is used to offer a combination of low noise figure and very high levels of performance at microwave frequencies.This is an important device for high speed, high frequency, digital circuits and microwave circuits with low noise applications.

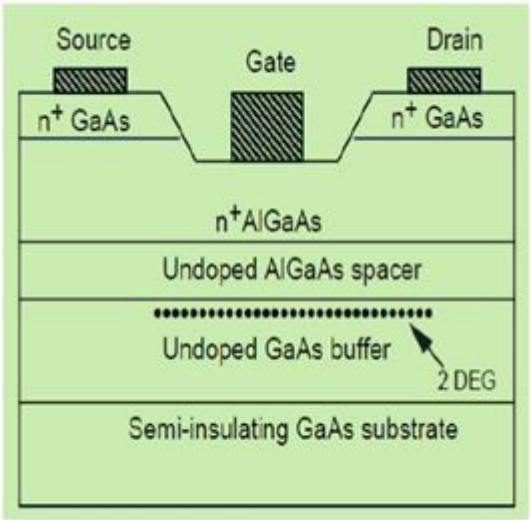


Figure 15: Schematic Cross section of an HEMT

3.8.1 Two Dimensional Electron Gas (2DEG) in HEMT

A two-dimensional electron gas (2DEG) is a scientific model in solid-state physics. It is an electron gas that is free to move in two dimensions, but

tightly confined in the third. This tight confinement leads to quantized energy levels for motion in the third direction, which can then be ignored for most problems.A schematic band diagram of a modulation doped heterostructure is shown in Figure 16. It consists of a wide gap semiconductor (AlGaN) and a semiconductor with narrower gap (GaN).At the interface a triangular quantum well is formed in the undoped narrow gap material. Electrons from the wider band gap material fall into this potential well and are confined within the well. Because of such quantum mechanical confinement in a very narrow dimension, they form a high density of electron gas in two dimensions. Electrons can move freely within the plane of the heterointerface, while the motion in the direction perpendicular to the heterointerface is restricted to a well-defined space region by energy, momentum, and wave function quantization, thus forms the so-called 2DEG. As the narrow gap material is undoped and these electrons are away from the interface, the electron mobility can be simultaneously increased with high concentration of carriers. Figure shows the polarization vectors in the AlGaN and underlying GaN. Within the AlGaN layer there are two polarization vectors Ppe, AlGaN and Psp, AlGaN for the piezoelectric and spontaneous polarizations respectively. The polarization in the AlGaN causes dipole charges to form at the borders of the material with a negative sheet charge at the surface and an equal positive sheet charge at the AlGaN/GaN junction. The polarization in the GaN layer causes a negative sheet charge at the AlGaN/GaN junction and an equal positive sheet charge on the bottom surface. Since the total polarization in the AlGaN is larger,the overall result is a net positive sheet charge at the AlGaN/GaN interface.Notice that the bottom GaN and AlGaN/GaN interfaces are both positive while the charge density at the top AlGaN interface is negative. The critical point to remember is that the interface sheet charges here are not free carriers. They are induced charges as in a typically polarised dielectric.However, it is the presence of these charges and the polarization induced electric field in the AlGaN which allows for 2DEG formation without barrier doping.

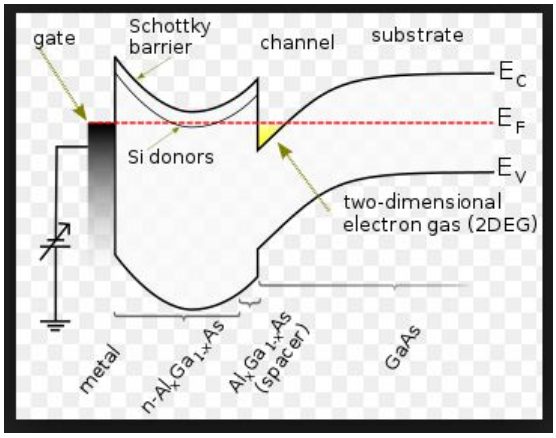


Figure 16: Band Diagram showing the 2DEG

3.8.2 Different types of Effects in HEMT

There are different effects present in the operation of HEMT devices such as Polarization effects and Trapping Effects. The following section describes more details about various effects in the HEMT devices.It is now widely recognized that built in electric fields due to polarization induced charges play an important role in the electrical and optical properties of Nitride heterostructures grown in [0001] orientation [13].These fields also provide a source of a 2-dimensional electron gas in AlGaN/GaN heterostructures.In HEMTs,the understanding and controlling of the source of electrons is important for the optimization of their performance.The polarization effect in HEMTs are well explained by [14].Spontaneous Polarization: Al-N and Ga-N bonds are highly ionic and each carries a strong dipole.For example, because the electronegativity of N is much higher than that of Ga,the electron wave function around the Ga-N pair is offset to the nitrogen side.The effect is even more exaggerated in the Al-N pair. This is a special feature of the III-nitrides as the degree of spontaneous polarization is more than five times greater than in most III-V semiconductors. Figure 9 shows GaN grown in the Ga-face and N-face orientation which is the norm for high performance AlGaN/GaN heterostructures.The c-axis polarization vector points from the nitrogen to the Gallium, as indicated, and creates an internal electric field pointing in the opposite direction,this is referred to as “spontaneous polarization”.In an AlGaN/GaN HEMT both the GaN and AlGaN layers have spontaneous polarization vectors which point in the same direction,from the N to the Ga(Al) towards the substrate (Figure 8). Piezoelectric Polarization: The lattice constants a0 and c0 for GaN are slightly larger than those for

AIN. As a result, thin AlGaN layers grown on GaN are tensile strained (the GaN is relaxed due to the thick buffer grown on the chosen substrate).In the nitride system the piezoelectric constants are more than ten times greater than those typical in most III-V semiconductors and this creates very large polarizations.In Ga-faced material under tensile strain the piezoelectric polarization due to the deformation of the AlGaN layer points parallel to the spontaneous polarization vectors.Trapping in Semiconductor Materials AlGaN/GaN HEMTs show strong current slump which is widely considered to be caused by electron trapping.Traps are very often surface related so it is not unreasonable to suppose they may contribute to current slump effects in AlGaN/GaN HEMTs.Aside from surface effects,traps may also be formed by dislocations, point defects or impurities.

3.8.2.1 Contacts in a HEMT:

Besides the electronic properties of the layer structure such as carrier mobility or conductivity of 2DEG, the metal contacts also determine the DC and RF properties of the final device.The quality of the contact is crucial to stable operation of transistor.Ohmic contact have to carry signal with minimal resistance and without rectification.On the other side Schottky contact have to dispone with high barrier height to AlGaN/GaN structure.

3.8.2.2 Ohmic Contacts:

The next type of contact present in the device is ohmic contact.In general, an ohmic contact is referred to a non injecting contact in which the current-voltage relationship under both reverse and forward-bias condition is linear and symmetrical.However,in reality,a contact is considered ohmic if the voltage drop across the metal semiconductor interface is negligible compared to the voltage drop across the bulk semiconductor.It is difficult to make ohmic contact to wide-gap semiconductor(e.g. III-group nitrides),because it does not generally exist in metal with low-enough work function to yield a low barrier.Therefore the practical way to obtain a low resistance ohmic contact is to increase the doping level near the metal-semiconductor interface to very high level.So in some cases a highly doped GaN layer is placed at the top of AlGaN/GaN heterostructure in effort to lower the barrier.Ohmic contacts allow current to pass into and out of the underlying semiconductor with ease.Formation of ohmic contacts with low resistivity is critical for optimal device performance.The cut-off frequency of a FET is strongly determined by the transconductance,g_m, of the device.

3.8.2.3 Schottky contacts in HEMT

Schottky contacts is one of the important building block for HEMT devices.The device formed using schottky contact may have great impact in the device performance.The critical elements at play for the Schottky contacts are diode idealities close to unity,low gate leakage current to allow for effective channel modulation,and small gate length to improve cut-off frequency.Ideally,fabrication of quality Schottky contacts on n-type material requires the use of metals with large work functions.Besides,the metalsemiconductor junction must be thermally stable and the gate metal must also be highly conductive to minimise the gate resistance.The energy barrier height is a key parameter of the junction,controlling both the width of depletion region in the semiconductor and the electron current across the interface.Barrier height is defined as the energy difference between the semiconductor conduction-band edge of the interface and the Fermi level in the metal.For undoped semiconductor the electrons cross through the barrier mainly by passing over the barrier, by thermionic emission.In the case of doped heterostructure, electrons also tunnel through the barrier at some elevated energies, by thermionic field emission.In the case of very high doping the depletion region is very thin and electrons tunnel through the barrier.The IV characteristic gets linear, when the resistance is low and the contact becomes ohmic. The value of barrier height depends on the difference between the electron affinities for the metal and the semiconductor.This is more or less only a theoretical case.In reality the deposition of metal to semiconductor gives a large number of interface states at the metal-semiconductor interface.High interface state density causes that Fermi level is pinned at certain level in the energy gap.Then the calculation of Schottky barrier requires detailed information on the distribution of interface states.The Schottky-barrier height is normally determined from experimental current voltage characteristics.Schottky Contact in HEMT Devices: High frequency RF device requires a perfect contact to work in close synchronisation with the high mobility 2DEG channel.A Schottky Source/Drain (SSD) HEMT reduces the leakage current and increases the on current of the device,the reduced leakage current simultaneously increases the breakdown voltage of the device.The Schottky Contact technology can be adopted to achieve a high improvement in the Offstate breakdown voltage of the lattice-matched In(0.17)-Al(0.83)N/GaN HEMT.The Schottky Source/Drain and Schottky-source (SS) AlGaN/GaN HEMTs are used.A Schottky-barrier normally off InAlN-based HEMT is another kind of HEMT device, which finds more application where high frequency is required.High Off-state breakdown, low gate leakage current and high frequency are the main advantage in these kind of

device.For the fabrication of the device 19 structure, Metal–Organic Chemical Vapor Deposition (MOCVD) is used.To create a negative polarization in the junction 1-nm InAlN/1-nm AlN barrier stack is capped with a 2-nm-thick undoped GaN.Negative polarization charge at the GaN/InAlN junction depletes the channel below the gate and reduces the gate leakage.After removing the GaN cap at access regions, electrons populate the channel.The relationship between Schottky gate leakage current and the breakdown voltage of AlGaN/GaN HEMT is based on the surface defect charge model.The leakage current caused by the positive charge in the surface portion of AlGaN layer induced by process damage such as nitrogen vacancies are represented in this model.To effectively suppress this surface charge influence,a field plated structure is effective.The gate leakage current increases with the defect charge due to thinning of the Schottky barrier and the field plated device structure reduces the electric field concentration at the gate edge.This will effectively increase the device breakdown voltage.To suppress the surface damage at the AlGaN layer,a low-damage fabrication process is most important point regarding development of the AlGaN/GaN-HEMT for the power electronics application due to low leakage current and high breakdown voltage.To further enhance the power performance of the device,the drain region design should be optimized.

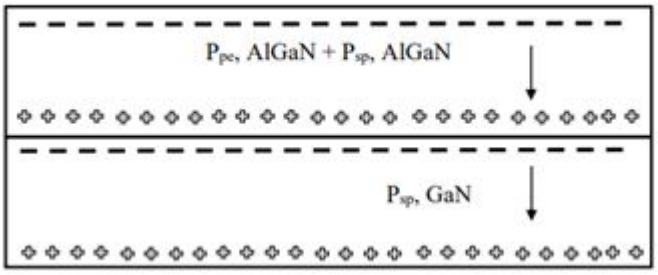


Figure 17: Spontaneous and piezoelectric polarization vectors in AlGaN and GaN

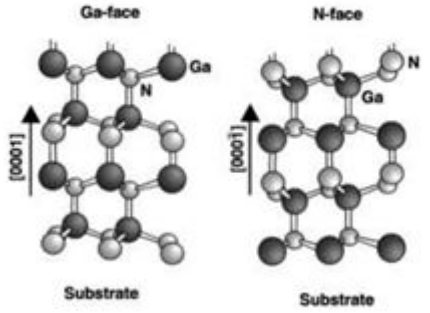


Figure 18: Ga-face and N-face GaN Structure

3.9 Gallium Nitride (GaN) Based High Power HEMT

HEMT was originally developed for high frequency RF application due to its outstanding performance in high frequency operation. The development of high quality GaN epitaxial films gave an extra mileage for the HEMT device in high power application. Nowadays it finds application where high frequency and high power are demanded, such as satellite communication and space applications.

GaN-on-SiC stands out in RF applications for several reasons:
(1)High breakdown field: Because of GaN's large bandgap, the GaN material has a high breakdown field, which allows the GaN device to operate at much higher voltages than other semiconductor devices. When subjected to high enough electric fields, the electrons in the semiconductor can acquire enough kinetic energy to break the chemical bond (a process called impact ionization or voltage breakdown). If impact ionization is not controlled, it can degrade the device. Because GaN devices can operate at higher voltages, they can be used in higher-power applications.
(2)High saturation velocity: Electrons on GaN have a high saturation velocity (the velocity of electrons at very high electric fields).When combined with the large charge capability, this means that GaN devices can deliver much higher current density.The RF power output is the product of the voltage and the current swings, so a higher voltage and current density can produce higher RF power in a practically sized transistor. Simply put, GaN devices can produce much higher power density.

(3)Outstanding thermal properties: GaN-on-SiC devices exhibit outstanding thermal properties, due largely to the high thermal conductivity of SiC. In practical terms, this means that GaN-on-SiC devices don't get as hot as GaAs or Si devices when dissipating the same power.A "colder" device means a more reliable device.

3.10 Device Characteristics

GaN devices exhibit certain characteristic features that need to be understood if a working model for the same is to be developed. It is essential to pay attention to the various nuances in measured characteristics that arise due to various physical phenomena.The DC, Microwave and breakdown characteristics of the HEMT are discussed analysed in detail in the coming sections.

3.10.1 Static characteristics

The static current characteristics of HEMT devices are obtained with the consideration of the self-heating effect on related parameters including polarization, electron mobility, saturation velocity, thermal conductivity, drain and source resistance, and conduction-band discontinuity at the interface between AlGaN and GaN.

3.10.2 Self-heating

The heat generation in the channel is caused by an energy transfer from the electron to the lattice, which is related to the inelastic phonon scattering processes of the electron.We can statistically calculate the local heat generation rate by counting the energy balance in the inelastic phonon scattering processes by employing the particle technique[17].

3.11 GaN ON SiC OR GaN ON Si

A PERFECT (MATERIAL) MATCH:
GaN and SiC are lattice-matched,meaning the lattice structures between the epitaxial layers allows a region of band gap change to be formed without changing the crystal structure of the SiC substrate material.This creates a lower defect density of the crystals,reducing leakage,improving reliability

and creating an overall superior product.In contrast,GaN on Si is a mismatched material system;the crystalline structure of Si doesn't align well with GaN.For GaN to grow on Si,a more complicated epi-structure is required to keep the wafer from warping,impacting time,cost and performance of the semiconductor.The crystal defect density determines how many good devices can be derived from the wafer.GaN on Si delivers fewer good devices than GaN on SiC because it has a higher defect density.GaN on SiC can operate at a higher electric field than GaN on Si,and because more good devices are derive the GaN on SiC chip can be about 20 percent smaller than those utilizing GaN on Si.

A MATTER OF EFFICIENCY:

While silicon has high resistivity at room temperature, wireless infrastructure generally operates hot.At high temperatures,silicon is conductive,and RF coupling to the substrate can occur.When it is cooled,the GaN will shrink more than the silicon substrate.With this,some RF power to the substrate is lost,decreasing efficiency.Because of its close match with GaN,GaN on SiC does not suffer from these same temperature change issues.In addition, the cost to grow the GaN epitaxy on silicon is more than the cost to grow GaN epitaxy on silicon carbide.This gives GaN on SiC significant efficiency and cost advantages over GaN on Si.

Understanding Total Life cycle Costs-In the end, for service providers building out networks to support the continuously increasing appetite for data,it is all about life cycle cost — kilowatt hours and the energy they are burning.

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Chapter 4

HEMT Equivalent Circuit parameter Extraction

4.1 Introduction

Heterojunction devices such as Heterojunction Bipolar Transistor (HBT) and HEMT are widely used in high frequency and high-power applications as they offer higher cut-off frequencies and large current driving capabilities [1].However, generalized models for HEMTs are still not part of most of the CAD tools considering that there are regular developments taking place in these devices.However, the accurate models of these devices are needed for analysis and investigation before utilization in high frequency circuit design.Heterojunction devices such as Heterojunction Bipolar Transistor(HBT) and HEMT are widely used in high frequency and high-power applications as they offer higher cut-off frequencies and large current driving capabilities [1].However,generalized models for HEMTs are still not part of most of the CAD tools considering that there are regular developments taking place in these devices.However, the accurate models of these devices are needed for analysis and investigation before utilization in high frequency circuit design.Heterojunction devices such as Heterojunction Bipolar Transistor (HBT) and HEMT are widely used in high frequency and high-power applications as they offer higher cut-off frequencies and large current driving capabilities [1].However,generalized models for HEMTs are still not part of most of the CAD tools considering that there are regular developments taking place in these devices.However,the accurate models of these devices are needed for analysis and investigation before utilization in high frequency circuit design.There have been multiple reports for the determination of the parameters of the small-signal model (SSM) of GaN HEMT [2] - [10].A small signal equivalent circuit model that considered the impact of coplanar wave guide effect capacitance was reported in [2] whereas a method that utilized biasing of the GaN HEMTs for the low value of the DC gate forward current

and floating drain for model parameter extraction was reported in [3].A 14 element GaN HEMT small signal model was established [4] for the parameter extraction under large forward gate voltage and zero drain-to-source voltage condition while a low biasing of gate model parameter extraction technique overcomes the effect of the gate forward bias [5].The technique reported in [6] identified the existence of a significant drain to source capacitance C_ds effect and proposed a suitable forward biasing condition for accurate parameter extraction.Time dependent output conductance G_{ds} was reported for the GaN HEMT equivalent circuit analysis which represented a time delay at the output and phase delay increment at the high frequencies [8].

Other approaches such as Artificial Neural Network (ANN) have been used for the SSM of the HEMTs.Extraction of multi bias model using ANN approach of GaN HEMTs including dependency on temperature is also proposed [9].Designing of first GaN HEMT power amplifier utilizing the technique of ANN modeling is also reported [10].
GaN high electron mobility transistors (HEMTs) are known as the promising devices for high-efficiency microwave power amplifiers [11–14].Accurate nonlinear transistor models are essential for the design of power amplifiers.Compared with physical-based model [15] and table-based model [16],the empirical large-signal equivalent circuit model is simpler and easier to be implemented in commercial simulators and has been widely used in circuit design [17].Basically, the generation of nonlinear empirical models requires nonlinear functions that account for the current flow (I–V functions) and the charge dynamic variation (Q–V or C–V functions).As for GaN HEMTs, I–V functions are much more complex than those of Si and GaAs devices [18].This is because the model must import more terms and parameters to account for the self heating and charge-trapping effects that GaN HEMTs encounter under working conditions.Thus, parameter extraction is a critical problem during the process of building nonlinear models. Angelov nonlinear model [18] has been widely used in GaN HEMT modeling [19–21].And extraction techniques have been widely exploited in the last decade. For example,some of the parameters in I–V models can be extracted straightforward from measured I–V curves by computing the slopes of specific regions [22].Some of the model parameters can be extracted by fitting the low frequency large-signal current waveforms and further numerical optimization [23].Low and high frequency large-signal measurements with numerical optimizations can also identify the parameters of the I–V and Q–V functions [24].
A structured method to extract these parameters is preferable than putting them into an optimizer and obtaining the values that may be contrary to their physical meaning.However, such organized methods or in other words,the fit-

ting details, are rarely mentioned in most published works.

In recent years, AlGaN/GaN high electron mobility transistors (HEMTs) technology has been applied widely and deeply because of its properties for high frequency and high power applications. Internationally,AlGaN/GaN monolithic microwave integrated circuit (MMIC) has entered a stage of application [11–27], whose products have reached a maximum operation frequency of W-band [26].A wideband and accurate small-signal model is the foundation of large-signal modeling in bottom-up method [27–32] and can also be used to build noise models [33–37], which makes small-signal modelling of great significance to the development and application of GaN MMIC.Many research works on GaN HEMTs modeling have been done in the past decade.Chigeava et al. established a GaN HEMT 14-element small-signal equivalent circuit model [4] by measuring 'cold field-effect transistor (FET)' S-parameters (Vds = 0 V) to extract parameters directly under a large gate voltage and zero drain voltage bias condition.

Crupi addressed the existence of a significant C_{ds} effect [6] in the parameter extraction process,and a suitable forward biasing condition that is high enough to suppress the channel resistance but low enough not to cause significant current flow through the gate terminal is used in the parameter extraction process.In order to avoid the gate-forward bias, Chen proposed a low gate bias model extraction technique [5]. Nonetheless, the procedure can only be applied to devices that the equivalent drain–source capacitance is negligible. Jarndal proposed a GaN HEMT 22-element small-signal equivalent circuit model [38],[39] in which genetic algorithm is used to optimize the parameters. Brady introduced a time dependency in the output conductance (g_{ds}) into the GaN HEMT equivalent-circuit topology [40] for the first time.It effectively represents a time delay at the output and accounts for the observed increase in phase delay at higher frequencies.Artificial neural network (ANN) approach has also been used for GaN HEMTs small-signal modeling. Lee et al. introduced the first GaN HEMT power-amplifier design using an ANN modeling technique [9].

The de-embedding technique [41] has been employed widely to extract intrinsic parameters by de-embedding the extrinsic parameters. However, there is an error accumulation problem in the de-embedding technique. If the extrinsic parameters are inaccurate, the errors will be taken into the process of extracting intrinsic parameters and even the calculation of optimization goal (i.e., the residual of S-parameters). Such an error accumulation problem will make the optimization algorithm difficult to reach the global minimum

or even get wrong elements' values. For millimetre-wave GaN HEMTs, a few extrinsic parameters (i.e., extrinsic capacitances) in small signal model are difficult to be extracted by direct measurement method.Typically, these parameters are set to be constant values, either by empirical estimation or rough calculation based on device's physical structure and further determined by optimization [42, 43].The low accuracy of the extrinsic parameters values that are empirically estimated or rough calculated will lead to the error accumulation problem.

In order to solve the error accumulation problem, this chapter proposed a highly efficient parameter extraction algorithm by a method of parameter scanning.The process gradually eliminates the impact of the extrinsic parameters' error on the extraction of intrinsic parameters. The algorithm has been implemented in MATLAB (R2013a) programming and validated by using a GaN HEMT 16 elements small-signal equivalent circuit model up to 40 GHz.The results show that the calculated S-parameters agree well with the measured S-parameters within the frequency range of 0.25 GHz to 40 GHz. This chapter includes the methodology adopted for carrying out the complete extraction procedure.

4.2 OVERVIEW OF SMALL SIGNAL MODELLING APPROACH

A small signal model derivation begins with defining an electrical equivalent circuit (EEC).There are various basic EEC given in reference section over the years [38][38].Having an accurate EEC depends on carefully studying the layout of the device taken into consideration along-with maintaining the aspects of device physics. The complexity of corresponding EEC increases with device layout, conductive substrate and underdeveloped device processing technology.In this work, small-signal model parameters of a FET are extracted using available S-parameter data under different bias conditions over a range of frequencies in conjugation with physical layout and geometry data.

4.3 Extrinsic Parameter Extraction Technique

The equivalent circuit and the origin of the components are known to us.Hence, our main focus is to use the methods through which the parameters can be extracted.We would begin with the capacitance extraction first.

4.3.1 Extraction Method of Pad Capacitances

The two kinds of most commonly used extraction methods for pad capacitances are

- **Open test structure method**
- **Pinch-off cold-FET method**.

Open Test Structure Method
In 1987[44] the standard "open" method was first proposed. In this technique the pad-substrate and the wire-substrate capacitance are calibrated by using an OPEN test structure. The layout of an OPEN test structure is same as the layout of the device-under-test (DUT) where only the transistor is removed. The pad capacitances are determined by measuring an open structure, with only the pads present.Figure 1 shows the open test structure layout with the corresponding equivalent circuit model.The simplicity of this model is that it has a semi-insulating GaAs substrate and there is proper device isolation done to this substrate.

In the above method,the test structures are drawn considering the dimension of the device.Source,drain gate part are all disjoint sets and hence the name is OPEN.The above mentioned method is very simple and easy but the main disadvantage is that separate OPEN structures are required for each device.Hence,the fabrication cost gets higher at each instance when a new device needs to be tested.This method is effective for insulating and semi-insulation substrate but not for the conducting one.
The Y parameter of the circuit can be written as shown in the following equations:

$$Y_{11} = jw(C_{pg} + C_{pgd}) \tag{1}$$

$$Y_{12} = Y_{21} = -jwC_{pgd} \tag{2}$$

$$Y_{22} = j\omega C_{pd} + j\omega C_{pgd} \tag{3}$$

$$C_{pgd} = -\frac{im(Y_{12})}{w} \tag{4}$$

$$C_{pg} = \frac{im(Y_{11}) + im(Y_{12})}{w} \tag{5}$$

$$C_{pd} = \frac{im(Y_{22}) + im(Y_{12})}{w} \tag{6}$$

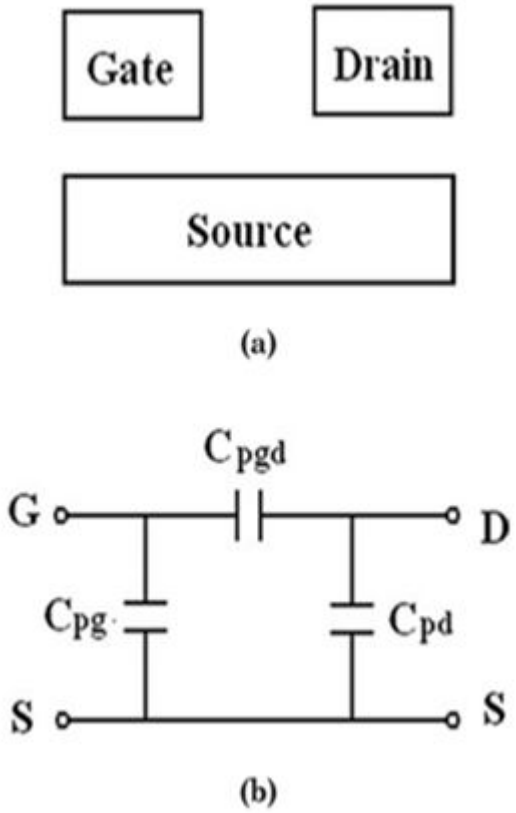

Figure 1: Open test structure (a) and equivalent circuit model (b)

Cold Pinch Off Method

The equivalent circuit of the COLD FET method has been shown in the figure below.

In this approach, the derived circuit equations are simplified by neglecting some terms depending on the frequency range (low and high frequencies) where the model parameters are extracted.The pinch-off cold-FET method has been widely used to extract the parasitic gate and drain capacitances C_{pg} and C_pd[45][46][41][10][47][48][49].An assumption made in this method is that the device is symmetrical with respect to the gate.Thus three identical capacitances are used to describe the pinch-off bias condition,C_{b1}=C_{b2}=C_b. The Y parameters of the equivalent circuit can be determined as follows:

$$Y_{11} = jw(C_{pg} + 2C_b) \tag{7}$$

$$Y_{12} = Y_{21} = -jwC_b \tag{8}$$

$$Y_{22} = j\omega C_{pd} + j\omega C_{ds} + j\omega C_b \tag{9}$$

The capacitance values can be calculated by using the following equations:

$$C_b = \frac{-im(Y_{12})}{w} \tag{10}$$

$$C_{pg} = \frac{im(Y_{11}) + 2im(Y_{12})}{w} \tag{11}$$

$$C_{pd} + C_{ds} = \frac{im(Y_{22}) + im(Y_{12})}{w} \tag{12}$$

If we assume that the pad capacitances are all equal in values, that is C_{pg}=C_{pd}, then the value of C_{ds} can be determined by the formula given below:

$$C_{ds} = \frac{im(Y_{22}) + im(Y_{12}) - im(Y_{11})}{w} \tag{13}$$

Modified COLD Pinch Off Method:

The assumption mentioned above is not always valid for the parasitic gate

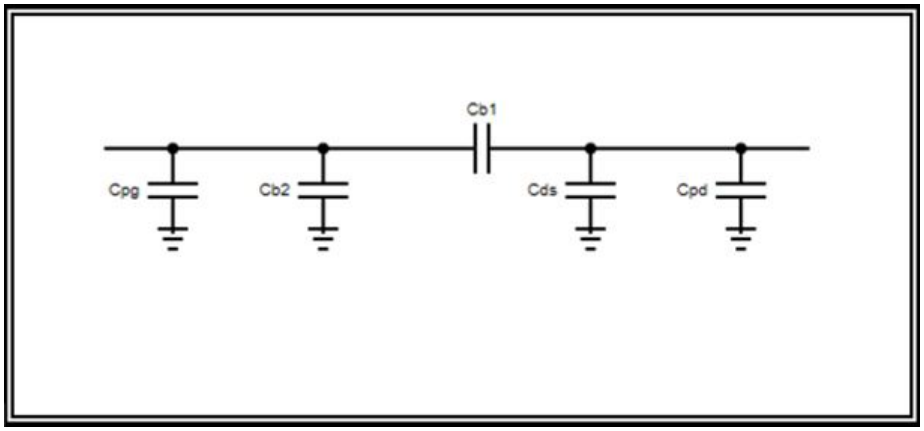

Figure 2: Cold FET Equivalent Circuit

and drain capacitances C_{pg} and C_{pd} of MESFETs and PHEMT, although their difference can be very small.In order to overcome these difficulties, a new pinch-off cold-FET method was proposed for the determination of the parasitic capacitance for PHEMTs which was based on a general equivalent circuit model [50]. In contrast with previous publications [45-49], this method has the following advantages:

- No restrictions or assumptions are imposed on the depletion-layer capacitances under pinch-off bias condition.Three different capacitances are used to describe the depletion-layer extension.
- No complex derivation and extraction procedures are needed.
- Four scalable PHEMT devices with same pad structures are employed to determine the parasitic capacitances.
- All parasitic capacitances C_{pg},C_{pd},and C_{pgd} can be extracted simultaneously.

The equivalent circuit model under pinch-off bias condition is shown in (Figure) below.
When we say the term "pinch-off bias condition" we define it as the condition when both junctions are zero or reverse biased. Under such a condition, the DC current is zero; hence gm would be extremely small and the device behaves like a passive circuit (Z_{12}=Z_{21}).At low frequency, the influence of the parasitic resistances and inductances can be neglected. The imaginary parts of Y-parameters can be written as:

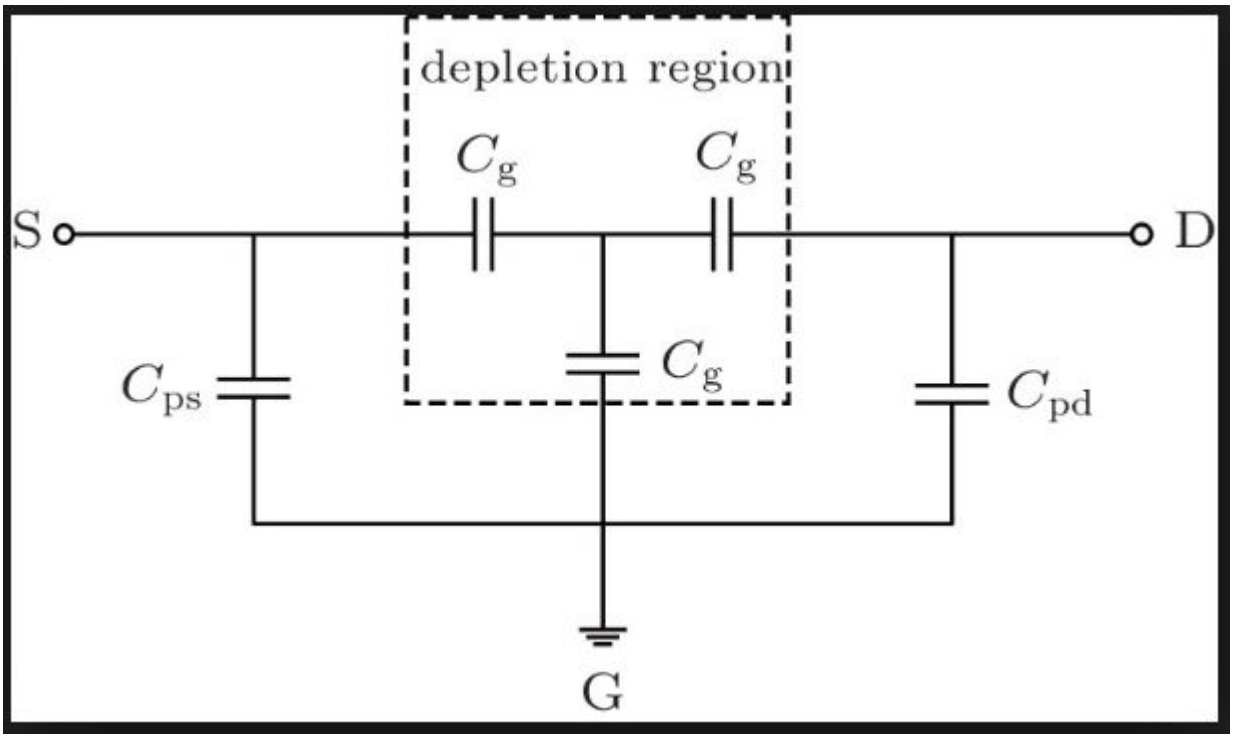

Figure 3: Depletion Layer capacitances

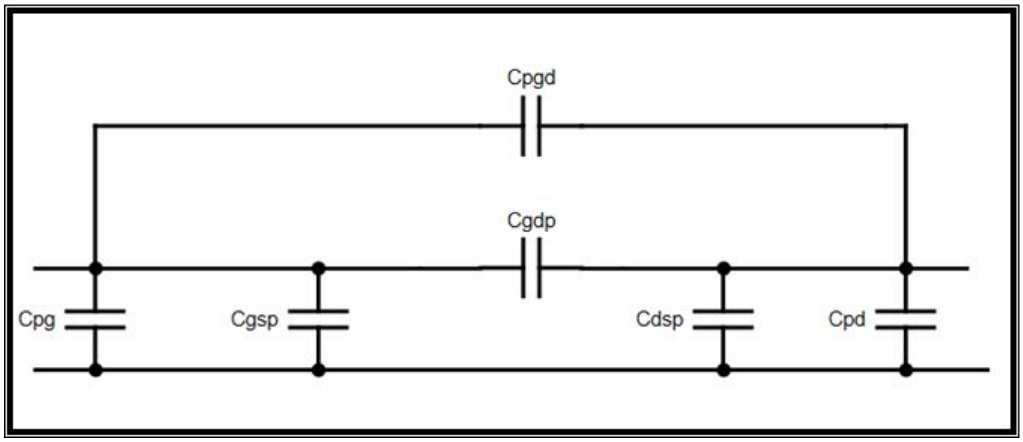

Figure 4: Modied Pinch O Equivalent Circuit

$$Y_{11} = jw(C_{pg} + C_{pgd} + C_{gsp} + C_{gdp}) \tag{14}$$

$$Y_{12} = Y_{21} = -jw(C_{pgd} + C_{dsp}) \tag{15}$$

$$Y_{22} = jw(C_{pd} + C_{dsp} + C_{gdp} + C_{pgd}) \tag{16}$$

The extrinsic capacitances in this case are C_{pg},C_{pd} and C_{pgd} and are going to be same for every type of model transistors but the intrinsic depletion capacitances would also vary.Now by using the scalable model of transistor, different capacitances can be calculated. The intrinsic capacitance value can be written as a function of width as shown below:

$$C_{gsp} = C_{gsp0}(W) \tag{17}$$

$$C_{dsp} = C_{dsp0}(W) \tag{18}$$

$$C_{gdp} = C_{gdp0}(W) \tag{19}$$

where C_{gsp0} and others are the depletion capacitance of the basic structure. That value is scaled with the transistor width to obtain the value of capacitance. Now the Y parameters in terms of scaled capacitances will be written as:

$$Y_{11} = jw[C_{pg} + C_{pgd} + W(C_{gsp0} + C_{gdp0}] \tag{20}$$

$$Y_{12} = Y_{21} = -jw[C_{pgd} + WC_{gdp0}] \tag{21}$$

$$Y_{22} = jw[C_{pd} + C_{pgd} + W(C_{dsp0} + C_{gdp0}] \tag{22}$$

The equation stated above looks like a straight line equation where the extrinsic part is the intercept and W is the slope of the line. Hence, plotting the magnitude Y_{ij}/w curve with respect to gate width ,the values of the capacitances C_{pg},C_{pd} and C_{pdg} can be obtained from the interceptions of the three linear regression lines versus the gate width. Therefore, the expressions for parasitic capacitance can be expressed as:

$$C_{pgd} = \frac{-im(Y_{12})}{w}|_{W\to 0} \tag{23}$$

$$C_{pg} = \frac{im(Y_{11}) + im(Y_{12})}{w}|_{W\to 0} \tag{24}$$

$$C_{pd} = \frac{im(Y_{22}) + im(Y_{12})}{w}|_{W\to 0} \tag{25}$$

and the values of the intrinsic capacitances can be calculated from the slope as:

$$C_{gdp} = \frac{d[\frac{im(Y_{12})}{w}]}{dW} \tag{26}$$

$$C_{gsp} = -\frac{d[\frac{im(Y_{11})}{w}]}{dW} - C_{gdp} \tag{27}$$

$$C_{dsp} = -\frac{d[\frac{im(Y_{22})}{w}]}{dW} - C_{gdp} \tag{28}$$

4.3.2 Extraction of Inductances Resistances

the feed lines between the device under test and the test pads causes the birth of the extrinsic inductances.There are three commonly used methods for determining extrinsic inductances: L_g, L_d and L_s:

- short test structure method
- cold-FET method

SHORT Test Structure Method:

In this particular method the circuit is modelled as a T-type network as shown in the figure.The operation of this method is similar to the OPEN structure method which was used to determine the extrinsic capacitance.Please find the figure below which shows the method structure of this process.

The Z parameters of this network can be written as:

$$Z_{11} = R_g + R_s + jw(L_g + L_s) \tag{29}$$

$$Z_{12} = Z_{21} = R_s + jwL_s \tag{30}$$

$$Z_{22} = R_d + R_s + jw(L_d + L_s) \tag{31}$$

$$L_s = \frac{im(Z_{12})}{w} \tag{32}$$

$$L_g = \frac{im(Z_{11}) - im(Z_{12})}{w} \tag{33}$$

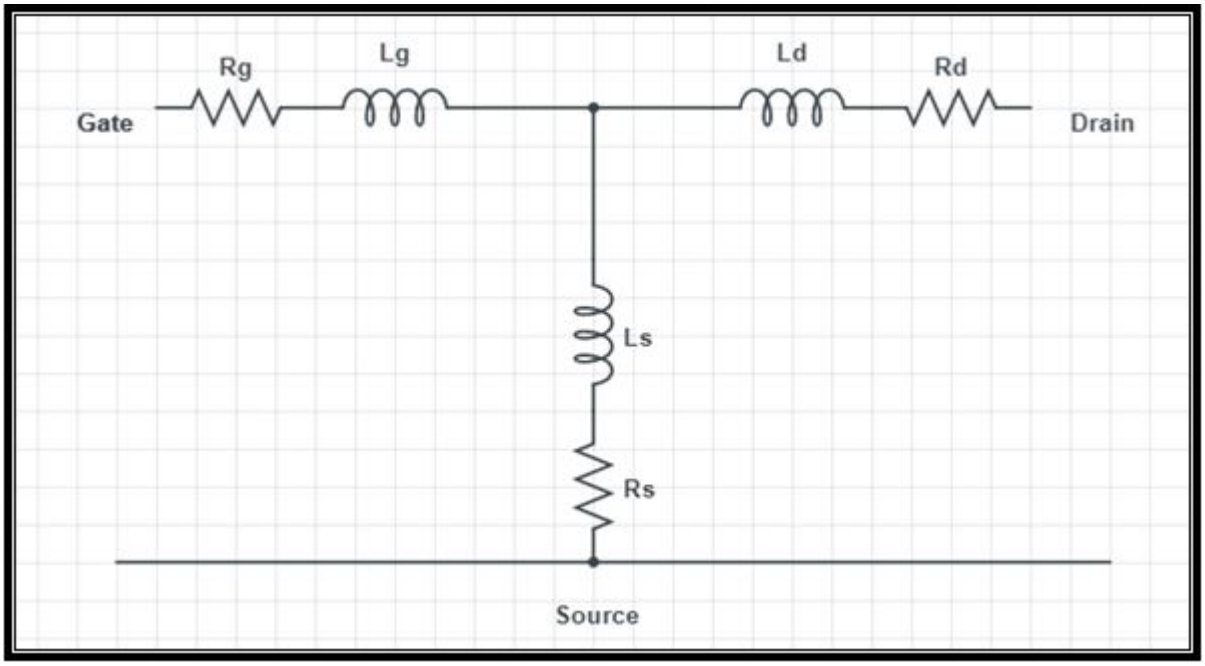

Figure 5: The equivalent circuit model of the Short test structure

$$L_d = \frac{im(Z_{22}) - im(Z_{12})}{w} \tag{34}$$

$$R_s = re(Z_{12}) \tag{35}$$

$$R_g = re(Z_{11} - Z_{12}) \tag{36}$$

$$R_d = re(Z_{22} - Z_{12}) \tag{37}$$

Forward -biased COLD FET Method:
In the cold-FET method the condition is applying a strong forward bias to the gate of FET, that is, when the gate-to-source voltage is larger than threshold voltage with zero drain to-source voltage [V_{gs} is greater than V_{th} V_{ds}=0] [47]. The device behaves like a passive component under this condition and we get to observe that: g_m=0, C_{gs}=C_{gd}=C_{ds}=0.
We have utilised the reverse-bias COLD FET condition to extract the extrinsic capacitance values.But here a strong forward bias is applied to the gate so that a high gate current flows through the device.The circuit will now consist of only inductive and resistive elements in it.The Z parameter equations which have been used to deduce are written as follows:

$$Z_{11} = R_g + R_s + R_{gs} + (R_{ch}/3) + jw(L_g + L_s) \tag{38}$$

$$Z_{12} = Z_{21} = R_s + (R_{ch}/2) + jwL_s \tag{39}$$

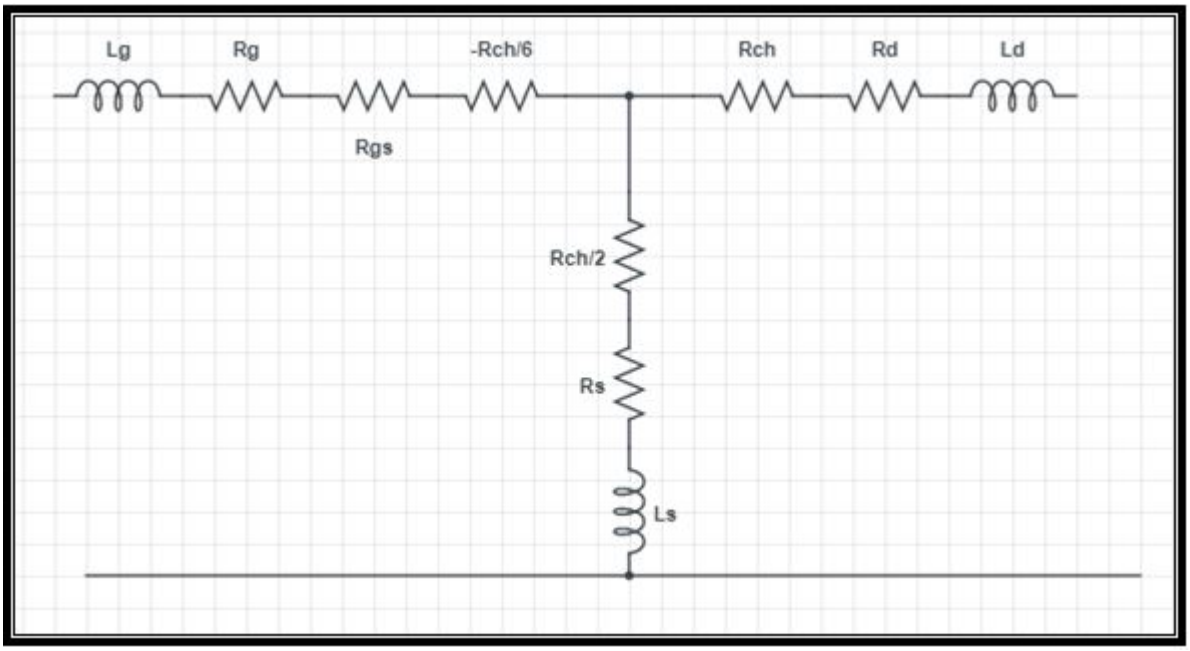

Figure 6: Forward Bias COLD FET Circuit

$$Z_{22} = R_d + R_s + 3(R_{ch}/2) + jw(L_d + L_s) \tag{40}$$

$$R_{schottky} = \frac{\eta kT}{qI_g} \tag{41}$$

$$R_s = re(Z_{12}) - (R_{ch}/2) \tag{42}$$

$$R_g = re(Z_{11}) - R_s - (R_{ch}/3) - R_{gs} \tag{43}$$

$$R_d = re(Z_{22}) - R_s - R_{ch} \tag{44}$$

4.4 De-embedding of the Extrinsic Parameters:

De-embedding of extrinsic parameters is the act of taking data that is measured during the extraction of the extrinsic parameters and removing the

effects of the extrinsic parameters so that the intrinsic data is accurate for our reference. As and when the extrinsic elements have been computed, this act of de-embedding becomes necessary to reach the internal terminals of the device. The de-embedding has been carried out in steps where at first the inductance L_g and L_d are subtracted.

Subtraction of the Extrinsic Elements:
Once the extrinsic elements are determined according to the previous sections, they can be removed from the measured S-parameters according to [51][52][53][10] resulting in the intrinsic Y-parameters. The obtained intrinsic Y-parameters are the basis for the further calculation of the intrinsic element values.

$$\mathrm{Z}_L = \begin{pmatrix} \mathrm{Z}_{11} - jwL_g & Z_{12} \\ Z_{21} & \mathrm{Z}_{22} - jwL_d \end{pmatrix} \quad (45)$$

The flow diagram for the de-embedding procedure and extraction of intrinsic Y-matrix has been adopted and shown in the figure 7 below.

The de-embedded Z-matrix is then converted into Y-matrix and the the capacitances C_{pg} and C_{pd} is de-embedded as:

$$\mathrm{Y}_C = \begin{pmatrix} \mathrm{Y}_{11} - jwC_{pg} & Y_{12} \\ Y_{21} & \mathrm{Y}_{22} - jwC_{pd} \end{pmatrix} \quad (46)$$

After this step the Z-parameter is obtained by converting the Y matrix to Z matrix.The extrinsic resistances R_g,R_d,R_s and R_ch and inductance L_s are subtracted and the de-embedding matrix that has been yielded is presented underneath:

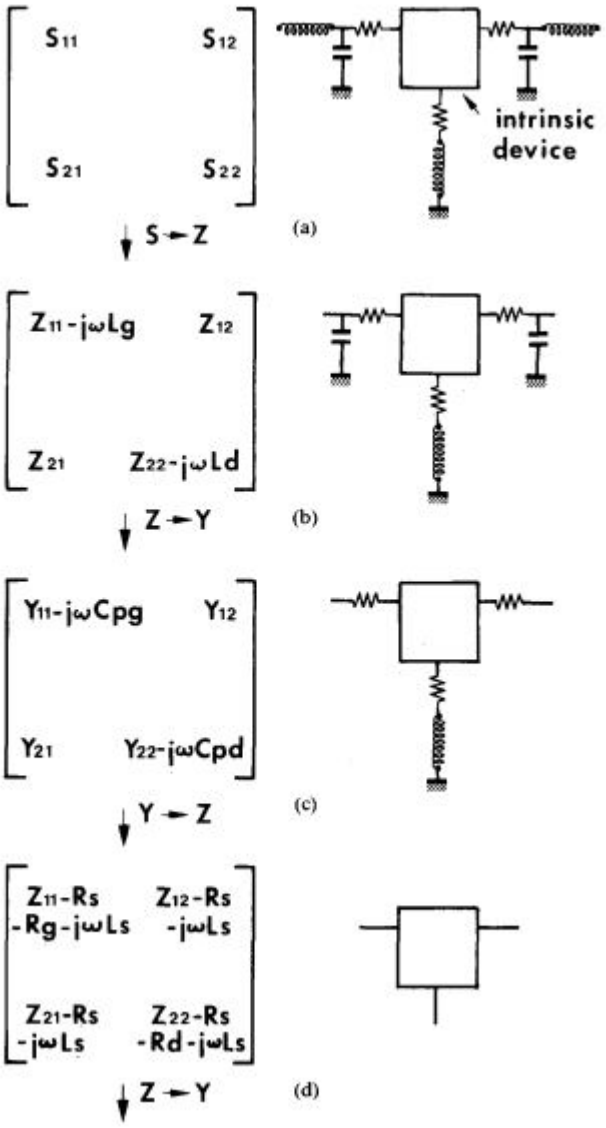

Figure 7: Method for extracting the device intrinsic Y matrix

$$Z_R = \begin{pmatrix} Z_{11} - R_g - R_s - jwL_s & Z_{12} - R_s - jwL_s \\ Z_{21} - R_s - jwL_s & Z_{22} - R_d - R_s - jwL_s \end{pmatrix} \quad (47)$$

4.5 Intrinsic Parameter Extraction:

Since the intrinsic device exhibits a PI topology, it is convenient to use the admittance (Y) parameters to characterize its electrical properties. The intrinsic part of device represented in the figure below,can be described by the following Y-parameters.

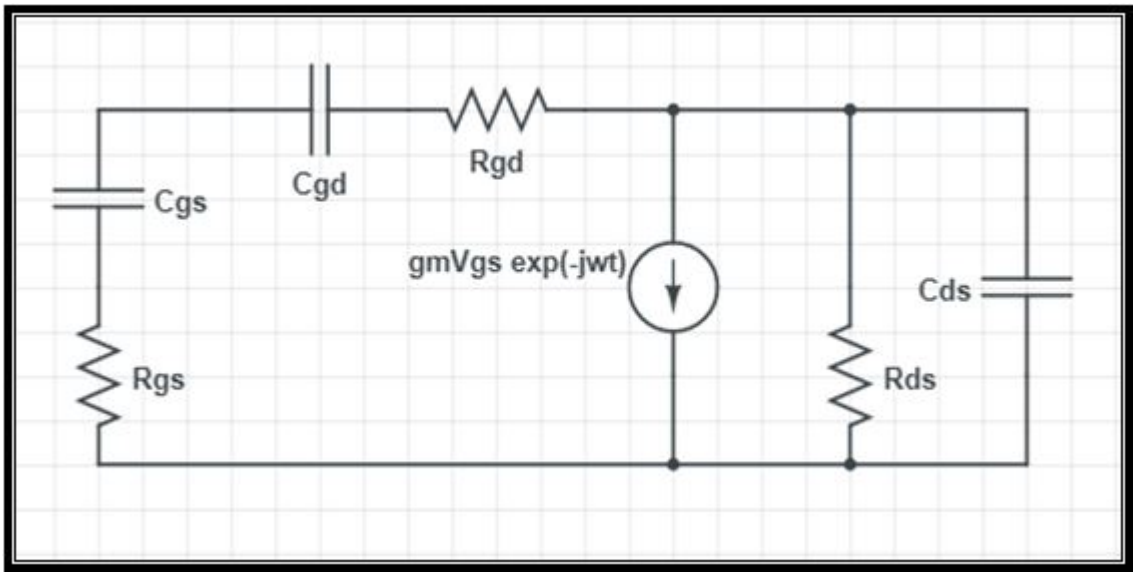

Figure 8: Intrinsic Device Equivalent Circuit

4.5.1 The Y-parameter expression for determining intrinsic elements:

Calculation of Y_{11}

Port 1 is short circuited to determine Y_{11} and Y_{21}. Since port 1 is short circuited, V_1=0. The figure shows the equivalent short circuit at port 1. $\mathrm{Y}_{11} = I1/V1, assuming \mathrm{V}_2$=0. From the figure we can clearly observe that, by applying KCL at node A,we get:

$\mathrm{i}_1 = i_a + i_b$

$\mathrm{i}_a = \left[\frac{V_1 j\omega C_{gs}}{1+R_i j\omega C_{gs}}\right]$

$\mathrm{i}_b = \left[\frac{V_1 j\omega C_{gd}}{R_{gd} j\omega C_{gd}+1}\right]$

Adding equations 1 and 2 we get,

$\mathrm{i}_1 = \left[\frac{V_1 j\omega C_{gs}}{R_1 j\omega C_{gs}+1}\right] + \left[\frac{V_1 j\omega C_{gd}}{R_{gd} j\omega C_{gd}+1}\right]$

$\mathrm{Y}_{11} = \left[\frac{R_i \omega^2 C_{gs}^2 + j\omega C_{gs}}{1+R_i^2 \omega^2 C_{gs}^2}\right] + j\omega C_{gd}$

Calculation of Y_{12}

$\mathrm{Y}_{12} = i_1/V_1, assuming, V_1 = 0$

$\mathrm{Y}_{12} = admittance of, C_{gd}$

$\mathrm{Y}_{12} = \frac{1}{j\omega C_{gd}}$

$\mathrm{Y}_{12} = -j\omega C_{gd}$

Calculation of Y_{21}

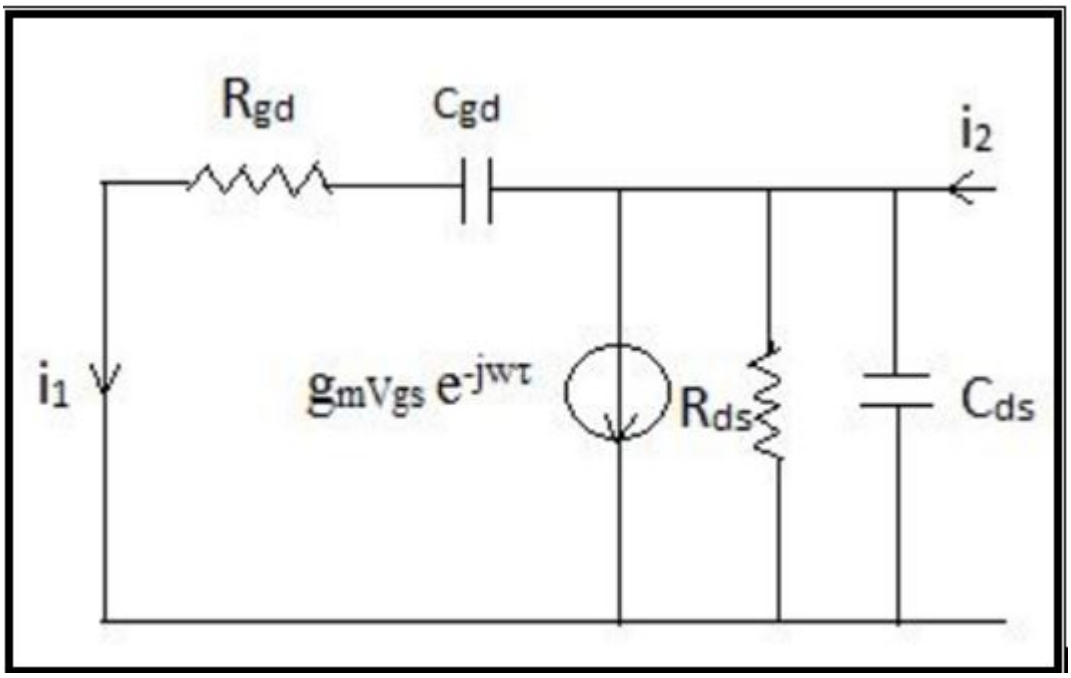

Figure 9: Equivalent circuit for short circuit at port 1

Applying KCL at node B we get $\mathrm{i}_b + i_2 = g_m V_{gs} e^{-j\omega\tau}$

$\mathrm{V}_1 = V_{gs} + R_i i_a$

$\mathrm{V}_g s = V_1 - R_i i_a$

$\mathrm{i}_b + i_2 = V_1 g_m e^{-j\omega\tau} - R_i i_a g_m e^{-j\omega\tau}$

$\mathrm{Y}_{21} =$
$\mathrm{R}_i j\omega C_{gs} + 1 - j\omega C_{gd}$

Calculation of Y_{22}

Port 2 is short circuited to determine Y_{12} and Y_{22}. Since port 2 is short circuited, V_2=0. The figure shows the equivalent short circuit at port 2.

$\mathrm{Y}_{22} = I2/V2, assuming V_1 = 0$

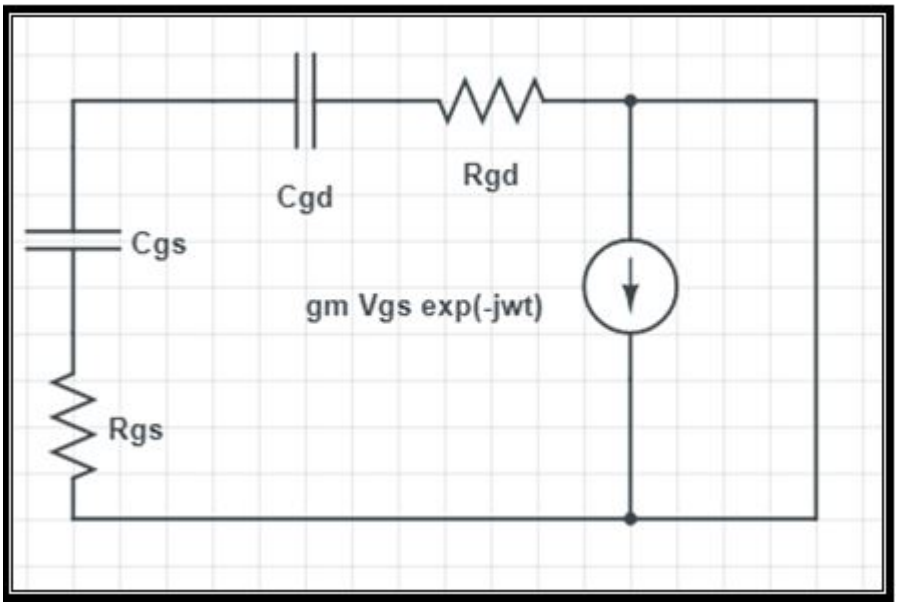

Figure 10: Equivalent circuit for short circuit at port 2

We know that
$Y_{22} + Y_{12} = admittance, between, g_d, and, C_{ds}$
$Y_{22} + Y_{12} = \left[\frac{R_{gd}j\omega C_{ds}+1}{R_{gd}}\right]$

$$Y_{22} = \left[\frac{R_{gd}j\omega C_{ds}+1}{R_{gd}}\right] + j\omega C_{gd}$$

$$Y_{22} = j\omega C_{ds} + j\omega C_{gd} + R_{gd}$$

Now the Y parameters are computed using the equations given below:

$$Y_{11} = \left[\frac{R_i\omega^2 C_{gs}^2 + j\omega C_{gs}}{1 + R_i^2\omega^2 C_{gs}^2}\right] + j\omega C_{gd} \tag{48}$$

$$Y_{12} = -jw(C_{gd}) \tag{49}$$

$$Y_{21} = \left[\frac{g_m e^{-j\omega\tau}}{R_i j\omega C_{gs} + 1}\right] - j\omega C_{gd} \tag{50}$$

$$Y_{22} = j\omega C_{ds} + j\omega C_{gd} + R_{gd} \tag{51}$$

Based on these Y-parameter values, the intrinsic device elements are calculated. For this purpose the equations given below have been used:

$$d(w) = \frac{re(Y_{11}(w) + Y_{12}(w))}{im(Y_{11}(w) + Y_{12}(w))} \tag{52}$$

$$c(w) = (Y_{12}(w) - Y_{21}(w))(1 + jwd(w)) \tag{53}$$

$$C_{gs} = \frac{1 + d^2(w)}{w} im(Y_{11}(w) + Y_{12}(w)) \tag{54}$$

$$R_i = \frac{d^2(w)}{(1 + d^2(w))(re(Y_{11}(w_i) + Y_{12}(w_i))} \tag{55}$$

$$C_{gd} = -\frac{im(Y_{12}(w_i))}{(w_i)} \tag{56}$$

$$g_m(w) = \sqrt{C^2(w)} \tag{57}$$

$$\tau(w) = \frac{-1}{w} arctan(im(c_w)), re(c(w)) \tag{58}$$

$$g_{ds} = re(Y_{22}(w) + Y_{12}(w)) \tag{59}$$

$$C_{ds} = \frac{im(Y_{22}(w) + Y_{12}(w))}{w} \tag{60}$$

4.5.2 Alternative approach for determining the intrinsic Y parameters:

The steps that should be followed for the determination of the intrinsic parameters in this alternative approach are described herein:

STEP 1:
Calculation of the impedance of each branch

$$Y_{gs} = \frac{jwC_{gs}}{1 + jwC_{gs}R_{gs}} = \frac{w^2{C_{gs}}^2 R_{gs}}{1 + w^2 C_{gs}^2 R_{gs}^2} + \frac{jwC_{gs}}{w^2 C_{gs}^2 R_{gs}} \tag{61}$$

$$Y_{ds} = G_d + jwC_{ds} \tag{62}$$

$$Y_{gd} = \frac{jwC_{gd}}{1 + jwC_{gd}R_{gd}} = \frac{w^2{C_{gd}}^2 R_{gd}}{1 + w^2 C_{gd}^2 R_{gd}^2} + \frac{jwC_{gd}}{w^2 C_{gd}^2 R_{gd}} \tag{63}$$

$$Y_{am} = \frac{g_m e^{-j\omega\tau}}{R_{gs} j\omega C_{gs} + 1} \tag{64}$$

STEP 2:
Representation of the impedance of each of the branches of the circuit in terms of the terminal parameters

$$Y_{gs} = Y_{11} + Y_{12} \tag{65}$$

$$Y_{gd} = -Y12 \tag{66}$$

$$Y_{am} = Y_{21} - Y_{12} \tag{67}$$

$$Y_{ds} = Y_{22} + Y_{12} \tag{68}$$

STEP 3:
Computation of the values of the intrinsic device elements.

$$C_{gs} = \frac{im(Y_{gs})}{w}(1 + [\frac{re(Y_{gs})}{im(Y_{gs})}]^2) \tag{69}$$

$$C_{gd} = \frac{im(Y_{gd})}{w}(1 + [\frac{re(Y_{gd})}{im(Y_{gd})}]^2) \tag{70}$$

$$R_{gs} = \frac{re(Y_{gs})}{(re(Y_{gs}))^2 + (im(Y_{gs}))^2} \tag{71}$$

$$R_{gd} = \frac{re(Y_{gd})}{(re(Y_{gd}))^2 + (im(Y_{gd}))^2} \tag{72}$$

$$g_m = sign(V_{ds})|Y_{am}[1 + j\frac{re(Y_{gs})}{im(Y_{gs})}]| \tag{73}$$

$$\tau = -\frac{phase(Y_{am}[1 + j\frac{re(Y_{gs})}{im(Y_{gs})}])}{w} \tag{74}$$

$$C_{ds} = \frac{im(Y_{ds})}{w} \tag{75}$$

$$R_{gd} = re(Y_{ds}) \tag{76}$$

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Chapter 5

Experimental Results and Discussions

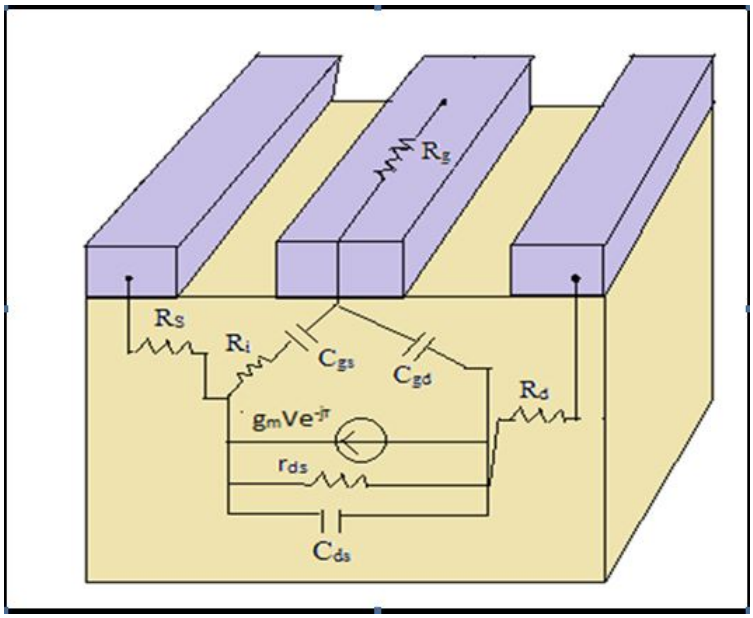

Figure 1: A 3D representation of HEMT

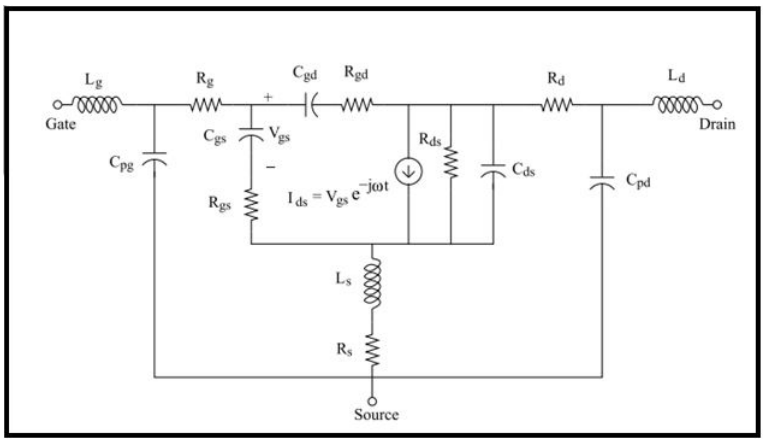

Figure 2: Equivalent circuit of HEMT

In Chapter 4 we have seen that the parameters were extracted using a definite algorithm. In this chapter the results have been displayed. The validity of this procedure is also verified by checking the frequency independence of the extrinsic elements as well as the intrinsic elements which is shown in Chapter 5. A 3-D representation of the HEMT structure has been displayed in Figure 1 and the corresponding equivalent circuit has also been shown in Figure 2.

5.1 EXPERIMENTAL RESULTS

Determination of the elements of a linear model is based on an experimental characterization of the transistor. A precise extrinsic equivalent circuit is desirable in order to obtain a physically representative intrinsic SSEC since errors in the extrinsic network flow into the intrinsic element values, potentially leading to misinterpretations of physical phenomena.

5.1.1 EXTRINSIC ELEMENTS:

Extrinsic capacitances:

Firstly, the extrinsic essential components are extracted from two group of S-parameter measured under 'cold' condition ($V_{ds} = 0$). The parasitic capacitances are determined from Y-parameters at the 'pinched cold' condition (V_{ds}= 0 and V_{gs} is less than V_{th}). The equivalent circuit can be reduced to figure 3 shown below in low frequency range.

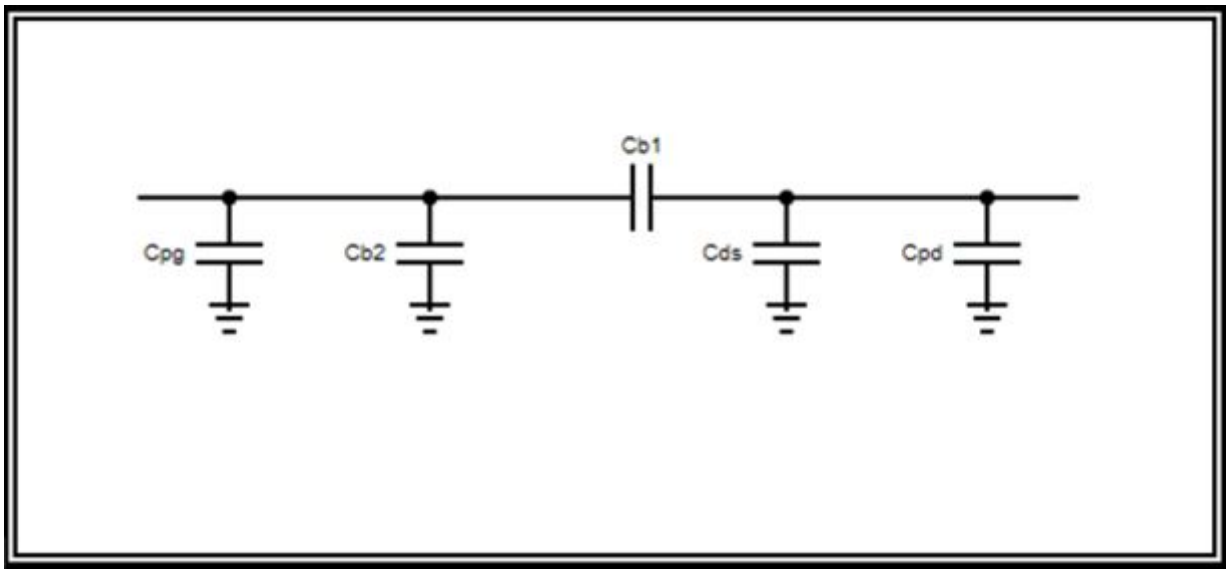

Figure 3: Cold FET Equivalent Circuit

The imaginary parts of Y-parameters were expressed in Chapter 4 (equations (7), (8) and (9).The total capacitances of gate-source, gate-drain, and drain-source branches can be derived from the slopes of Im(Y_{11}), Im(Y_{12}) and Im(Y_{22}) versus frequency curves. Depending on the equivalent circuit , the gate and drain parasitic capacitances, C_{pg} and C_{pd}, can be estimated from cold pinch-off S-parameters data. The inductances can be neglected at low frequencies and the simplified expressions can be deduced using T to converted equivalent circuit.

Plot of the Imaginary part of Y-parameters versus frequency:

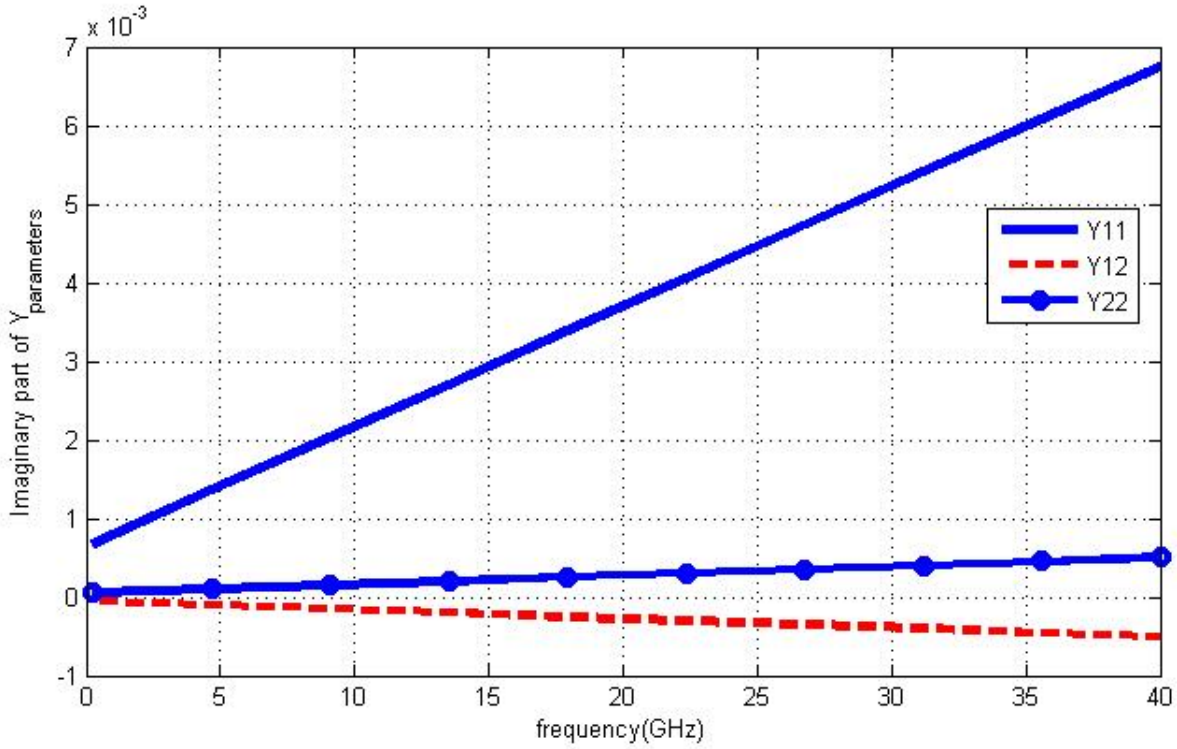

Figure 4: Plot of the Imaginary part of Y-parameters versus frequency

The equivalent circuit shown in Figure 3 is observed to give better parasitic capacitances for FETs having gate and drain bond pads similar in shape and size. This has been observed for this GaN on SiC HEMT (figure 3) where its parasitic capacitance is dominated by the bond pads and $\mathrm{Im}(Y_{11}) = \mathrm{Im}(Y_{22})$.

This significant contribution is mainly due to the dimensions of the gate and drain electrode and their distance to the source air-bridge interconnect. $\mathrm{Im}(Y_{22})$is almost similar but with small increment due to same reason.

Next, we need to separate each extrinsic capacitance. This is done by following the equations (10)-(13) of Chapter 4. So far, all extrinsic capacitances are obtained respectively.

Experimental results showing the variation of the extrinsic capacitances versus frequency

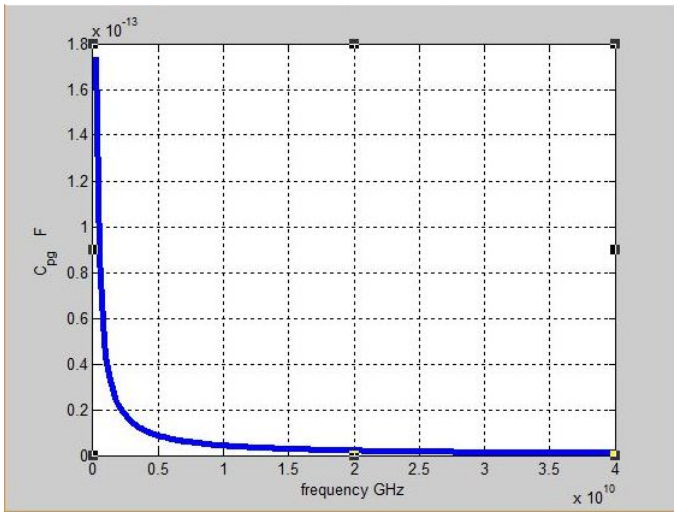

Figure 5: Plot of the extrinsic capacitance C_{pg} versus frequency

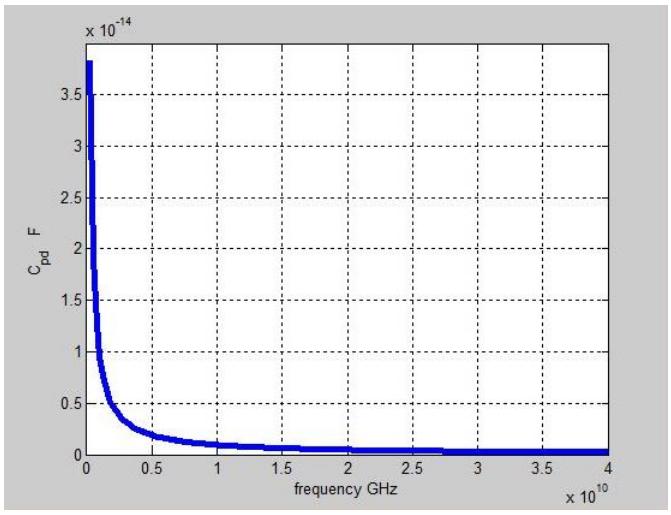

Figure 6: Plot of the extrinsic capacitance C_{pd} versus frequency

From the slope of the $\mathrm{Im}(Y_{11})$, $\mathrm{Im}(Y_{12})$ and $\mathrm{Im}(Y_{22})$ versus plots in Fig. 4, the values for C_{pg} and C_{pd} are 52.656 fF and 26.3391 fF respectively for the GaN-on-SiC HEMT.

Extrinsic Inductances and resistances :

Traditionally, S-parameters measured under gate-forward condition of the cold-FET were used to determine parasitic resistances and inductances. The Schottky barrier under the gate is modelled by distributed R-C network. But this old procedure cannot be directly used for HEMTs. Because first, the gate-to-channel contact for HEMTs is not only Schottky barrier as in MESFETs but a Schottky contact in series with a heterojunction and second, the high gate forward bias is not a typical operating condition of a FET and such measurement may also damage the device. This procedure may also result in overestimated source and drain resistances. Secondly, we ascertain parasitic inductances and resistances from measurement under unbiased cold condition ($V_{ds} = 0$ and $V_{gs} = 0$). The equivalent circuit can be reduced to figure 6 in high frequency, when $V_{ds} = 0$ and $V_{gs} = 0$.

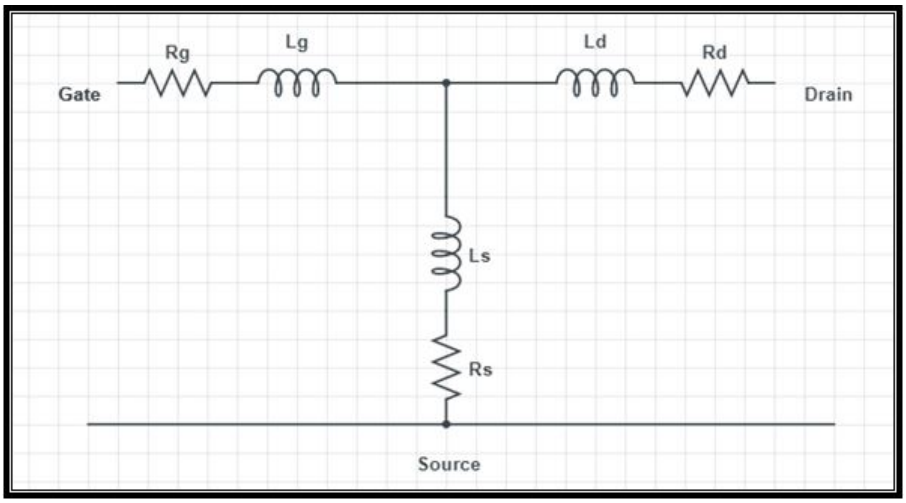

Figure 7: Forward Bias COLD FET Circuit

R_{ch} represents the channel resistance under the gate. The Z-parameters in figure 3 can be written as displayed in equations (38-40) in Chapter 4. The values of L_g, L_d, and L_s can be extracted according to these equations too. The results obtained have been plotted against the frequency axis to procure the validity of the results.

Experimental results showing the variation of the extrinsic resistances versus frequency

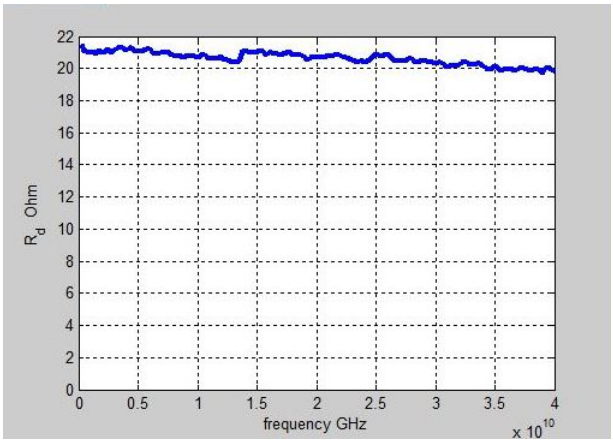

Figure 8: Plot of the extrinsic resistance R_d versus frequency

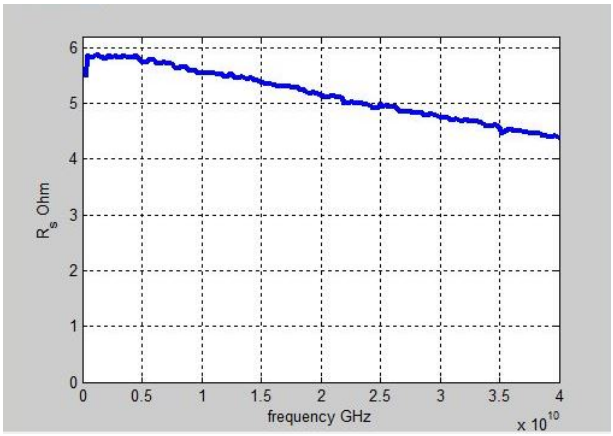

Figure 9: Plot of the extrinsic resistance R_s versus frequency

Now we consider the real parts of the branch impedances of the above equation set and the plots in figures above. One notes that R_g can be obtained from the horizontal asymptote of $\mathrm{Re}(R_g)$ plot where r_g/D becomes negligible. The resistance $R_s + R_c/2$ and $R_d + R_c/2$ are also identified from $\mathrm{Re}(Z_s)$ and $\mathrm{Re}(R_d)$ plots, respectively. And then we calculated R_s , R_d and R_g in that order. The extrinsic resistive parameters determined are summarized herein:

- R_s=5.1596 ohm
- R_d=20.6316 ohm
- R_d=2.4471 ohm

It is interpreted that,R_d is higher than R_s, which is justified by the fact that that drain-gate length of the device is few times greater than the gate-source length.

Using the small signal extraction technique, the bias independent small signal parameters for the device were extracted at a chosen operating frequency of up to 40 GHz.

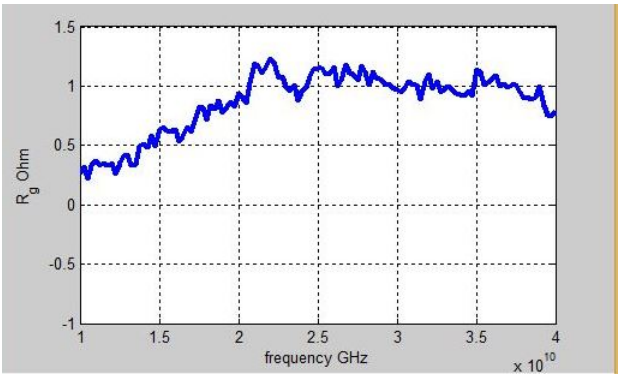

Figure 10: Plot of the extrinsic resistance R_g versus frequency

The parasitic device-connection impedances can be determined by measuring a test pattern, which consists of the pads, the device feeds, and a short replacing the transistor (shown in Chapter 4). The short test structure is modelled as a T network of series resistors and inductors. Chapter 4 shows the shorted test structure and corresponding equivalent circuit model. The extrinsic inductances can be directly determination from Z parameters of the short test structure using the equations from (32) to (34).

Experimental results showing the variation of the extrinsic inductances versus frequency

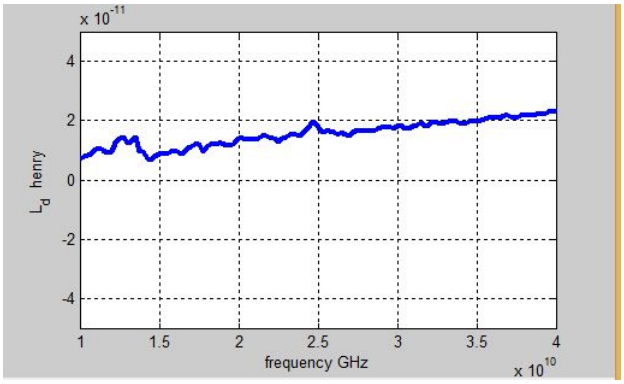

Figure 11: Plot of the extrinsic inductance L_d versus frequency

It can be found that the feed line losses are very small (less than 1 ohm normally), therefore can be neglected compared with the contact resistances.
The conventional cold-FET method is defined as the condition when applying a strong forward bias to the gate of FET, that is, when the gate-to-source voltage is larger than threshold voltage with zero drain-to-source voltage [V_{gs} greater than V_{th},V_{ds}=0]. Under such conditions, the device behaves like a passive component and has gm =0 and C_{gs}=C_{gd}=C_{ds}=0. The equivalent circuit thus becomes much more simpler to deal with. The values of the extrinsic inductances are:

- L_s =9 pH
- L_d =15.535 pH
- L_g =5.024 pH

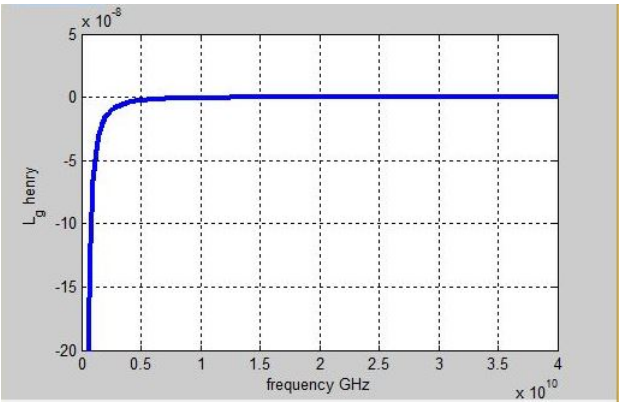

Figure 12: Plot of the extrinsic inductance L_g versus frequency

5.1.2 INTRINSIC ELEMENTS:

After calculating the extrinsic parameter values, their effects are subtracted from S-parameters measurements at each bias point of interest, to obtain the Y-parameters matrix of the intrinsic transistor. This process is known as de-embedding and has been well elaborated in the previous chapter. After de-embedding the extrinsic parameters obtained above, we can get the intrinsic Y parameters, from which the bias-dependent intrinsic parameters can be extracted.

Once the extrinsic elements are determined according to the previous sections, they can be removed from the measured S-parameters according to (64) – (67) resulting in the intrinsic Y-parameters. Figure 7 of Chapter 4 shows the entire diagrammatic flow of the procedure undertaken. The equations (45)-(47) of chapter 4 are used for reference. The experimental results obtained during the extraction procedure have been displayed herein.

The intrinsic parameters C_{gd} and C_{gs} appears as a parallel-plat capacitance whose two plates are formed by the gate metal and the 2 DEG channel charge. It can also observed from the following curves, that with $V_{DS} = 0$V and V_{GS} increasing from pinch-off towards 0 V, C_{gs} increase to a maximum value, which occurs around the V_{GS} value that corresponds to the maximum transconductance g_m.

It can also observed that with $V_{DS} = 0$ V and V_{GS} increasing from pinch-off towards 0 V, C_{gs} increase to a maximum value, which occurs around the V_{GS} value that corresponds to the maximum transconductance g_m. After that maximum point, C_{gs} will show again a notable decrease.

With a fixed V_{GS}, rising V_{DS} from 0 V presents positive charges in the drain that prevent the capacitive effects of the gate-drain region, leaving the gate-source region unaffected. Thus, effects denoted by C_{gs} remain roughly constant. But it can be noted that gradual increase for C_{gs} with increasing the drain voltage is observed around the grounded gate voltage ($V_{GS} = 0$ V).

This reduction is due to decrement in depletion layer depth and it is because of the lateral electric field established by the drain voltage, accelerates charge carriers in the channel to scat-

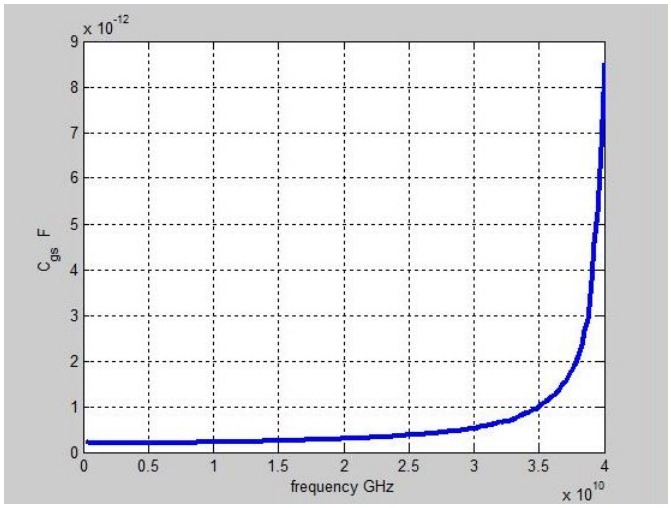

Figure 13: Plot of the intrinsic capacitance C_{gs} versus frequency

ter into the barrier layers and reduces effective amount of available carriers.

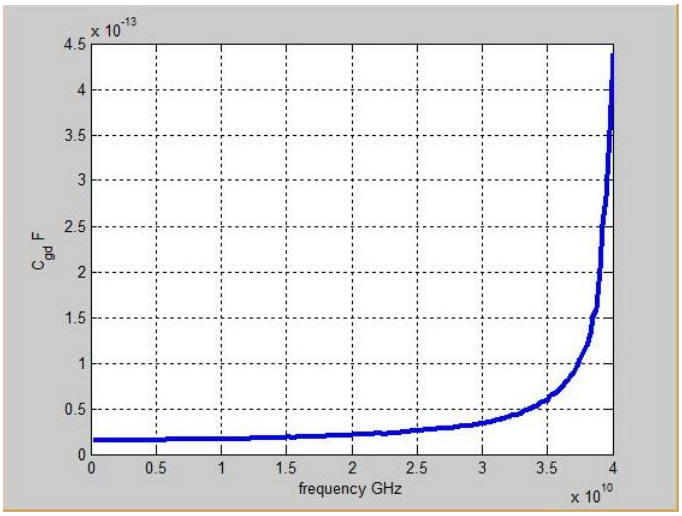

Figure 14: Plot of the intrinsic capacitance C_{gd} versus frequency

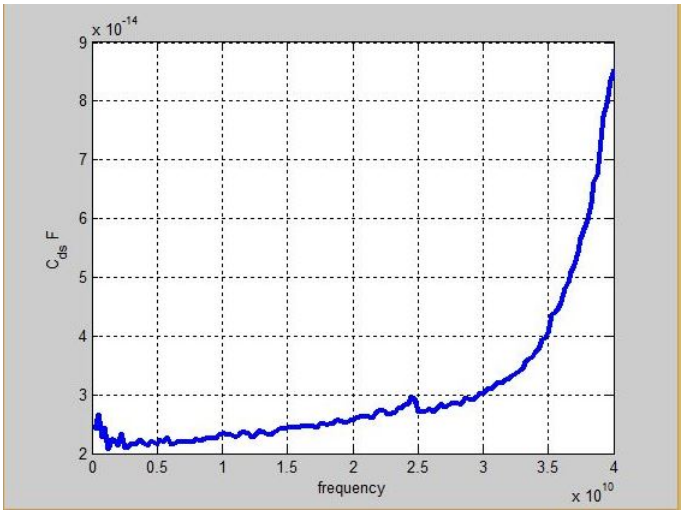

Figure 15: Plot of the intrinsic capacitance C_{ds} versus frequency

The physical origin of C_{ds} is the geometrical capacitance between drain and source. C_{ds} values decrease as V_{GS} increase and allows the 2 DEG formation. The abrupt negative value of C_{ds} in the ohmic region (at low V_{DS}) is known in small-signal model parameters extraction procedures of FET. It is explained that the negative capacitance observed is as inductive effect of a resonant circuit below its resonance frequency. This leads to that an R-L-C circuit is required in the drain-source circuit. But we have already used an R-L-C model. So in this case, C_{pd} or L_s may have been underrated. The response of C_{ds} has been displayed in figure 15.

Experimental results showing the variation of the other intrinsic parameters versus frequency

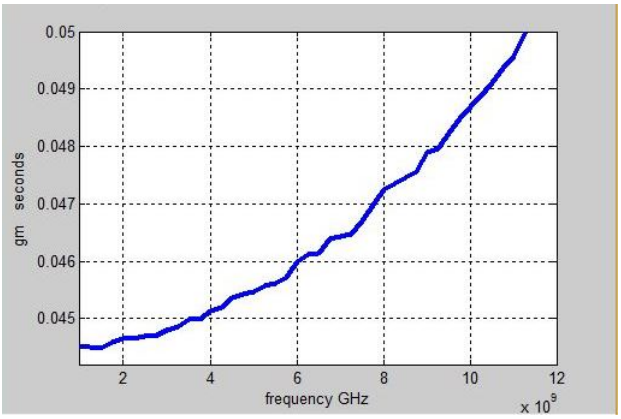

Figure 16: Plot of g_m versus frequency

g_m is defined as the rate of change of the drain current with respect to the gate voltage. The study of previous papers says that, its bias dependency can be inferred from the DC IV transfer characteristic. With $V_{DS} = 0$ V or with V_{GS} near pinch-off or more negative, the values of g_m are expected to be low. It increases rapidly in the low V_{DS} range when V_{GS} increase from the pinch-off.

For large V_{DS} values g_m is expected to show a saturated behavior that allow high drain currents. It can also be inferred that due to high electric field condition electron velocity saturates.

With V_{DS} above 0 V, it is a known characteristic of GaN HEMTs that the transconductance has a non-symmetrical bell-shaped structure with respect to V_{GS}, with an increase from pinch-off than gradual decrease after the peak value.

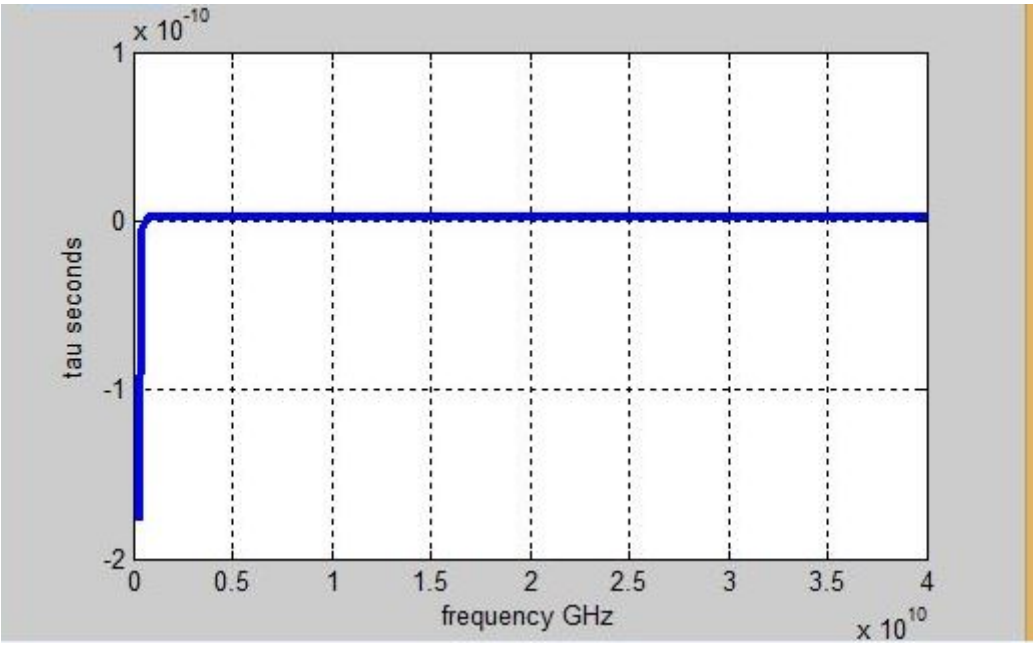

Figure 17: Plot of *tau* versus frequency

The parameter represents the time delay due to the drift of electrons along the 2 DEG. It increases strongly as the gate voltage approaches the pinch-off region and as the drain voltage approaches 0 V.

Experimental results showing the variation of the intrinsic resistances versus frequency

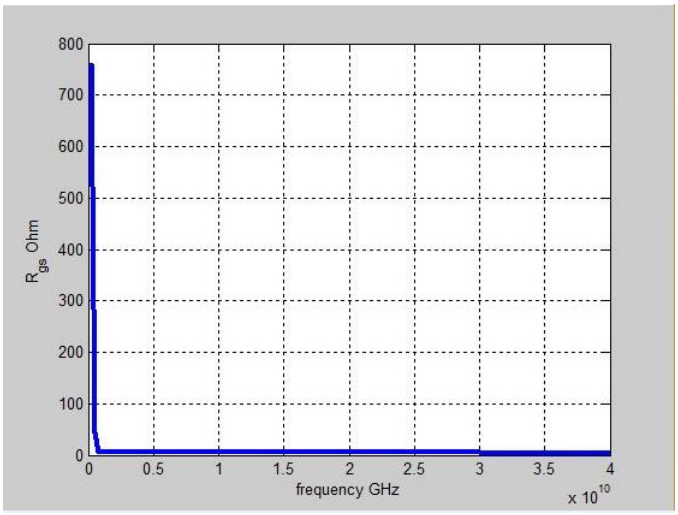

Figure 18: Plot of the intrinsic resistance R_{gs} versus frequency

R_{gs} models the undepleted part of the channel under the gate, and represent spatial delays in the set-up of the charge storage effects related to gate-source capacitance. The value of R_{gs} is equal to the ratio of the potential drop in this channel part and the channel current, which is more or less equal to the drain current. Therefore, it is expected that the value of R_{gs} should be high in the low drain-current region.

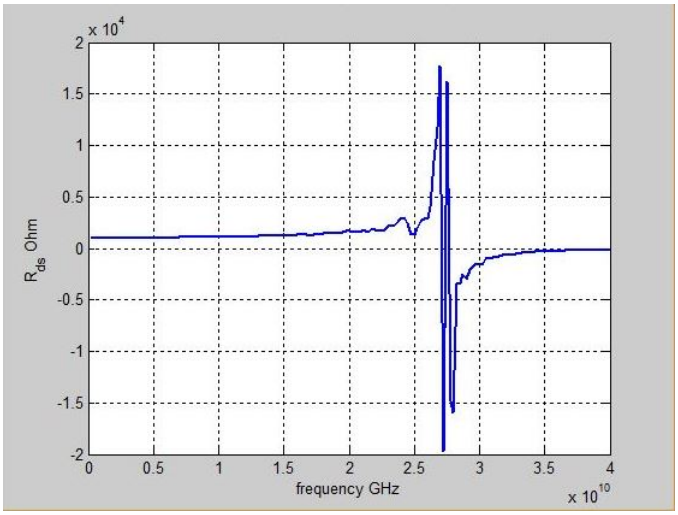

Figure 19: Plot of the intrinsic resistance R_{ds} versus frequency

R_{ds} models the change of the drain current with the drain voltage.
Increasing the gate voltage decreases R_{ds} because it increase the channel charge density and thus the drain current. This increase will become observable in the ohmic region due the reduction of the depletion layer.

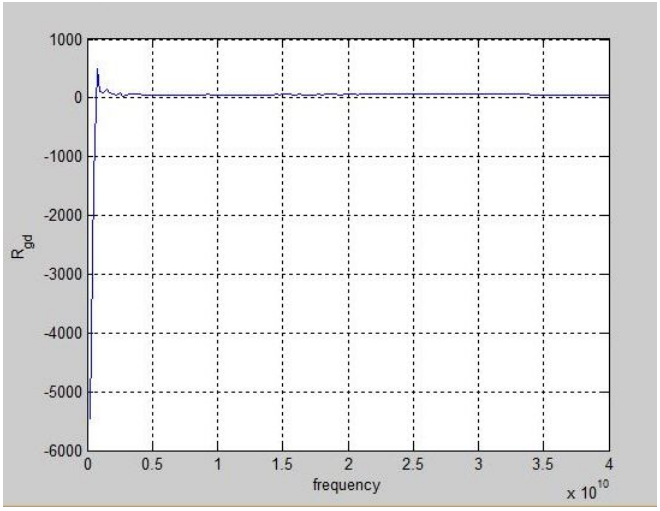

Figure 20: Plot of the intrinsic resistance R_{gd} versus frequency

R_{gd} has same physical definition as R_{gs} and it also represent spatial delays in the set-up of the charge storage effects related to gate-drain capacitance.

The extracted values of the intrinsic parameters are as follows:

- C_{gd} =39.595 fF
- C_{gs} =177.43 fF
- C_{ds} =30.425 fF
- R_{gs} =10.2581 Ohm
- R_{ds} =712.2535 Ohm
- g_m =55.9 ms
- R_{gd} =18.3661 Ohm
- tau =1.2831 ps

The chapter covers the results obtained during the extraction of the small signal elements of a $40.175m^2$ GaN/SiC HEMT in detail.

5.2 SMALL- SIGNAL MODEL VERIFICATION

The small-signal modelling is verified through the simulation of the S-parameter for the GaN on Sic device. Figure 21 shows the results of S-parameter simulation at a definite bias point, in pinch off and saturation regions, over a wide frequency range from 1 GHz to 40 GHz. A considerable agreement is achieved between measurements and simulations at bias points with $V_{GS} = 2$ V and $V_{DS} = 20$ V.

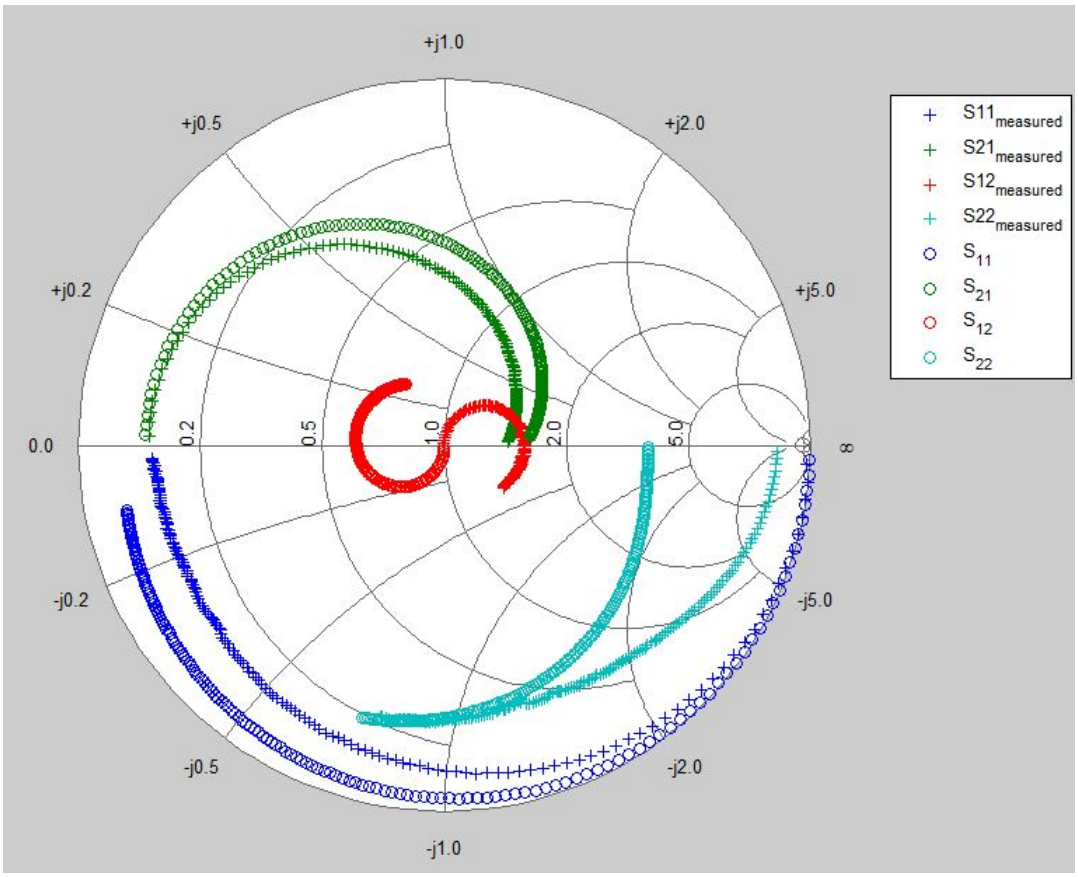

Figure 21: Comparison of the modelled data and measured data

The model's capability of being accurate has been observed in the Smith-plot of GaN HEMTs was also demonstrated. A thorough validation in a multi-bias set-up was extensively carried out with measured data for $40.175m^2$ GaN/SiC HEMT device with and a reliable agreement between measured and modelled results was obtained.With the help of the values of the extracted parameters, one shall be able to study the characteristics of the device and proceed to further modifications alongside implementation of definitive algorithms for optimizing them.

Chapter 6

CONCLUSION AND FUTURE SCOPE OF WORK

6.1 CONCLUSION

The emergence of hetero-junction based high electron mobility transistors (HEMTs) has spearheaded the revolution in microelectronics in the latter half of the 20th century. Ever since the inception of HEMT technology in 1980, it has undergone tremendous advancement at an enormous pace, with the sole aim of producing faster transistors with better noise performance. Over the past three decades, the material systems employed for the fabrication of HEMTs have evolved from the first generation lattice matched AlGaAs/GaAs HEMTs to AlGaAs/InGaAs/GaAs pseudomorphic HEMTs, InAlAs/ InGaAs lattice matched and pseudomorphic HEMTs, metamorphic HEMTs and AlGaN/GaN HEMTs to name a few. Significant improvement in epitaxial growth techniques has further fuelled the rapid progress in HEMT devices.

GaN HEMTs or heterojunction FETs (HFETs) are currently the most widespread and most advanced electronic nitride devices. They make full use of heterostructure and the advantageous breakdown and transport properties of undoped GaN. They exhibit high cut-off frequencies and thus are advantageous in RF circuits. They are advantageous in power-supply circuits because they exhibit high maximum current, high breakdown strength due to large band gap and can be operated at high temperatures. To get a clear understanding of the device geometry small signal modelling is essential. An accurate extraction of the extrinsic elements lays an essential foundation for successfully setting up the SSEC representation of the device.

Two main approaches to determine the extrinsic SSEC elements have proven successful:

- The cold extraction technique, setting the transistor in the passive condition V_{ds} =0 V in order to determine the parasitic in reverse and/ or forward gate bias mode.
- The passive extraction technique, using passive test structures to independently determine parasitic.

  The thesis covers the topic of small signal modelling of GaN HEMT devices in detail. It lists out the ways of extracting the model parameters, the building of the equivalent circuit and the considerations needed to match the measured data and the modelled data. Having discussed the achieved results for the above listed cases, there remains a scope of improvement in many respects.

6.2 FUTURE SCOPE OF WORK

If we look deeply at the Smith plot, we can see there have been discrepancies in the values of the S-parameters, which needs further modification. This is an open area of research which needs considerable attention. In our thesis, we could only carry out the studies related to the extraction procedures and comparisons. The actual task is to develop analytical equations so that they can be incorporated in the device behavior.

Last of all, small signal modelling is only the first step of modelling. Ultimately, a large signal model is required for the full non-linear behavior prediction. So, development of accurate large signal model is of paramount importance for cases where the device is pushed into the non-linear region e.g. power amplifier, mixers, etc. However, the accuracy of large signal models depends on the small signal models, so being able to solve a more complicated circuit where phenomenon like charge trapping, impact ionization ,memory effects are taken into consideration, will enhance the reliability of the model.