A Compendious Study on U-shaped TFET & PNPN-DGTFET Towards Enhanced Device Performance

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ABBREVIATIONS

CHAPTER 1

IC - Integrated **C**ircuit
MOSFET- Metal **O**xide **S**emiconductor **F**ield **E**ffect **T**ransistor
TFET- **T**unnel **F**ield **E**ffect **T**ransistor
AMD - **A**dvanced **M**icro **D**evices
SOI - Silicon on **I**nsulator

CHAPTER 2

LSI- Large **S**cale **I**ntegration
VLSI- Very **L**arge **S**cale **I**ntegration
ULSI- Ultra **L**arge **S**cale **I**ntegration
CMOS- Complementary **M**etal **O**xide **S**emiconductor
SCE- **S**hort **C**hannel **E**ffect
DIBL- **D**rain **I**nduced **B**arrier **L**owering
DGTFET- Double **G**ate TFET
SDGTFET- Strained **D**ouble **G**ate TFET
LG-TFET- L-shaped **G**ate **T**FET

CHAPTER 3

SCE- Short **C**hannel **E**ffects
DIBL- **D**rain **I**nduced **B**arrier **L**owering
CA- Centrally **A**linged
DGTFET- Double **G**ate **T**FET
BTBT- Band to **B**and **T**unnelling

CHAPTER 4

QCE- Quantum **C**onfinement **E**ffect

CHAPTER 5

UC-TFET– U-**S**haped **C**hannel **T**FET

ABSTRACT

The Microelectronic industry has largely been benefitted by the scaling of MOSFET. Rapidly downscaling of MOSFET continued throughout the last two decades, converging Moore's law and yielding advantages in terms of smaller device footprint, lowering the power consumption and higher device density and the function become more complex. However, the aggressive downscaling of the MOSFET faced various performance bottlenecks in terms of its ability to work in ultra-low power, leakage currents, short Channel Effects (SCE), speed improvements etc. leading to its limited performance.

Tunnel Effect Transistor is one of the promising alternatives to the conventional MOSFET's based on various performance parameters as mentioned below: Potential of achieving below 60mV/decade subthreshold swing, ultra-low power and ultra-low voltage, reduced short channel effects, reduction in the leakage current, exceeding the speed requirements due to tunneling effects, ability to work on sub-threshold and super-threshold voltage, similarity in fabrication process as compared with MOSFET and higher I_{ON}/I_{OFF} current ratio.

Although TFET has the above advantages, it suffers low ON current and ambipolar effects. In this context centrally aligned PNPN TFET is considered as promising candidate in providing higher ON current compared to conventional double gate TFET due to efficient tunneling at the source-channel interface. The drawbacks of TFET can be further improved by incorporation of gate and dielectric engineering concepts. This thesis work investigates the various possible techniques to increase the ON current while suppressing the ambipolar effect of the device without affecting the other performance parameters.

At the same time scalability is the need of the hour in semiconductor industry. Quantum confinement needs to be taken care of in scaled devices having dimensions in the range of 15 to 20 nm. In this work, an attempt has been made to incorporate quantum confinement in CA-PNPN-TFET (centrally aligned TFET) based on non-local tunneling model along with self-consistent Schrodinger-Poisson quantum model. Quantum confinement is considered in 1-D. As a result effective band gap and subsequent tunneling barrier width is increased.

The second work presented in this thesis is a novel U-shaped TFET structure and the variation of performance parameters for different materials, gate work functions, oxide thickness, doping concentration and dielectric constant have been extracted.

The various models used in the SILVACO, ATLAS simulations have also been discussed in detail.

CHAPTER 1:
INTRODUCTION AND ORGANIZATION OF THESIS

1.1 INTRODUCTION

In the present era of human civilization, electronic components have become indispensable in every sphere of life from industrial process control, till automotive and consumer electronics/wireless communication. In the last few decades, this excessive dependence on process automation and people's desire for a lavish lifestyle, increased safety, security and high speed real-time interconnectivity have been the driving force behind the explosive growth of all industrial processes and consumer electronics. This rapid growth has been accompanied by constant device miniaturization in the field of electronics. Reduction of circuit dimension reduces the overall circuit area, allowing more devices on a single die without negatively impacting the cost of manufacturing. Constant miniaturization [1] of electronic device from the beginning has become the standard option to increase integration density, circuit speed and to reduce the cost and power. The ever-increasing demand for reliable electronic equipment of smaller size and low power requirement has led to the growth of microminiaturized circuits.

A popular example of one such circuit, called integrated circuit(IC), is a combination of components like diodes, transistors, resistors, capacitors, and their interconnections, collectively grown into one or more complete circuits with several complex functions being implemented on the same chip. Ever increasing trend of device dimension down-scaling to a quasi-nanometer level allows the researchers to explore complex integrated systems on a single chip which drastically reduce their volume and power consumption per function, thereby increasing their speed of operation significantly .

With the evolution of microelectronics into nanoelectronics, the physical dimension of semiconductor devices has been scaled down. The natural advantages of nanoscale transistors are higher current drive and densely packed chips, resulting in faster processing speed and the implementation of many more functions in a single chip.

Since the late 1960s, the number of transistors on a silicon chip has followed an exponential dependence. In 1965 it is observed by Intel executive Gordon Moore that silicon transistors were undergoing a continual process of scaling downward. This observation has been later codified as Moore's law [2]. Moore predicted that an increase in transistor count in a single chip would continue every 18 months. This trend has persisted over four decades and transistor dimensions still continue to scale down almost by a factor of two. The development of the field of nanoelectronics enables the continued realization of Moore's law by using new methods and materials to explore electronic devices in the nano meter range. This continuous scaling trend as predicted by Moore has led to dramatic improvements in computation with reduced power resulting in the development of better consumer products at much reduced cost. For more than last two decades the rapid progress in CMOS technology has taken place through the tremendous pace of scaling, which eventually results in a tremendous increase in speed and functionality of electronic devices.

Hence, with each technology node, it is becoming increasingly difficult to improve device performance and reliability only through traditional scaling and it is now obvious that conventional scaling trend cannot continue indefinitely.

Achieving further miniaturization and retaining the same functional efficiency is only possible through a combined effort of device miniaturization, innovative device structures and improved material property, which is again limited by the fundamental physical constraints so as to meet the aggressive specifications of the International Technology Roadmap for Semiconductors (ITRS).

1.2 Literature Survey and Background Research

In the year 1994, Reddick and Amaratunga [2] proposed the first Silicon-based BTBT transistor. They were motivated by the scope for increased functionality due to negative differential resistance that was prevalent in existing tunneling devices. They were able to fabricate the proposed reverse biased diode on bulk silicon. This structure was able to achieve modulation in

tunneling current upon modulation of tunneling width, which itself is a function of applied bias, depletion width and energy bang gap Eg. They also acknowledged that the mechanism of the BTBT transistor could lay the foundation of a new class of devices that had the potential to replace MOSFETs and allow further scaling in feature size.

TFET structures are broadly classified as-(1) planar TFETs that possess a planar current carrying surface, (2) three dimensional TFETs whereby the current carrying surface extends over all three dimensions. The early TFETs were SOI (Silicon on Insulator) based. The buried oxide layer served to block any leakage paths from the source to the drain, in the bulk region. Additionally, since the source-body and drain-body depletion regions are limited, the structure provides better gate control. However, conventional planar TFETs usually have very low I_{ON} and also suffer from poor SS. This is mainly due to poor BTBT rates observed during practical demonstrations, as opposed to the theoretical expectations. Several structural and material variations been proposed to overcome the limitations of the conventional planar TFETs.

Similar to Double Gate MOSFETs [3-6], the concept of Double Gate TFETs (DGTFETs) was being explored in the 2000s. In 2010, Hoof *et.al*. [7] presented a pseudo-2D surface potential model for DGTFETs, thus laying the foundations for quantification of electrical parameters for the proposed device. In 2011, M. J. Kumar *et.al*. [8] estimated the effects of process induced variations on DGTFETs and proposed strained Double Gate [9] TFETs (SDGTFET) to reduce the impact of process-induced variations on the performance characteristics, thereby improving the reliability of DGTFETS for future applications in CMOS technology. Basically, double gate TFETs comprise of two gates, the top/ front gate and the bottom/back gate. Such a configuration enhances the electrostatic control of the gates on the channel, as the gate electric field lines from one gate terminate on the other gate, instead of the channel. Also, the presence of two gates ensures the formation of two channels and hence, escalates the amount of current that can flow through the device.

In 2011 M. J. Kumar *et.al*. [10] proposed a dual material gate TFET (DMG TFET) based on the concept of dual material gate MOSFETs [11-12]. This structure comprised of two gate metals with different work functions. The gate near the source was called the tunneling gate, as the source-channel interface is where the useful BTBT occurs, and the gate near the drain was termed as auxiliary gate. Taking the example of p-type DMG TFET it was justified that if the

tunneling gate had a higher work function material compared to the auxiliary gate, a higher potential difference between the source and the channel would result in reduced tunneling length and subsequently, increased I_{ON}. Similar arguments can be made to justify the usage of lower work function metal at the drain end, which results in reduced I_{OFF}. Such a structure has better subthreshold slope and is less prone to DIBL effects.

In 2008, Woo *et.al*. [13] introduced the concept of PNPN type configuration. In the PNPN TFET [14] configuration, the P+ source is followed by an N+ pocket doping region. The channel and the drain are intrinsic and N+, respectively. The pocket so formed, creates a conduction band edge (E_C) local minima when V_{GS}=0. This creates a region of abrupt change and a significant lowering of the tunneling width. Moreover, the structural modification enhances the lateral electric field at the source-channel interface resulting in higher I_{ON}.

In 2010, Liu *et.al*. [15] proposed a raised Ge-source TFET to overcome the limitations of Si-based TFETs. Owing to low bandgap, germanium is a popular replacement for silicon as source material. The raised source configuration serves to increase the tunneling area as the entire lateral extent of the source is interfaced with the channel region. Due to increased tunneling area, BTBT is enhanced leading to high I_{ON}.

In 2011, Dutta *et.al*. [16] conceptualized the formation of a heterojunction at the source channel interface for achieving higher I_{ON}. This laid the basis for a new class of TFETs known as the heterojunction TFETs. The proposed structure comprised of $In_{0.7}Ga_{0.3}As$ as the material of choice for the drain and channel, and $GaAs_{0.35}Sb_{0.65}$ as the source material. This leads to staggered characteristics in the band diagram at the source-channel junction that results in shorter tunneling barrier width.

In 2016, Yang [17] proposed an L-shaped gate TFET (LG-TFET) which consisted of an inverted L-shaped gate metal region inserted into the channel. The resultant channel was hence, U-shaped. The P+ source was enveloped by an N+ pocket rendering this structure a PNPN configuration. The structure ensured a relatively large tunneling area as the tunneling junction was perpendicular to the channel. The LG-TFET exhibited a minimum SS of 38.5 mV/decade at V_{GS}=0.2V.

In 2018, Rafat *et.al.* [18] proposed a novel line TFET structure that consisted of a gate over source-channel overlap pockets (GO-SCOPs). This structure provided an inverted C-shaped junction, enabling both vertical and lateral tunneling. The structure was able to achieve an average SS of 48 mV/decade at V_{GS}=2V and V_{DS}=0.5V.

In 2019, Park *et.al.* [19] conceptualized and simulated a double gate TFET having vertical channel regions sandwiched between lightly doped Si (VS-TFET). The vertical junction at the source end enabled steeper subthreshold swing and higher I_{ON} by restricting the tunneling width and increasing the tunneling area. The structure exhibited a minimum SS of 17mV/decade and maintains SS value less than 60mV/decade over a considerable range of $I_{D.}$

In 2019, Kim and Woo [20] presented a novel covered source-channel TFET (CSC-TFET) with a trench gate configuration. This structure aided the enhancement of the tunneling junction area and was able to achieve I_{ON}/I_{OFF} ratio of 10^{10}, subthreshold swing below 40 mV/decade and I_{ON} of approximately 10^{-5} A/μm.

Wu *et.al.* [21] in 2019 proposed a Si-based fin-type TFET where the traditional semiconductor material drain was replaced by a metal silicide drain. Hence, a P-I-M TFET was achieved instead of the conventional P-I-N TFET. TCAD simulations revealed that with appropriate work function of 4.25eV the ambipolar effect was greatly suppressed and the OFF-state current was improved by a factor of 276. This was due to reduced Band-to-Band Tunneling (BTBT) and low Shockley-Read-Hall (SRH) recombination rate at the channel-drain interface due to the metal silicide drain. The I_{ON} remains unchanged while altering the metal silicide work function as it depends only on the BTBT at the source-channel interface.

With feature sizes of 20nm or less, present-day TFET structures suffer from quantum confinement effect (QCE). It is hence, imperative to the study the effect of this phenomenon on the performance of TFETs. In 2019, Najam and Yu [22] explored the impact of geometrical quantum confinement effect (QCE) in LTFET that was proposed by [23]. Such a consideration was necessary as the overlapped channel between the source and gate was of length 4 nm. This work describes the discretization of the conduction band into energy subbands while the valence band remains continuous, under the QCE. The quantum confinement effect in the proposed structure was visualized by employing the self-consistent Schrödinger-Poisson (SP) model which

solves the Schrödinger and Poisson equations for bound state energies and potential, respectively. It was revealed that at V_{GS}=0.2V, without including the QCE, Band-to-Band Tunneling is possible as E_C and E_V are aligned. However, by considering QCE, the first discrete energy subband in the conduction band is not in alignment with the source valence band. This stalls BTBT in the overlapped region of the channel at the given V_{GS}. Hence, higher gate bias is necessary in the LTFET while considering QCE.

1.3 THESIS ORGANIZATION

The thesis has been organized in five main chapters.

- **Chapter 1** deals with the recent developments in the area of semiconductor devices along with a conventional MOSFET structure as well as the drawbacks of these structures are also illustrated. Also the need for a new device with better performance is discussed here.
- **Chapter 2** deals with the basic TFET structure and operating principle. It also deals with the various band diagrams and transfer characteristics and other dependency parameters (viz. workfunction, doping etc) of TFET.
- In **Chapter 3** the centrally aligned PNPN TFET is analyzed through Silvaco, Atlas simulations. The essential performance parameters are analyzed and contrasted for varying gate lengths in order to obtain the most optimized structure.
- In **Chapter 4** Schrodinger-Poisson quantum model has been incorporated in the centrally aligned PNPN TFET structure. In the nanometer below 10nm regime quantum mechanical effects become more pronounced. It is hence necessary to study these effects for our proposed device.
- In **Chapter 5** proposes a Stepped-Tunnel Phenomena in U-Shaped Tunnel Field Effect Transistor. The structure has a U-shaped channel to enhance the channel area of gate control. The device performance parameters are compared to obtain the most optimized structure.
- **Chapter 6** concludes the thesis and discusses the future scope of the work presented here.

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CHAPTER 2:
BASICS OF TUNNEL FIELD EFFECT TRANSISTOR

2.1 Introduction

2.2 Technological Limitation of MOSFET

2.3 Band to Band Tunneling

2.4 Device Structure and Working Principle

2.5 TFET Performance Dependence on Device parameters

2.6 Softwares

2.1 INTRODUCTION

Scaling the length of a MOSFET has many benefits, besides the increased number of transistors in a chip. A reduced gate length leads to a reduced gate capacitance, thereby increasing the switching speed of the circuit. Moreover, the voltage scaling that is a necessary part of device miniaturization also causes reduction in the power consumption of the device.

However, as the device dimensions were reduced to 50 nm and the power supply to 0.5 V, the OFF-state power consumption of MOSFETs became a major challenge. The drain current of a MOSFET is controlled by the thermionic emission from the source into the channel. As the gate voltage increases, the potential barrier between the source and the channel decreases, leading to an increase in the drain current. This leads to two problems – a larger OFF-state current due to subthreshold conduction and a higher subthreshold slope. The subthreshold slope (SS) of a MOSFET is the change in gate voltage V_{gs} required to increase the drain current I_{ds} by a factor of 10. A lower subthreshold slope would allow for a higher ratio of ON-current to OFF-current (ION/IOFF), and would lead to a lower power dissipation in the OFF-state.

One such device is the tunneling field-effect transistor (TFET) [1–4].TFETs can exhibit subthreshold slope below 60 mV/decade due to a fundamental difference in the mechanism of current control as compared to MOSFETs. In MOSFETs, the current depends on the thermionic emission of free carriers across the potential barrier between the source and the channel. On the other hand, the current in TFETs depends on the charge carriers tunneling through a potential barrier between the source valence band and the channel conduction band [1]. As this potential barrier is very wide in the OFF-state of the device, TFETs exhibit very low OFF-state current.

Apart from the limitation imposed by the subthreshold slope, MOSFETs in the sub-50 nm channel regime also suffer from various short channel effects, such as drain-induced barrier lowering, threshold voltage roll-off, charge sharing between gate and drain, etc.[2]. As we shall study later in the chapter, TFETs have a greater immunity to these short channel effects. It may be pointed out that TFETs differ from the MOSFET only in the type of source doping. Therefore, the integration of the TFET fabrication process with the current MOSFET fabrication process would be easy.

2.2 Limitation of MOSFET Technology

As device channel length is continuously decreased, gate control over channel deteriorates due to enhanced nearness of MOSFET's source and drain. As a result, Short–Channel–Effects (SCEs) become a serious challenge associated with downscaled MOSFETs. When the channel length is shrunk to the order of source and drain depletion-layer width SCE s emerges. SCEs lead to several reliability issues as the basic device parameters (such as threshold voltage), become dependent on channel length. [3]-[10]

Five different short-channel effects are:

1. Drain-induced barrier lowering
2. Threshold voltage roll off,
3. Surface scattering,
4. Velocity saturation and
5. Hot electron effect

2.2.1 Induced Barrier-Lowering (DIBL):

Drain induced barrier lowering is the primary short channel effect that come into picture. The effect of the barrier lowering can be observed by a shift of threshold voltage as a function of drain voltage of short channel device. In short channel MOSFET, the depletion width at source and drain junction become comparable to the channel length.

As the gate voltage is increased the barrier gets reduced and the carriers flow due to the electric field. This simple process becomes complex in small-geometry MOSFETs. In this case, the potential barrier gets controlled not only by the gate-to-source voltage V_{gs}, but also by the drain-to-source voltage V_{ds}. On increasing the drain voltage, the channel potential barrier decreases, resulting in the short-channel effect termed as the Drain-Induced Barrier Lowering (DIBL).

Even if the gate-to-source voltage is lower than the threshold voltage, this lowering of the surface potential barrier ultimately allows electron flow between the source and the drain. The current that flows in the channel under this conditions ($V_{gs}<V_{T0}$) called the sub-threshold current.

2.2.2 Threshold Voltage Roll-Off

The expression of Short-Channel Effect (SCE) can be derived from the above mentioned VDT model [5]:

$$\mathrm{SCE} = 0.64\frac{\mathcal{E}_{\mathrm{Si}}}{\mathcal{E}_{\mathrm{ox}}}\left[1+\frac{\mathrm{x_j^2}}{\mathrm{L_{el}^2}}\right]\frac{\mathrm{t_{ox}}}{\mathrm{L_{el}}}\frac{\mathrm{t_{dep}}}{\mathrm{L_{el}}}\mathrm{V_{bi}}$$

The threshold voltage (Vth) of MOSFET can be deduced as:

$$\mathrm{V_{th}} = \mathrm{V_{th\infty}} - \mathrm{DIBL} - \mathrm{SCE}$$

This is typically measured in mV/nm.

2.2.3 Surface scattering

With the gradual reduction of channel length, the gate oxide thickness also gets scaled down. As a result, the transverse electric field normal to the channel becomes dominant. The collisions suffered by the electrons which are accelerated toward the interface by the influence of the electric field, is known as the surface scattering. This phenomenon degrades the channel carrier mobility. Since the carrier transport in a MOSFET is confined within the narrow inversion layer, the electrons face greater difficulty in moving parallel to the interface. Therefore, even for small values of perpendicular electric field, the average surface mobility is about half as much as that of the bulk mobility.

2.2.4 Velocity saturation

The increase in channel electric field due to reduction of device dimension results in an increased carrier velocity. At this high electric field, the linear relationship between electric field and velocity fails to exist and the velocity gradually saturates reaching the saturation velocity. Both the electron and the hole drift velocity saturate at applied electric fields in excess of about 100 kV/cm. In short-channel devices, the electric field near the drain attain excessive value (could be more than 400kV/cm). The reason behind this carrier velocity saturation [6-8] is the increased scattering rate of highly energized electrons, mainly due to optical phonon emission. This consequently increases the transit time of carriers through the channel. In sub-micron MOSFETs, it can be observed that the average electron velocity is much larger than in bulk MOSFETs. As a result, velocity saturation is not quite as much of a restriction as initially presumed.

2.2.5 Hot Electron Effect

Another important consequence of the high source-drain electric field strength is the strong carrier heating associated with this field. The channel electric field of the short channel MOS is sufficient to heat the carriers to a very high kinetic energy near the drain causing “hot-electron effect”. This term was first coined by Conwell et.al to describe non-equilibrium electrons in semiconductor. The term refers to the electron distributions that can be represented by the Fermi function, but with a higher effective temperature. This concept is not so relevant for metals because the electron mobility does not vary significantly with their energies. However, in case of semiconductors, the carrier mobility varies considerably with the effective temperature making

the “hot-electron” phenomenon very much prolific. This effect is seen where the electrons are able to rise above the conduction band. As the “hot” electrons have sufficient kinetic energy, instead of being conducted through the material to a collector or recombining with holes, the ‘hot’ electrons can penetrate the semiconductor material. These electrons give away their excess energy in the form of phonons. In MOSFETs, it can also be noticed that these ‘hot’ electrons may jump from the drain to the gate or the substrate, consequently heating up the devices and increasing the device leakage currents.

2.3 Band to Band Tunneling

2.3.1 Analytical Modeling

In semiconductors, two different kinds of models are used to calculate the current resulting from tunneling – local and non-local models. Non-local models treat tunneling as a process that occurs in spatial coordinates, where electrons tunnel from one point in space to another, as shown in Figure 2.1. The WKB approximation and Landauer’s tunneling formula [9-14] that we have considered earlier can be classified as non-local models. Local models, on the other hand, treat tunneling as a phenomenon taking place from one energy band to another in the E–k space of the material.

(i) Non-local tunneling models

Since the non-local models approach tunneling from a spatial perspective, we need to know the spatial dependence of all the parameters in Schrodinger’s equation to obtain the tunneling probability. If an external bias is applied to a semiconductor, the shape of the potential barrier V(x) is complicated. The band structure of the semiconductor also needs to be incorporated into the potential V(x) in Schrodinger’s equation. Moreover, the potential in the semiconductor depends on the current (Ohm’s law), while the current in turn depends on the shape of the potential barrier (Schrodinger’s equation). All these complicated spatial dependencies make it difficult to solve Schrodinger’s equation analytically. Therefore, numerical approaches need to be applied to obtain a solution for calculating the tunneling probability. However, because all these complex dependencies are incorporated, non-local models provide an accurate estimation of the current in the device although they are difficult to solve analytically. As non-local models cannot be used to obtain analytical models, they are used in device simulation. On the other

hand, analytical models are essential for use in circuit simulation and to understand the functioning of devices. To develop analytical models, we use local tunneling models**.**

(ii) Local tunneling models

To understand local models, let us consider the problem from an energy band perspective. Semiconductors have various energy bands, which result from the interaction of the individual fields created by the atoms in its lattice. These energy bands are usually represented in an E–k diagram, which shows the allowed values of energy E that the electron can take. We can observe the presence of a valence band and a conduction band [15-20], separated by the bandgap – a potential barrier. Since we have considered an intrinsic material, there are very few electrons in the conduction band. In the presence of an external electric field, these few electrons will flow to generate a very low current. However, if this electric field is sufficiently large, it is possible for electrons to tunnel from the valence band to the conduction band without a change in energy, as shown in Figure 2.1. In other words, the electric field causes the bands in the semiconductor to be modified in such a way that the electrons in the valence band can tunnel through the potential barrier (the bandgap) and reach the conduction band. Now that there are sufficient electrons in the conduction band due to tunneling, an appreciable current can flow in the material.

An important approximation made while deriving local models is that the electric field is assumed to be constant, which is rarely true in a real device. Because of the assumption of a constant electric field, local models predict a single tunneling rate throughout the device. In case the electric field is position-dependent, we estimate the tunneling rate using the local electric field at every point in the device.

The tunneling rate at each point is then integrated throughout the device to give the total number of electrons that have tunneled from the valence band to the conduction band. Since no generation or recombination is assumed, the total current is dependent only on the rate at which the electrons tunnel from the valence band to the conduction band. Therefore, in local models, it is assumed that each electron that reaches the conduction band is swept away to form a part of the total current. Local models are extensively used in analytical modelling of TFETs as they give an analytical expression for the tunneling rate at each point.

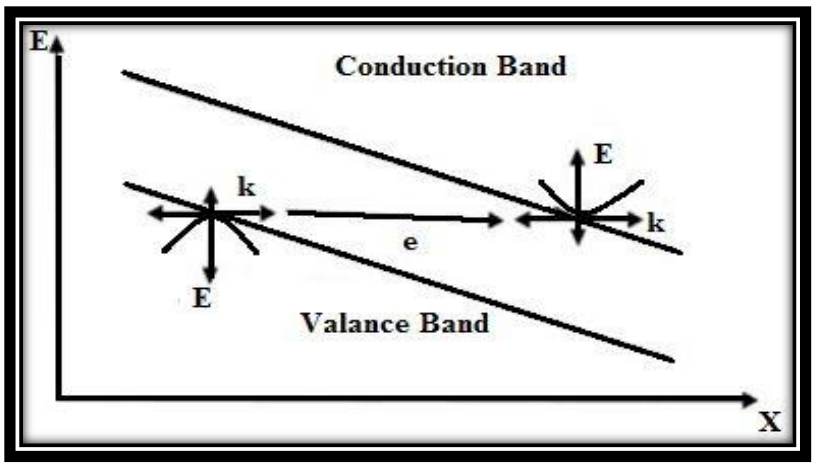

Figure 2.1 Band to band Tunneling

2.4 TFET STRUCTURE AND WORKING PRINCIPLE:

2.4.1 Basic Structure

Figure 2.2 (a) and (b) shows the basic structure[21-26] of an p-channel-TFET and n- channel - TFET. The device has three regions – the source, the channel and the drain. Comparing the structure of an n-channel TFET with that of an n-channel MOSFET, the source doping in a TFET is p-type, whereas it is n-type in the MOSFET. This is the only major difference between a TFET and a MOSFET. The channel region in the TFET is usually intrinsic, or very lightly doped.

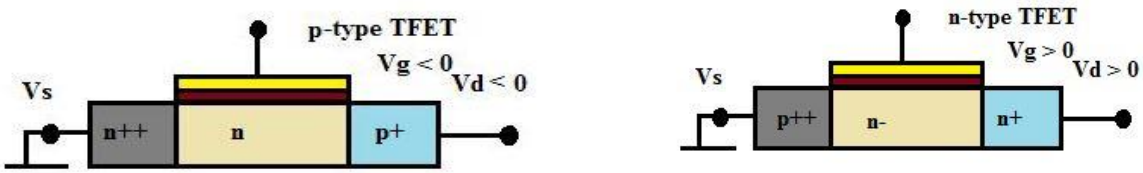

Figure 2.2 Basic Structure of TFET (a) p-TFET (b) n-TFET

2.4.2 Operation Of TFET

(i) Thermal Equilibrium

The thermal equilibrium band diagram of a TFET, that is with no external bias (V_{gs} = VS = V_{ds} = 0), is shown in Figure 2.3. There are two depletion regions formed – one at the source–channel junction and the other at the channel–drain junction.

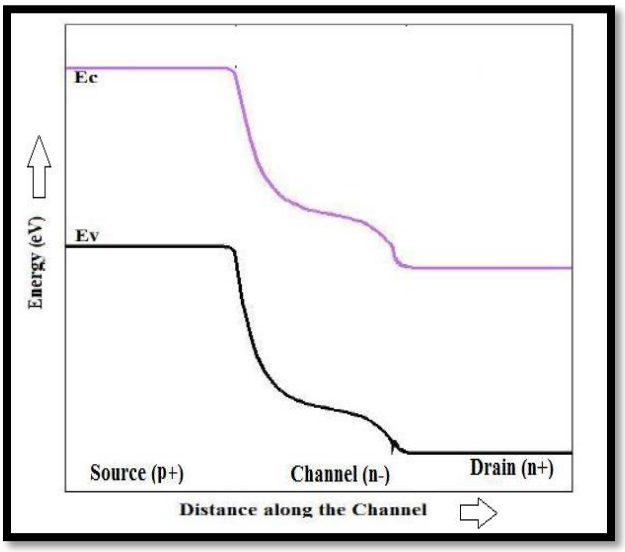

Figure 2.3 Band diagram at the surface of a n-channel TFET in thermal equilibrium (i.e. at zero bias).

(ii) Off State

The TFET is in OFF-state when the drain voltage V_{ds} > 0 and the gate voltage V_{gs} = 0, which is similar to the OFF-state of a MOSFET. The band diagram for this case is shown in Figure 2.4.

In the OFF-state of the TFET, any charge carriers present in the conduction band of the channel would have a tendency to drift to the drain and thus generate a current. However, as the source is p-type, there are very few free electrons in its conduction band, and therefore very few electrons can be injected into the channel. This leads to a negligible OFF-state current. However, in the case of a MOSFET, the source is n-type and has free electrons in its conduction band. Through thermionic emission, a few of these electrons will be injected into the channel over the potential barrier at the source–channel junction. This leads to a higher OFF-state current in a MOSFET as compared to a TFET.

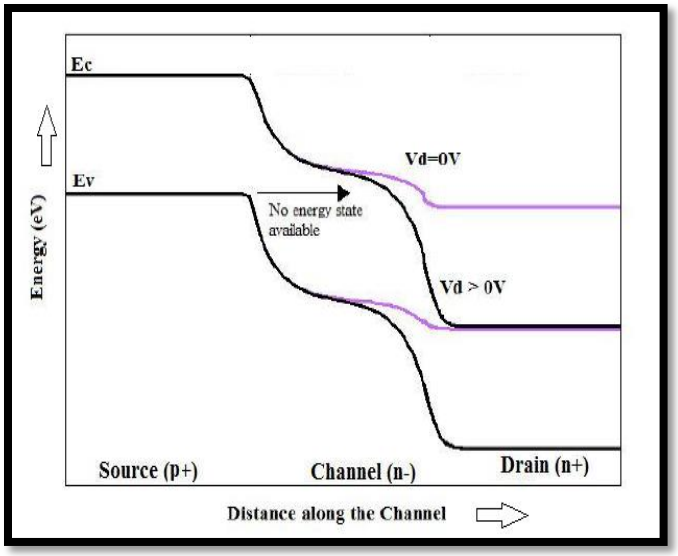

Figure 2.4 Band diagram along the surface of a TFET in the OFF-state (i.e. at V_{gs} = 0 V).

(iii) On State

As we increase the gate voltage V_{gs}, the energy bands in the channel change with respect to the source as shown in Figure 2.5. At a certain value of the gate voltage V_{gs}, the valence band in the source gets aligned with the conduction band in the channel, as shown in Figure 2.5. In the OFF-state of the device, the electrons in the valence band of the source did not have any available energy state in the channel into which they could tunnel. Now that the valence band of the source is aligned with the conduction band of the channel, electrons can tunnel from the former into the latter through the potential barrier formed by the bandgap E_g

As the gate bias is further increased, the bands in the channel region are further lowered in energy, and electrons occupying energy levels from the valence band edge of the source E_v, Source to the conduction band edge of the channel E_c, Channel can tunnel to the conduction band in the channel. This leads to a steep increase in the current. In addition, an increase in the gate voltage not only increases the number of electrons that are able to tunnel but also increases their tunneling probability due to reduced tunneling length. Therefore, the current would vary significantly with a changing gate voltage.

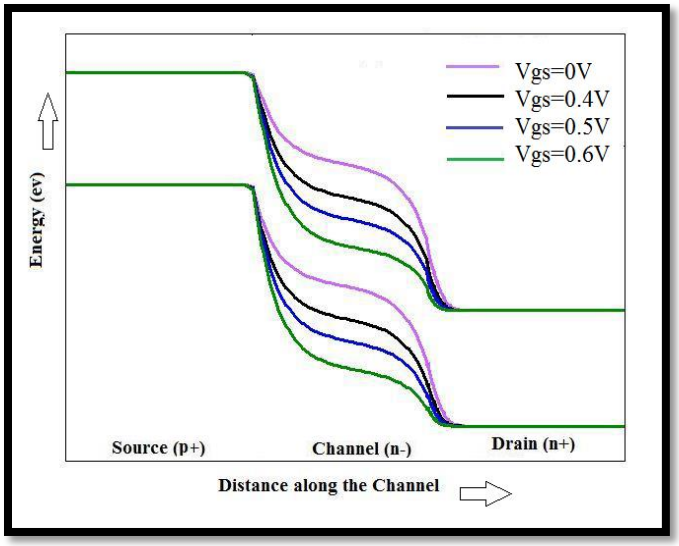

Figure 2.5 Band diagram along the surface of the TFET with increasing value of the gate voltage (V_{gs}) in the ON-state.

2.4.3 Transfer characteristics

Figure 2.6 shows the transfer characteristics of a TFET in which the source and drain dopings are equal and opposite. The regions of operation discussed in the previous section have been marked on the figure. As we can observe, there is a very low current in the OFF-state of the device, when the conduction band of the channel is not aligned with the valence band of the source. As the gate bias is increased, the current rapidly increases due to reduction of the tunneling width and an increase in the number of initial states in the source from where tunneling can occur. At a higher gate bias, the rate of increase of current reduces since the contribution of the additional initial states in the source valence band is negligible. As the gate bias approaches the drain potential, the rate of increase of current further decreases due to pinning. A similar behavior is observed in the negative bias region.

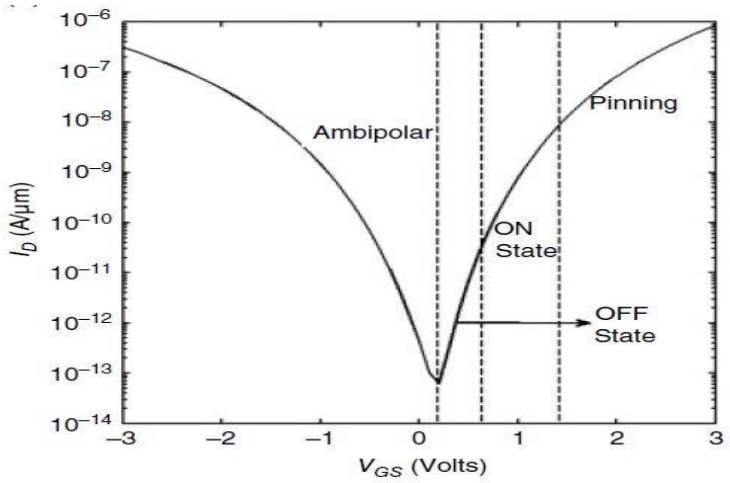

Figure 2.6 Transfer characteristics (I_{ds} $-V_{gs}$) of an n-channel TFET for a positive value of V_{ds} showing different regions of operations.

2.4.4 Pinning Of the Channel Potential:

When the gate voltage is further increased, an inversion layer forms in the channel region. The layer consists of electrons as the gate voltage is positive. At a sufficient high voltage i.e. the gate voltage above drain voltage (VGS> VDS) the electron density of the inversion layer, formed into the channel became comparable with the n+ drain region. This makes the channel being shorted with the drain, making them equipotential. This phenomenon is known as 'Pinning'. However when the channel is pinned to drain potential the further increase of gate voltage will have no longer had a capability to lower the conduction band energy of the channel.

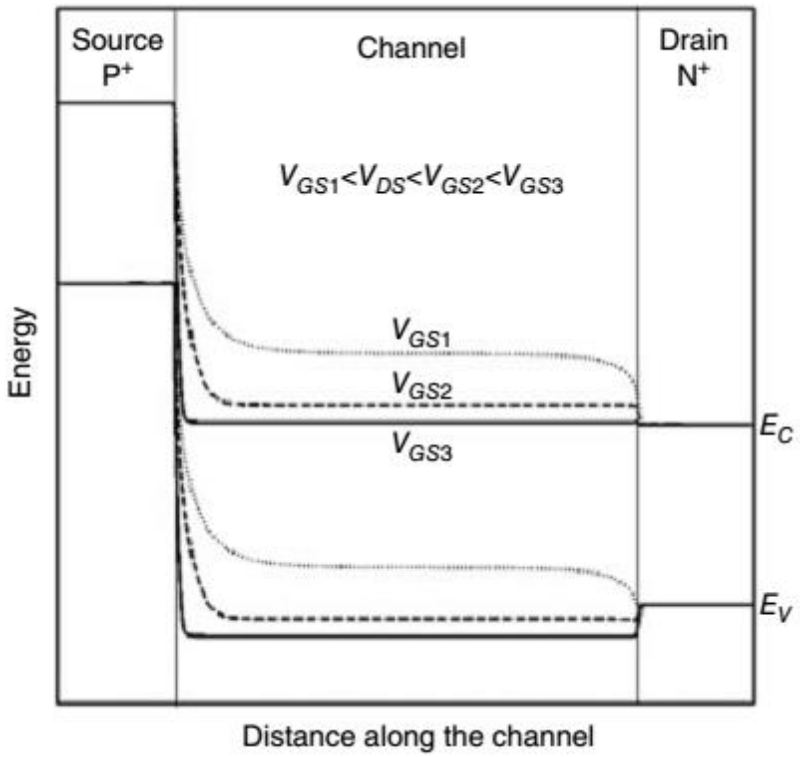

Figure 2.7 Band diagram along the surface of the TFET with increasing value of gate voltage

Ambipolar Behavior:

As the gate voltage is decreased below 0 V, the energy band of the channel moves upward with respect to the source. When the valence band of the channel is aligned with the conduction band of the drain, electrons from the valence band of the channel can tunnel into the conduction band of the drain, resulting in a current flow. The electrons tunnel in the same direction as in the case of a positive gate bias. This results in the device current having the same polarity even at a negative gate bias.

A further increase in the negative gate bias causes a significant increase in the drain current due to (i) reduction of the tunneling length at the channel–drain junction and (ii) an increase in the number of states in the channel valence band from where electrons can tunnel to the conduction band of the drain. This is called ambipolar conduction and is shown in Figure 2.8

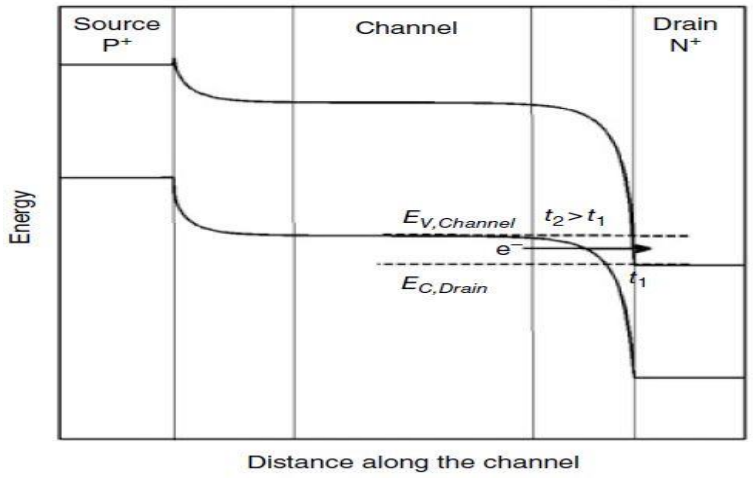

Figure 2.8 Band diagram along the surface of a TFET for a negative gate voltage (V_{gs}) and a positive drain voltage (V_{ds})

As the negative gate bias is further increased, the channel potential gets pinned to the source potential. Therefore, as discussed in the section on pinning, the channel potential no longer depends on the gate potential. After this point, increasing negative gate voltage causes an increase in the drain current solely due to a decrease in the tunneling length. Therefore, the drain current increases at a lower rate.

2.5 PERFORMANCE DEPENDENCE ON DEVICE PARAMETERS:

2.5.1 Doping

(i)Source Doping

A higher doping in the source leads to a shorter depletion region at the source–channel junction. Due to this, as indicated in Figure 2.9, the electron occupying the valence band edge in the source would have to tunnel through a shorter distance in the case of higher source doping, as compared to the larger distance in the case of lower source doping. Therefore, the tunneling probability would be greater in the case of a higher source doping, thereby resulting in a larger ON-state current.

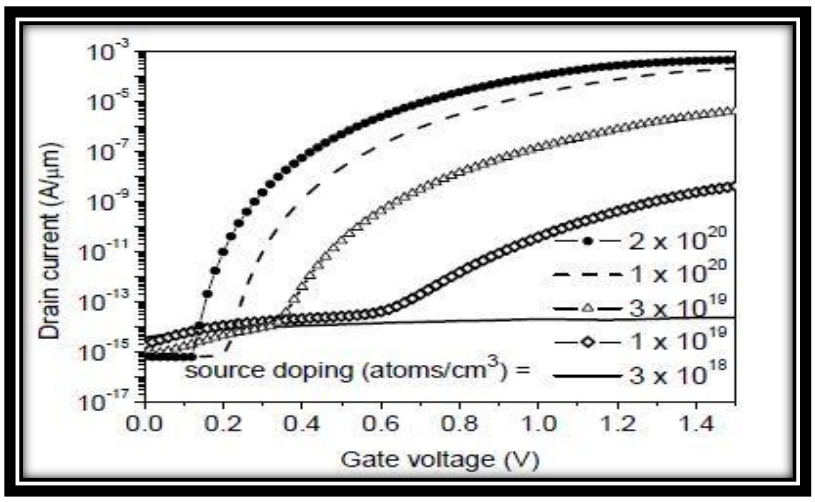

Figure 2.9 $I_{ds}-V_{gs}$ for varying source doping levels.

A very high source doping level is advantageous because it leads to a smaller swing and higher on-current when V_{ds} = 1 V.

(ii)Drain Doping:

By increasing in the drain side doping would lead to a greater drain–channel tunneling in the case of negative gate bias, thereby it increases the ambipolar current. In many applications, the ambipolar current is sought to be minimized, that may be accomplished by reducing the drain doping.

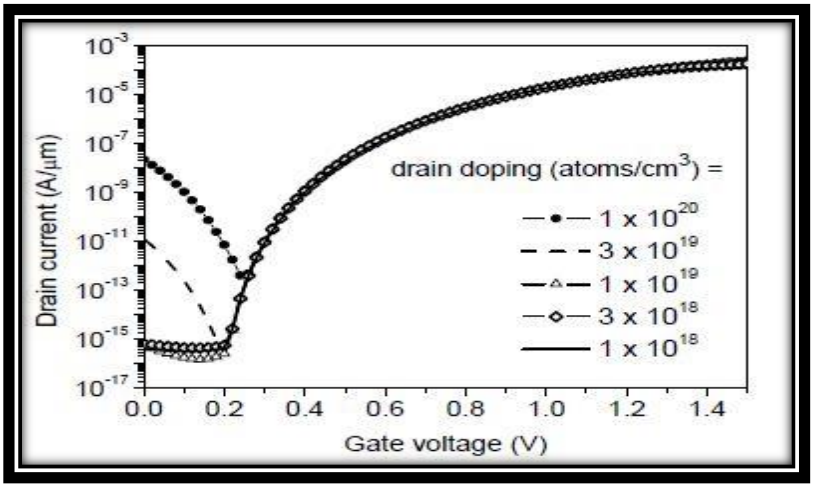

Figure 2.10 $I_{ds}-V_{gs}$ for varying drain doping levels. The ideal drain doping level is low enough to suppress ambipolarity. V_{ds} = 1 V.

2.5.2 Gate work function

By the comparison of the band diagram of a TFET with a higher gate work function Φ_{G1} to that of a TFET with a lower gate work function Φ_{G2} we can see in the transfer charecteristics curve that right sideof the curve i.e the on current is increased besides off it the left side of the curve i.e the off current is decreased.

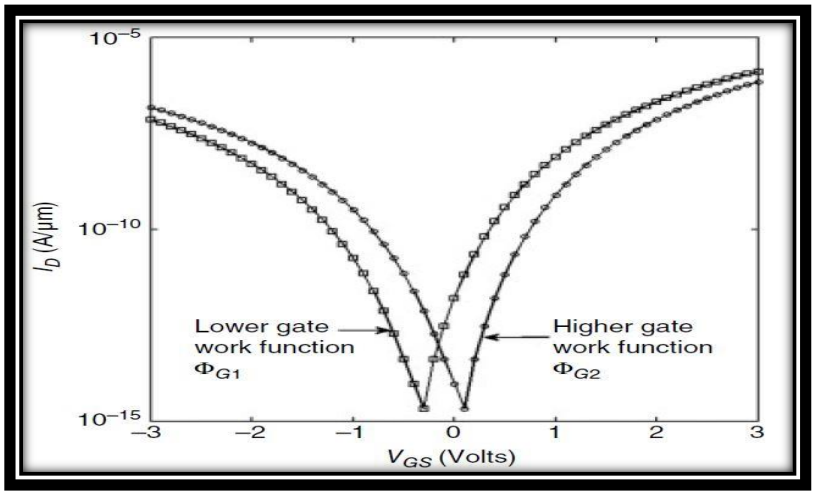

Figure 2.11 Transfer characteristics of an n-channel TFET with different values of the gate work function.

2.6 Softwares:

2.5.1 Simulation software

All the simulations during the research work is done in Silvaco ,Atlas.[32]

ATLAS provides general capabilities for physically-based two (2D) and three-dimensional (3D) simulation of semiconductor devices. It predicts the electrical behavior of specified semiconductor structures and provides insight into the internal physical mechanisms associated with device operation.

2.5.2 Quantum simulation

Several local and non-local tunneling models can be incorporated in quantum simulation [32] Moreover density gradient model and self-consistent Schrodinger –Poisson model is also included in simulation Variation of several parameters are also analyzed in these quantum models in that study. Following that research work we have also attempted the same in the double source TFET structure.

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CHAPTER 3:
Centrally Alinged PNPN-DG TFET

3.1 Overview and Proposed Work

In this work, a novel 2D tunnelling field effect transistor (TFET) with centrally aligned source pocket doping has been proposed and its performance metrics have been explored through simulations. The symmetric double- gate TFET structure is incorporated with a centrally aligned heavily doped pocket region at the source end. This structural modification improves source tunnelling, resulting in higher I_{ON}/I_{OFF} ratio and reduced ambipolarity, as compared to conventional planar TFETs. In order to study the performance characteristics, the gate metal length has been varied-24nm, 14nm and 7nm. Hafnium Oxide (HfO_2) has been used as the gate oxide material. The three resulting structural variations are compared to obtain the most optimized structure. All 2D simulations were performed on Silvaco, Atlas.

The essential deficiencies of MOSFET innovation, lead to the widespread of TFET devices [1-5] which prompted the nanoscale business because of its sundry alluring interest. The fundamental advantage of TFET is that conduction is facilitated through balance of quantum mechanical Band-to-Band Tunnelling (BTBT), which is better over the thermionic injection in the case of MOSFET. The subthreshold swing of a TFET is under 60mV/decade due to the BTBT mechanism that leads to higher Ion/Ioff [6] ratio. Besides, TFETs have higher invulnerability to short channel effects. Moreover, they demonstrate a small leakage current in the range of femto amperes (fA) making it productive for low power applications [7]. Moreover, another preferred advantages of TFETs contrasted with other device ideas are that it requires less complex

fabrication steps. Also, the tunnelling process upgrades the device speed and helps in reducing the threshold voltage.

The real worries for TFET device over MOSFETs are ambipolar conduction that originates at the channel-drain intersection in view of band to band tunnelling and the other is low ON current. In this paper another thought of including a centrally aligned source pocket doping region in the symmetrical double gate TFET has been proposed to compensate the ambipolar current. Likewise the doping concentrations are kept to such an extent that we can get higher ON current. The gate lengths are changed and contrasted to get the most improved variant. In all of these structures the source pocket regions are heavily doped contrasted with the channel. Hafnium Oxide has been used as the gate oxide. With this plan we can discover numerous attractive improvements like smothering the ambipolar conduction [8-9] and obtaining low leakage current.

In this proposed work, a 2-D analytical model for DG TFETs with two source pocket doping regions is presented. Another thought of including a centrally aligned source pocket doping region in the symmetrical double gate TFET has been proposed to compensate the ambipolar current. Likewise the doping concentrations are kept to such an extent that exhibits higher ON current. The gate lengths are changed and contrasted to get the most improved variant. In all of these structures the source pocket regions are heavily doped contrasted with the channel. Hafnium Oxide has been used as the gate oxide. With this plan we can discover numerous attractive improvements like smothering the ambipolar conduction and obtaining low leakage current. All the graphs are simulated, and results are verified by the SILVACO ATLAS data. The work is organized as follows. The device structure is described using TCAD simulation and its design parameters. Then graphs for potential distribution, electric field, band to band tunnelling rate for different gate lengths has been shown and last transfer characteristics is represented to validate the I_{ON}/I_{OFF} current.

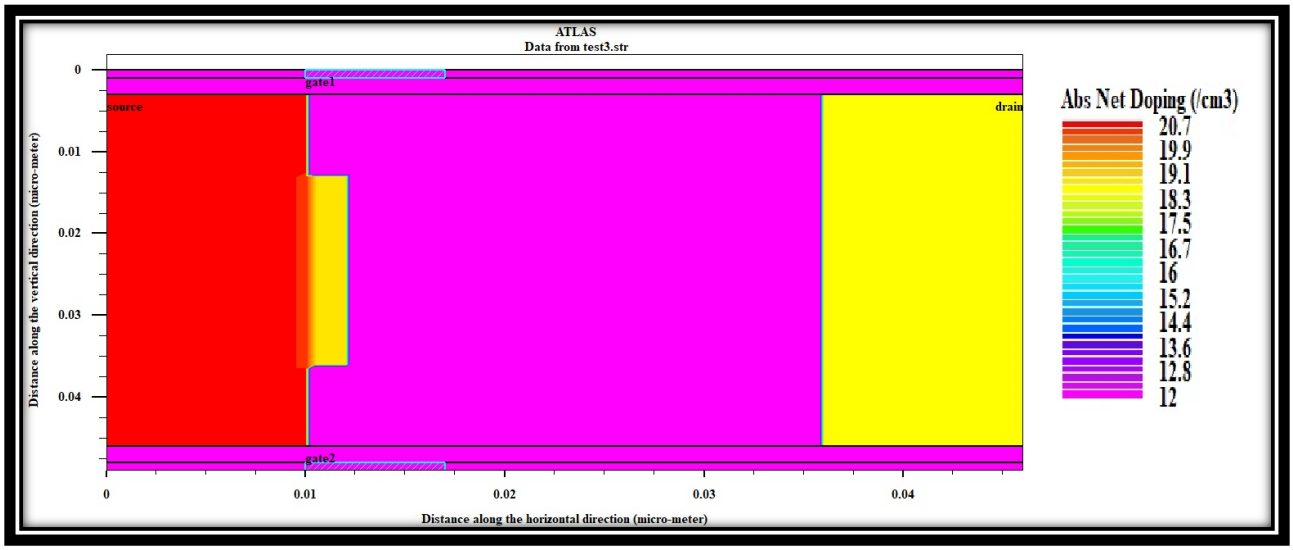
3.2 Device structure and Parameters

The 2-D cross-sectional perspective on the p-channel TFET structures[10-11] with absolute net doping profile are given in Fig. 3.1 utilizing Silvaco Atlas. The structure contains centrally aligned Source Pocket region [12] that is absent in a traditional TFET. This is a heavily doped

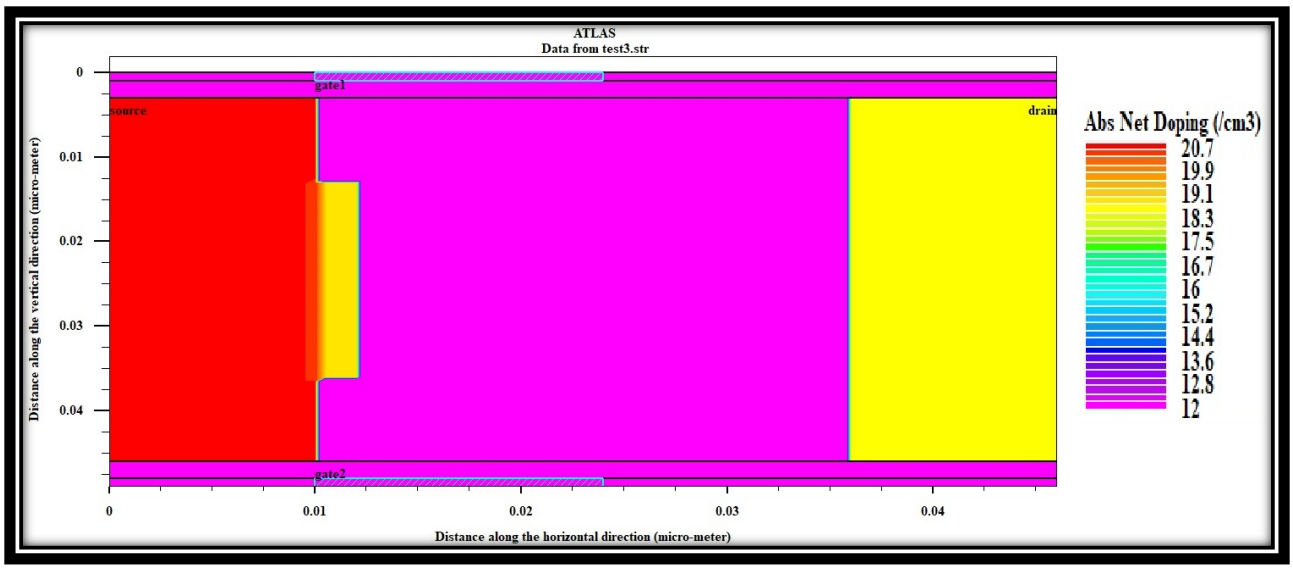
region. The specific doping concentration of the TFET models are: P+ type source region (1×10 20 cm-3), P channel region (1×10 12 cm-3), N+ type Drain region (1×10 18 cm-3) and the N+ Pocket region (1×10 19 cm-3), which are kept constant for all the simulations. Such doping fixations create a tunnelling junction between source and channel where the phenomenon of interband tunnelling can happen.

The simulated device has a total length of 46nm and vertical dimension of 49nm. The gate length is varied to 24nm, 14nm and 7nm. But the effective channel length is examined to be 22nm. The lateral and the vertical dimensions for both the Source and Drain regions are 10nm and 43nm, respectively. The Pocket Region has a lateral and vertical dimension of 2nm and 25nm respectively.

The dielectric used for gate electrode is Hafnium Oxide (HfO2) which has a thickness of tox = 2nm and dielectric constant is approx. 4.



(a)



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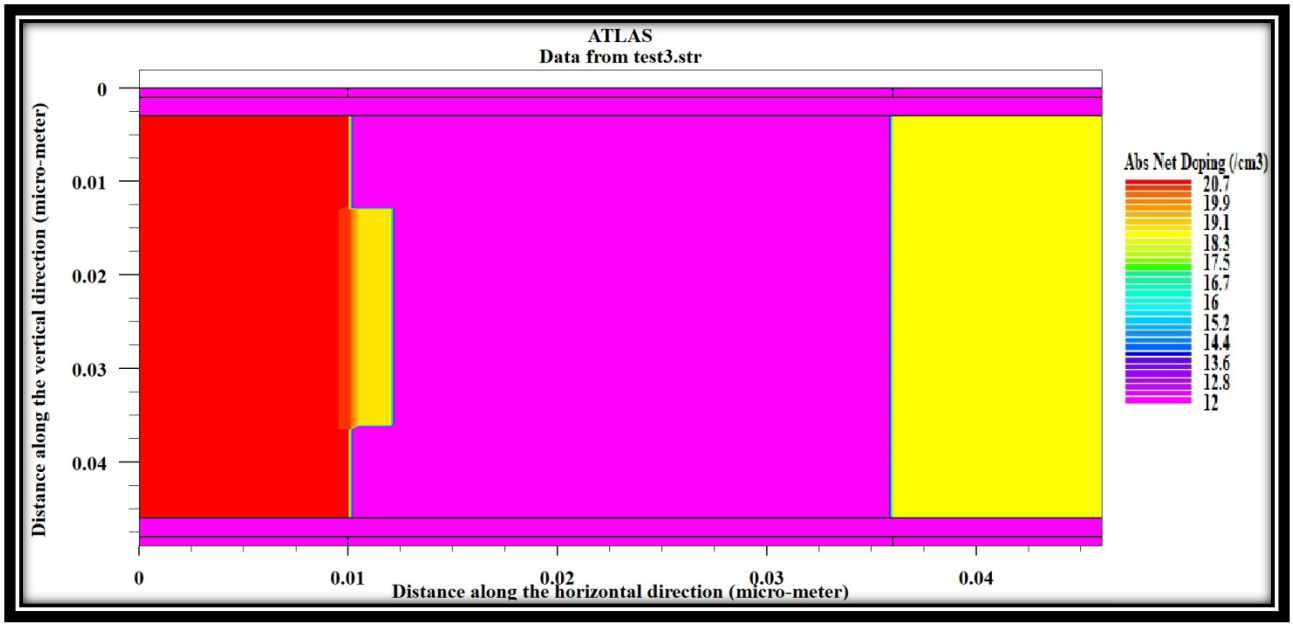


(c)

Figure 3.1: Structure of CA-PNPN-DG TFET along with the doping concentration of the proposed TFET structure for (a) 7nm, (b) 14nm and (c) 24nm gate length.

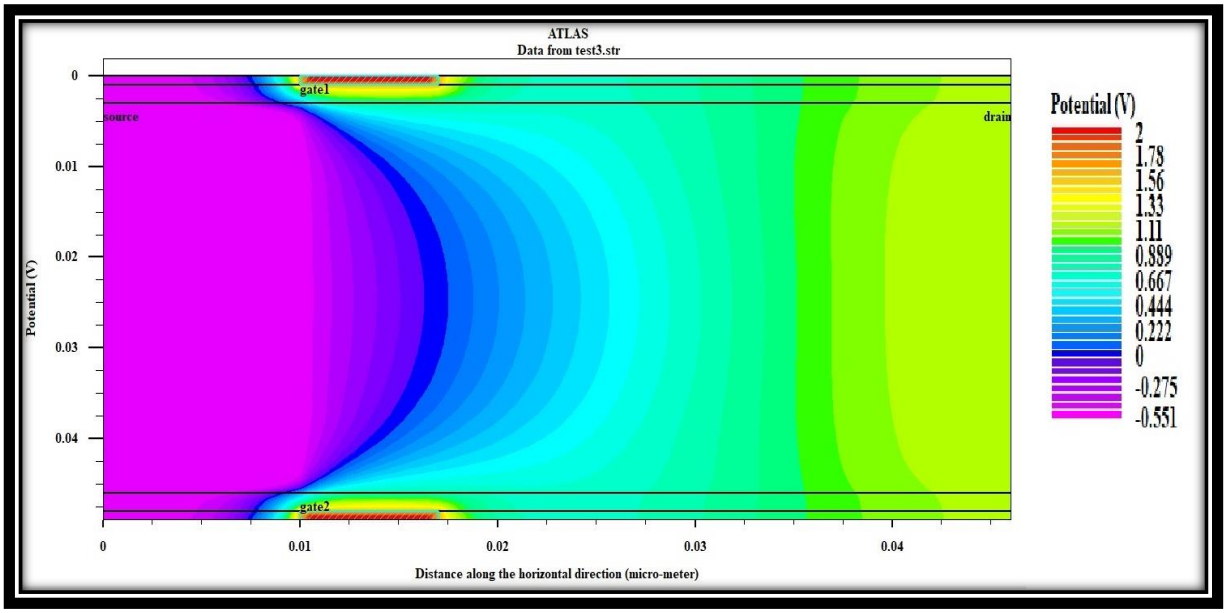
Both the gate contacts have work function of 5.1eV and the source and drain contacts are considered to be in vertical direction on two opposite sides of the proposed structure.

3.3 Results And Discussions

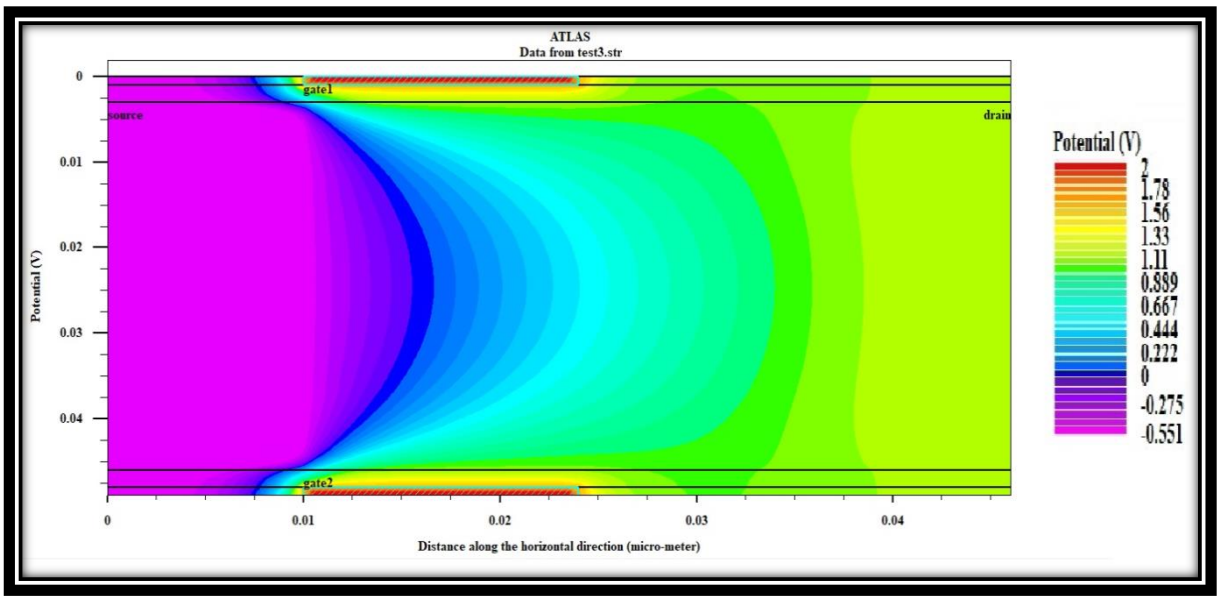
Endeavours are made for simulation predicated validation studies of the proposed contrivance structures. The simulation results along with visual graphical plots of potential profiles, electric field, electron current, hole current, total current etc. for different gate lengths of the structure are portrayed in this section.

3.3.1 Potential Distribution & Electric Field Distribution

The potential distributions for various gate lengths have been shown in Fig.3.2. For gate length 7nm, the discrepancy of potential along the vertical dimension at any vertical line is nearly nil as portrayed in Fig.3.2.(a) while for gate length of 14nm and 24nm, the potential fluctuates in vertical dimension which is obvious from the curvature as seen in Fig.3.2.(b) and Fig.3.2.(c) respectively. So it implies that the 7nm structure shows insignificant ambipolarity and furthermore is increasingly stable.



(a)



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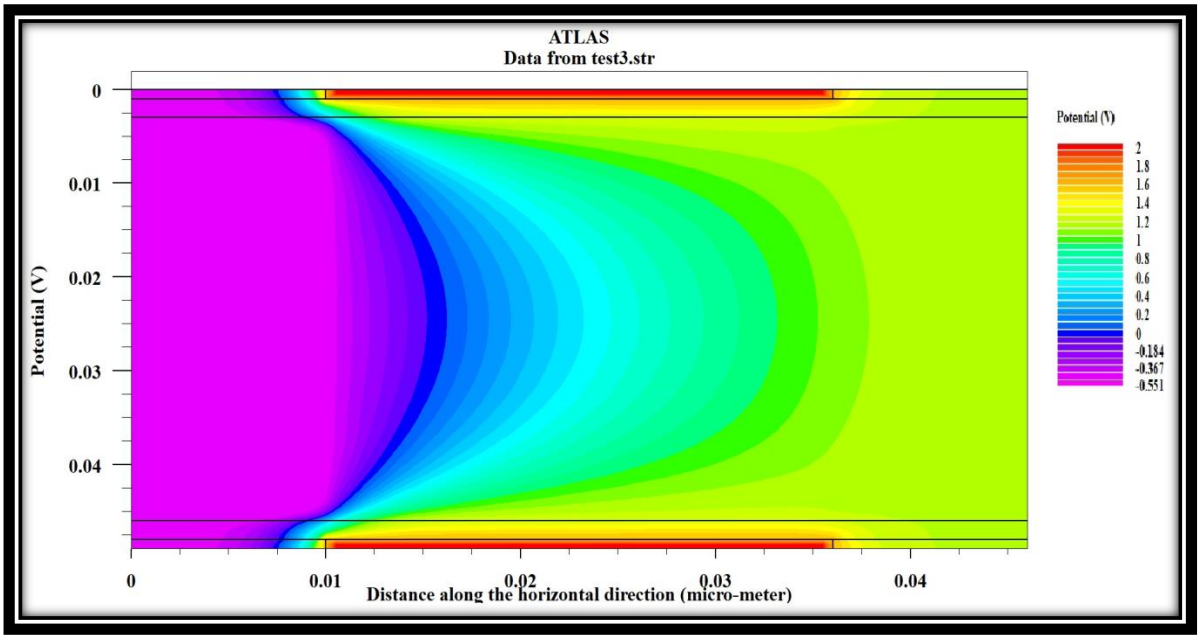
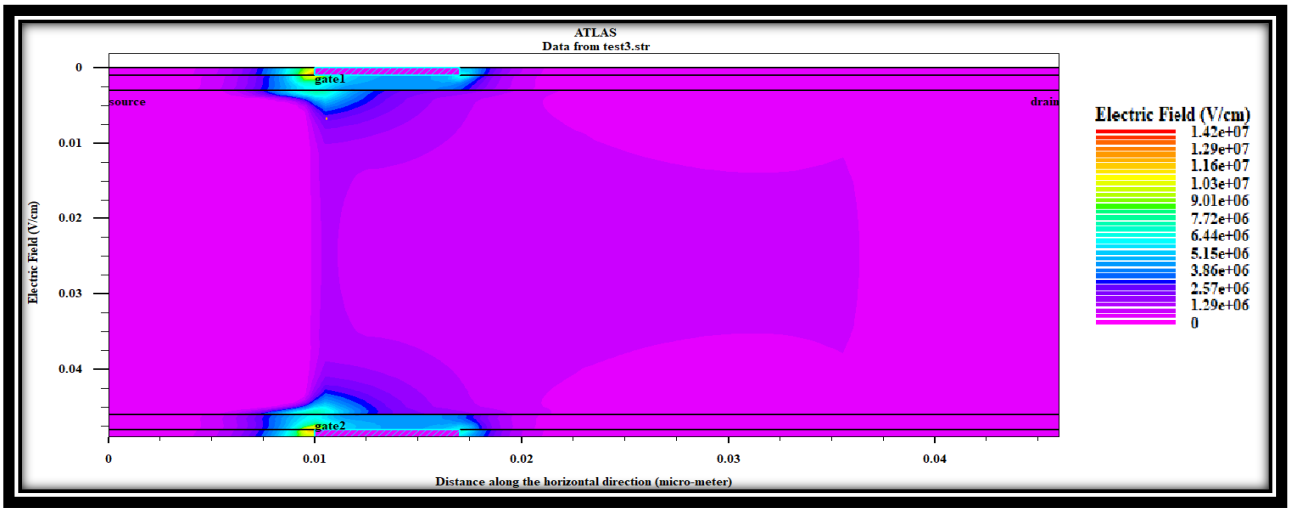


(c)

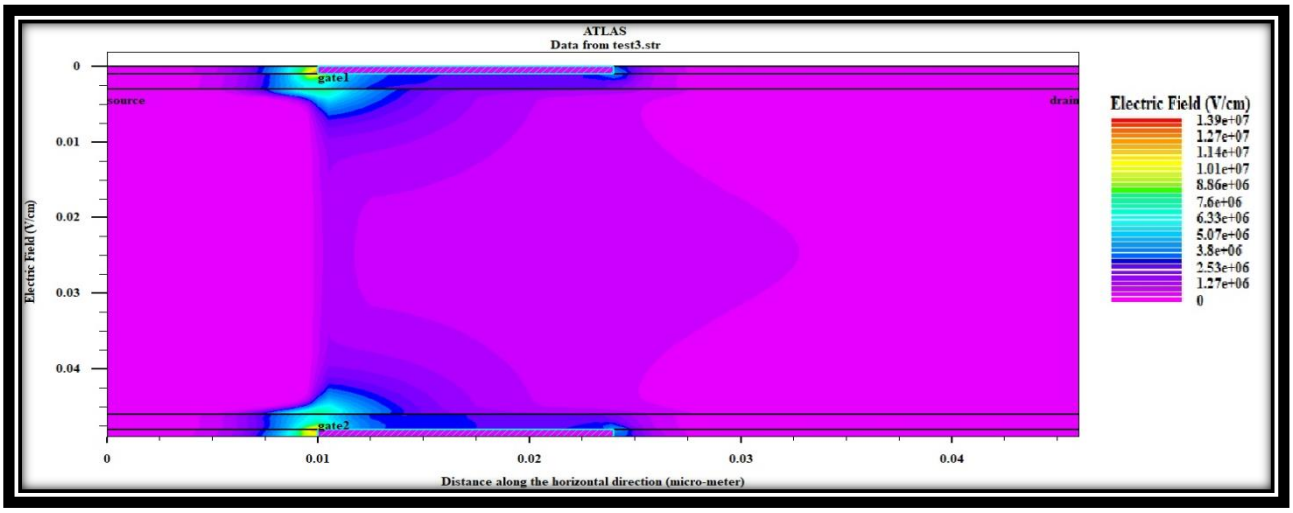
Figure 3.2 : Potential distribution of the proposed CA-PNPN-DG TFET structure for (a) 7nm, (b) 14nm and (c) 24nm gate length.

The electric field profiles for various gate lengths have been delineated in Fig.3. For a gate length of 14nm and 24nm, the electric field is non-uniform in the channel which is obvious from

the distribution curvature in Fig.3.3 (b) and Fig.3.3 (c). Besides that two symmetrical zero electric field regions are shaped towards the drain side of the channel for these two cases. Considering Fig.3.3 (a) 7nm gate length structure, it is noticeable that the electric field is uniform at the channel side and the zero field areas are practically missing.



(a)



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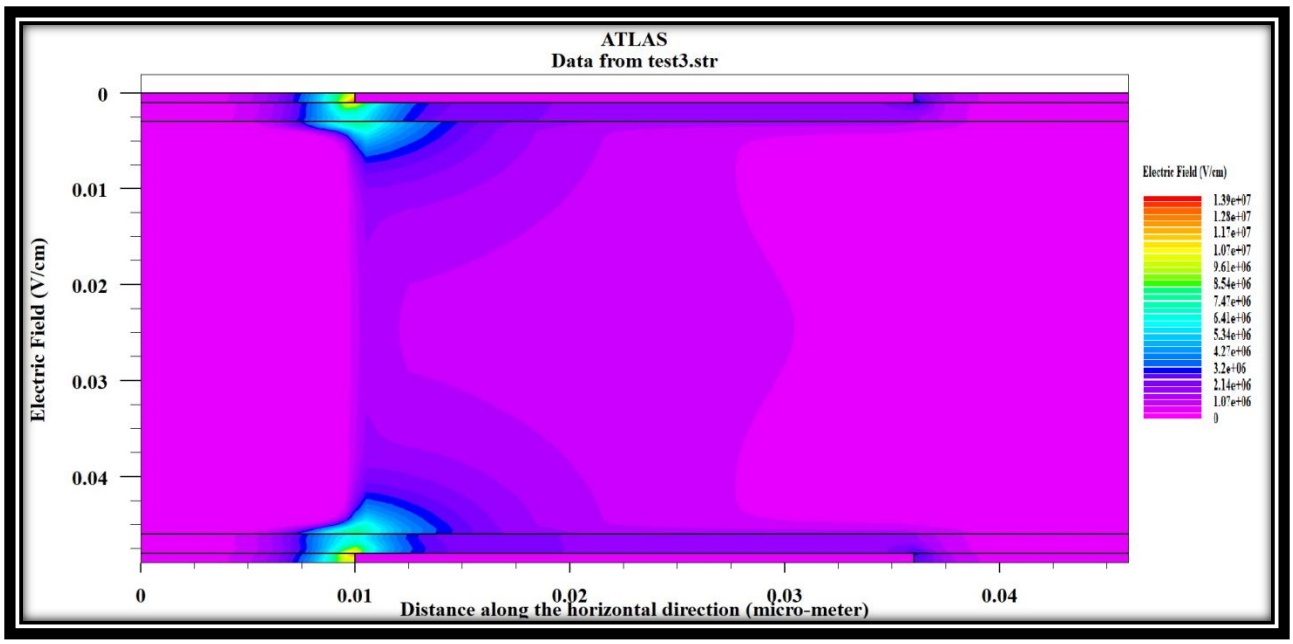

(c)

Figure 3.3: Electric field distribution of the proposed CA-PNPN-DG TFET structure for (a) 7nm, (b) 14nm and (c) 24nm gate length.

3.3.2 Potential Profile

The Potential Profile along the length of the PNPN-DG TFET for 7nm, 14nm and 24nm gate lengths have been portrayed in Fig.3.4.

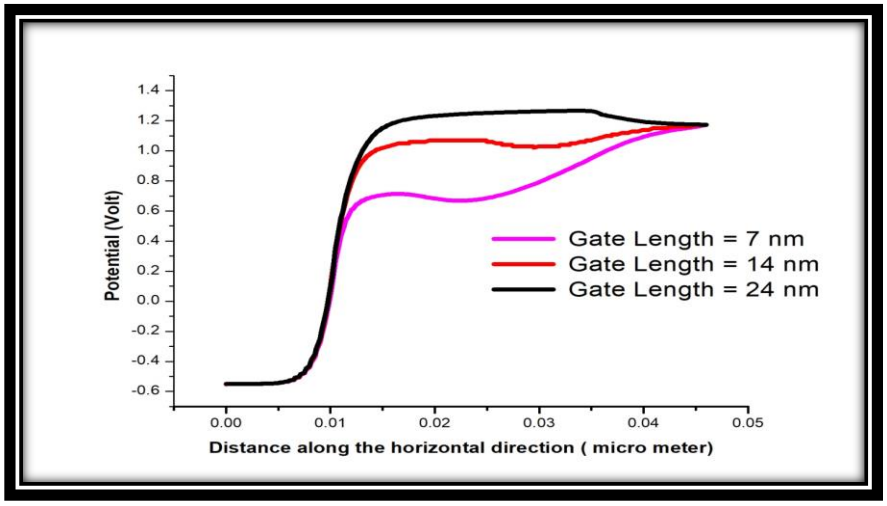

Figure 3.4: Potential Distribution along the length of the proposed CA-PNPN-DG TFET structure for (a) 7nm, (b) 14nm and (c) 24nm gate length

3.3.3 Electric Field

The electric field along the length of the PNPN-DG TFET for 7nm, 14nm and 24nm gate lengths have been portrayed in Fig.3.5. The high electric field at the source channel intersection clarifies the tunnelling phenomena while the expansion of electric field at the channel-drain intersection exhibits that the electrons from drain side cannot pass to the channel. Thus diminishing the ambipolarity of the device.

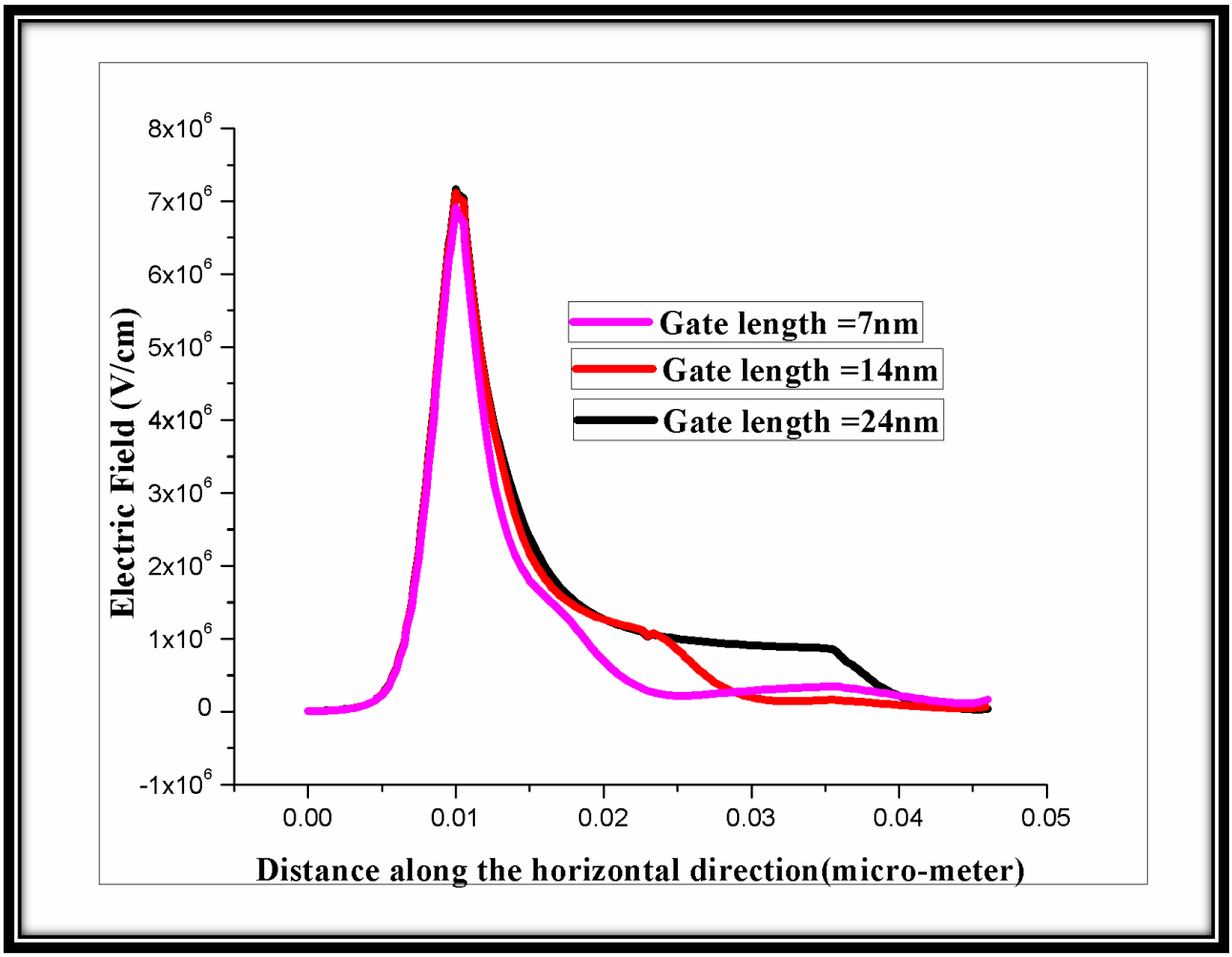

Fig 3.5: Electric field along the length of CA-PNPN-DG TFET for 7nm, 14nm and 24nm gate lengths.

3.3.4 Band Diagram Analysis

The correlation of conduction and valence bands for the structures with three diverse gate lengths is represented in Fig.3.6.It can be noticed from the diagram that the tunneling is practically comparative for the three cases, however, 7nm gate length structure displays reverse band bending at the channel-drain junction which shows the reason for decreased ambipolar conduction for the resultant structure. Likewise, it is clear that valence and conduction bands are getting parallel to one another along the drain region which invalidates the further plausibility of ambipolar conduction.

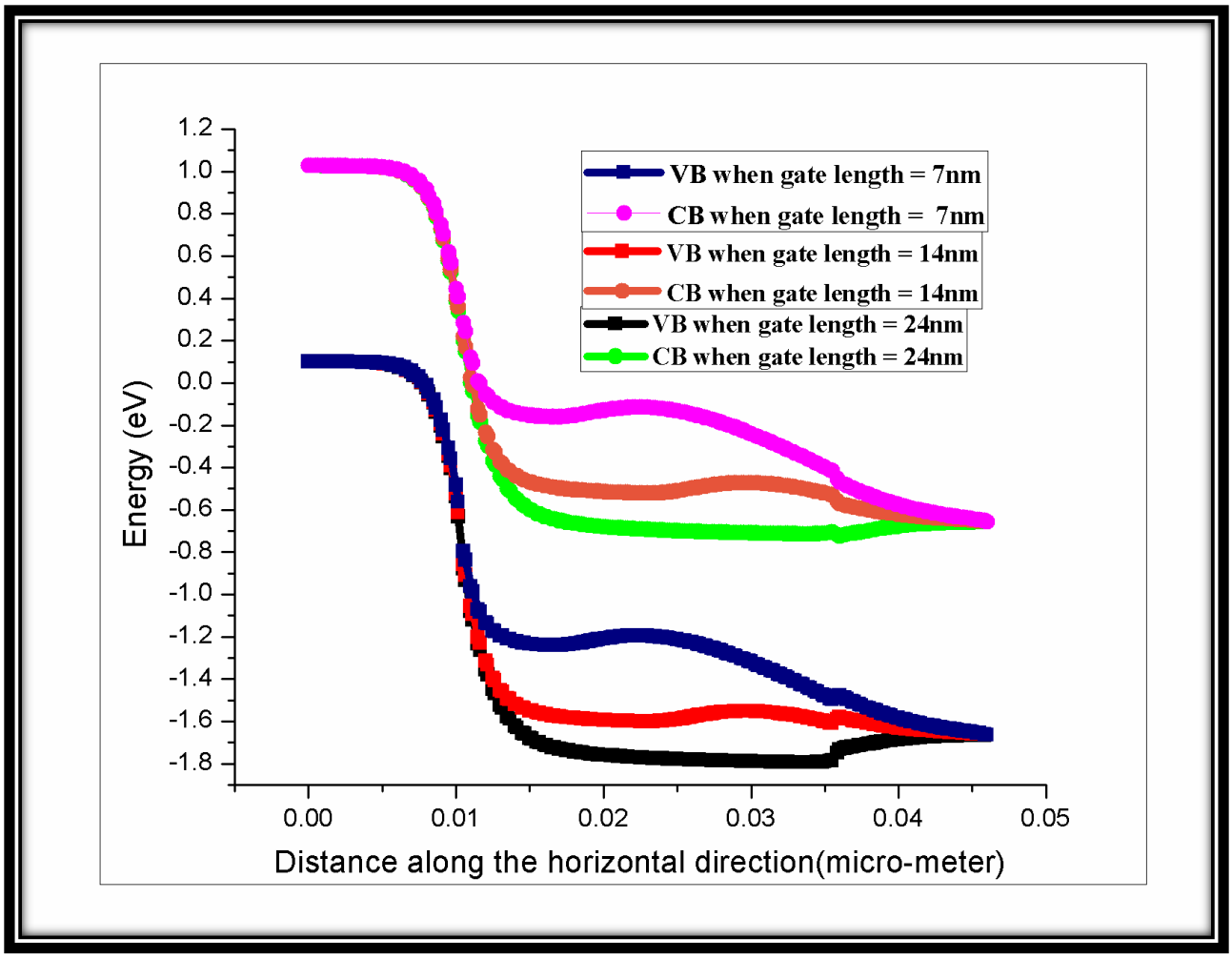

Fig 3.6: Comparison of valence and conduction band energy for 7nm, 14nm and 24nm gate lengths.

3.3.5 Band to Band Tunnelling Rate Analysis

Comparison of BTBT tunnelling rate for PNPN-DG TFET of three different gate lengths 7nm, 14nm and 24nm have been illustrated in Fig.3.7. The curves of 14nm and 24nm have been completely overlapped showing the same rate of band to band tunnelling whereas the 7nm gate length curve shows better tunnelling rate to some extent at the source channel junction.

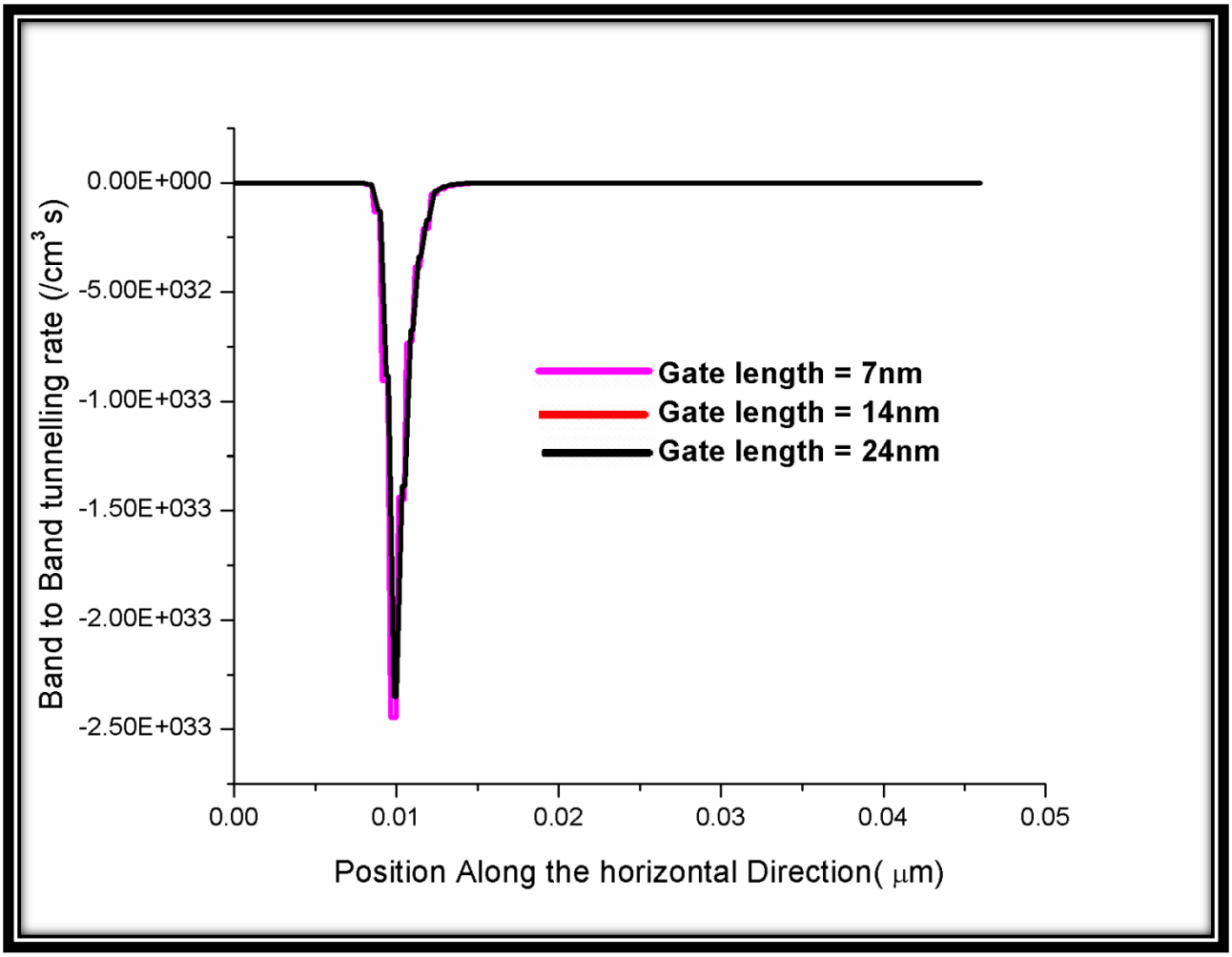

Figure 3.7: Band to Band Tunneling rate of the proposed CA-PNPN-DG TFET structure for (a) 7nm, (b) 14nm and (c) 24nm gate length.

3.3.6 Transfer Characteristics Analysis

The transfer characteristics of CA-PNPN-DG TFET for three diverse gate lengths of 7nm, 14nm and 24nm have been illustrated in Fig 3.8. The structure with the minimum gate length of 7nm displays OFF current of the order of 10-16 to 10-17. It illustrates that the smaller gate length upgrades the execution of the device and henceforth 7nm structure is the best among the three considered in this work.

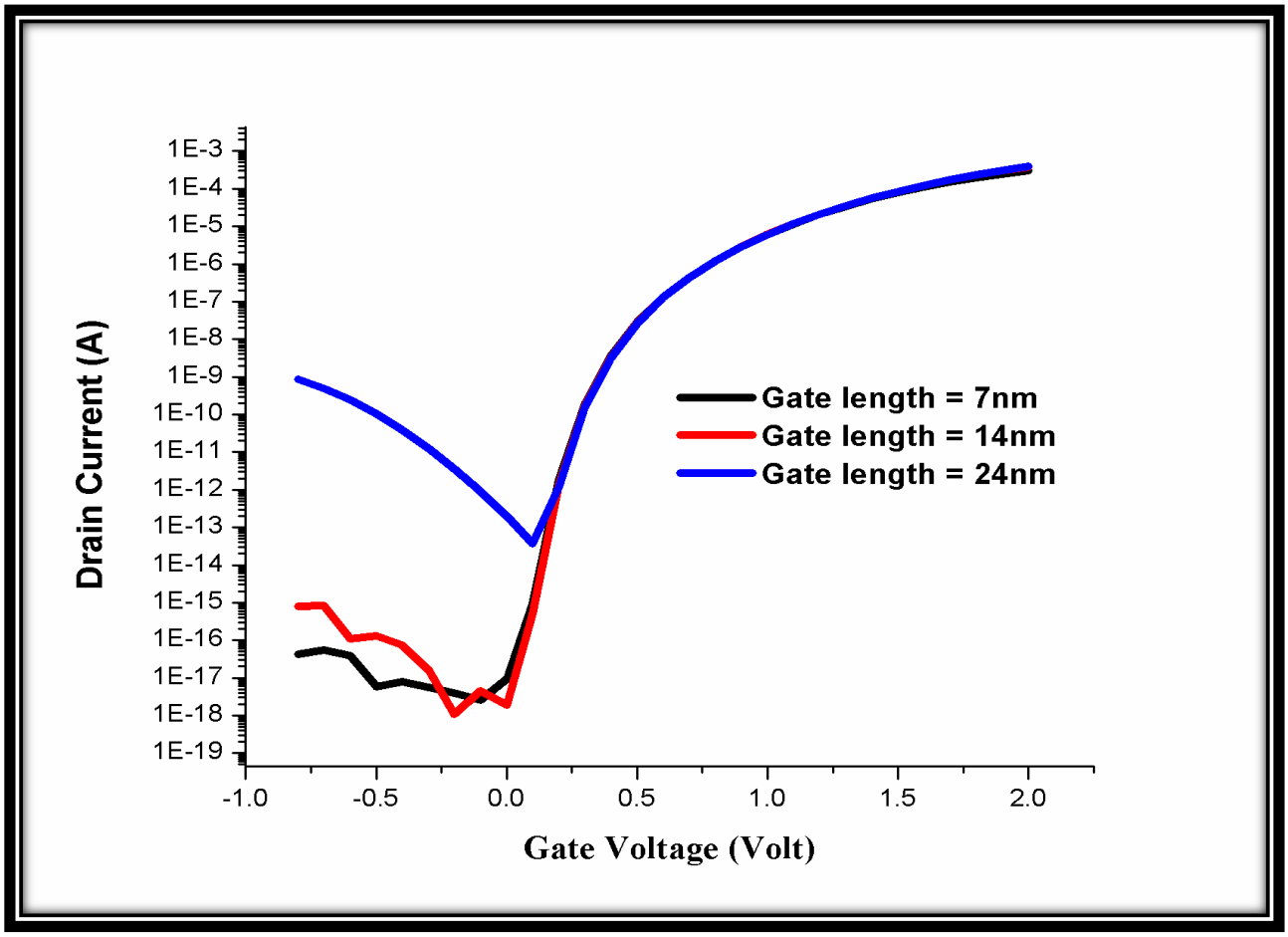

Figure 3.8: Transfer Characteristics of CA-PNPN-DG TFET for 7nm, 14nm and 24nm gate lengths.

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CHAPTER 4:
Centrally Aligned PNPN-DG TFET- A Quantum Confinement Based Approach

4.1 Overview and proposed work

Tunnel field effect transistors are being extensively studied due to their excellent sub threshold behavior and low power applications [1-5].At the same time scalability is the need of the hour in semiconductor industry. Quantum confinement [6] needs to be taken care of in scaled devices having dimensions in the range of 15 to 20 nm. In this work, an attempt has been made to incorporate quantum confinement in CA-PNPN-TFET (centrally aligned TFET) based on non-local tunneling model along with self-consistent Schrodinger-Poisson quantum model. Quantum confinement is considered in 1-D. As a result effective band gap and subsequent tunneling barrier width is increased [7]. Hence the results obtained through quantum approach are more practical than semi-classical ones.

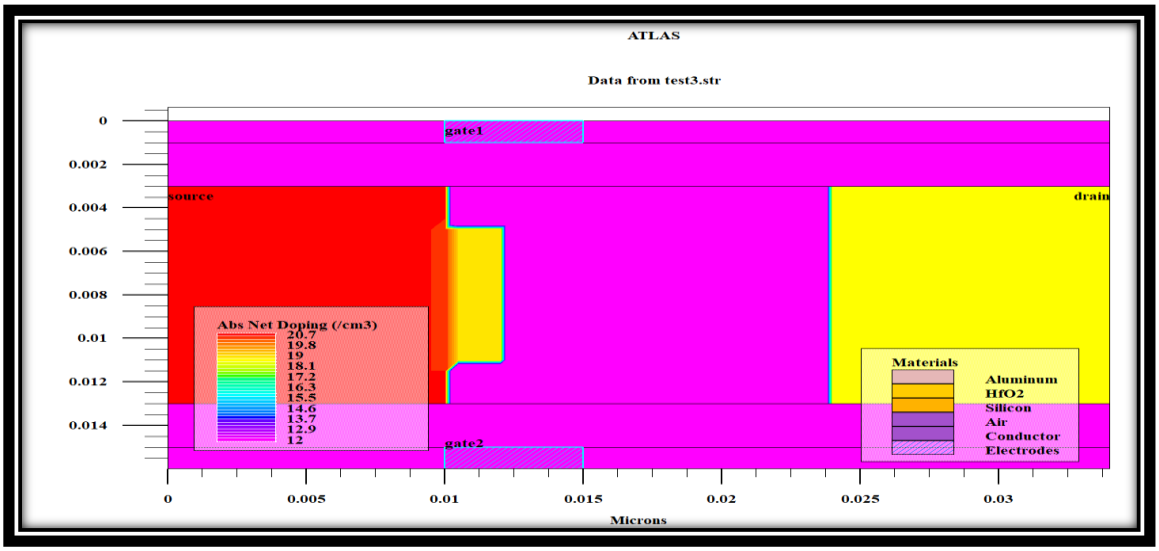
4.2 Device structure and optimized parameters:

The 2-D cross-sectional perspective on the p-channel TFET structures[8-11] with absolute net doping profile are given in Fig.4.1 utilizing Silvaco Atlas. The structure contains centrally aligned Source Pocket region [12] that is absent in a traditional TFET. This is a heavily doped region. The specific doping concentration of the TFET models are given a table below which are kept constant for all the simulations. Such doping fixations create a tunnelling junction between source and channel where the phenomenon of interband tunnelling can happen.

The simulated device has a total length of 34nm and vertical dimension of 16nm. The gate length is varied to 5nm, 7nm and 14nm. But the effective channel length is examined to be

14nm. The lateral and the vertical dimensions for both the Source and Drain regions are 10nm and 10nm, respectively. The Pocket Region has a lateral and vertical dimension of 2nm and 6nm respectively.

Hafnium oxide(HfO2) is used as a gate dielectric and the source and the drain contacts are considered to be in vertical direction on the two opposite sides of the proposed structure.



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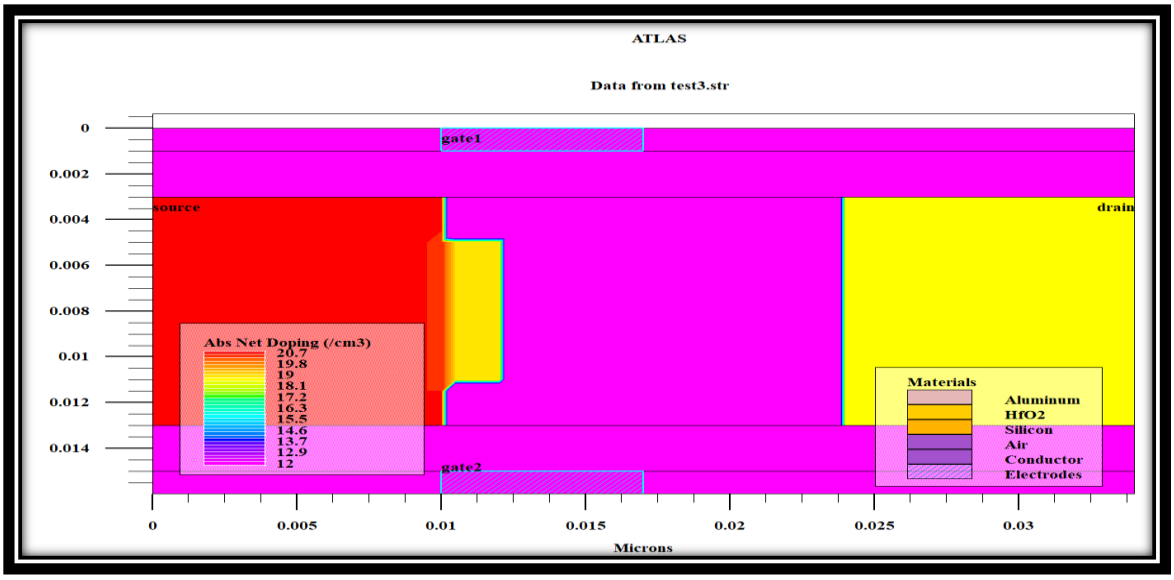

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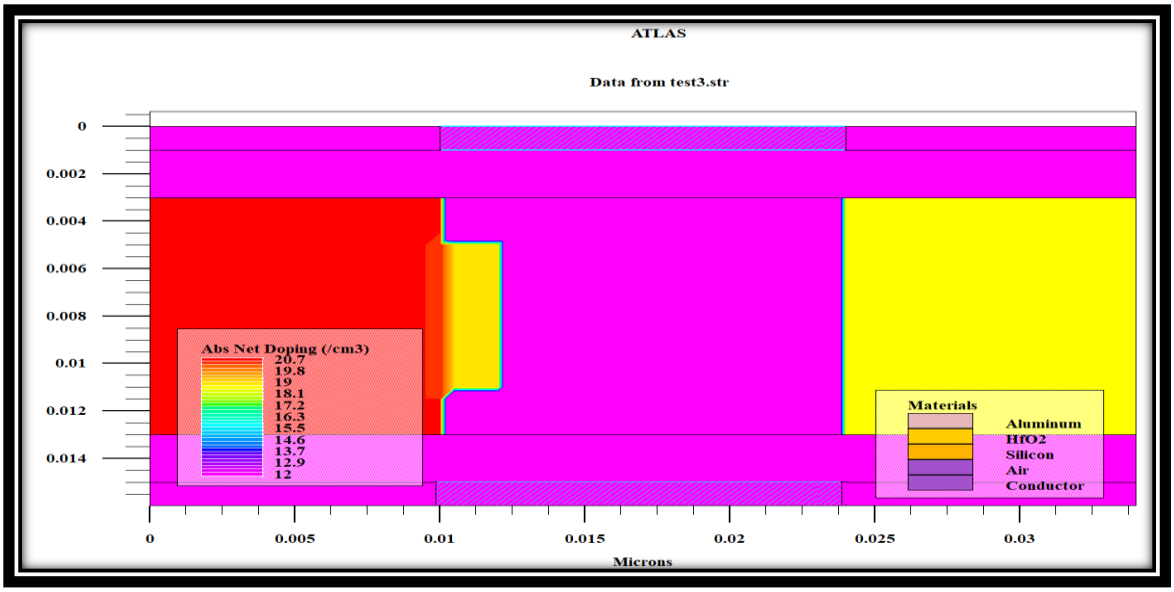


(c)

Figure 4.1. 2D cross sectional view of CA PNPN-TFET with gate length (a) 5nm (b) 7nm (c) 14nm

Table 4.1

Doping concentration of different regions

Region	**Doping type**	**Doping Concentration (/cm^3)**
Source	p-type	$1 * 10^{20}$
Drain	n-type	$1 * 10^{18}$
Channel	p-type	$1 * 10^{12}$
Pocket	n-type	$1 * 10^{19}$

4.3 Results and Discussions

Several comparisons are done in this study. Those are provided in the following sections.

4.3.1 Comparison of sub threshold slope for different drain to source voltage

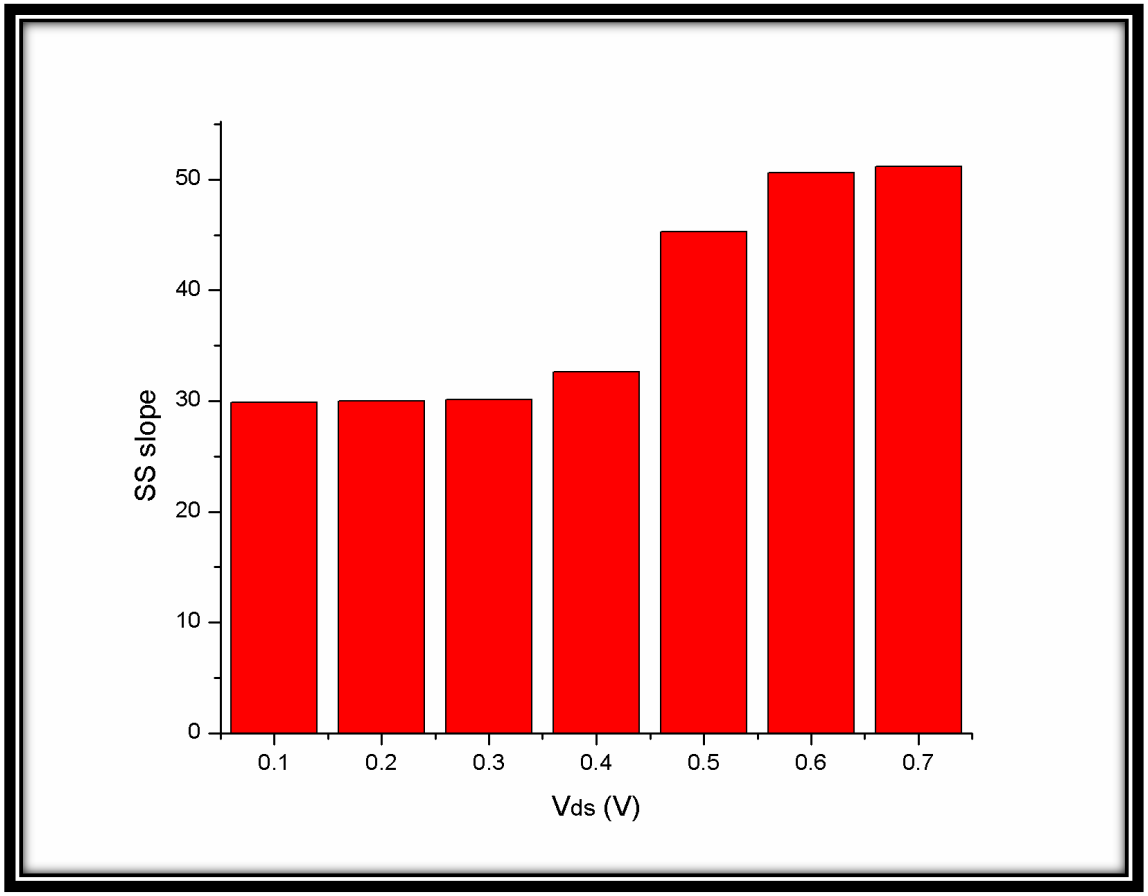


Figure 4.2 Sub threshold slope for different drain to source voltage

We choose 0.2 v as a V_{ds} and it remains constant throughout the experiment.

4.3.2. Comparison of transfer characteristics for different gate length

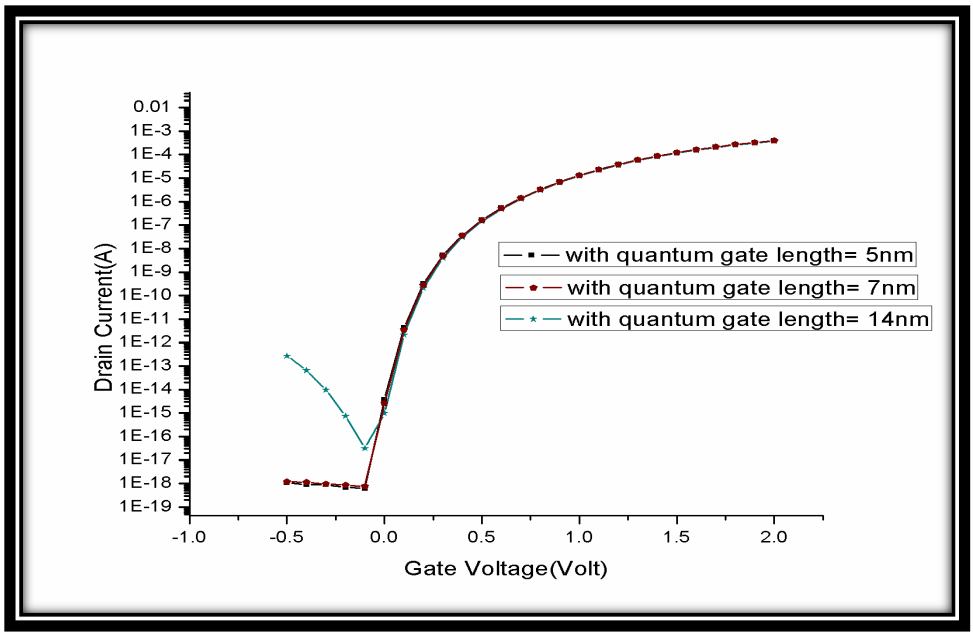


Figure 4.3. Transfer characteristics comparison for different gate length

From fig. 4.3.we can see that current remains almost same once we incorporate quantum model. Only performance based on ambipolarity is degraded, that too is negligible. From this curve we can come to the conclusion that this device has excellent scalability. Quantum confinement consideration reduces the BTBT rates due to energy band discretization, thereby lowering the subthreshold swing. This is clearly observed from the graphs.

4.3.3 Comparison of transconductance

Transconductance is one of the most important parameters in device physics. A comparison chart of transconductance with the variation of gate length is provided in table 4.2.

Table 4.2.

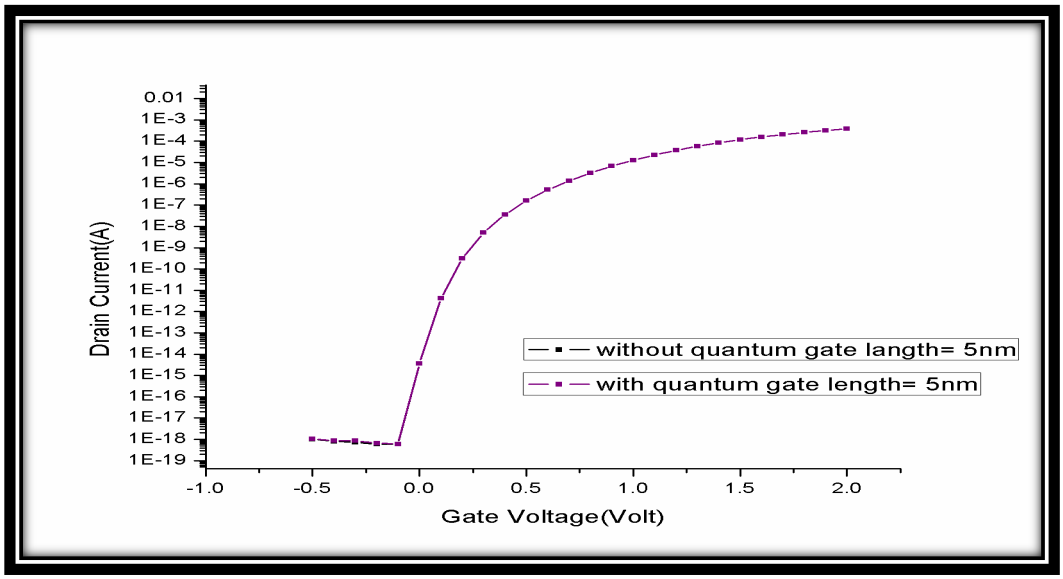
Comparison of transconductance

Gate Length(nm)	**Transconductance (siemens)**
5	2.39×10^{-15}

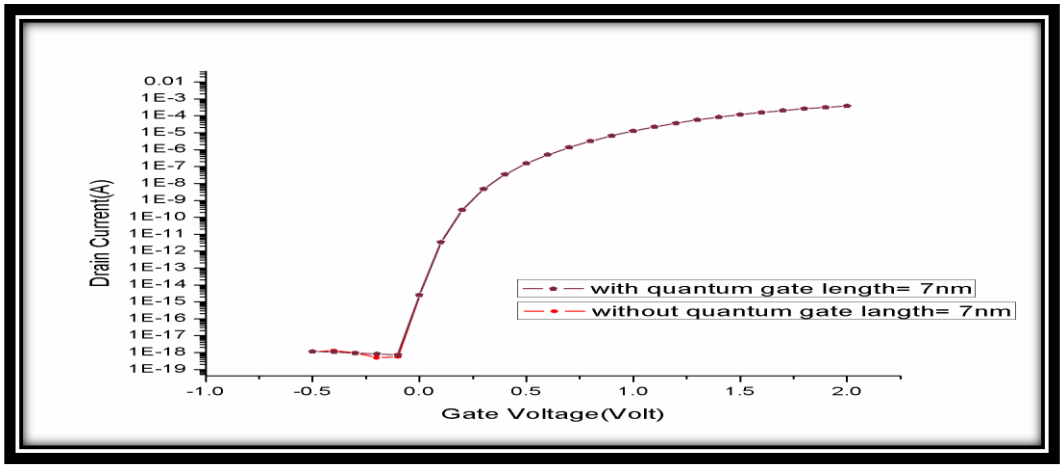
7	1.84×10^{-15}
14	2.09×10^{-15}

We can see from the table 4.2 that we have got better result for the gate length 5nm.

4.3.4 Difference with Semi-classical model



(a)



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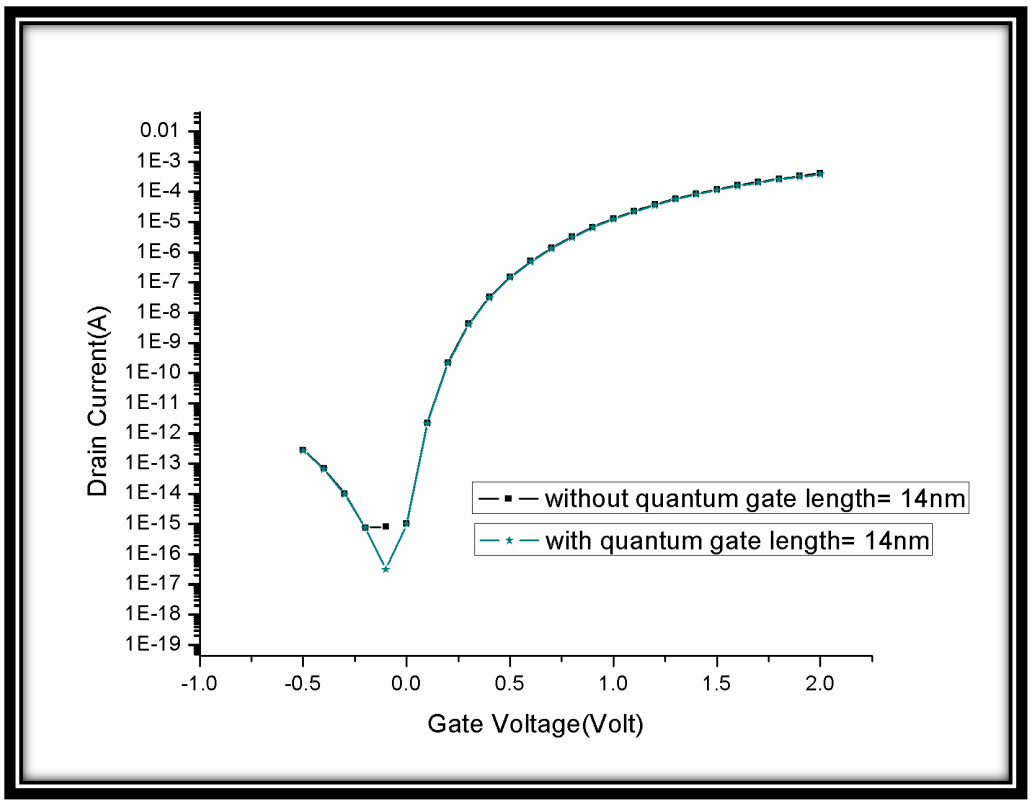

(c)

Figure 4.4. Comparison of quantum model with standard semi-classical model (without quantum model)

From fig. 4.4. it is clearly understood that in quantum model the slope is little bit more than the standard one. This result is quite natural because we are moving towards practical implementation of device. Output characteristics will differ naturally from the ideal case because now we are considering sub band quantization and this deviation is acceptable.

4.3.5. Electric Field and Potential Profile

Electric Field and potential curve of the proposed structure is shown in fig. 4.5. and fig. 4.6. respectively. The peak in electric field noticed for gate length 14nm is indicative of better overall tunneling and hence, increased ON-current in this case. The peak in the potential profile at the source-channel interface is indicative of the overall tunneling. Higher value of potential at the channel-drain interface indicates that the electrons which tunnel at the source-channel interface effectively reach the drain.

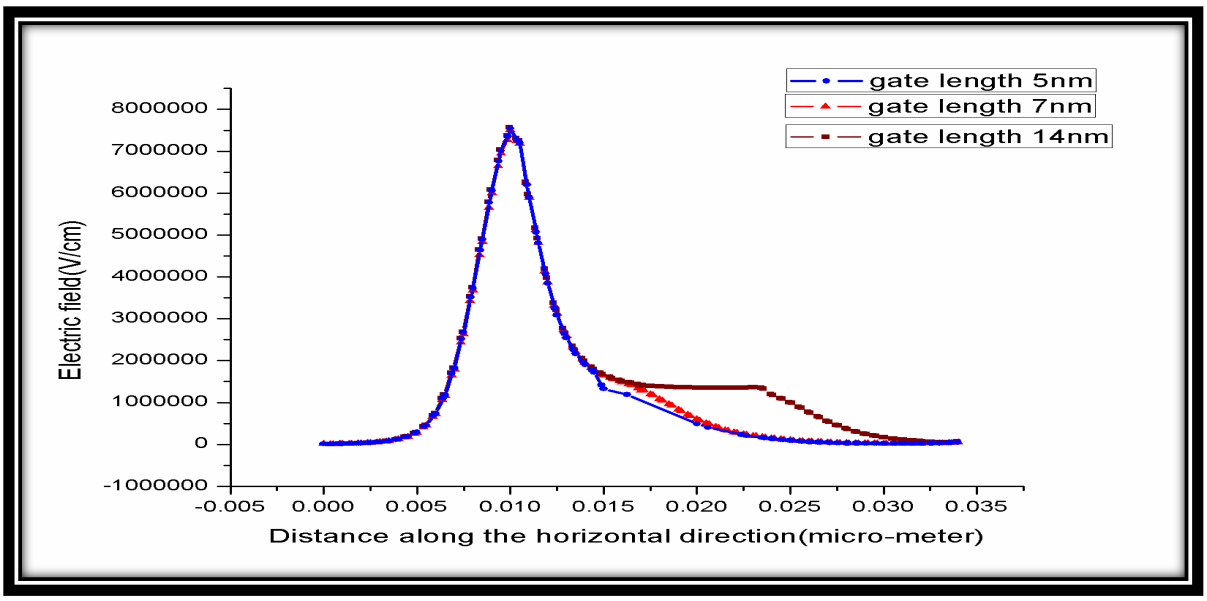

Figure 4.5.Electric Field

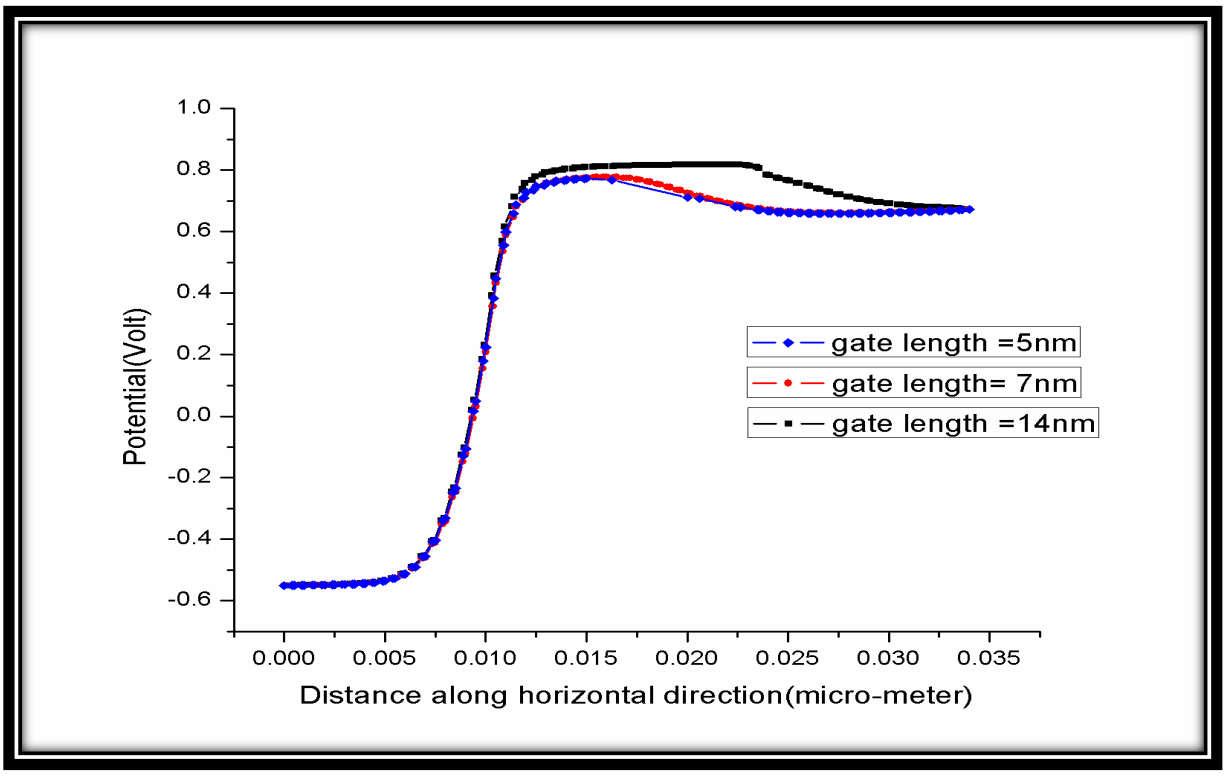

Figure 4.6. Potential curve

The electric field distribution and electron concentration for the gate length 14nm are shown in figure 4.7 and figure 4.8

Owing to extensive scaling, in the present nanodevice scenario, a phenonmena known as quantum[13] confinement effect (QCE) has become more pronounced. In this phenomena, the enrgy band structure is altered under the influence of ultra-low length scale. For group IV, II-V and II-VI, the length scale between 1 to 5 nm corresponds to the pronounced quantum confinement regime. Such low dimensions impose geometrical constraints on the electrons. In particular, as the particle size approaches the Bohr exaction radii, the QCE becomes more pronounced. Thus, in QCE the continuous energy bands of the bulk material collapse into discrete energy levels. The QCE in the proposed structure was visualized by employing the self-consistent Schrödinger-Poisson (SP) model on Silvaco, Atlas. Due to energy band discretization, the conduction band-valence band overlap region gets significantly reduced at the source channel junction resulting in greater tunneling length. This reduces the extent of BTBT significantly.

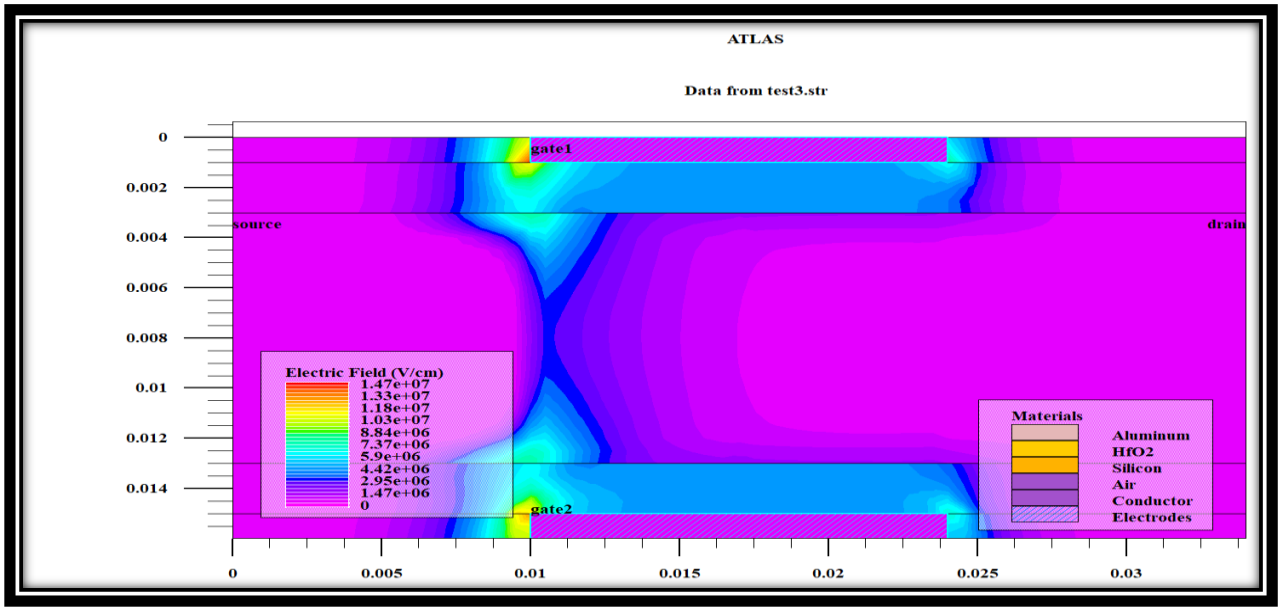

Figure 4.7. Electric field distribution for the gate length 14nm

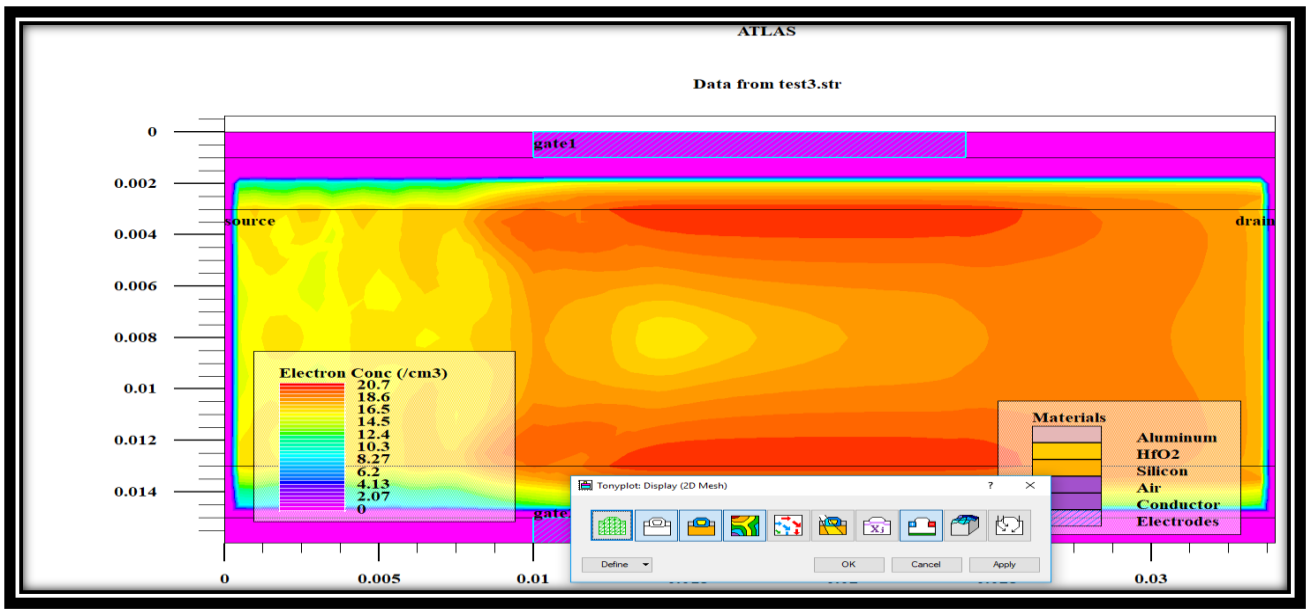

Figure 4.8. Electron Concentration for the fate length 14nm

References

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CHAPTER 5:
Demonstration of Stepped-Tunnel Phenomena in U-Shaped Tunnel Field Effect Transistor

5.1 OVERVIEW AND PROPOSED WORK

Conventional MOSFET structures have several drawbacks in the nanoscale range which have been compensated by TFET devices [2-4]. The fundamental phenomena upon which TFET is based is quantum mechanical Band-to-Band Tunneling (BTBT) as opposed to carrier In this paper we have proposed a novel U-shaped TFET structure based on channel engineering, which has been experimentally demonstrated and investigated. This structure offers several advantages over the conventional planar TFET in terms of reduced OFF-state current and hence suppressed ambipolar [1] conduction. Four U-shaped channel structures have been simulated and named according to the materials used: (a) Silicon-Gallium Arsenide-Silicon U-shaped Channel TFET SGS-UC-TFET, (b) Gallium Arsenide-Silicon-Gallium Arsenide U-shaped Channel TFET GSG-UC-TFET, (c) Silicon-Silicon-Silicon U-shaped Channel TFET SSS-UC-TFET and (d) Gallium-Gallium-Gallium U-shaped Channel TFET GGG-UC-TFET . All the fundamental device parameters have been analyzed to demonstrate the tunneling phenomena in the U-shaped channel based TFET structure under various biasing conditions[2]. All the simulations have been performed using Silvaco,Atlas.transport by thermionic injection in MOSFETs. The subthreshold swing of a TFET is less than 60mV/decade at room temperature, a value that cannot be achieved in MOSFETs. Also steeper

switching behavior in TFETs makes this device suitable for high speed and low power applications. TFET is immune to short channel effects and show very low leakage currents in the range of femto amperes (fA) making it suitable for high frequency applications.

Despite the inherent merits of TFETs the primary area of concern in TFETs is ambipolar conduction, which arises due to BTBT at the drain-channel junction. Also the ON current is considerably low as compared to MOSFETs. To suppress the ambipolar conduction, various structures have been previously demonstrated. These include gate–drain underlap structure, [5]-[8] which lowers the ambipolar conduction considerably although it reduces the current driving capacity in the process and other drain doped engineering approaches [9-14]. In this work, we have opted for a channel engineered U- shaped TFET to suppress ambipolar conduction. The channel engineering is obtained by using different combinations of semiconductor materials for the source, channel and drain materials along the U-shaped channel. The electric field profile has been studied to show reverse band bending in the drain-channel interface. This has the effect of greatly reducing the tunneling probability at the drain end of the structure and hence ambipolar conduction can be effectively suppressed. The OFF current is in the range of 10^{-18}A, thereby offering high I_{ON}/I_{OFF} and hence reduced subthreshold swing. The structures have been named according to the corresponding materials used in the source- channel-drain regions respectively, (a) Silicon-Gallium Arsenide-Silicon U-shaped Channel TFET SGS-UC-TFET and (b) Gallium Arsenide-Silicon- Gallium Arsenide U-shaped Channel TFET GSG-UC-TFET. After analyzing the effects of varying the gate bias and oxide permittivity on the band diagram and other parameters like electric field and potential, we have reported the ramifications of the structure and the materials used for optimal evaluation of desired and undesired characteristics.

5.2 DEVICE STRUCTURE AND SIMULATION SETUP

The 2-D cross-sectional view of the U shaped intrinsic- channel TFET structure with absolute net doping profile are shown in Fig.5.1, for the two structures: (a) Silicon-Gallium Arsenide-Silicon U-shaped Channel TFET (SGS-UC-TFET) and (b) Gallium Arsenide-Silicon- Gallium Arsenide U- shaped Channel TFET (GSG-UC-TFET), using Silvaco, Atlas.

The oxide region is composed of HfO_2-HfO_2-SiO_2 as shown in the Fig5.2.

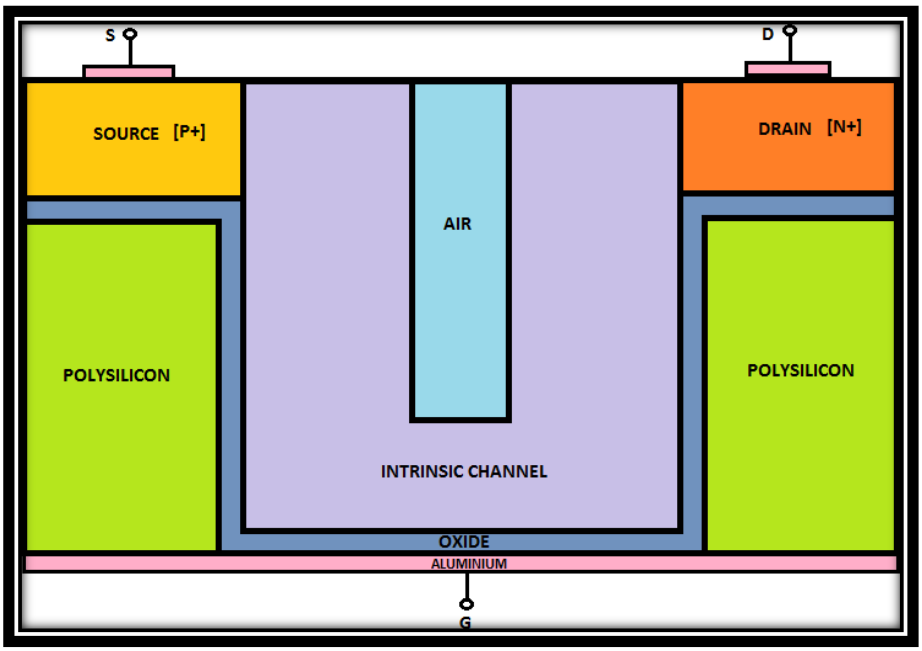

Figure 5.1: Basic structure of the U-shaped channel TFET

The doping profile of the TFET models are: P type source region (5×10^{21}cm−3), intrinsic channel region and N doped drain region (5×10^{18} cm−3) which are kept constant for all the simulations. The total lateral length of the device is 110nm and simulated with lateral dimensions of 30nm, 30nm, for source and drain respectively. The vertical dimensions of source and drain are 20nm and 20nm respectively. The dimensions of U shaped channel are 20nm-50nm-20nm on lateral side and 76-nm-56nm-76nm on vertical side. The thickness of the oxide layer is 3 nm and it runs along the channel from the drain end to the source end. There are three combinations of oxide materials used in the structures as mentioned above. All the simulations have been performed using Silvaco Atlas version 5.20.2.R by including appropriate models such as Lombardi mobility model (CVT), nonlocal BTBT (BBT.NONLOCAL), Auger recombination models, bandgap narrowing model, the Shockley–Read–Hall, Fermi–Dirac statistics, and Drift-diffusion carrier transport is used. The band structures have been demonstrated under various biasing conditions.

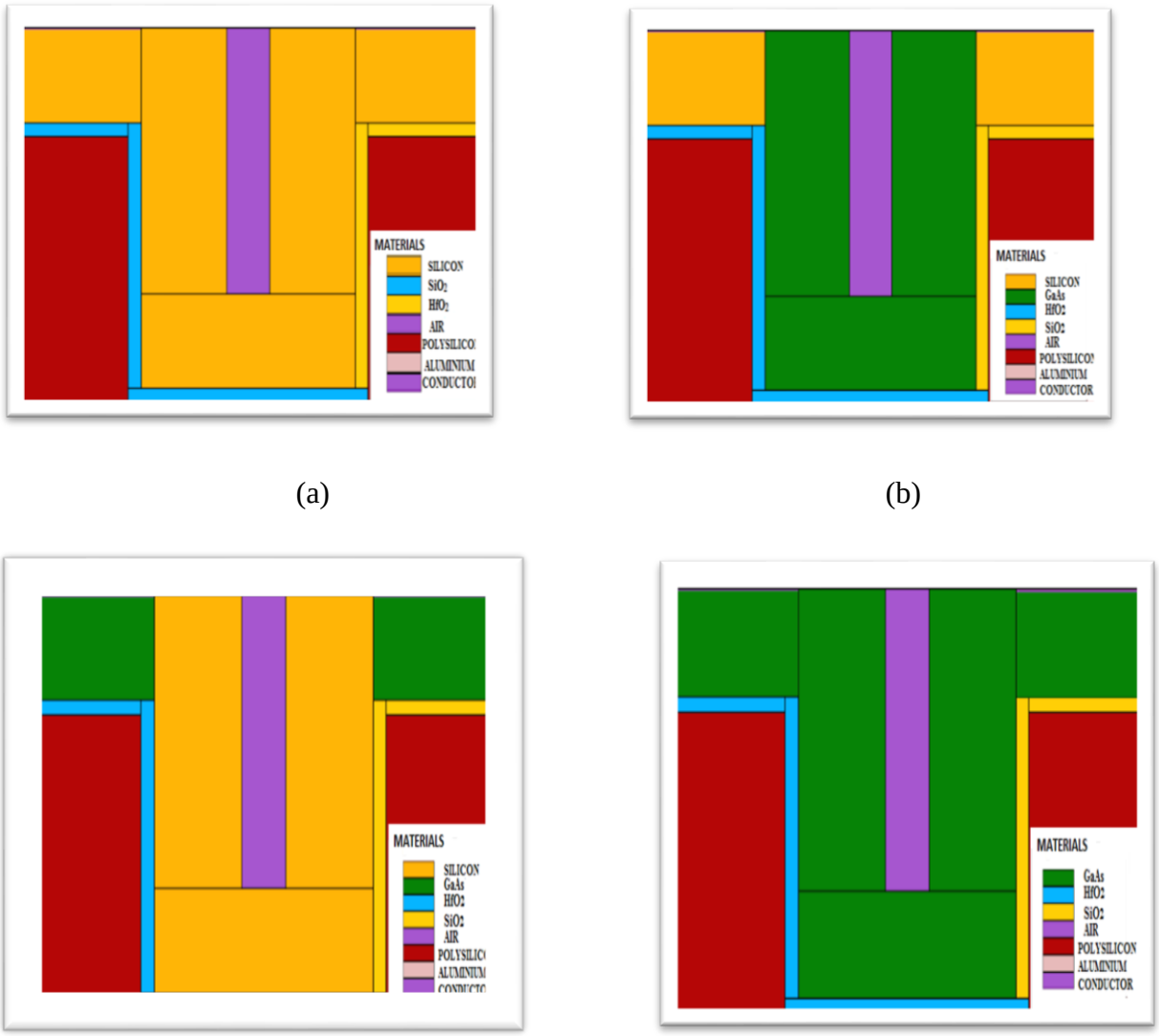

Fig.5.2. Structure for (a) Si-Si-Si U-shaped Channel TFET SSS-UC-TFET (b) Si-GaAs-Si U-shaped Channel TFET SGS-UC-TFET (c) GaAs-Si-GaAs U-shaped Channel TFET GSG-UC-TFET (d) GaAs- GaAs -GaAs U-shaped Channel TFET GGG-UC-TFET

5.3 RESULTS AND DISCUSSIONS

5.3.1 Band Diagram Analysis

Fig 5.3. shows the Band Diagram of the general structure in OFF-State. It can be clearly seen that no tunneling occurs at the source-channel interface when V_{gs} and V_{ds} are biased to OFF-state. Also, the reverse band bending at the channel-drain interface is an indicator of suppressed ambipolar current in the OFF-state. Fig 5.4. compares the band diagram of the (a) Silicon-Silicon-Silicon U-shaped Channel TFET SSS-UC-TFET (b) Silicon-Gallium Arsenide-Silicon U-shaped Channel TFET SGS-UC-TFET (c) Gallium Arsenide-Silicon- Gallium Arsenide U-shaped Channel TFET GSG-UC-TFET and (d) Gallium Arsenide- Gallium Arsenide- Gallium Arsenide U-shaped Channel TFET GGG-UC-TFET for maximum effective channel length of 202nm. The drain voltage is kept at 0.2V while the gate voltage is 0.5V. The simulation is performed for T=300K. The band structures suggest better tunneling profile, lower leakage and lower ambipolar conduction as compared to conventional planar TFETs. It is seen that the tunneling probability is lower at the source-channel interface for GSG-UC-TFET as compared to the other three structures as the tunneling length is higher. The reverse band bending at the channel-drain interface is more in SGS-UC-TFET . So, it can be concluded that this structure is more immune to ambipolar

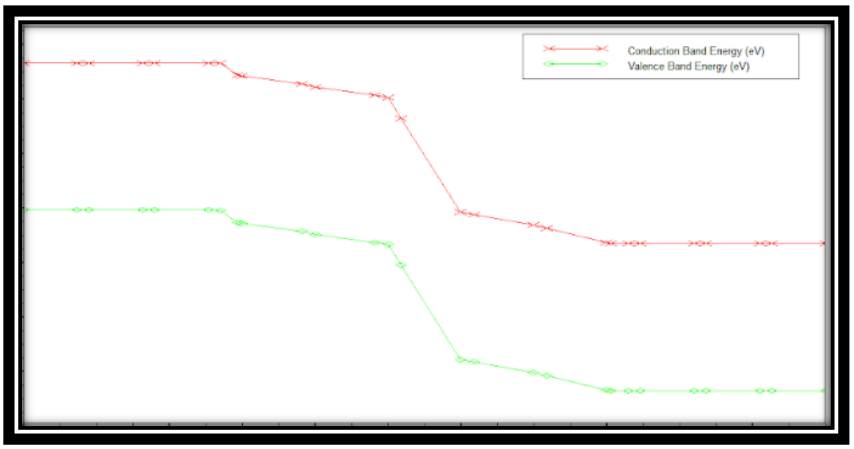

Figure 5.3. OFF-state band diagram of the proposed structure.

conduction as compared to the other three structures. The energy band diagram can be further optimized by modulation in dimensions of the structure and variation in the doping profile. The Fig 5.5.shows conduction band energy for the SGS-UC-TFET structure. The conduction band energy profiles of the other three structures are almost similar to the one in Fig 5.5. As expected the conduction band energy is highest at the source end, reduces at the source-channel interface and is lowest at the drain end.

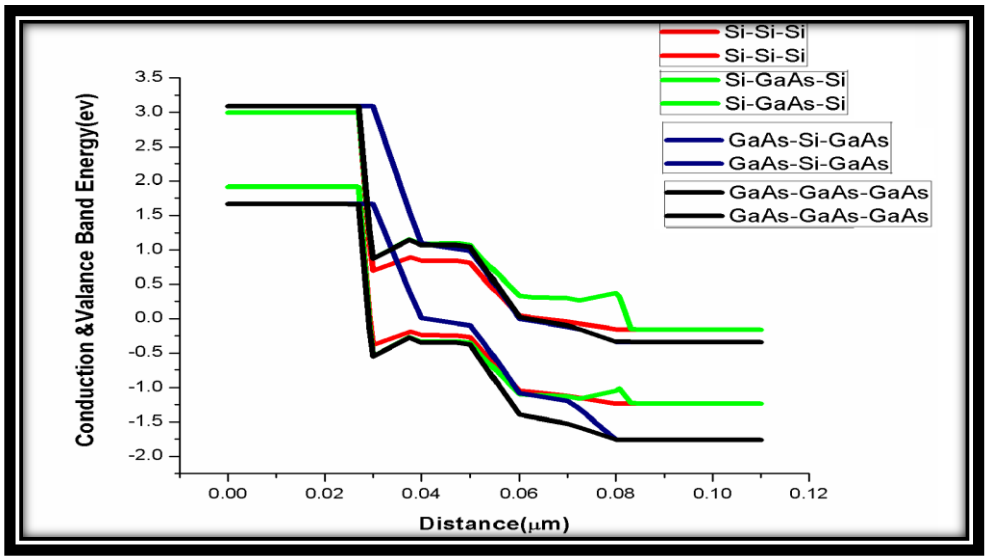

Figure 5.4. ON-state band diagram of (a) Silicon-Silicon-Silicon U-shaped Channel TFET SSS-UC-TFET (b) Silicon-Gallium Arsenide-Silicon U-shaped Channel TFET SGS-UC-TFET (c) Gallium Arsenide-Silicon- Gallium Arsenide U-shaped Channel TFET GSG-UC-TFET and (d) Gallium Arsenide- Gallium Arsenide- Gallium Arsenide U-shaped Channel TFET GGG-UC-TFET.

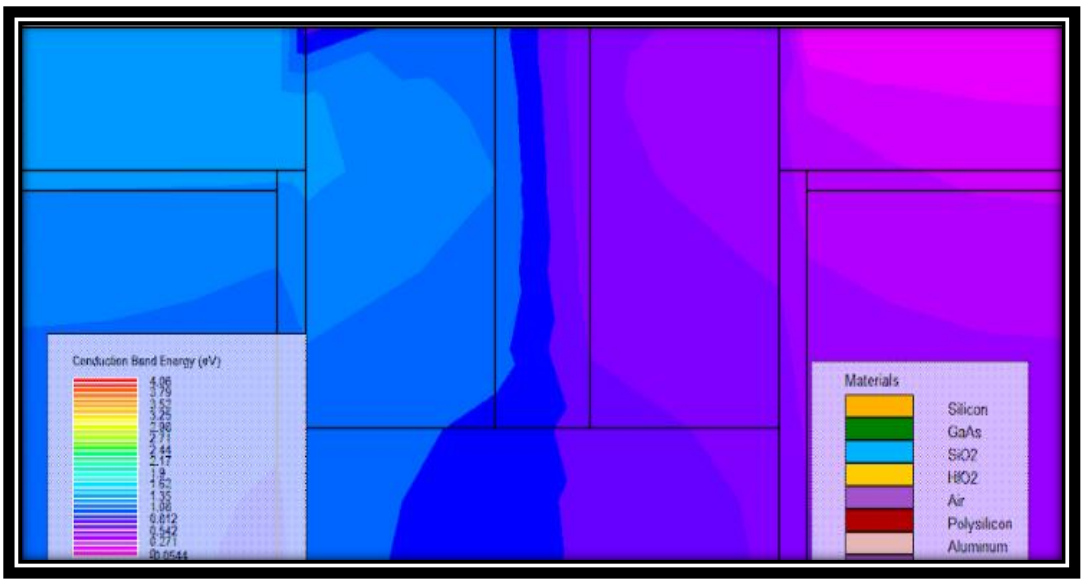

Figure 5.5. Conduction Band Energy for SGS-UC-TFET

We can see the dark blue is higher energy which is at the source channel interface it becomes light blue and then violet near the drain region.

5.3.2 Potential and Electric Field Profile Analysis

A comparative analysis of the potential profile is presented in Fig 5.6. for the four structures. The peak in the potential profile at the source-channel interface is indicative of the overall tunneling. It can be seen from the figure that overall tunneling is better for SSS-UC-TFET, SGS-UC-TFET and GGG-UC-TFET as compared to GSG-UC-TFET. Higher value of potential at the channel-drain interface indicates that the electrons which tunnel at the source-channel interface effectively reach the drain.

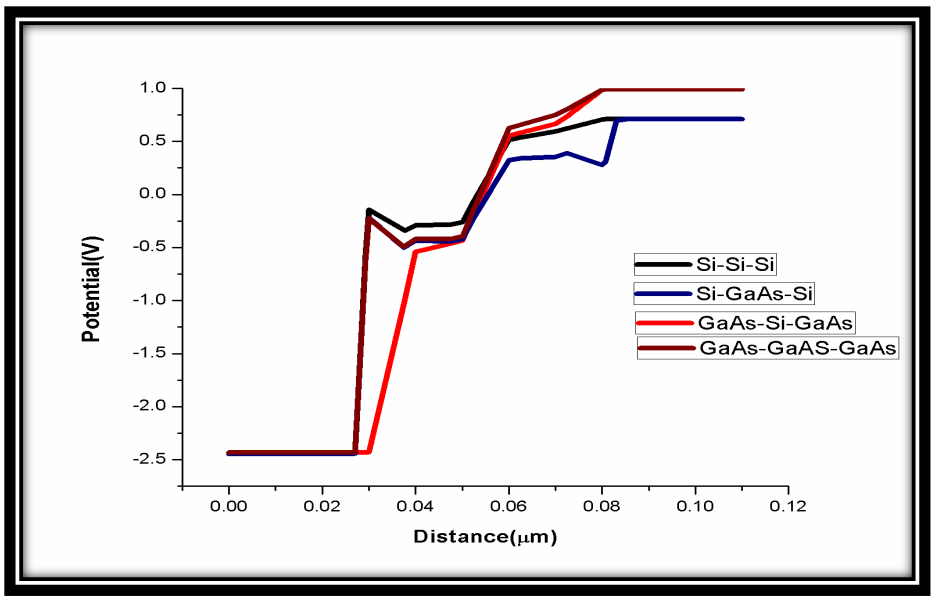

Figure 5.6. Potential Profile of (a) Silicon-Silicon-Silicon U-shaped Channel TFET SSS-UC-TFET (b) Silicon-Gallium Arsenide-Silicon U-shaped Channel TFET SGS-UC-TFET (c) Gallium Arsenide-Silicon- Gallium Arsenide U-shaped Channel TFET GSG-UC-TFET and (d) Gallium Arsenide- Gallium Arsenide- Gallium Arsenide U-shaped Channel TFET GGG-UC-TFET.

The electric field for all four structures are shown in Fig.5.7. Maximum overshoot at the source-channel interface is seen for SGS-UC-TFET suggesting highest degree of tunneling in this structure. The peak in the electric field profile at the channel-drain interface acts as barrier to reverse tunneling. This peak indicates immunity to DIBL. The peak of the electric field profile at the channel-drain interface is lower than that in the source-channel interface implying reduced hot carrier effect at the drain end. SGS-UC-TFET shows highest peak at the channel-drain interface and hence, is more immune to ambipolar conduction.

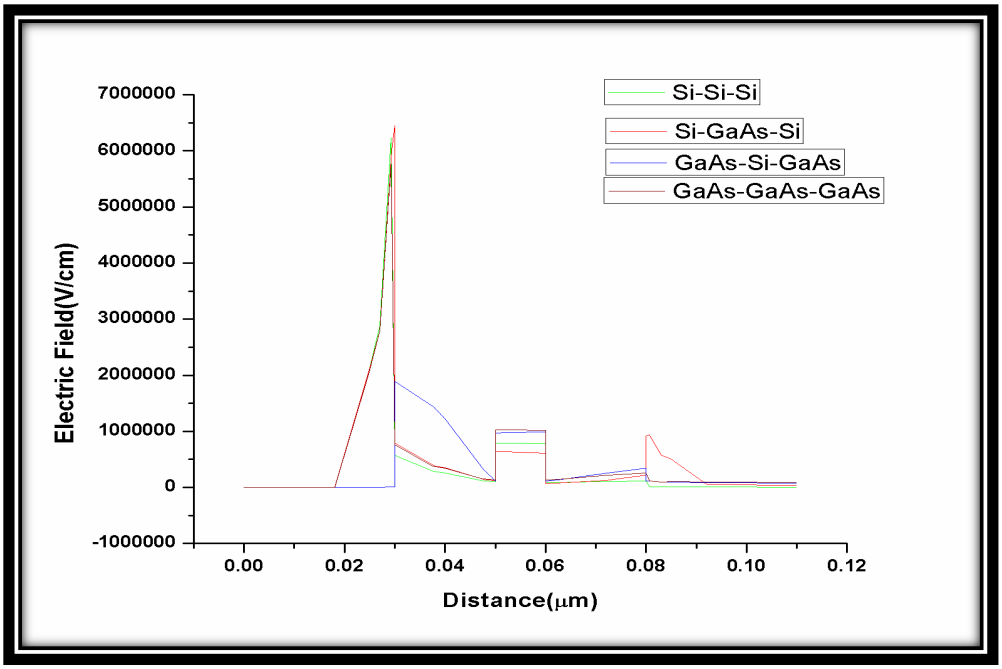

Figure 5.7. Electric Field Profile of (a) Silicon-Silicon-Silicon U-shaped Channel TFET SSS-UC-TFET (b) Silicon-Gallium Arsenide-Silicon U-shaped Channel TFET SGS-UC-TFET (c) Gallium Arsenide-Silicon- Gallium Arsenide U-shaped Channel TFET GSG-UC-TFET and (d) Gallium Arsenide- Gallium Arsenide- Gallium Arsenide U-shaped Channel TFET GGG-UC-TFET.

5.3.3 Electric and Potential Distribution

As expected, the electric field shows a peak at the source-channel interface as tunneling occurs in this region shown in Fig. 5.8. By the Fig.5.9 shows the potential profile of GSG-UC-TFET. The potential is highest at the drain end suggesting that all the tunneled electrons effectively reach the drain.

5.3.4 Electron Mobility Analysis

The electron mobility of the SGS-UC-TFET is depicted in Fig. 5.10. From this diagram it can be clearly seen that no tunneling occurs through the air region as the electron mobility is zero here and the flow of electrons is confined strictly within the U-shaped channel. Hence, the flow of carriers is controlled by the U-shaped gate. However, we have not considered quantum effect in

our analysis.

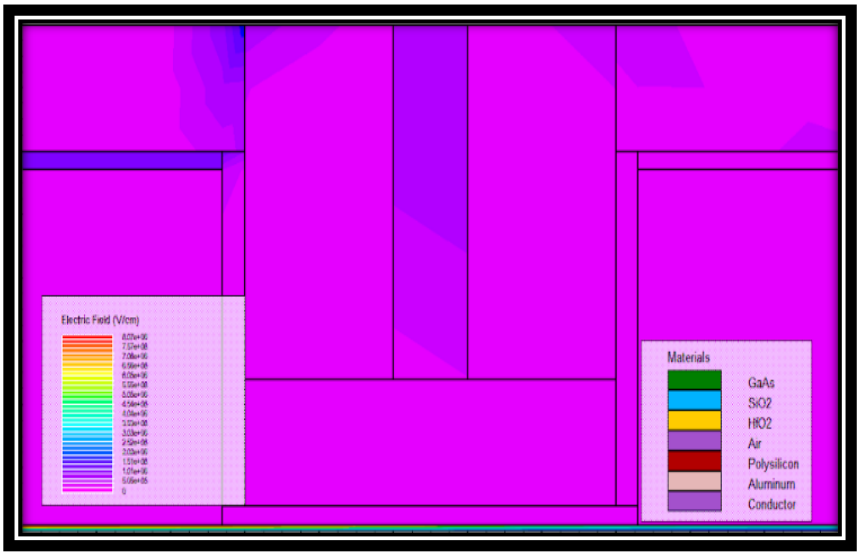

Figure 5.8. Electric Field Profile of SGS-UC-TFET.

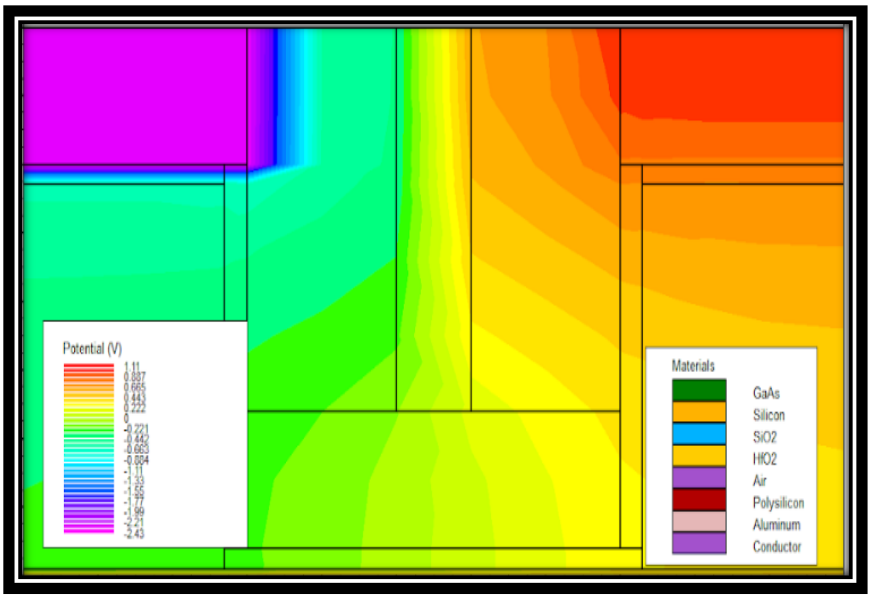

Figure 5.9. Potential Profile of SGS-UC-TFET.

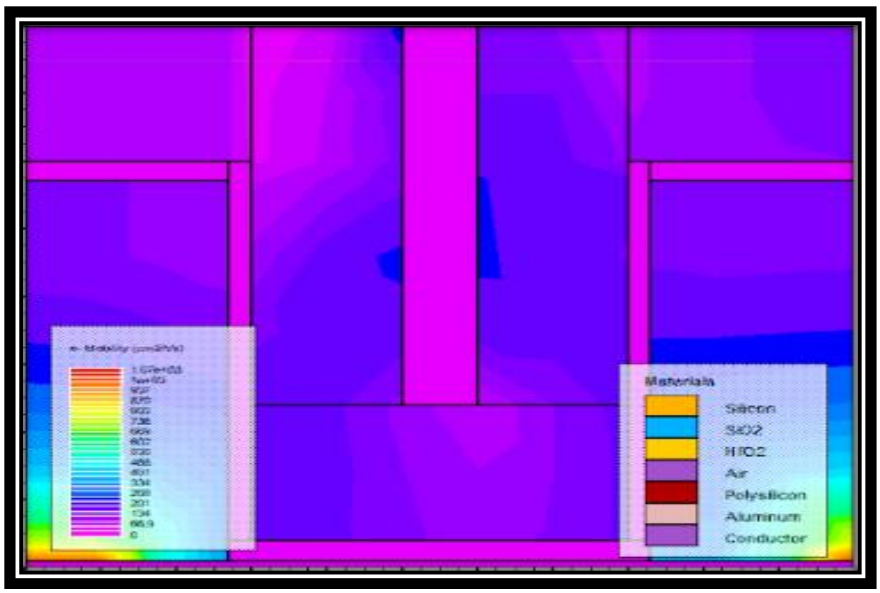

Figure 5.10. Electron Mobility of SGS-UC-TFET.

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CHAPTER 6

CONCLUSION AND FUTURE ASPECTS

6.1 CONCLUSION

In Chapter 3 the gate length of the 2D PNPN DG TFET has been varied and contrasted with one another. The pocket region in the source area improves tunneling at the source channel intersection. The correlation clarifies that the 7nm proposed structure outmatches 14nm and 24nm structures regarding the decrease of ambipolar conduction and consequent suitability for low power applications. The source pocket doping serves to enhance tunneling at the source end. This structure offers superior advantages over the conventional planar TFETs.

In Chapter 4 it is aimed to incorporate quantum mechanical effects in the behavior of CA PNPN-TFET. This device is acceptable for low power applications. For high power application, the device structure should be adjusted accordingly based on the power requirement. Quantum models other than Schrodinger-Poisson are yet to be included in this study. CA PNPN-TFET has ON/OFF ratio in the range of 10^{11} which is better than conventional TFET and has a great advantages in low power electronics.

In Chapter 5, a novel U-shaped TFET structure has been proposed and the electrical properties and tunneling phenomena has been studied for four different structures. The SGS-UC-TFET shows superior characteristics as compared to four different combination of the structure.Reverse band bending is highest at the channel-drain end for this structure making it more immune to ambipolar conduction. Maximum overshoot in the electric field profile indicates highest degree of tunneling. This structure is also immune to DIBL. All the U-shapped structures show better tunneling and reduced ambipolar conduction as compared to conventional planar TFETs.

6.2 Future Aspects

- The analytical model for the CA-PNPN TFET will be incorporated to produce more accurate result.
- The TFET structures that have been studied in this thesis show superior performance characteristics as compared to conventional planar TFETs. The proposed structures will be further explored for low power, RF and analogue applications, in future works.
- Quantum Analytical modelling will be further explored to obtain realistic models that can capture the quantum confinement effect in highly miniaturized devices in the sub-20 nm node. Further optimization will enhance the viability and feasibility of the proposed TFETs in circuit applications which is the ultimate aim of device research.

Research publications of Arindam Haldar relevant to the current thesis

Conferences:

1. Bijoy Goswami, Sutanni Bhowmick, **Arindam Haldar**, Debadipta Basak, Goutika Paul and Subir Kumar Sarkar, "Implementation of L-shaped Double Metal Dual Gate TFET towards Improved Performance Characteristics and Reduced Ambipolarity" in Information, Photonics and Communication 2019 (IPC'19) 1 st -3rd February, 2019, B. P. Poddar Institute of Management and Technology (BPPIMT), Kolkata **(WIE Best Student/Research Scholar Paper Awarded)**

2. Bijoy Goswami, **Arindam Haldar** ,Sutanni Bhowmick ,Debadipta Basak, Ayan Bhattacharya, Subir Kumar Sarkar "2-D Analysis of a Centrally Aligned PNPN-DG TFET to Preclude Ambipolar Conduction" , ECTI CON 2019, Thailand.