DESIGN OF POWER EFFICIENT VEDIC MULTIPLIER USING ADIABATIC LOGIC

A THESIS

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I hereby declare that this thesis titled "**Design of Power Efficient Vedic Multiplier using Adiabatic Logic**" is an original research work done by me under the guidance of my supervisor. This work has not been submitted previously to any other institute.

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LIST OF ABBREVIATIONS

CPAL	**:**	**Complementary Pass Transistor Adiabatic Logic**
ECRL	**:**	**Efficient Charge Recovery Logic**
PFAL	**:**	**Positive Feedback Adiabatic Logic**
PDP	**:**	**Power Delay Product**
ALU	**:**	**Arithmetic and Logic Unit**
MAC	**:**	**Multiply and Accumulate**
FFT	**:**	**Fast Fourier Transform**
DCT	**:**	**Discrete Cosine Transform**

Abstract

Various “arithmetic operations”, “signal and image processing systems” and “communication devices” incorporate multipliers as the basic element. Power consumption and speed are the main challenging areas of VLSI design. “Vedic mathematics” is an ancient mathematical system which focuses on solving tedious problems using “16 Vedic Sutras” in a simpler and faster manner. Among these sutras, “Urdhva Triyagbham sutra” can be applied to all cases of higher bit multiplication with much ease and low delay. The design of multiplication algorithm adapting the “Urdhva Triyagbham sutra” of “Vedic mathematics” has flourished to meet the demand of fast computations. With the evolution of technology, low power consumption has become the limelight of research in the domain of integrated circuit design. This led to the invention of varied adiabatic logic families for low power operations. Adiabatic technique, which is one of the promising energy-efficient technologies, emphasizes on slow charge transfer during switching and energy recovery from the load, leading to the reduction of “dynamic power consumption”. The uniqueness of “Vedic mathematics” and adiabatic logic is combined to design high speed and power efficient multipliers. In this thesis, a new adiabatic logic “Complementary Pass Transistor Adiabatic Logic” (CPAL) is used to design 8-bit Vedic multiplier. The predominance of CPAL is basically attributed to its regular architecture and its ability to eliminate “non adiabatic loss”, which is one of the major components of losses in adiabatic circuits. To authenticate the superiority of the proposed design, comparative performance analysis is carried out with respect to CMOS and other adiabatic logics like 2N-2N2P and “Efficient Charge Recovery Logic” (ECRL) based on 150nm technology. The simulation has been accomplished by the use of TANNER SPICE 16 tool. Simulation result validates the reduction of “Power Delay Product” (PDP) of the proposed CPAL Vedic multiplier design in comparison to the aforementioned techniques. The proposed technology offers a potential solution for power efficiency in modern designs.

CHAPTER 1

INTRODUCTION

1.1 OVERVIEW

In today's era, "digital signal processors" are considered to be a vital component in the domain of electronics industries. Over the last few decades, processors have evolved exponentially to meet the demand for optimized design in various fields of applications. Since the multipliers are a significant block associated with the processors, evolution of processors involves optimization of the multipliers. Hence, the focus of the researchers is emphasized on developing various algorithms of multiplication to reduce the complexity and improvise the performance of multipliers. The performance of a multiplier can be evaluated based on certain basic parameters like "speed", "power consumption", and "area". Now a day, power consumption has also become a key challenge in the VLSI technology due to the increase in number of devices on a chip. Various techniques are being developed to minimize power dissipation in integrated circuits. The optimum efficiency of the design can be achieved by integrating low power logic of circuit design with the efficient multiplier algorithm.

1.2 MOTIVATION

In earlier times, "area", "reliability", "throughput", and "cost" were regarded to be the prime aspects for designing a processor. But, with the passage of time, increasing demand for "high speed processors" compelled the researchers to consider power consumption as an important design parameter. The continuous enhancement of speed is associated with increase in number of operations processed per second. This increase in circuit complexity led to enhancement of density of components on a chip, thus causing power dissipation. Hence, in recent times with the successful growth of "high speed processors" like i3, i5 and i7, the main concern of the researchers is focused on reducing the power consumption along with increasing speed. The wide applications of multipliers in the field of "signal and image

processing", "wave transforms" etc. [1-3] act as a driving factor for designing a high speed multiplication algorithm with low power consumption.

From the aspect of environment, a great emphasis is being laid on the concept of "Green Computing" [4], which deals with reduction of power consumption and heat dissipation of electronic systems during computations. Low power consumption is also linked with low consumption of electricity from power sources, which helps in reducing the effect on global environment.

The motivation for designing a high speed, power efficient multiplier can be attributed to our need of reduced power consumption and delay. Since mid-sixties, the applications of "Vedic mathematics" [5] in various mathematical operations have been studied in various research works. The concept of adiabatic technique as an effective way to significantly reduce power consumption came into existence since mid-nineties and has been an important research topic till now. Various research papers have been proposed recently using various families of adiabatic logic in Vedic multiplication algorithm [6-7]. In this thesis work, we have designed an 8-bit multiplier circuit based on "Complementary Pass Transistor Adiabatic Logic" (CPAL) and "Urdhva Triyagbham sutra of Vedic multiplication".

1.3 Objective of the Thesis

The design of power efficient, high speed processors requires designing of low power, high speed multiplier circuits. High speed of the multipliers can be achieved by reducing the complexities of the architecture. Various multiplication algorithms like "Array", "Booth", "Wallace Tree", etc. are being continuously studied to obtain the best possible achievement in this regard. "Vedic multiplication" is established to be the most appropriate owing to its simplicity and speed. In terms of power efficiency, the performance of the multiplier circuit can be further optimized by the use of different adiabatic logic. This has been authenticated in various research papers [8-11]. The main objective of this thesis work is to introduce a novel design of Vedic multiplier using an effective adiabatic logic namely CPAL which reduces the "Power Delay Product" (PDP) by significant proportion. Another objective of this thesis is to

deduce a comparative performance analysis of the aforementioned architecture with Vedic multiplier based on CMOS and other adiabatic logic families such as 2N-2N2P and "Efficient Charge Recovery Logic" (ECRL).

Initially, mathematical expressions required to implement the "Vedic multiplication algorithm" is deduced. Then, the aforesaid algorithm is implemented by the use of CPAL logic and simulated to obtain a further optimal PDP. The main aim of any research work lies in an attempt to improvise the existing models and optimize the result. To achieve this, Vedic multiplier is designed using CPAL logic and compared with CMOS, 2N-2N2P and ECRL methodologies. The "Urdhva Triyagbham multiplier" based on CPAL offers the power efficient solution for modern designs.

1.4 Contribution of the Thesis

In this thesis, the design of power-efficient 8-bit multiplier circuit has been proposed. The major contributions related to this work are as follows:

- A high speed and low power multiplier has been proposed combining "Urdhva Tiryagbham sutra" of Vedic multiplication and a novel adiabatic logic CPAL.

- Using the "Urdhva Triyagbham sutra" of "Vedic mathematics", the mathematical expressions of the algorithm required for the architectural design of 8-bit multiplier is derived.

- The basic gates based on CPAL logic required for implementation of aforesaid algorithm is implemented using 150nm VLSI technology in TSPICE platform. All these basic gates are then assimilated to obtain the desired structure.

- The basic gates based on CMOS, 2N-2N2P and ECRL logic required for implementation of aforesaid algorithm is also implemented using the same platform. These gates are assimilated in accordance with the desired design for the purpose of comparison.

- The effectiveness of the proposed design has been evaluated by comparing its performance with different design methodologies of CMOS, 2N-2N2P and ECRL in terms of power, speed and PDP.

1.5 Outline of the Thesis

The organization of this thesis paper is as follows:

- Chapter 2 presents the detailed literature survey of related designs already proposed previously.

- Chapter 3 introduces the concept of "Vedic sutra" used for multiplication and its basic algorithms. This chapter also provides a vivid knowledge about adiabatic logic and its different techniques.

- The proposed design of 8-bit CPAL based Vedic multiplier is discussed in Chapter 4. This is followed by the design of CMOS, 2N-2N2P and ECRL based 8-bit Vedic multiplier.

- Chapter 5 summarizes the simulation results and their critical analysis.

- Finally, the paper is concluded in Chapter 6. Some of the related works that can be performed in the future is also considered.

CHAPTER 2

LITERATURE REVIEW

2.1 OVERVIEW

In this chapter, initially a thorough outline of the previous works, related to various types of multiplication algorithm and their effort to minimize the basic design parameters, have been presented. This has been followed by the analysis of those works where the efficiency of "Vedic multiplication" has been established with respect to other conventional algorithms. Then, the contribution of researchers in the domain of application of different types of adiabatic logic has been studied and their comparative analysis has been reviewed to figure out the performance of various evolving techniques in obtaining an optimized design. Lastly, works related to the design of "Vedic multiplier" with the help of different adiabatic logic have been summarized. Some of these works are related later in this thesis to deduce the performance analysis.

2.2 REVIEW OF THE RELATED WORK

Low power consumption has become the main area of concern for the researchers with the evolution of technology. Along with this criterion, other design parameters like "speed", "area" and "Power Delay Product" (PDP) are taken into consideration to optimize the overall performance of a design. A multiplier is an important functional block profoundly used in various units like "Arithmetic and Logic Units (ALU)", "Multiply and Accumulate (MAC)", etc. and different operations such as "Fast Fourier Transform (FFT)" [1], "Discrete Cosine Transform (DCT)" [2], etc. in connection with "digital signal processors". The design of multipliers is continuously being improvised in order to meet the above criteria. Varieties of multiplication algorithms had been explored to meet the demand for high-speed, power efficient multipliers.

Recently, research articles are concentrated on the development of multiplication algorithms that exhibit reduced computational complexities. The simpler architecture of hardware for designing multiplication and division algorithms can make the manufacturing of large scale, scientific computers feasible from the economic point of view. This concept was proposed in a paper in 1964 [12]. This was achieved by development of the design of multiplier with use of combinational logic, i.e. in a "single gating step". The improvement of this process in terms of speed can be obtained by reducing number of "summands", generating "summands" quickly and adding "summands" rapidly. The design is based on "Diode Transistor Logic" (DTL) and is able to perform multiplication and division of 40 bit digits. Furthermore, the logic is also implemented in designing a "high speed square root" model. The proposed design, when compared with conventional methodologies results in improvement of speed by a factor of four. But an alternate simpler design is desirable for performing "two step multiplications", which can be performed by half of the number of adders to reduce cost and increase speed.

"Parallel multipliers" have always drawn attention of the researchers owing to their high speed. Various design methodologies of "parallel multipliers" have been evolved with time to optimize their architecture [13-14]. To achieve this, a fast "serial-parallel multiplier" structure was designed by utilizing "carry-shift add-shift" (CSAS) multiplier architecture [15]. In the "carry-shift add-shift" multiplier, multiplier input is accepted and output is generated in a serial fashion. 2n clock cycles are required to perform multiplication on two n bit unsigned numbers. Out of these 2n clock cycles, n clock cycles are consumed by n row "carry-save addition" and the rest are used to transfer the left carries. This structure can also be improvised to use it as "carry-shift add-shift" module in the first n clock cycles and n bit "ripple carry parallel adder" in the next (n+1) clock cycles. This enables the carry to ripple without delay in last n clock cycle. This proposed design enhances the speed by two-third with respect to same increase in hardware. The multiplier technique is also used to design "2's complement" multiplication. Comparison with "Booth's algorithm" verifies the efficiency of the aforementioned design in terms of hardware complexity and speed.

The “Booth’s multiplication algorithm” is applied for multiplication of signed numbers in “2’s complement form”. Kuang, Wang and Guo [16] improvised the conventional modified “Booth algorithm” in terms of power consumption, delay and area. The drawback of conventional “modified Booth encoding” (MBE) is that it generates (n/2+1) rows of “partial product” instead of n/2 rows due to generation of extra negative bit at LSB of each “partial product” row. This led to the formation of an irregular array. The authors proposed an approach where the negative LSB is merged into the sign extension bit of initial “partial product” row, thus generating a regular array. This reduces the height of the tree along with delay, area and power consumption of the proposed design. The proposed design, when implemented in “post-truncated MBE”, can also be optimized in terms of the aforementioned criteria.

The proposed paper [17] focuses on a method to optimize 64 bit “Radix-16 Booth Multiplier”. This method emphasizes on reducing the maximum height of “partial product” columns to n/4 as compared to [(n+1)/4] for conventional multipliers. This has been achieved by performing parallel addition of “carry propagate” with “partial product”. Reduction of delay, area and power are the main advantages associated with this proposed design. “Radix-16 Booth Multiplier” has been popularly accepted as basic element in power-efficient devices.

A novel methodology of high speed parallel multiplier based on “modified Booth’s encoding” (MBE) algorithm has been proposed in [18]. A modified MBE algorithm has been presented for generation of “partial products”. For performing the final addition, “multiple-level conditional-sum adder” (MLCSMA) incorporating a new algorithm has been constructed. Hence, in accordance with properties of cell and delay profile of input, the final addition design has been optimized. When the proposed architecture is compared with “binary tree-based conditional-sum adder”, 25% enhancement of performance in terms of speed has been observed. Moreover, the proposed design also shows 8% reduction in total delay as compared to parallel multipliers.

In [19], a remarkable method has been presented to design an improved 8-bit parallel multiplier by utilization of improved “MOS current mode logic” (MCML) in terms of low power consumption. In this work, the adders in the multiplier circuit have been constructed with proposed MCML design and also with conventional design for comparison purpose. The simulation is carried out using 350 nm CMOS technology. Though static CMOS design exhibit accurate result at low frequency, but power consumption increases linearly with the reduction of charging and discharging time due to increase of operational frequency, thus leading to inaccurate output signals. This problem is resolved by the adaptation of MCML design. The low “input capacitance”, small signal amplitude and use of static power source make this design power efficient with increasing frequency and faster than CMOS logic. The disadvantage of high power consumption of MCML at low frequency is eliminated by the use of NMOS transistor. The proposed design is verified to exhibit 9.4% reduction in power consumption and 9.4% reduction in PDP as compared to conventional CMOS circuits.

Pishvaie, Jaberipur and Jahanian [20] designed a modified “4:2 compressor” with optimized “CMOS adder circuit”. Analysis of the above design shows enhancement in performance. The above design is implemented in 54-bit multiplier circuit for practical evaluation. In another similar work, Marimuthu, Rezinold and Mallick [21] presented a unique approach to implement “5:3 compressors” as key element in design of “15:4 compressor”. The proposed compressor design has been used to simulate a 16-bit multiplier. The analysis result reveals that the proposed design shows significant reduction of power consumption and improvement in pass rate as compared to the multiplier implemented by accurate “15:4 compressor”. Application of this design in “image processing” improves the peak “signal-to-noise” ratio to 30 db. These techniques are suitable for the design of “parallel multipliers”. Various other innovative designs have also been developed to improve the performance of different multipliers in various aspects.

The novel principles of “Vedic mathematics” were initially researched and introduced by Swami Bharati Krsna Tirthaji in his book “Vedic Mathematics or Sixteen Simple Sutras from the Vedas” [5].The efficiency of this technology based multipliers in comparison with other multipliers with respect to speed and reduction of complexity has been substantiated by

various authors in their research work. Some of such works are briefly summarized in this section of the chapter.

The efficiency of the conventional multiplier methodologies and multipliers based on ancient "Vedic mathematics" has been compared in [22-23]. An 8-bit Vedic multiplier circuit has been designed with the use of 8-bit "macro" in [22]. Simulation results illustrate the effectiveness of the proposed architecture in terms of area and speed. In another research work [23], the authors designed a 4-bit multiplier circuit incorporating both "Vedic mathematics algorithm" and conventional methods. SPICE simulator is used as the design platform. It has been established in this work that "Vedic multipliers" use less adders in comparison with the conventional technologies and thus reduces delay. Simulation result verifies that the "Vedic multiplier" design exhibits reduction of average power by 29%. Hence, the paper validates the efficiency of arithmetic design based on ancient mathematics in application of ALU models.

Pohokar et al. [24] implemented 16 x16 multiplier using "Urdhva Triyagbham sutra" of "Vedic mathematics" and compared it with the conventional "Array" multiplier in his work. The proposed design has been found to be efficient in terms of speed and memory size. A similar approach was used by Kaharand and Mehta to design a 64 x 64 multiplier in [25] and the comparative analysis revealed increase in speed and decrease in area and complexities with respect to both "Array" and "Booth" multiplier.

To improvise the performance further, various innovations have been implemented in the design and technology and comparative analysis has been performed. A novel approach was presented by Deodhe, Kakde and Deshmukh in [26] where an 8-bit Vedic multiplier has been designed using four 4-bit Vedic multipliers and three 16-bit adders in 180nm technology. A 75% power reduction was obtained at a power source of 2.5V when compared to the "gate level implementation" of the same multiplier architecture.

Improvised "Vedic mathematics" based low power and high speed multiplier architecture has been proposed in [27]. The proposed 4-bit and 8-bit design was based on "Urdhva

Triyagbham sutra" and has been implemented using 45 nm CMOS technology. The "pass transistor logic" and "transmission gate logic" has been used to design a "5T AND gate" design. Additionally, "9T based half adders" and "14T based full adders" topologies have also been used to simulate the multiplier circuit. An improvement of power, delay and PDP has been visualized in the simulation results. Moreover, reduction of area due to the application of these modified topologies has also been established in this paper.

Kaur and Prakash [28] presented a unique 8-bit Vedic multiplier that utilizes compressors as adders. N: 3 compressors were used for "partial product" generation where N = 4, 5, 6 and 7. This design has been simulated by the use of 180 nm CMOS technology. The use of "compressor adders" has reduced number of intermediate stage for "partial product" addition. Performance analysis shows a significant reduction of PDP and area in multiplier circuit for all types of "compressor adders".

An efficient "Urdhva Triyagbham sutra" based 4-bit multiplier was implemented in [29]. The basic gates used for generation of "partial products" are designed in a compact structure, thus reducing the number of count of transistor. Moreover, the methodology followed for performing addition is "carry skip" method, which causes reduction of hardware, and as a result reduces delay. All the simulations are done in 45 nm technology. The power consumption is also obtained to be reduced in this architecture. This method is effective for implementation of high order multipliers.

In [30], the author has focused on the design of a modified 2-bit Vedic multiplier circuit using "Gate Diffusion Input" (GDI) technique. GDI technique is mainly implemented to decrease the power consumption and delay. This technique generally leads to reduction in the number of transistors. All the basic gates are designed using this technique. Simulation results have revealed significant reduction in power, delay and PDP of the proposed design with respect to conventional multipliers.

A power efficient "Vedic multiplier" using combination of GDI technique based AND gate and "6T full adder" circuit has been realized in [31]. The "transistor level implementation" of

the entire design has been simulated using 180 nm technology. AND gates and adder circuit designs are optimized by the use of less number of transistors, which lead to decrease in total number of transistors in the entire circuit. The overall design incurs significant improvement in terms of speed and power as the transistor count of the entire design has been considerably reduced.

The authors introduced "Multiple Channel CMOS" (McCMOS) technology, which reduces leakage, in combination with "Vedic multiplication" to design an 8-bit multiplier in [32]. The design has been integrated using 130 nm, 90 nm, 65 nm and 45 nm technology. Simulation result indicates significant improvement of PDP by about 80% in comparison with conventional multipliers. Dey et al. [33] realized a power efficient and high speed 8-bit "Vedic multiplier" using 16 nm technology. The proposed design was compared with "Vedic multiplier" using 65 nm technology and McCMOS technique. Comparative analysis reveals improvement of the design in terms of power, delay and PDP.

A high speed 8-bit multiplier based on "Vedic mathematics" algorithm has been designed in [34]. This architecture of "Vedic multiplier" employs the method of "add and shift" in obtaining the product of two numbers which is different from the methodology used in conventional methods. Combined with the process of "vertical and cross" multiplication technique, this proposed modified design computes in a fast and efficient manner. The complexity in the architecture of the design is also reduced. The proposed architecture has been simulated using "VHSIC Hardware Description Language" (VHDL) and the code has been synthesized with EDA tool, Xilinx ISE 12.2i. Comparison is drawn between 8-bit Vedic multiplier using the proposed design and conventional design like "Booth" and "Array" multipliers. The analysis result shows that the delay associated with 8-bit Vedic multiplier is 21.449 ns, whereas delays of "Array and Booth" multipliers are 32 ns and 29.6 ns respectively. Finally, the conclusion can be drawn that "Vedic multiplier" exhibits higher efficiency in terms of speed than "Array and Booth" multipliers.

Adiabatic logic is a power efficient logic style capable of recovering the energy either completely or fully, thus causing reduction in power consumption. The main characteristic of

adiabatic circuit lies in the use of AC power clock as supply, with slow transition periods and charge recovery circuitry. Designing low power adiabatic circuits effectively requires proper understanding of the operation of the logic styles. This enables to modify the design to obtain optimum power consumption. Various research works are being carried out to reduce the power consumption along with various design criteria.

Some previous works related with this methodology has also been analyzed for proper implementation of this thesis work. The technique of adiabatic switching has been proposed by Indermaur and Horowitz in their paper [35] and a comparison has also been drawn in terms of speed and power consumption with the existing CMOS technology. The analysis has been performed considering inverter as the basic circuit. The authors have compared the performance at different supply voltages and proved the proposed charge recovery circuit to be significantly power efficient. Though the energy recovery technique has drawn immense attraction, but its operation is limited at low operating conditions and the area overhead is high.

A varied type of low power adiabatic logic namely "Efficient Charge Recovery Logic" (ECRL) has been introduced in [36]. The performance analysis has been performed using a chain of inverters and 16-bit "Carry Look-Ahead Adder" (CLA). ECRL adiabatic logic circuit is generally based on "Cascade Voltage Switch Logic" (CVSL) and four phase of clock. ECRL based CLA has been devised in a pipelined structure to obtain the same output like static CMOS CLA. The analysis has been carried out using CMOS technology of 1.0 µm and the minimized threshold voltage of 0.2 V. The result indicates that the proposed logic incurs power reduction by 4-6 times when compared with the static CMOS CLA and 2N-2N2D based CLA at various supply voltages, various practical load capacitances and various operational frequencies. The ECRL based design introduces significant improvement in power consumption which makes it suitable for power efficient applications.

The proposed paper [37] introduces a "32-bit register file" containing one "read" and one "write" port based on ECRL adiabatic logic. The authors also designed a "clock generator" to provide four phase clock to the register circuit. The energy saving is done by recovery of

charge in adiabatic logic. In the proposed research work, the charge stored in the capacitive interconnections of the "word" and "bit lines" has been recovered to reduce the power consumption. All the circuits have been designed using 0.8 μm CMOS technology. Comparative analysis of the proposed "register file" incorporated with proposed "clock generator" with conventional CMOS design shows significant reduction of power consumption by a factor of 3.5. The proposed design can be further used in memory design applications.

In 1994, another variety of adiabatic logic namely 2N-2N2D has been proposed in [38]. This logic has replaced the previous works, which performed energy reversal using diodes, by introducing NMOS transistors. The main objective of the researchers was to provide a nearly constant capacitive load, which is independent of data, to the clock generator. The input capacitance of 2N-2N2D logic is low but area overhead is high by only 20%. This proposed logic has been incorporated in designing shift registers. The proposed shift register incurs reduction in power consumption by a factor of three with respect to CMOS design at frequencies below 100 MHz.

The design of 2N-2P and 2nd order 2N-2N2P was first introduced in [39]. The power consumption has been reduced due to absence of "floating point" at the output and absence of the diodes, thus reducing "non adiabatic" loss. The proposed logic has been implemented to design a shift register having 1000 shifts using 0.80 μm CMOS technology and has been operated for a frequency range of 1 MHz to 100 MHz. The proposed circuit demonstrated an adiabatic power saving by a factor of three when compared with CMOS.

A different family of adiabatic logic has been demonstrated in [40]. The proposed adiabatic architecture uses power clock supply and "positive feedback amplifier". The logic gates use "dual rail encoded signal paths". Furthermore, the "positive feedback" circuit helps it to become immune to noise and also helps in recovery of energy. The paper provides the detailed information about the operation and the mathematical derivations of the logic style. The proposed logic has been integrated to form a shift register in 1 μm process technology and simulated for different load capacitance ranging up to 100 fF. The design exhibits

significant improvement when compared with the logic style using NMOS transistors and diode.

Another new type of adiabatic logic, “Complementary Pass Transistor Adiabatic Logic” (CPAL) was introduced by Jianping, Lizhang and Xiao [41]. The proposed CPAL logic circuit utilizes “complementary pass transistor logic” for evaluation of logic and transmission gates for restoration of energy. Additionally, this logic design eliminates “non adiabatic” loss completely and provides a regular topology. The authors designed an inverter circuit with the use of 0.25 μm CMOS technology in SPICE simulation. Chain of inverter based on this logic has proved to be 2.5 to 3 times and 3 to 9 times power efficient with respect to 2N-2N2P logic and static CMOS logic respectively, when operated at an operational frequency range of 25 MHz to 300 MHz. Hence, it can be concluded that CPAL logic architecture proves to be power efficient, insensitive to load capacitance and less dependent on clock frequency. However, the designers also have to carefully consider the energy loss of “power clock generators” along with the losses of the proposed circuit. Recently, designers are focusing to use the proposed design in integrating different complex circuitries like microprocessors and multipliers. Furthermore, design of high frequency operated “power clock generator” is being studied to optimize the proposed circuit.

A “low power register file” was implemented using the CPAL logic in [42]. The “register file” consists of “storage cell arrays”, “address decoders”, “read/write control circuits”, “sense amplifiers” and “read/write drivers”. The “storage cell arrays” have been designed using conventional designs whereas the rest of the circuitry has been implemented using CPAL logic. The simulation has been carried out using HSPICE. The power consumption has been observed to be minimized by 65% to 85% with respect to CMOS technology when operating at a frequency between 25 MHz to 200 MHz.

CPAL was also implemented in the design of sequential circuits [43] to substantiate the efficiency of the logic in various applications. The circuit has been operated by the use of two phase clock. The CPAL based sequential circuit has been proved to be advantageous than “CMOS transmission gate” based design and 2N-2N2P based design in terms of count of

transistor. Initially, adiabatic flip-flops such as “D, T and J-K” have been designed using CPAL logic and these components have been integrated to prepare a practical sequential circuit. The circuit has been designed using 250 nm technology. Performance analysis depicts CPAL sequential circuits to be 2-3 times power efficient with respect to 2N-2N2P and 3-6 times less dissipative in comparison with CMOS.

Adiabatic logic families are being continuously modified by designers and are compared for various operations to authenticate their efficiency. Bakshi and Sharma [44] introduced the concept of ECRL and PFAL in implementation of various basic gates. The designs are integrated by using 1.25 micron process technology. PFAL based circuits are found to be more complex than ECRL circuit; hence PFAL is capable of producing “distortion free” output for a higher value of load capacitance than ECRL. The authors have observed the average power consumption for various operational frequencies and load capacitances for both the logic and have deduced PFAL to be more efficient than ECRL.

CPAL based basic gates has been presented in [45] to achieve a high performance design. CMOS and CPAL inverter, NAND and XOR circuits have been implemented using 90 nm technology. The performances of the basic circuits have been analyzed for a period of 200 ns and using power supply of 1 V. Comparative power analysis shows that CPAL based logic gates saves power by 86% to 93%. The CPAL logic circuits using “power gating” method have been proved to be efficient with respect to other conventional designs.

Sheokand, Bhargave and Kaur [46] presented a design of basic gates like AND, NOR and XOR using “two phase clocked energy recovery logic”. The proposed logic style has been implemented by combination of ECRL and “2-Phase Adiabatic Static CMOS Logic” (2-PASCL). The circuitry uses 2 phase clock as supply. The analysis is performed for frequency range from 10 MHz to 200 MHz for a load capacitance of 10 fF using 90 nm technology. The power dissipation of modified inverter circuit has been observed to be 30 nW, 250 nW and 414 nW for frequencies 10 MHz, 100 MHz and 200 MHz respectively. 85% reduction of overall power consumption has been obtained when compared with CMOS logic design.

An improvised structure of ECRL logic has been presented in [47] and has been implemented for the design of NAND and NOR gates. Comparative study, using 180 nm technology, has been studied for a frequency span of 50 MHz to 400 MHz for inverter, NOR and NAND gates. The low power concept has been implemented from the "system level" to "process level". The proposed design demonstrates power saving of 64%, 14.02% and 22.6% for inverter, NAND and NOR gates respectively in comparison with conventional ECRL design. Furthermore, the device has also been effective at high frequency operations.

A 4:1 multiplexer circuit has been designed using CMOS and various adiabatic logic namely 2N-2N2P, ECRL and PFAL logic in [48]. All the designs have been simulated using 180 nm process technology. The power efficiency of adiabatic logic based circuit has been obtained to be more than 90% with respect to conventional CMOS logic in case of low frequency applications and more than 50% beyond 1000 MHz. Among the different adiabatic logic families analyzed in the paper, PFAL shows better result in terms of power consumption. Analysis has been performed up to 1 GHz and the result depicts the efficiency of adiabatic logic for low power operations.

A low power based "content addressable memory" (CAM) has been realized by using ECRL and CPAL logic in [49]. The storage unit has been designed by the use of "9T CAM" cells, whereas the decoders that drive the "bitlines" and "wordlines" have been realized using ECRL and CPAL logic. The "bitlines", "wordlines" and "matchlines" are the main sources of power consumption and the charges of the "node capacitances" of these lines can be recovered using this adiabatic logic, leading to reduction in power consumption. Performance analysis has been simulated using 180 nm technology and power supply of 1.8 V. The Adiabatic logic based CAM proves to be 40% better with respect to conventional CAM architecture. Moreover, among the adiabatic logic compared in this paper, CPAL logic is found to be the most efficient. The CAM design can also be implemented using other adiabatic logic in future.

Adiabatic logic families are also used for integration of various multiplier circuits to improve their performance. The performance of "Energy Efficient Adiabatic Logic" (EEAL) based "8-

bit tree multiplier" by the "4:2 compressor" has been analyzed in [8]. EEAL is designed on the basis of "differential cascode voltage swing (DCVS) logic" and utilizes single sinusoidal signal as supply. The proposed design logic uses fewer clock overhead and removes the "floating output", which reduces "non adiabatic" losses. This enables the circuits to consume only 25% - 30% of power when simulated in 180 nm technology. In this work, the authors have established that their proposed technique is efficient enough as far as speed and power consumption of the multiplier is concerned.

A "4-bit Array multiplier" using "2-Phase Adiabatic Static CMOS Logic" (2PASCL) is proposed in [9]. Here, the performance analysis of the proposed technique is compared with CMOS logic using 180 nm technology for a frequency range of 10 MHz to 100MHz at 0.01 pF load capacitance. An effective power improvement of 36.96% has been observed for the proposed circuit in comparison with the CMOS logic design. Significant improvement in terms of delay and PDP has also been established in this work.

In [10], "2-Phase Clocking Adiabatic Logic" in "sub-threshold regime" (2PCSAL) has been studied to obtain optimized power efficient design. The logic has been implemented to device a "4-bit Dadda multiplier" with "Brent-Kung adder". The circuits have been simulated by the use of 180 nm CMOS technology. The full adders are designed using two XNOR gates and one 2:1 multiplexer. The similar circuit has also been constructed by CMOS logic gates using 45 nm process technology. Comparative analysis indicates that the power consumption of the "2PCSAL Dadda multiplier" is 20.14 μW whereas that of 45 nm based CMOS "Dadda multiplier" is 81 μW. The proposed design incurs 75.1 % reduction of power consumption and proves to be optimized in terms of power.

A novel approach has been represented in [11] to improve delay time and power consumption. Low power 2-bit multiplier based on "Radix 4 Booth's Algorithm" has been designed using "Split Charge Recovery Logic" (SCRL). SCRL uses "four phase clock supply" and differs from conventional CMOS design by introduction of transmission gates at the output. The circuits have been simulated using 120 nm technology. Analysis reveals that the SCRL based multiplier consumes 1.016 mW and CMOS based multiplier consumes 1.055

mW power. The result verifies the SCRL based design to be power efficient than conventional CMOS design.

Recently, the power consumption of 2-bit Vedic multiplier based on PFAL and ECRL using 180 nm technology has been compared with CMOS and the superiority of the earlier one has been established [6]. The analysis has been carried out for load capacitances ranging from 10 fF to 60 fF and operational frequencies ranging from 10 MHz to 50 MHz. The study of the simulation result affirms 64% power saving of PFAL than CMOS technology. Moreover, PFAL logic is also considered to exhibit least power consumption. The result reveals the efficiency of adiabatic logic based circuits over CMOS based circuit in terms of power consumption.

In [7], the designs of 2-bit and 4-bit "Urdhva Triyagbham multipliers" based on adiabatic logic have been depicted. Further optimization of design has been achieved by use of "3T AND gate", "5T Half-Adder", and "8T Full-Adder" in the circuit. The analysis has been conducted using Tanner EDA Tool 13.0 in 180 nm technology. Reduced power consumption of the proposed "Vedic multiplier" has been established with respect to the conventional CMOS design.

In [50], a low power "modified complementary pass transistor adiabatic logic" (MCPAL) has been presented. The design is supplied by "4-phase power clock supply". Initially, a basic inverter circuit is designed using MCPAL and other adiabatic logic families like 2N2P, 2N-2N2P, PFAL, CPAL, and DCPAL. Efficiency of the proposed logic has been established by comparison with other aforementioned adiabatic logic families. The proposed logic circuit incurs low "leakage power", "glitch free output" and "low switching noise". The next part of the paper utilizes the use of "self-aligned double gate FinFETs" in MCPAL based inverters and cascaded inverters consisting of 512 stages. The simulation has been carried out for 32 nm FinFET technology and 32 nm CMOS technology. The power optimization of FinFET based circuits has been verified in this paper.

A modified version of "Diode Free Adiabatic Logic" (DFAL) namely "Complete Charge Recovery Diode Free Adiabatic Logic" has been introduced in [51]. The main characteristic of the proposed logic is that it eliminates the effect of "non adiabatic" loss. An inverter circuit has been implemented using the modified circuit in TANNER SPICE and comparison has been drawn in terms of power, delay and PDP for 10 fF to 200 fF at the frequency of 200 MHz. The analysis reveals about 34% to 60% and about 46% to 80% power efficiency of the proposed circuit in comparison with DFAL and CMOS design respectively.

The proposed paper [52] focuses on comparing two adiabatic logic families namely ECRL and "True Single Phase Energy Recovery Logic" (TSEL) for different frequencies and temperatures. The result has been analyzed for an inverter circuit using TANNER Version 13.0 on 90 nm process technology. The result displays that at 10 MHz TSEL based circuit shows 60% efficiency than ECRL for most of the temperatures and 100% efficiency at room temperature. This superiority of TSEL is also present for 100 MHz. However, for 500 MHz, ECRL supersede TSEL by performing 62% more efficiently. Hence, ECRL performance supersedes TSEL mainly at extreme temperatures.

In [53], an adiabatic logic has been operated in "subthreshold regime" to minimize "dynamic power consumption". In "subthreshold" logic design, the circuit operates at a voltage below "threshold voltage" of transistor and it uses "subthreshold" current for operation. "Arithmetic and Logic unit" (ALU) has been chosen as the component to implement "Subthreshold Adiabatic Logic" (SAL) and the implementation has been simulated using 180 nm technology. The proposed design proves to be efficient in terms of power consumption when compared with CMOS designs.

2.3 Outcome of the Review

From the above review, it has been identified that power consumption and delay are prime aspects of design in VLSI technology. The "Vedic mathematics", which is the basis of various mathematical operations, has profound applications in various fields. The architecture gained importance due to its simplicity, speed and less area overhead. These advantages have

been well proved in the above review. Moreover, power consumption can be drastically reduced to a large extent by adoption of adiabatic logic in place of CMOS technology. This concept has been experimentally validated in the aforementioned papers.

Chapter 3

Theoretical Background of Vedic Multiplier and Adiabatic Logic

3.1 Overview

This chapter presents vivid theoretical information about the two basic components of this thesis work namely, "Vedic multiplier" architecture and adiabatic logic. Multiplier based on "Vedic mathematics sutras" has gained wide application due to its simplicity, speed, power consumption and area. This thesis work is based on "Urdhva Triyagbham sutra" of "Vedic mathematics". The algorithm of this sutra has been analyzed in this chapter. In addition, adiabatic logic methodology along with its different branches is also introduced. Later, ECRL, 2N-2N2P and CPAL logic of partial adiabatic logic family are described in vivid manner.

3.2 Vedic Multiplier

3.2.1 History of Vedic Mathematics

Swami Bharati Krsna Tirthaji of Govardhana Matha, Puri (1884-1960) [5] researched on ancient "Indian mathematics" from 1911to 1918. This ancient system of mathematics, which was depicted from ancient "Vedas", meaning "storage of knowledge", was named as "Vedic mathematics". Vedic mathematics usually comes under the category of "Sthapatyaveda", which is an "Upaveda' of "Atharvaveda'. This category of "Upaveda" or engineering includes all types of architectural and structural related works of mankind along with all visual arts. Swamiji considered the field of mathematics, computations as well as calculations to be a part of this "Upaveda". Various sections of mathematics such as "arithmetic", "algebra", "plane and solid geometry", "trigonometry", "factorization", "differential and integral calculus", "quadratic equations", "geometrical and analytical conics", "astronomy" etc. [5] are all explored in this category. Swamiji performed extensive research and

discovered “16 sutras” or formulae and “16 upsutras” or sub formulae to accomplish various basic and complex mathematical operations. Owing to its outstanding characteristics, “Vedic mathematics” has become the limelight of research topics all over world. A brief description of the “16 sutras of Vedic mathematics” has been provided in [5].

The “Vedic mathematics” is a novel approach for learning mathematics. It is based on “pattern recognition”, which is helpful in increasing the creativity of students [54]. It is widely accepted because the tedious mathematical calculations can be simplified into easier conventional methods. Its operation is basically similar to the principle on which our brain works. Since, large and difficult calculations can be performed with simplicity and ease by the use of this ancient system it is proved to be efficient with respect to the modernized system in terms of speed and accuracy. In this system, one general technique can be applied for wide range of problems, both simple and special cases; hence use of this technique provides clarity of mind [54]. Moreover, these principles can be easily used to implement further innovative works.

3.2.2 Vedic Multiplication

Multiplication operation is regarded as the most complicated and difficult method among the other basic mathematical operations namely addition, subtraction and division. Multipliers, being a basic building block and critical among other basic mathematical operational blocks, are being developed by researchers to enhance their power efficiency and speed. Application of “Vedic principles” in performing multiplications enables to perform this critical operation in a simplified and fast manner. In addition to these, “Vedic multiplication” also reduces power consumption and area to a large extent as compared to conventional multiplication methodologies [22-25]. “Vedic multiplication” is usually applied for multiplications of decimal numbers [55]. But, nowadays, it is also applied to “binary multiplication” system for attaining compatibility with the available hardware design [22-23]. Among the aforementioned sutras, multiplication based on “Urdhva Triyagbham sutra” is an effective and simplified methodology.

3.2.3 Urdhva Triyagbham Sutra

"Urdhva Triyagbham sutra" [5] is the most commonly used methodology, which is applicable for both multiplication as well as division of two numbers. This sutra is based on the concept of "vertical and crosswise". The multiplication, based on this sutra, produces "partial products" and addition of these "partial products" in a single iterative step. Thus, this method of parallel operation reduces complexities and delay with respect to other conventional multiplication architectures. This sutra can be used to implement small to large N bits multiplication with much ease and less time. The large bit multipliers can be implemented by using smaller bit blocks of multiplier. Hence, the area overhead and power consumption increases slowly with the increase in number of bits as compared to other multiplication algorithms. To obtain a broader idea of the "Urdhva Triyagbham" based multiplication, the algorithm [5] is illustrated below in details.

3.2.3.1 Algorithm of Vedic Multiplier Based on Urdhva Triyagbham Sutra

To understand the algorithm of "Vedic multiplier" based on "Urdhva Triyagbham sutra", let us consider 4-bit multiplication. Fig. 3.1 [5] shows the methodology of 4-bit "Vedic multiplier" based on the above sutra where bits of multiplier and multiplicand are multiplied in "vertical and crosswise" fashion to generate the "partial products". These "partial products" are then added to obtain the "final product". Both the "partial product" generation and addition are performed in a single step.

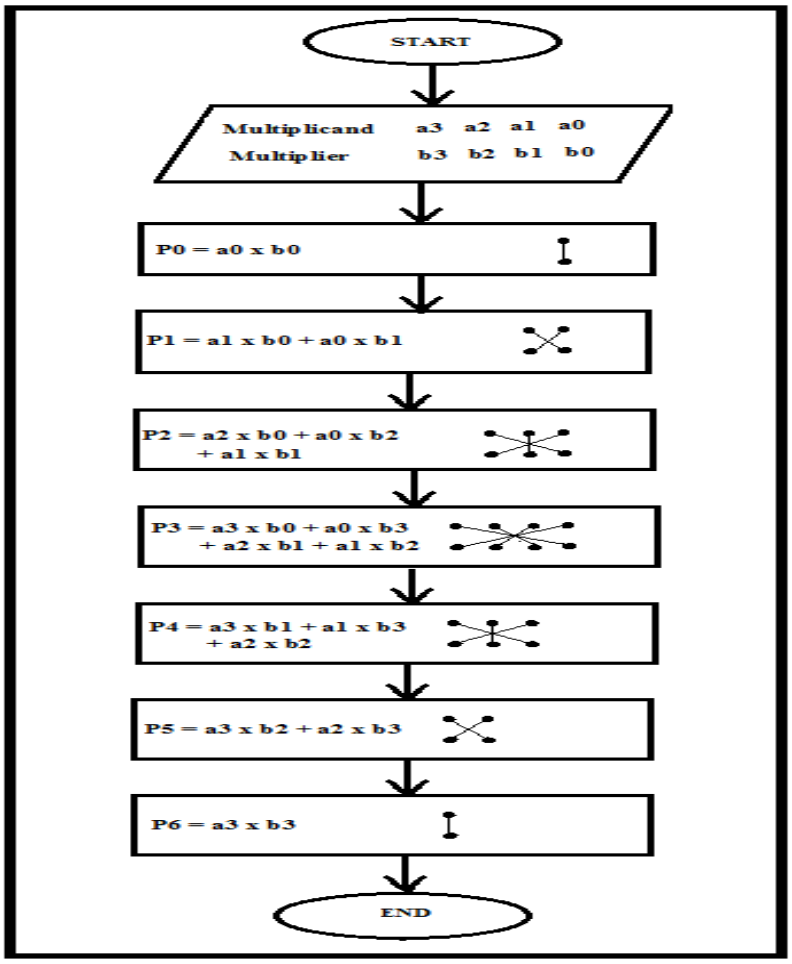

Fig.3.1 4-bit Vedic Multiplier Algorithm

The multiplicands and multipliers are represented by ai and bi, respectively where i = 0, 1, 2, 3. The partial product is represented by Pi, where i = 0, 1, …, 7. In the 1st step, "partial product" P0, which is the LSB of the "final product", is obtained by a0xb0. This is vertical operation of the sutra. In the next step, a1xb0 and a0xb1 are generated and their sum gives the "partial product" P1. This is the crosswise operation. In the similar manner, "partial products" P2, P3, …, P6 are obtained and their addition taking into consideration the intermediate carry during generation of "partial products" and final carry gives the final 8x8 bit product [5]. The additions are performed by either half adders or full adders.

3.3 Adiabatic Logic

The term “adiabatic” [56] is derived from the Greek word “adiabatos”, which refers to “thermodynamic system” that undergoes no “energy transfer” with the environment. The adiabatic circuit is considered to be an efficient solution related to modern circuit design as it exhibits less power consumption with respect to conventional CMOS circuitry. This becomes possible because of the following facts [56]:

- Instead of dissipation, it conserves energy from the load during the discharge process and employs it in the succeeding computations.
- It introduces a novel approach of AC power source, thus providing a small voltage across the switching devices.

The power consumption in static CMOS circuit [57] can be divided into three major components namely “static or leakage” power consumption, “short circuit” power consumption and “switching power or dynamic” power consumption. The leakage current ($I_{leakage}$) flowing in a circuit during its idle state is the cause of “static power consumption” and is given by $I_{leakage}.V_{dd}$. When both the PMOS and NMOS transistors are turned on, the “short circuit current” (I_{SC}) flows, which lead to the “short circuit power consumption” denoted by $I_{SC}.V_{dd}$. On the other hand, during switching, the charging and discharging phenomenon of the node capacitance C_L by the constant DC power source V_{dd} governs the irretrievable “dynamic power dissipation’ of $C_L V_{dd}^2$ [57]. This power consumption due to switching is overcome by adiabatic computation, where the power consumption is less than the lower limit of that of static CMOS [58].The adiabatic logic is basically a “circuit level implementation” in low power VLSI design.

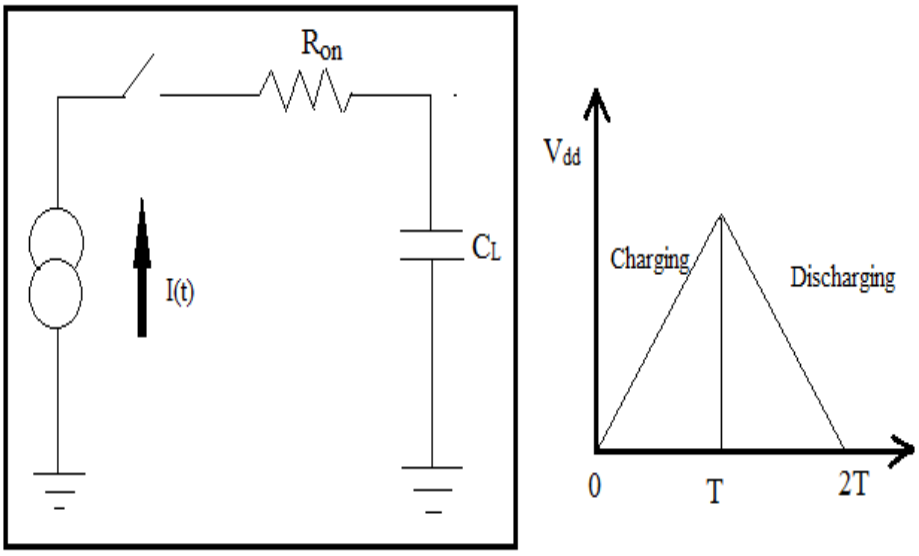

Fig. 3.2 Adiabatic Circuit Charging and Discharging

The model of a structure based on adiabatic logic is shown in Fig. 3.2 [58]. The on-resistance of CMOS transistors along with signals path resistances is represented by R_{on}. The load capacitance is depicted by C_L, which is charged and discharged by a constant current source I(t).

The current generated in the circuit [58] is given by

$$I(t) = C_L \times \frac{V_c(t)}{t} \tag{1}$$

The energy dissipated during charging [58] is calculated to be

$$E_{dissipated} = R_{on} \times \int_0^T I^2(t)dt = R_{on} \times I^2(t) \times T = \frac{R_{on} \times C_L}{T} \times C_L \times V_c^2(T) \tag{2}$$

The total energy dissipation [58] can be approximated to be

$$E_{dissipated} = \frac{2 \times R_{on} \times C_L}{T} \times C_L \times V_c^2(T) \tag{3}$$

It is obvious from equation (3) that if T becomes more than $2R_{on}C_L$, i.e., if the transition becomes slow, the loss can be reduced. This led to the usage of "pulsed power supply", also known as "power clock" in adiabatic logic circuits.

The "adiabatic logic families" [41] mostly comprises of cross coupled circuit. They basically contain "dual rail encoded signal paths" i.e. the inputs and outputs both are in true and complemented forms. This structural phenomenon is helpful in simplifying functions, decreasing number of cascades and hence reducing power consumption. The adiabatic families can be distinguished as "fully adiabatic" and "partially or quasi-adiabatic" [41]. The former logic family exhibits zero "non adiabatic" losses along with complex circuitry, difficult "power clock generator" design and large area overhead. Examples of "fully adiabatic logic" circuitry include "Pass Transistor Adiabatic Logic" (PAL) [59] and SCRL [11].In the later version, the entire charge cannot be recovered; hence it realizes some "non adiabatic" losses. "Quasi-adiabatic family" incurs simpler circuit architecture and power clock design. 2N2P logic, 2N-2N2P logic [39], ECRL [36], "Positive Feedback Adiabatic Logic" (PFAL) [40], CPAL [41], "NMOS Energy Recovery Logic" (NERL), "True Single Phase Adiabatic Logic" (TSEL) [52], "Clocked Adiabatic Logic" (CAL) [60], "Source Coupled Adiabatic Logic" (SCAL) [61] etc. are some examples of conventional "quasi-adiabatic logic" families. Three types of losses exist in adiabatic circuits such as "adiabatic loss", "leakage" current loss and "non adiabatic" loss [41]. The "adiabatic losses" are associated with the current flowing through non-ideal switches and are dependent on the clock frequency. The "non adiabatic losses", on the other hand, can be attributed to the voltage difference between the terminals of the switch (V_{th}) and are proportional to $C_L V_{th}^2$ [41].

The four stages of a power clock are termed as "Wait", "Evaluation", "Hold" and "Recovery", as shown in Fig. 3.3 [41].

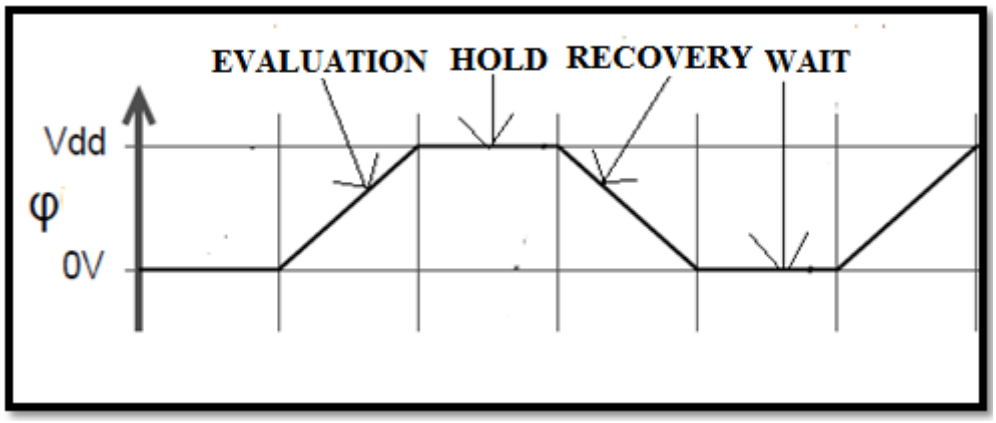

Fig. 3.3 Different Stages of Trapezoidal Clock

The operations performed at each stage of the pulsed clock are as follows:

- Evaluation- Inputs are stable and outputs are evaluated
- Hold- Outputs are applied to various stages
- Recovery- Energy stored in "node capacitors" are transferred to "power supply"
- Wait- Waiting time for symmetry before next iteration starts

Using four phase trapezoidal clock, the inherent pipelining of the circuits [43] can be utilized to eliminate the latches in "retimed circuits", thus reducing power consumption. Adiabatic logic based circuits use this four-phase clock, with a difference of quarter period between two consequent clocks.

Since in this thesis work, adiabatic methodologies of ECRL, 2N-2N2P and CPAL are the main areas of concern, operations of these are discussed vividly.

3.3.1 Efficient Charge Recovery Logic (ECRL)

The schematic of the "Efficient Charge Recovery Logic" (ECRL) inverter circuit is illustrated in Fig. 3.4 [36]. This circuit, being "quasi-adiabatic logic", is based on "Differential Cascode Voltage Switch Logic" and contains "dual-rail encoded signal paths", i.e., both true inputs and their complemented forms are required to evaluate logic properly and it generates both

true and complemented outputs [36]. Cross-coupled PMOS transistors (MP1 and MP2) form the pull-up network, whereas two NMOS transistors (MN1 and MN2) of the pull-down network represent the functional blocks. During the "Evaluation" stage of the clock, inputs a and a_b are turned high and low, respectively. MN1 is turned on and Out node is clamped to the ground level. This node eventually turns on MP2, and Out_b node follows the clock pulse. The valid logic values are retained during the "Hold" stage. As the clock falls from V_{dd} in the "Recovery" stage, charge at Out_b is recovered to the power supply in adiabatic manner. The ECRL logic family suffers from "non adiabatic" loss [35] which is represented by (C_L. V_{tp}^2), where V_{tp} is the "threshold voltage" of PMOS transistor. Other disadvantages associated with this circuit are observed to be the coupling effects caused by interference of two outputs connected by PMOS latch and "floating outputs" [35].

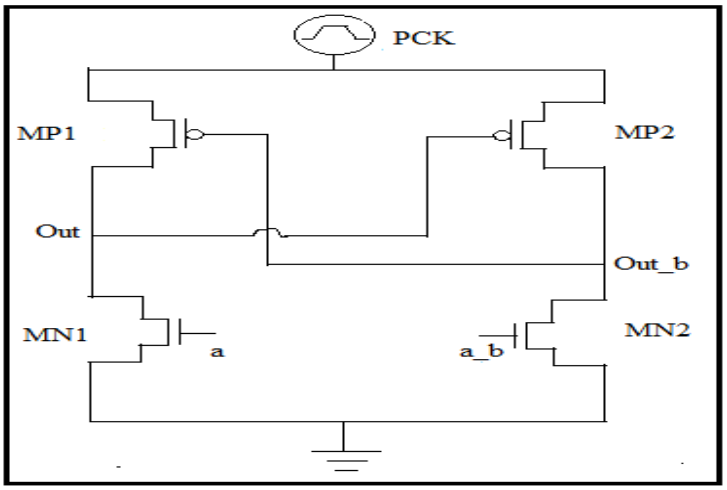

Fig. 3.4 Schematic of ECRL Inverter

3.3.2 2N-2N2P Logic

This adiabatic approach is an extension of ECRL, consisting of two additional cross-coupled NMOS transistors, MN1 and MN2, connected in parallel to functional blocks of ECRL [39]. The main disadvantage associated with ECRL is the presence of "floating outputs". These additional NMOS transistors are incorporated to compensate this limitation, thereby providing non-floating stable output levels for prominent part of the "Recovery" stage and minimum crosstalk. This logic adopts differential signaling logic and generates both true and

complemented outputs [39]. 2N-2N2P based inverter circuit is shown in Fig. 3.5 [39], where two NMOS transistors, MN3 and MN4 represent the functional blocks. The "non adiabatic" loss is similar to that of ECRL.

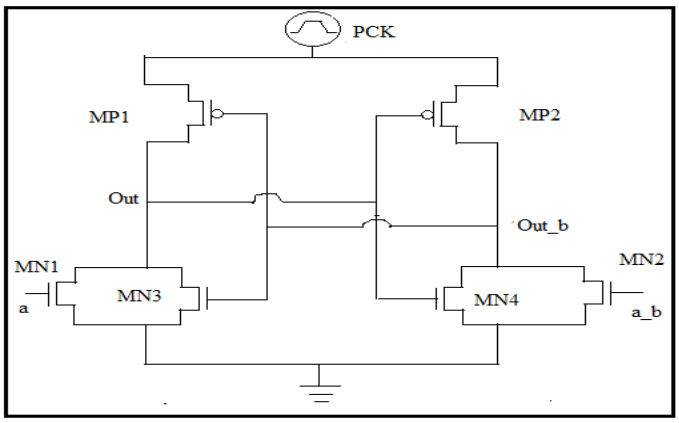

Fig.3.5 Schematic of 2N-2N2P Inverter

3.3.3 Complementary Pass Transistor Adiabatic Logic (CPAL)

CPAL [41] is a unique approach to realize more efficient low power circuit design, due to the elimination of "non adiabatic" losses by the use of "complementary pass transistor logic" for evaluation stage and "transmission gates" for recovering energy following adiabatic process. The circuit design is simpler due to its regular architecture. The structural design is also modular as only the permutation of input signals is required to implement various gate functions. The circuit is operated under single power clock supply and contains "dual-rail encoded signal paths". Due to the presence of "complementary pass transistor", the circuit exhibits properties like low input capacitance and high speed of operation [42]. Fig. 3.6 [41] depicts the basic circuit of CPAL inverter.

The logic circuitry consists of two parts: the logic function block, realized by NMOS transistors MN5, MN6, MN7, and MN8 and the "bootstrapped load driven" circuitry, comprised of two transmission gates MN1, MP1 and MN2, MP2. MN3 and MN4 act as clamp transistors to ground the un-driven output [41].

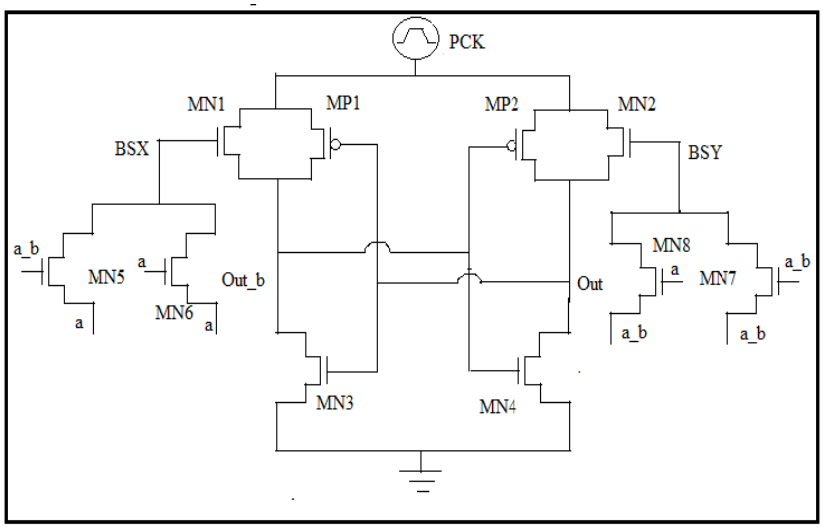

Fig. 3.6 Schematic of CPAL Inverter

"Bootstrapping" technique is used to feedback some part of output to the input of the circuit in power efficient VLSI design. This technique involves a pair of transmission gates which helps to retrieve part of the energy from the bootstrapped nodes BSX and BSY. Thus, it cancels the "non adiabatic" losses. The advantages of CPAL help it to outperform other aforementioned adiabatic technologies in various aspects [45, 49].

Initially, the input node a is kept high and its complement input node a_b is kept low. Thus, MN6 is turned on and it pre-charges the bootstrapped node BSX to $V_{dd} - V_{tn}$, V_{tn} being threshold voltage of NMOS. Simultaneously, MN7 is turned on and the node BSY is discharged to ground. During the "Evaluation" stage, with the clock increasing towards V_{dd}, MN1 is turned on and the node Out_b follows the rising clock pulse. Eventually, as Out_b exceeds V_{tn}, MN4 is turned on and Out node is grounded. As the Out node attains the voltage of V_{tp}, MP1 is activated and transmission gate MN1, MP1 charges Out_b to full swing output. During the "Hold" stage, the output nodes are maintained at stable logic levels. As the clock falls towards the ground, node Out_b charge is recovered following adiabatic process [56].

CHAPTER 4

PROPOSED MODEL OF 8-BIT VEDIC MULTIPLIER USING COMPLEMENTARY PASS TRANSISTOR ADIABATIC LOGIC (CPAL)

4.1 Overview

This chapter gives a brief description of the design environment used for the work presented in this thesis followed by vivid architectural implementation of the proposed "Urdhva Tiryagbham sutra" based 8-bit CPAL Vedic multiplier. Design of CMOS and other adiabatic methodologies like 2N-2N2P and ECRL based 8-bit Vedic multipliers are also presented to obtain comparative performance analysis in this thesis. The descriptive design of several segments of the multiplier architecture along with gate level designs is also analyzed in this chapter.

4.2 Design Environment

The simulation platform used in all the designs is TANNER SPICE version 16.0, which provides a CMOS level design of the proposed structure along with information regarding power consumption and delay. The settings of different parameters for the design of the proposed model as well as for the entire simulations have been summarized below:

- All the design structures are simulated referring to150 nm technology.

- The architectures are operated at a frequency of 20 MHz and analyzed for the load value of 30 fF.

- As per the requirement of drastic power saving in adiabatic circuits, slow transition clock power supply, i.e. trapezoidal clock is applied at the supply. In this thesis, both the rise time and fall time of the clock are considered to be 4 ns and pulse width to be 20 ns.

- Varied bit patterns with pulse width of 100 ns and both rise time and fall time of 1 ns is applied as inputs in all the simulations.

- All the simulations are carried out with the voltage of 5 V.

4.3 Architecture of the Proposed 8-bit Vedic Multiplier

The basic architecture of 8-bit Vedic multiplier is illustrated in Fig. 4.1. The 8-bit Vedic multiplier is formed of four 4-bit Vedic multipliers, one OR gate and three 8-bit Ripple Carry Adders. To understand the entire architecture, the design of 4-bit multiplier circuit consisting of four 2-bit Vedic multipliers, one OR gate and three 4-bit Ripple Carry Adders has been depicted in Fig. 4.2. In this context, the internal circuit of 2-bit Vedic multiplier, which comprises of four AND gates and two Half Adders is also depicted in Fig. 4.3. The designs are carried out in accordance with the mathematical expressions of Vedic multiplication described in the previous chapter.

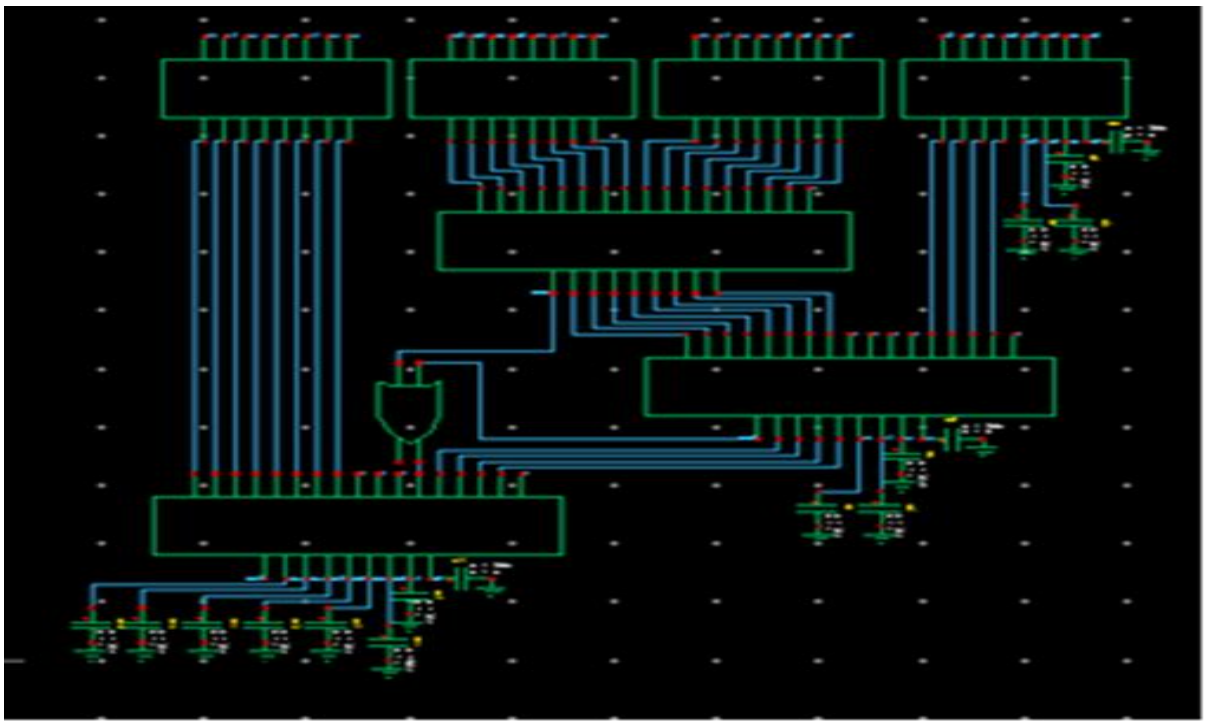

Fig. 4.1 Proposed 8-bit Vedic Multiplier

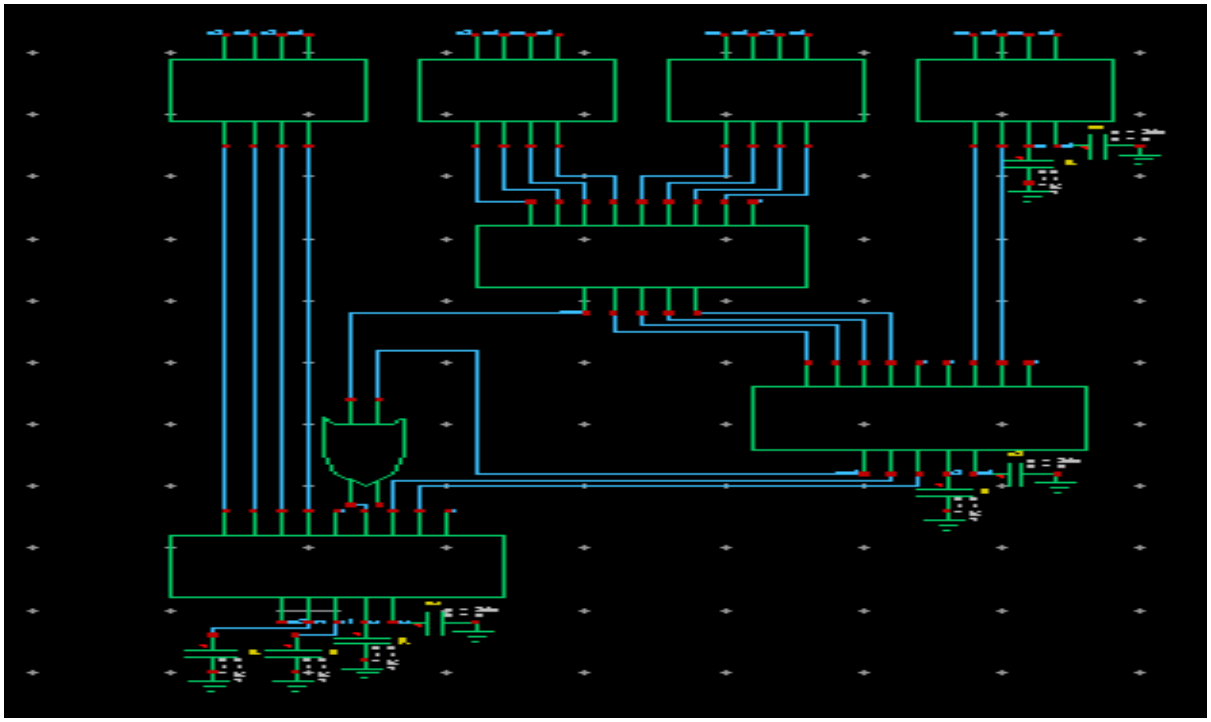

Fig. 4.2 4-bit Vedic Multiplier

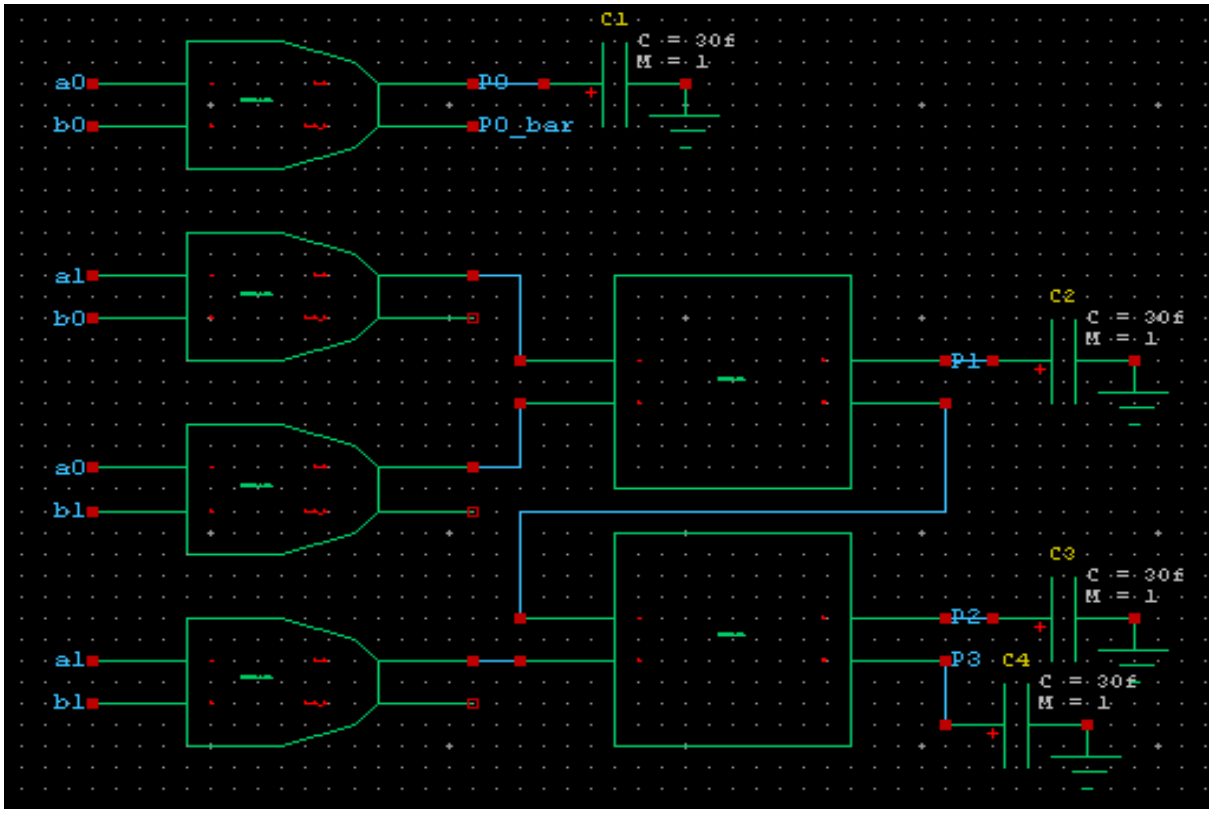

Fig. 4.3 2-bit Vedic Multiplier

In this thesis, initially, 2x2 power-efficient multiplier has been designed, based on which 4x4 multiplier has been developed. This design has further been explored for the design of 8x8 low power multiplier circuits. The internal circuitry of each block and sub-blocks of the multiplier circuits contains various logic gates and functional blocks like Half Adders, Full Adders etc. All the designs are implemented using CPAL adiabatic logic in this thesis. Moreover, the implementation of basic gates based on CMOS, 2N-2N2P and ECRL are also demonstrated in this section for the purpose of comparison.

4.3.1 Design of Logic Gates using CMOS Logic

The design of CMOS basic gates namely AND, OR and XOR are shown in Fig. 4.4, 4.5 and 4.6 respectively. All these gates are assimilated together to obtain the desired architecture.

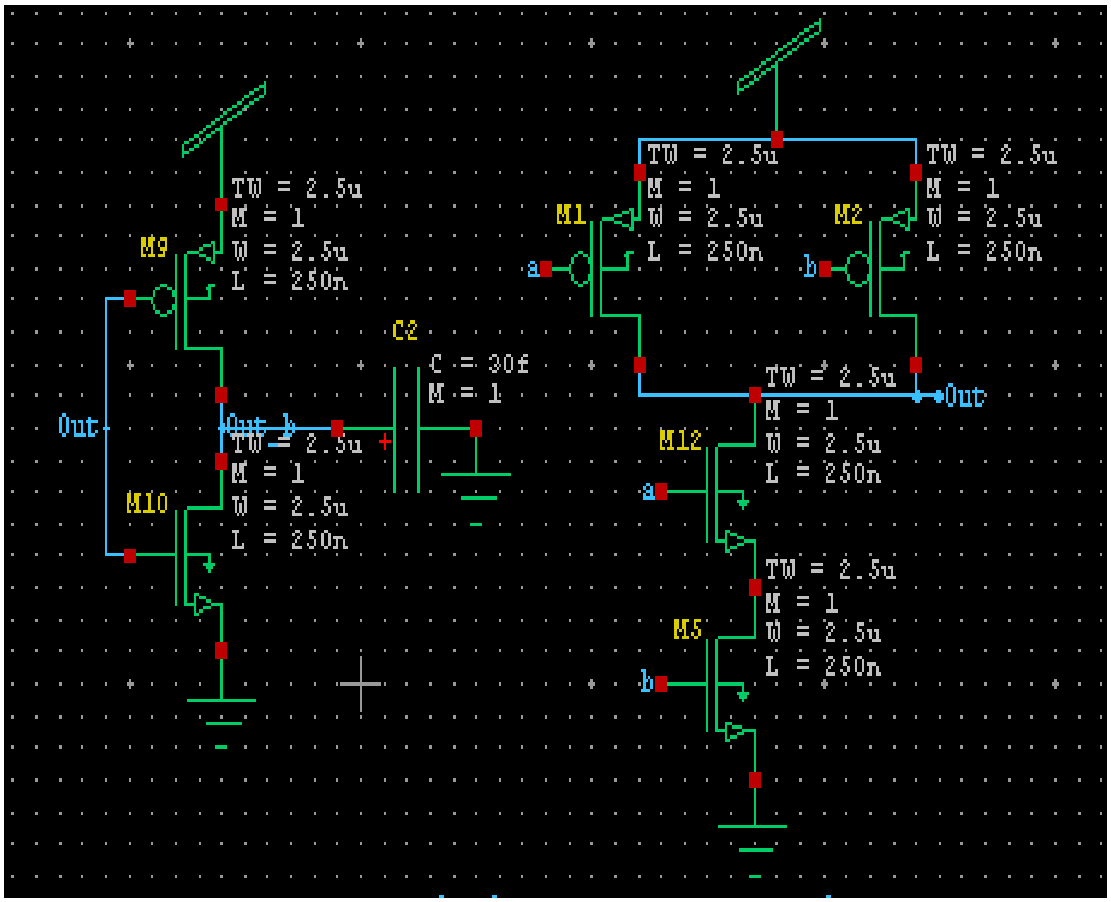

Fig. 4.4 Schematic of CMOS AND Gate

In the Fig. 4.4, the pull down NMOS network is implemented using a.b function. Using the duality principle on the pull down network, the pull up PMOS network is based on a+b function. The entire circuit produces NAND output, which on inversion produces AND output.

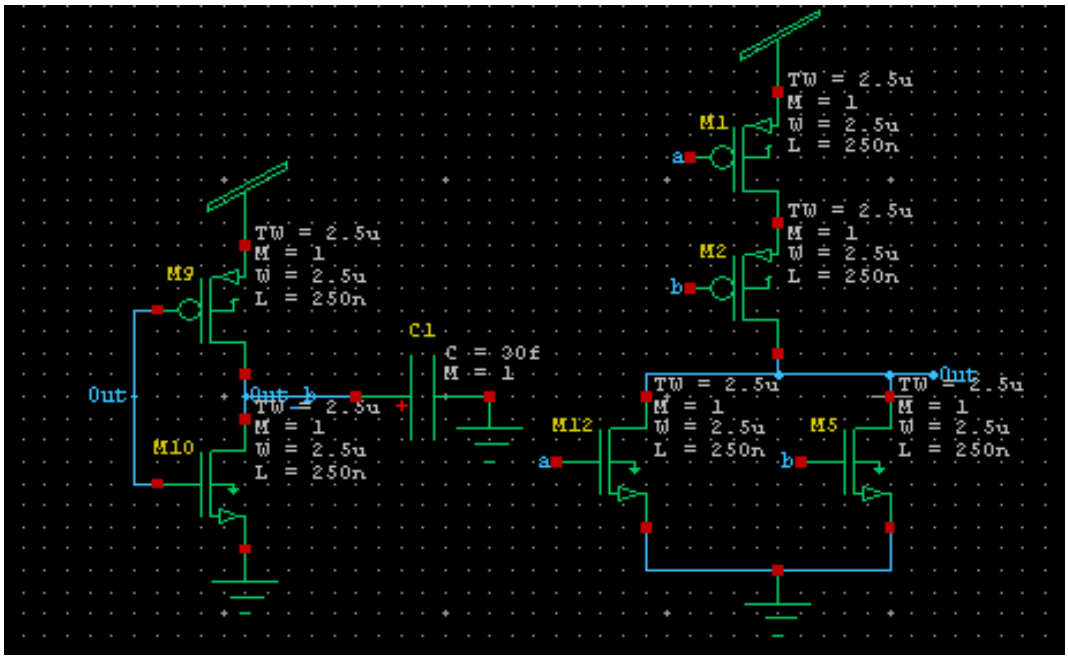

Fig. 4.5 Schematic of CMOS OR Gate

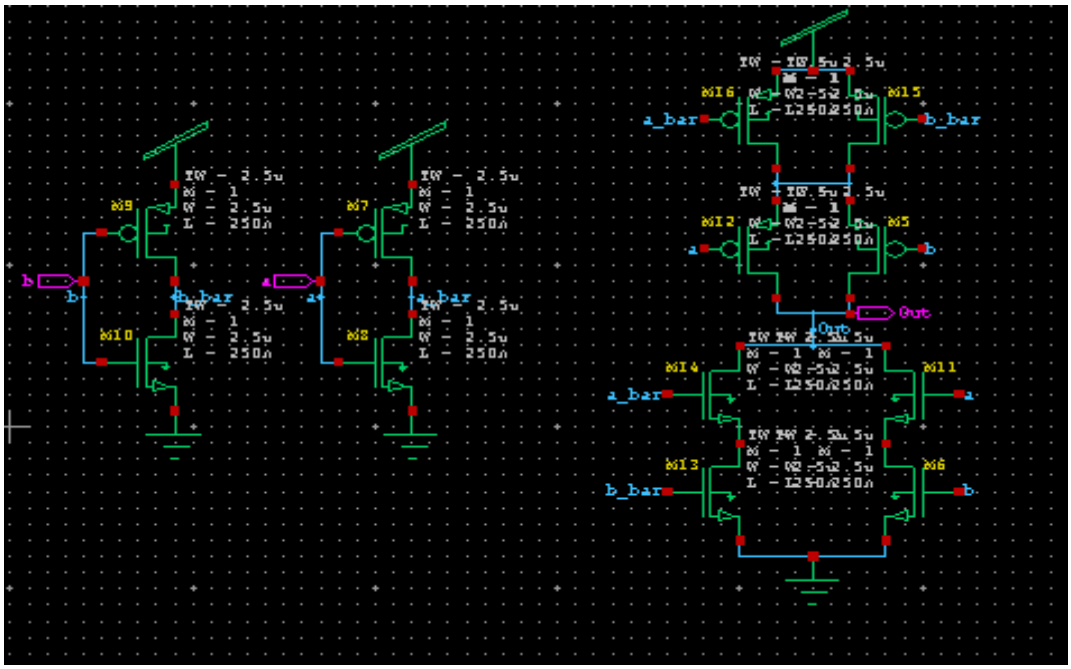

Fig. 4.6 Schematic of CMOS XOR Gate

Similarly, in CMOS OR gate schematic, function a+b is applied at the pull down NMOS network and its dual function a.b is applied at the pull up PMOS network, thus generating NOR output function. Inverter is used to generate the OR output. On the other hand, in CMOS XOR gate, inverted version of XOR output, i.e. (a_bar.b+a.b_bar)'= (a.b+a_bar.b_bar) forms the NMOS pull down network, and its dual function forms the PMOS pull up network. The pull down and pull up networks combine together to form the XOR circuit.

4.3.2 Design of Logic Gates using 2N-2N2P Adiabatic Logic

As described in the Chapter 3, adiabatic logic families recover energy during discharge phase of slow transition clock supply, thus decreases the power dissipation during switching to a large extent. 2N-2N2P, belonging to quasi-adiabatic family, recovers the energy partially, thus making the design efficient compared to CMOS technology. This point has also been established in literature survey. The pull up PMOS network is used to recover energy whereas the pull down network represents the logic functions in addition with an extra cross coupled NMOS transistors. Both the outputs and the inputs in this design are in true form as well as complemented form. The designs of basic gates such as AND, OR and XOR required for implementation of 8-bit Vedic multiplier using 2N-2N2P logic are visualized in Fig. 4.7, 4.8 and 4.9 respectively.

In the Fig. 4.7, a set of NMOS transistors in pull down network are connected to implement a.b function. Connection of another set of pull down NMOS transistors implements the dual version of a.b. Combination of the PMOS and NMOS networks lead to the generation of both AND output (Out) and NAND output (Out_b).

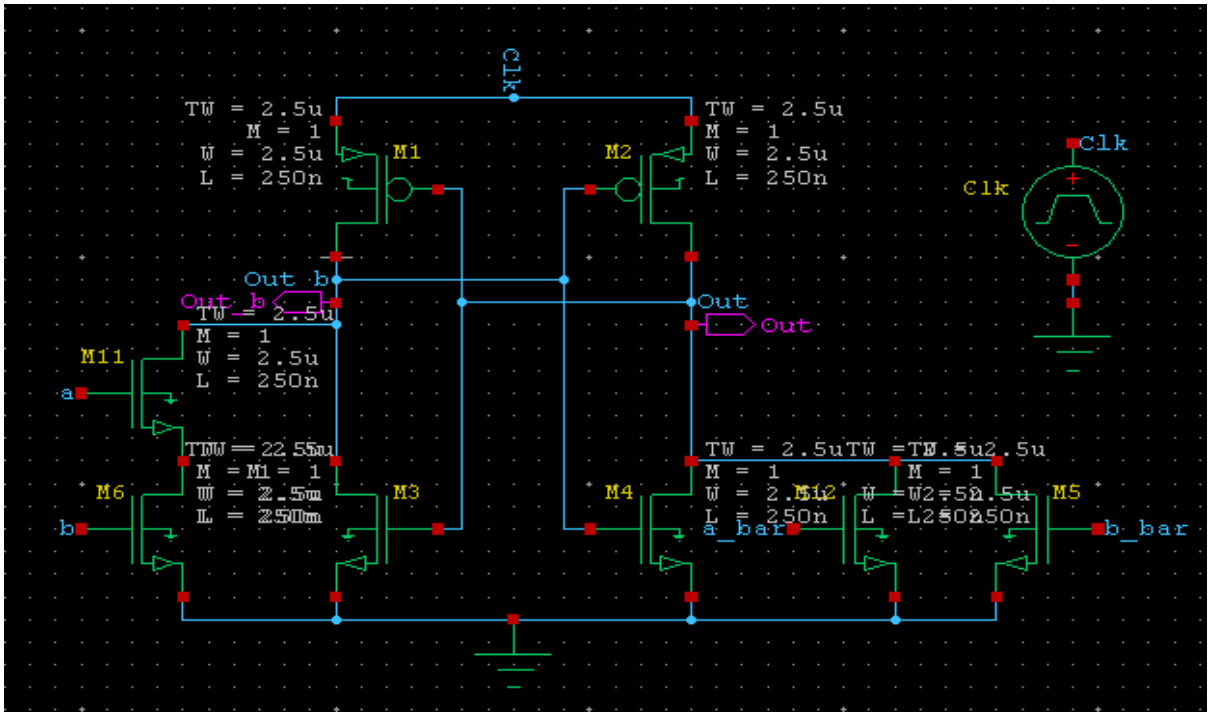

Fig. 4.7 Schematic of 2N-2N2P AND Gate

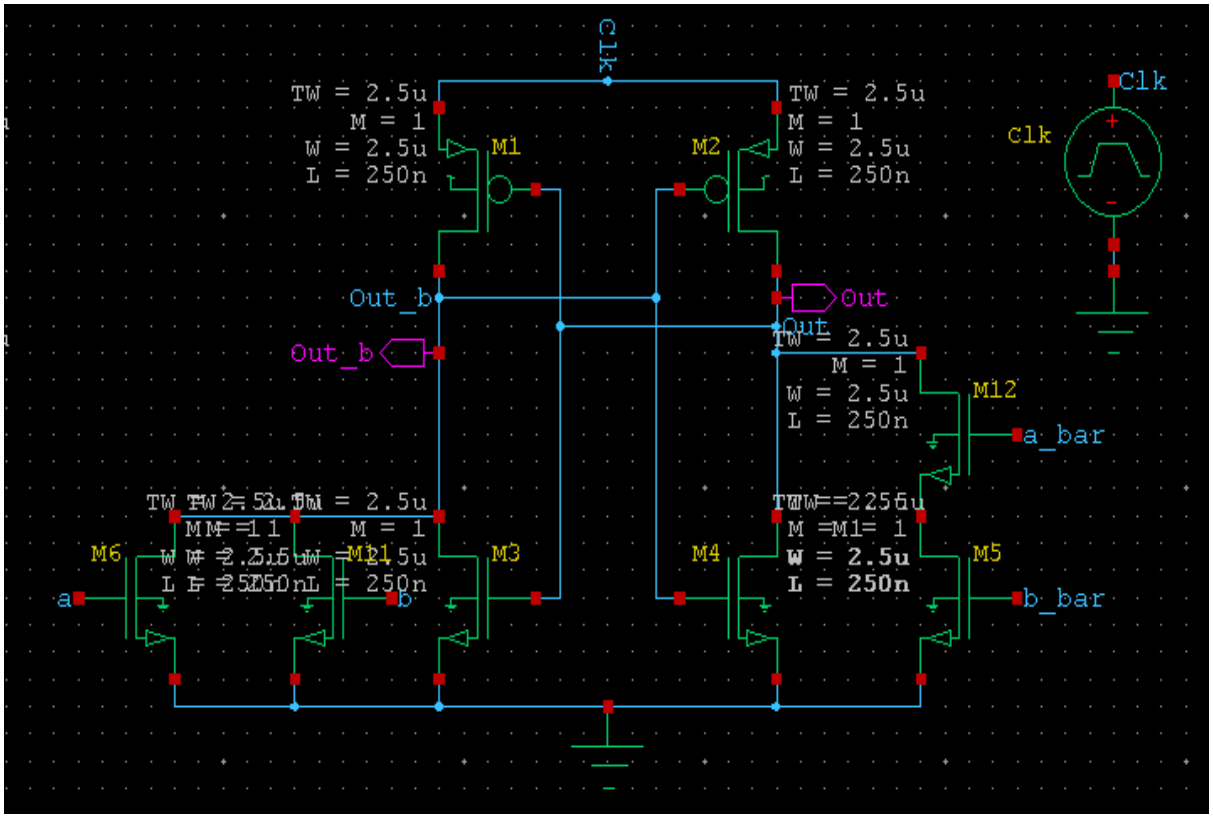

Fig. 4.8 Schematic of 2N-2N2P OR Gate

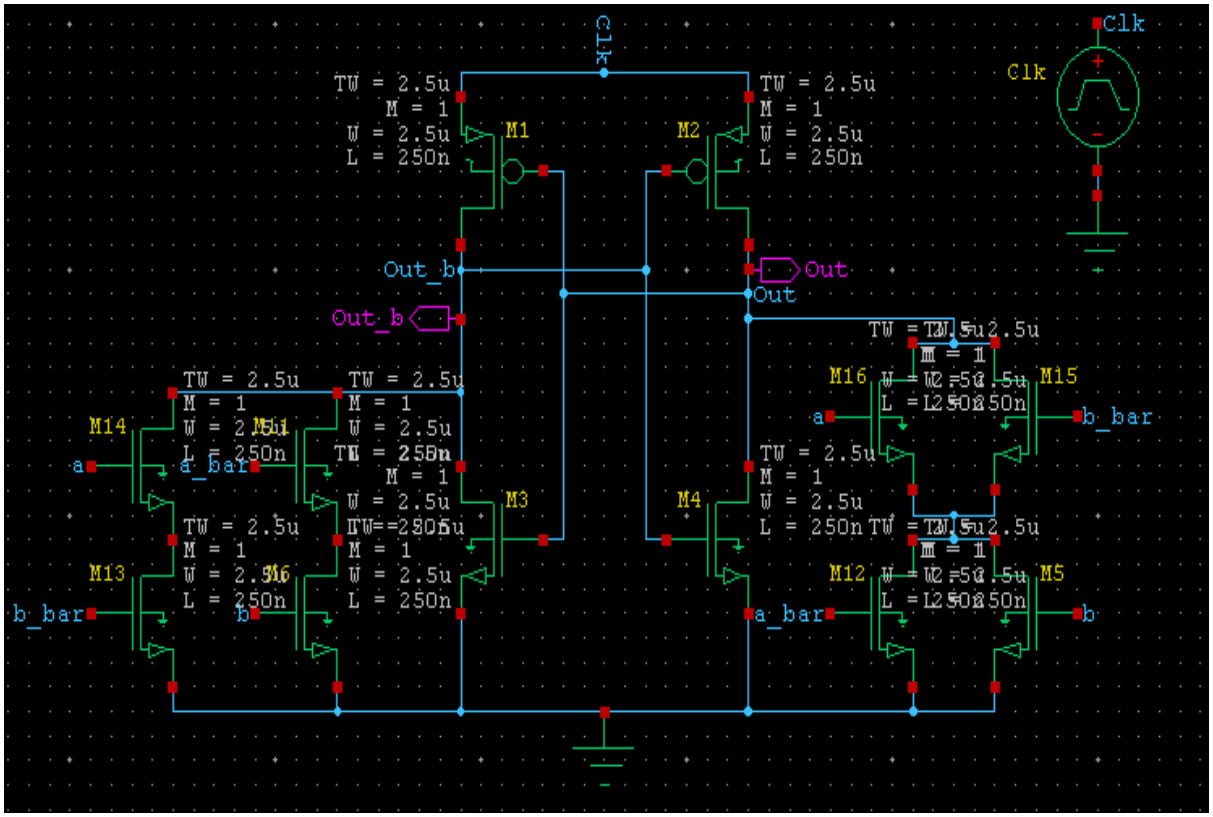

Fig. 4.9 Schematic of 2N-2N2P XOR Gate

The schematic of 2N-2N2P OR gate portrays the implementation of both a+b function and its dual function in the pull down network to produce both OR output namely Out and NOR output namely Out_b in a single design. A similar design of architecture is followed in the schematic of XOR gate, where both the function (a_bar.b+a.b_bar) and its dual version are represented by networks of NMOS transistors.

4.3.3 Design of Logic Gates using ECRL Adiabatic Logic

ECRL is another example of quasi-adiabatic logic circuits as discussed in previous chapter. The cross coupled PMOS transistors form the pull up network as similar to 2N-2N2P. But the pull down network in this case only consists of true and complemented NMOS logic functional blocks. The efficiency of this design is based on partial energy recovery with respect to CMOS technology.

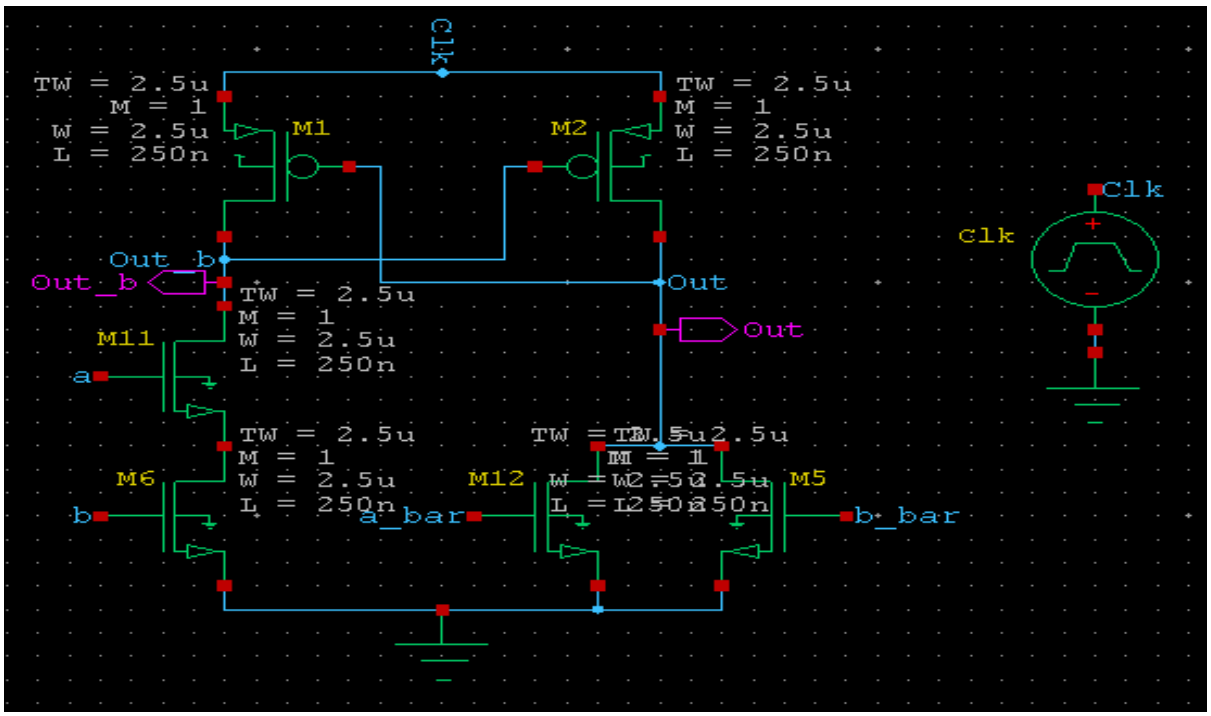

Fig. 4.10 Schematic of ECRL AND Gate

Fig. 4.10 depicts the circuit diagram of AND gate based on ECRL logic. Similar to the previous adiabatic logic circuit of AND gate, this cross coupled circuit is comprised of a.b function and its dual version as functional blocks to obtain Out and Out_b.

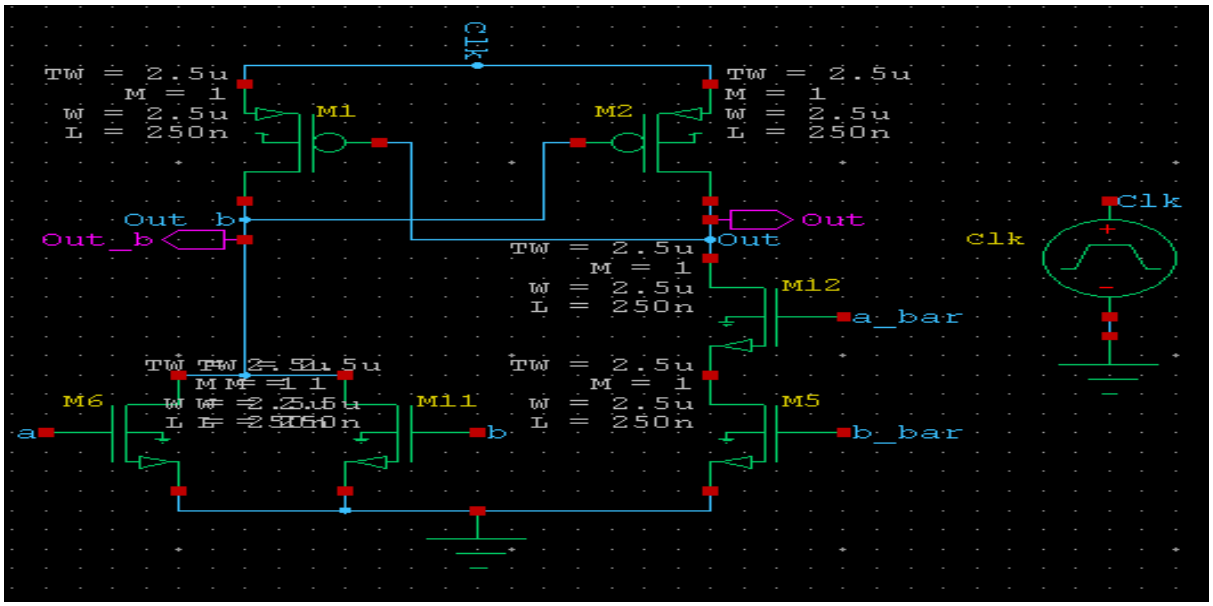

Fig. 4.11 Schematic of ECRL OR Gate

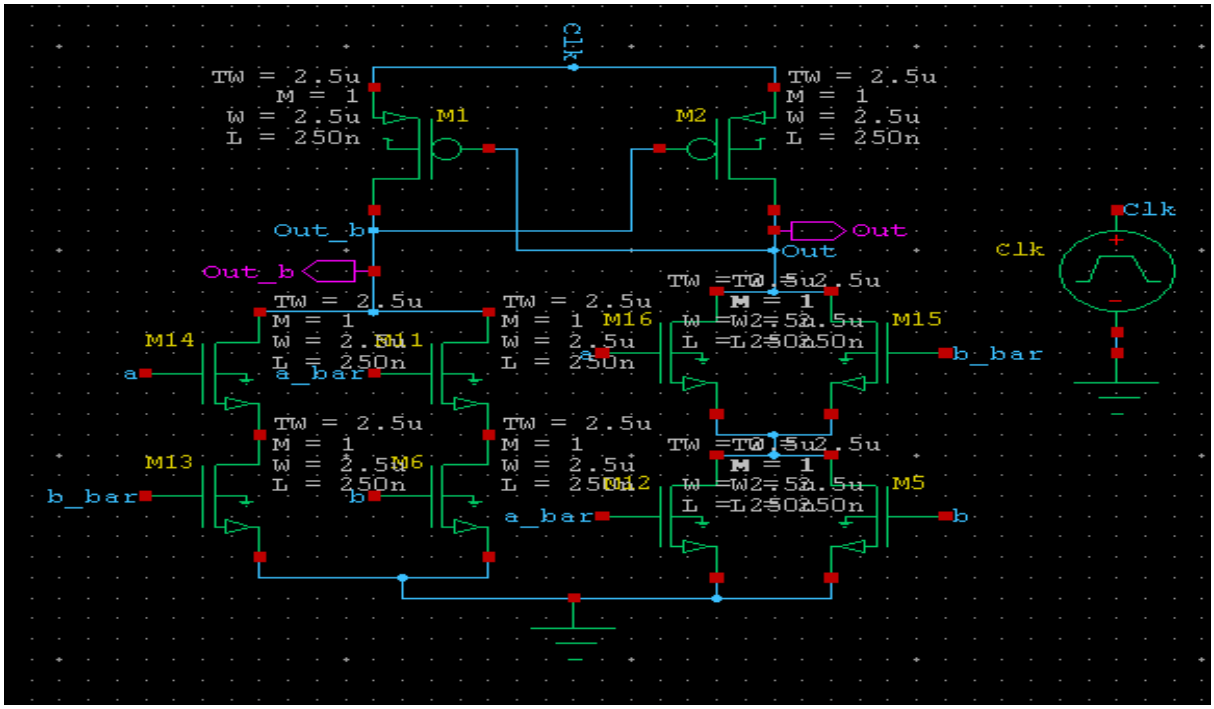

Fig. 4.12 Schematic of ECRL XOR Gate

Fig. 4.11 and 4.12 shows the circuit design of ECRL OR and XOR gate respectively. The NMOS connections of logic blocks in the pull down networks of both OR gate and XOR gate are the same as that of 2N-2N2P logic design.

4.3.4 Proposed Design of Logic Gates using CPAL Adiabatic Logic

The main advantage of CPAL adiabatic logic, as discussed previously, is due to the elimination of non adiabatic loss by introduction of complementary pass transistors and transmission gate. These make CPAL logic the most efficient among all the aforementioned design technologies. Another advantage is that various basic gate functions can be obtained by only permutation of inputs in the same circuit. Fig. 4.13, 4.14 and 4.15 display the basic logic gate circuits such as AND, OR and XOR respectively based on CPAL.

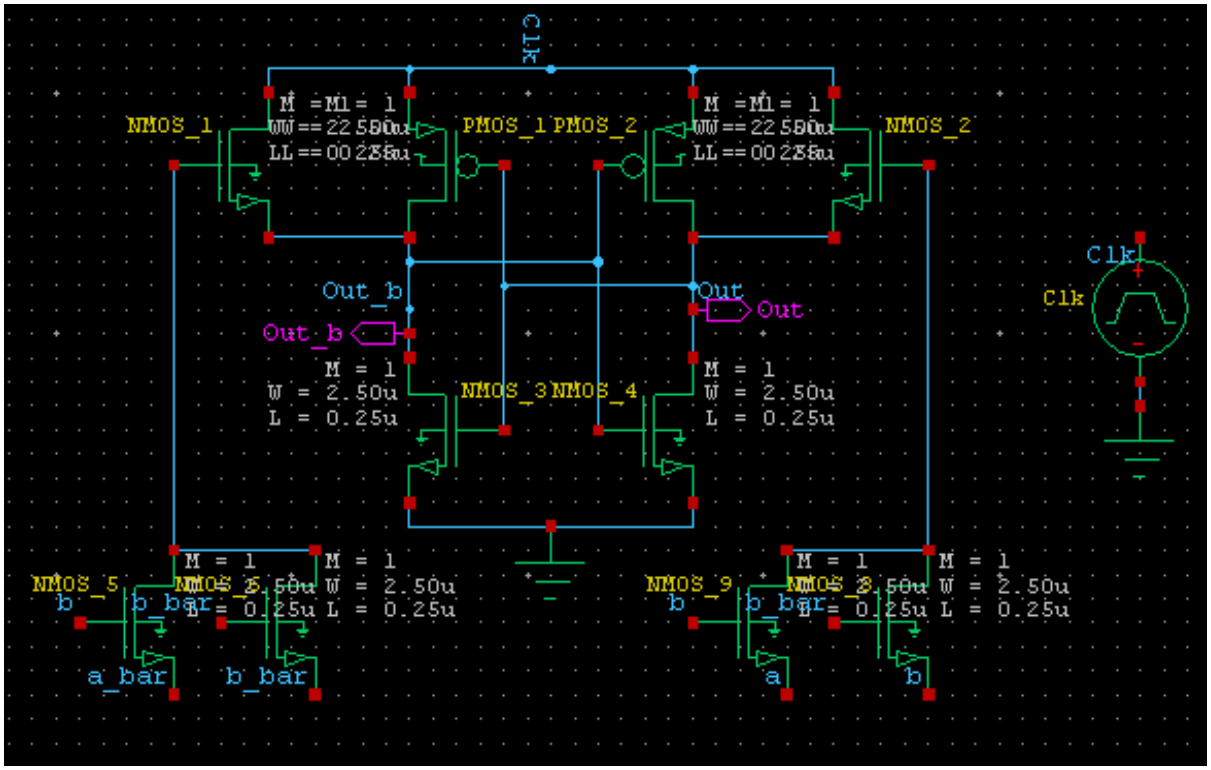

Fig. 4.13 Schematic of CPAL AND Gate

In CPAL AND gate design, the inputs a, b and their complemented forms a_bar and b_bar are applied to the complementary pass transistor design. The combinations of inputs to the circuits generate a.b function at Out node and its complemented function at Out_b node.

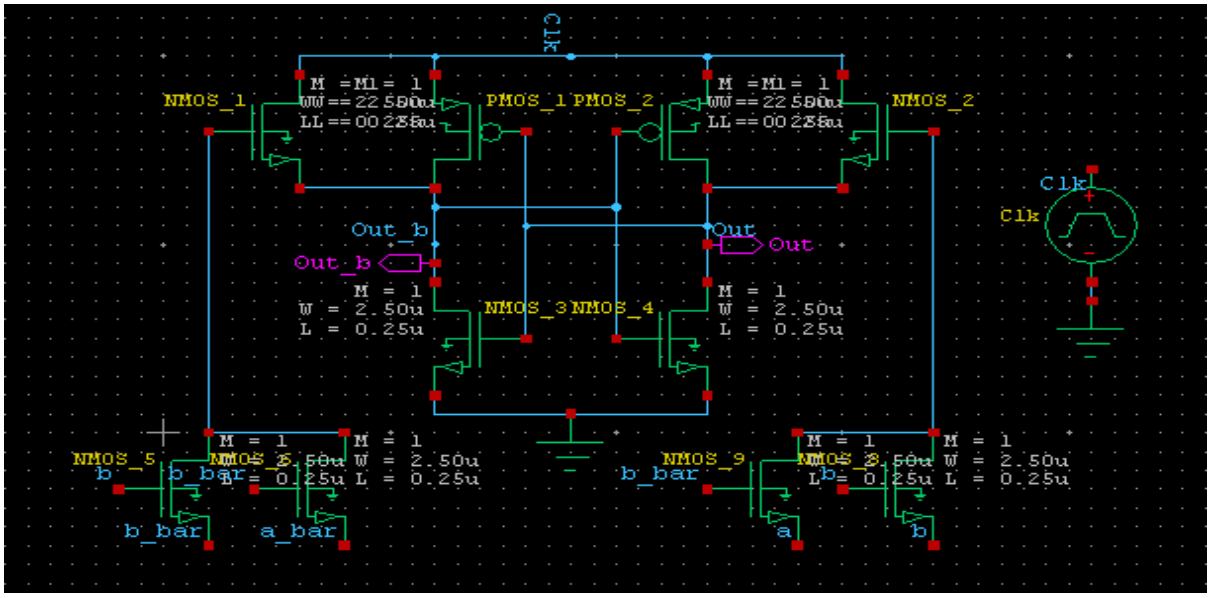

Fig. 4.14 Schematic of CPAL OR Gate

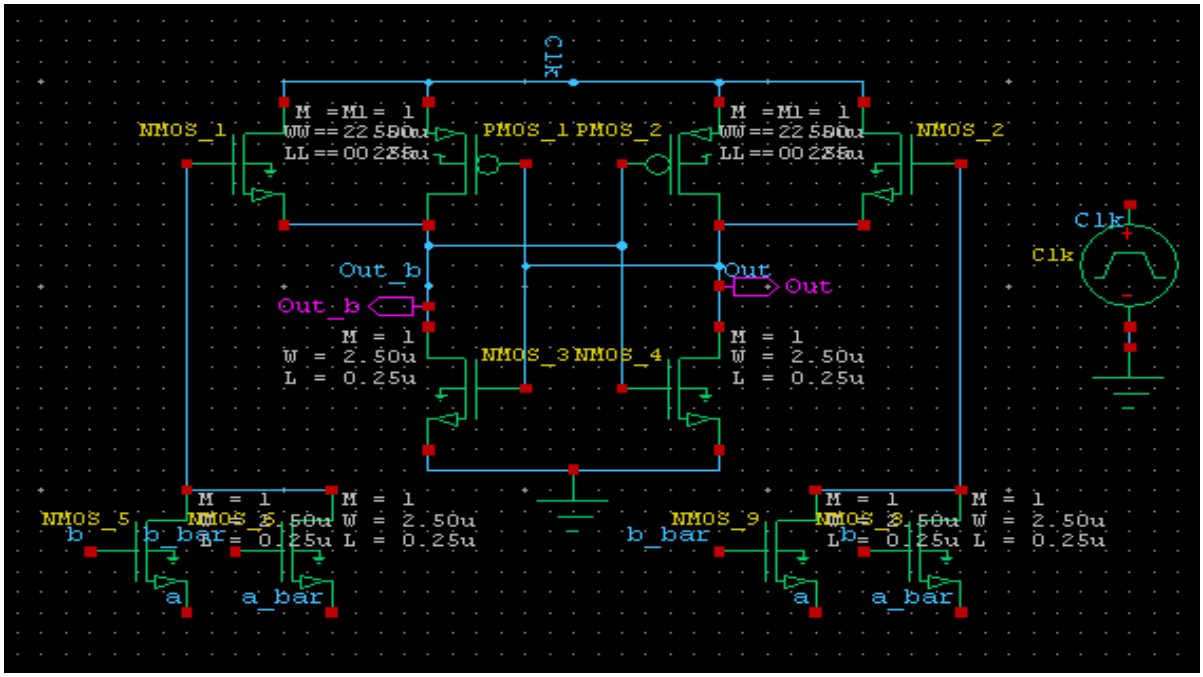

Fig. 4.15 Schematic of CPAL XOR Gate

In a similar fashion, in CPAL OR and XOR circuits, modification of the input combinations is sufficient enough to produce respective outputs in true and complemented forms.

4.3.5 Design of Basic Functional Blocks

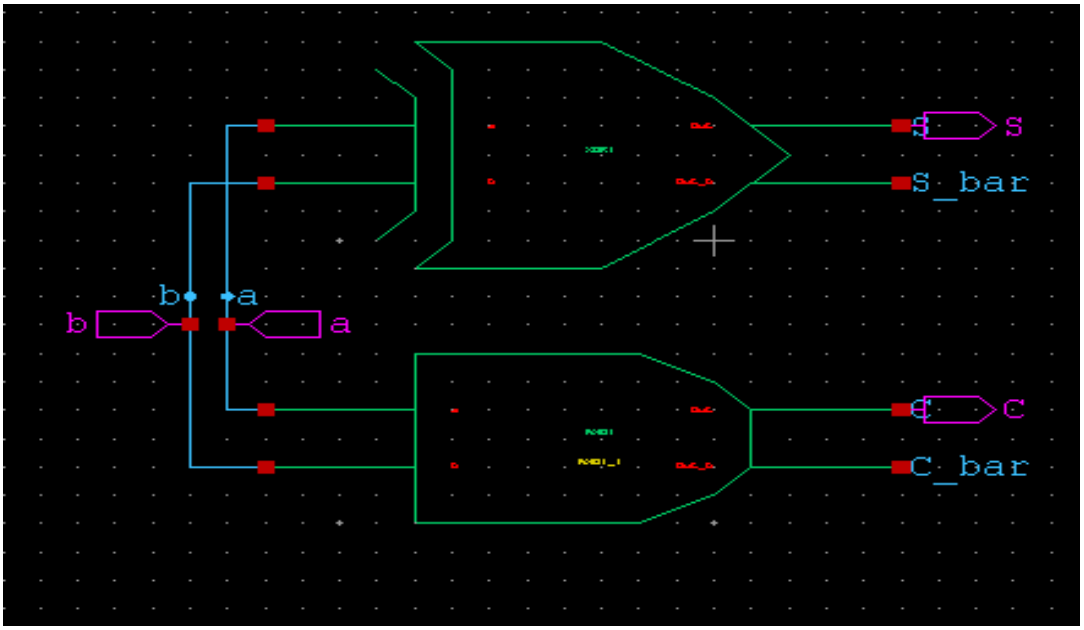

Fig. 4.16 Schematic of Half Adder Block

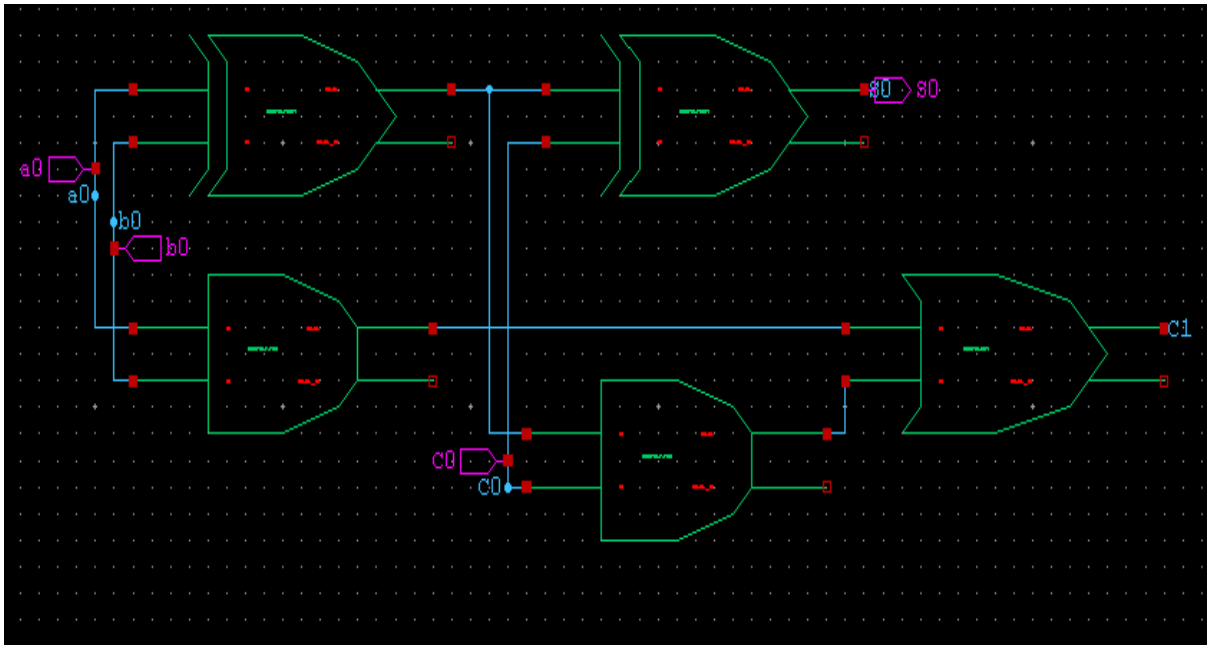

Fig. 4.17 Schematic of Full Adder Block

Fig. 4.16 represents the gate level design of Half Adder circuit whereas Fig. 4.17 demonstrates the gate level design of Full Adder circuit, which are implemented by appropriate assimilation of the basic gates explained previously. The Half Adder circuit acts as a sub-block in design of 2-bit Vedic multiplier. The Full Adder circuit is used to design Ripple Carry Adder circuit, which is required in 4-bit and 8-bit Vedic multipliers.

4.4 Discussions

In this chapter, the design parameters required for the proper simulation of the circuits are summarized in details. In addition to this, the circuit design of basic gates for different methodologies and gate level design of blocks are also depicted here for better understanding. All these designs are used to implement the architecture of 8-bit Vedic multiplier successfully.

CHAPTER 5

SIMULATION RESULTS

5.1 OVERVIEW

This chapter summarizes the simulation results of the work and their critical analysis. Initially, a multiplier based on "Urdhva Tiryagbham sutra" of ancient "Vedic mathematics" is selected for performing binary multiplication with high speed. This unique multiplier architecture is combined with a novel power efficient adiabatic logic, CPAL. Hence, both the advantages of high speed and low power have been incorporated in the proposed multiplier circuit. The proposed design has been implemented using 150 nm VLSI technology in TSPICE platform. The effectiveness of the proposed design has been evaluated by comparing its performance with different design methodologies of CMOS, 2N-2N2P and ECRL.

The flow of this chapter is as follows: Initially, the outputs of the Urdhva Triyagbhum based multipliers of different sizes using different logics such as CMOS, 2N-2N2P, ECRL and CPAL have been presented through timing diagrams for various inputs. Additionally, output waveforms for these designs are also demonstrated to establish the proper simulation of these comparative models. Later, the comparative performance analysis of the proposed multiplier design with respect to CMOS, 2N-2N2P and ECRL has been summarized. The comparison is drawn on the basis of essential design parameters namely power, delay and PDP. Moreover, the analysis is carried out for all 2-bit, 4-bit and 8-bit multipliers.

5.2 OUTPUT WAVEFORMS OF CMOS VEDIC MULTIPLIER

The output waveforms of 2-bit, 4-bit and 8-bit CMOS Vedic multiplier are illustrated in Fig. 5.1, Fig. 5.2 and Fig. 5.3 respectively. The outputs of the multipliers subjected to various inputs have been summarized in Table 5.1. The results are in resemblance with the theoretical calculations. The analysis is carried out for a period of 400 ns and each value of input conditions is validated for a period of 100 ns in all the cases.

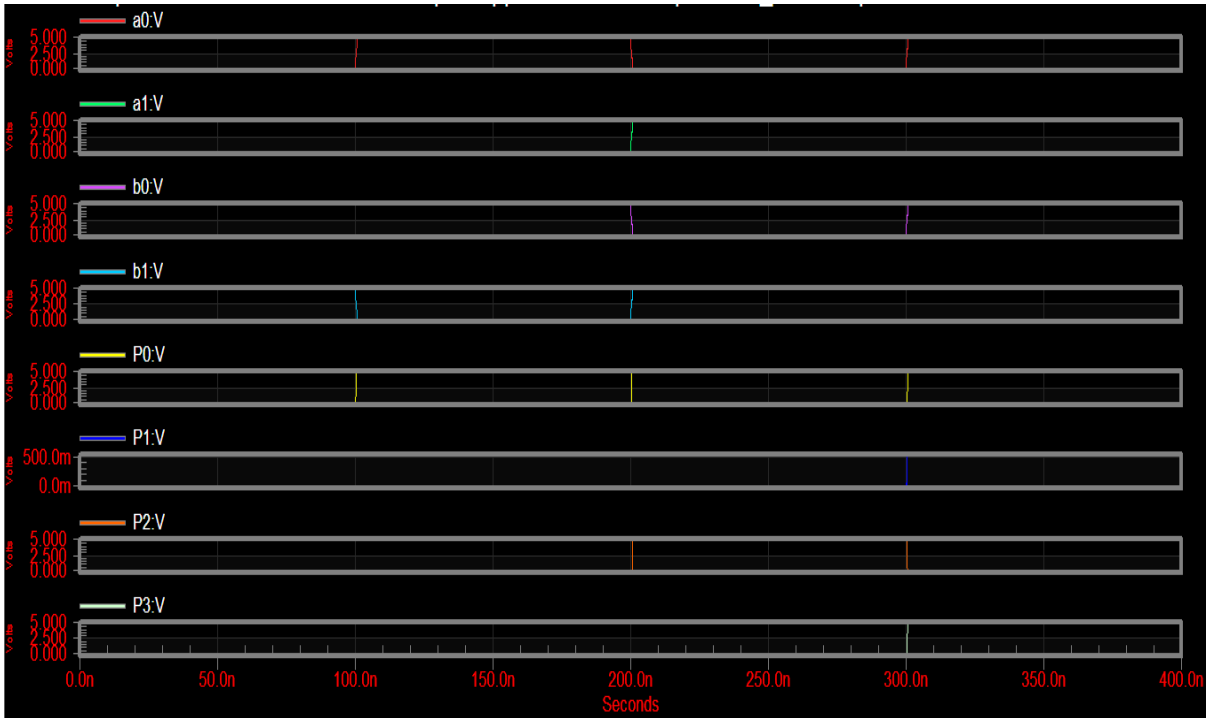

Fig. 5.1 Output Waveform of 2-bit CMOS Vedic Multiplier

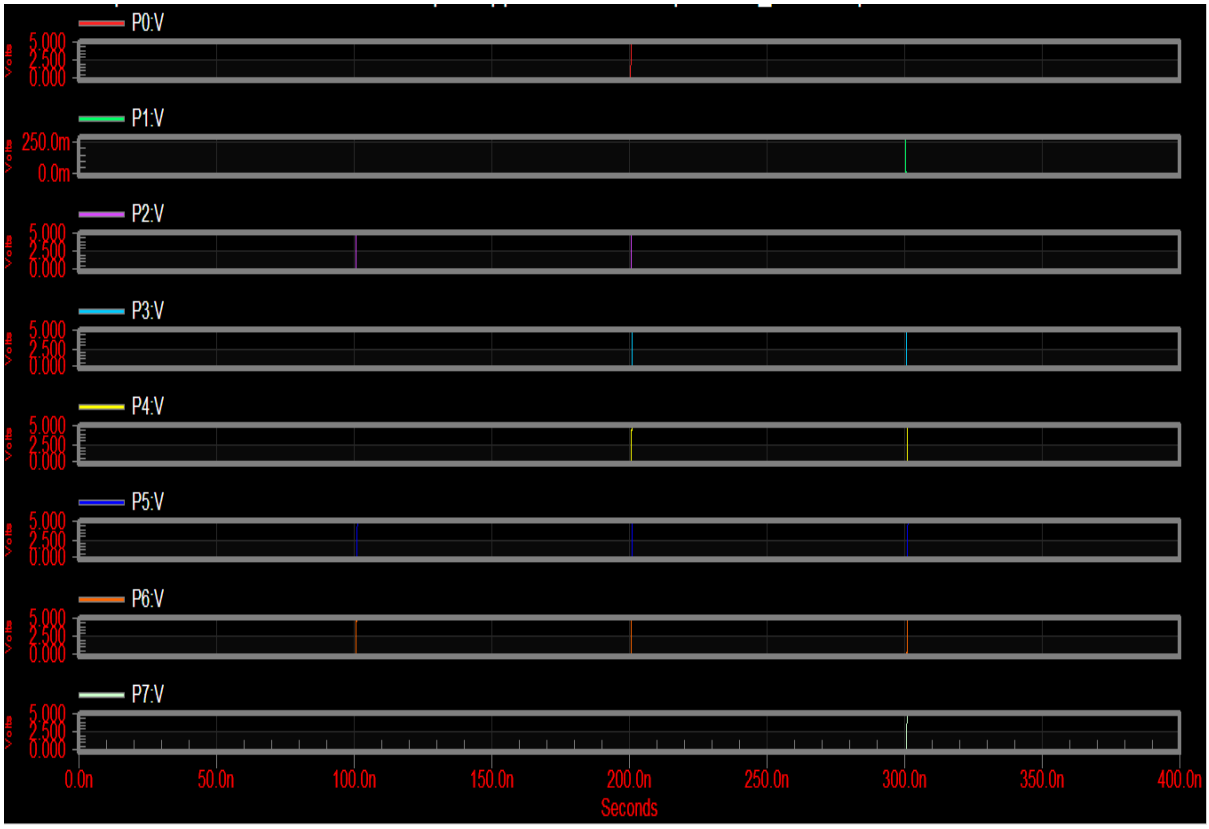

Fig. 5.2 Output Waveform of 4-bit CMOS Vedic Multiplier

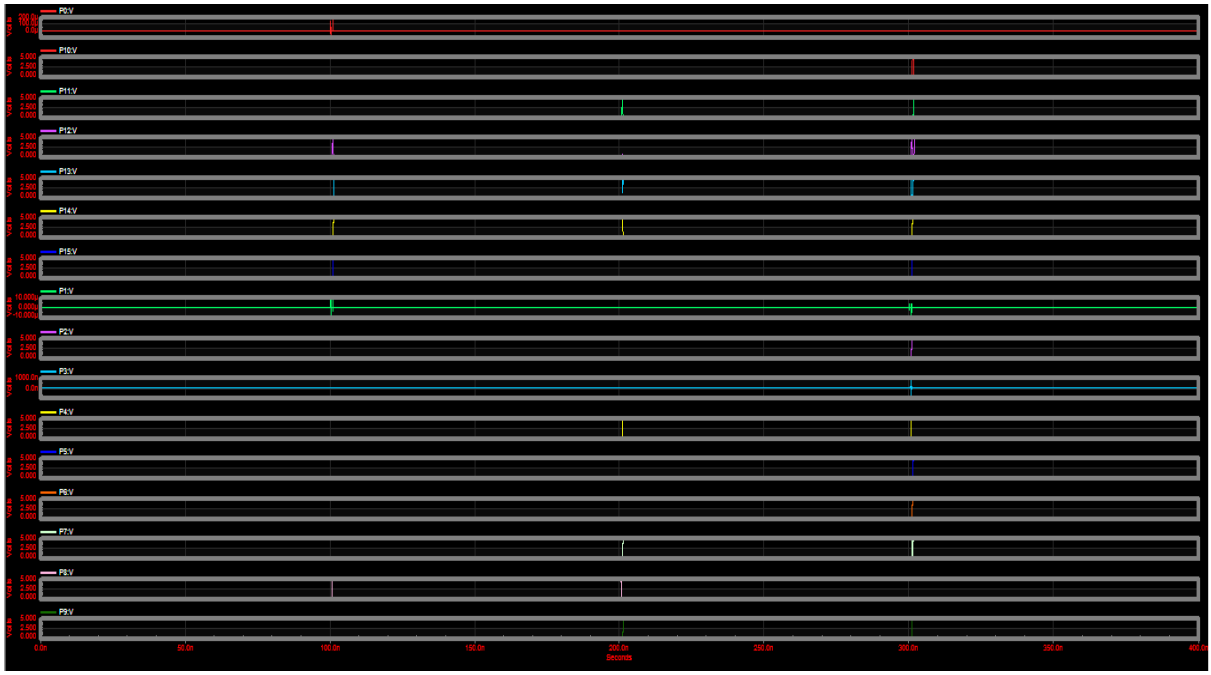

Fig. 5.3 Output Waveform of 8-bit CMOS Vedic Multiplier

5.3 Output Waveforms of 2N-2N2P Vedic Multiplier

The output waveforms of 2-bit, 4-bit and 8-bit 2N-2N2P Vedic multiplier are given in Fig. 5.4, Fig. 5.5 and Fig. 5.6 respectively. The input conditions and analysis period are kept same and the practical results are obtained in conformity with the theoretical results.

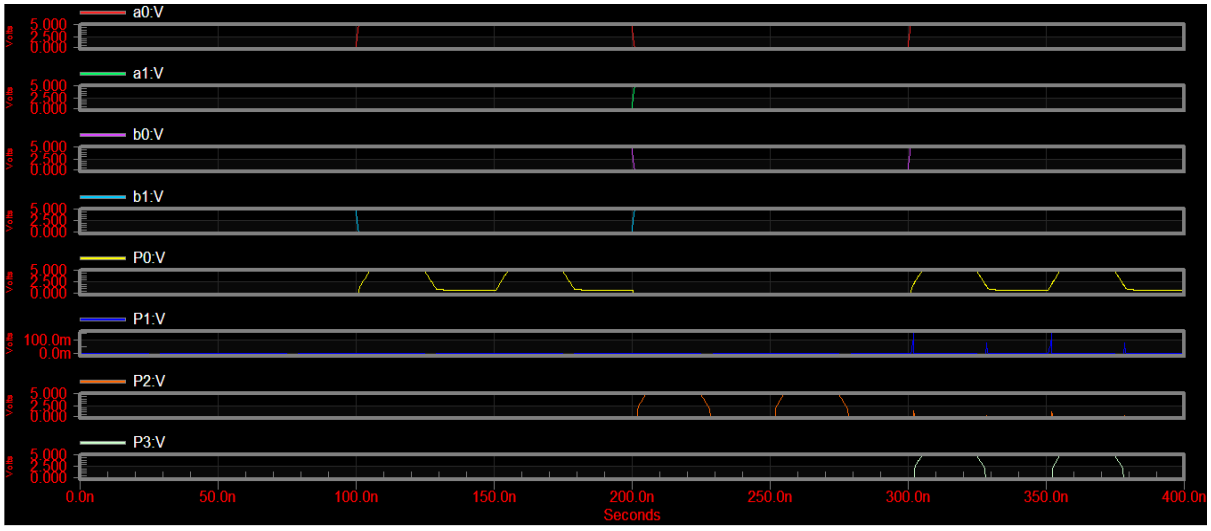

Fig. 5.4 Output Waveform of 2-bit 2N-2N2P Vedic Multiplier

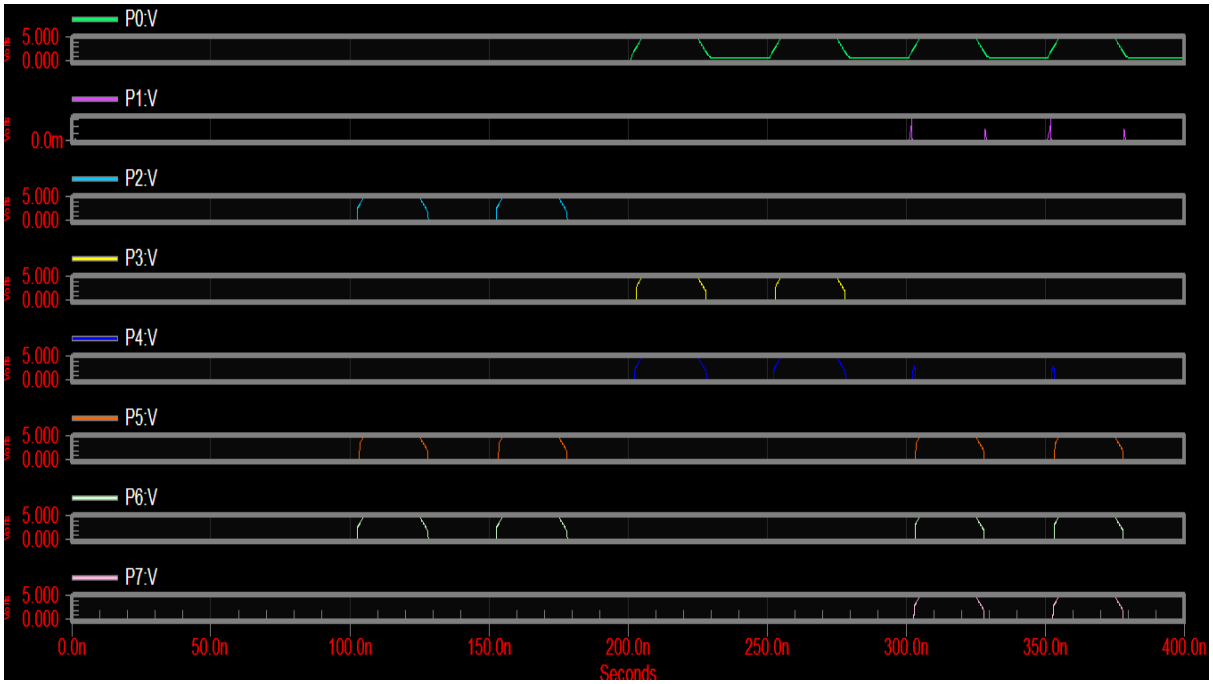

Fig. 5.5 Output Waveform of 4-bit 2N-2N2P Vedic Multiplier

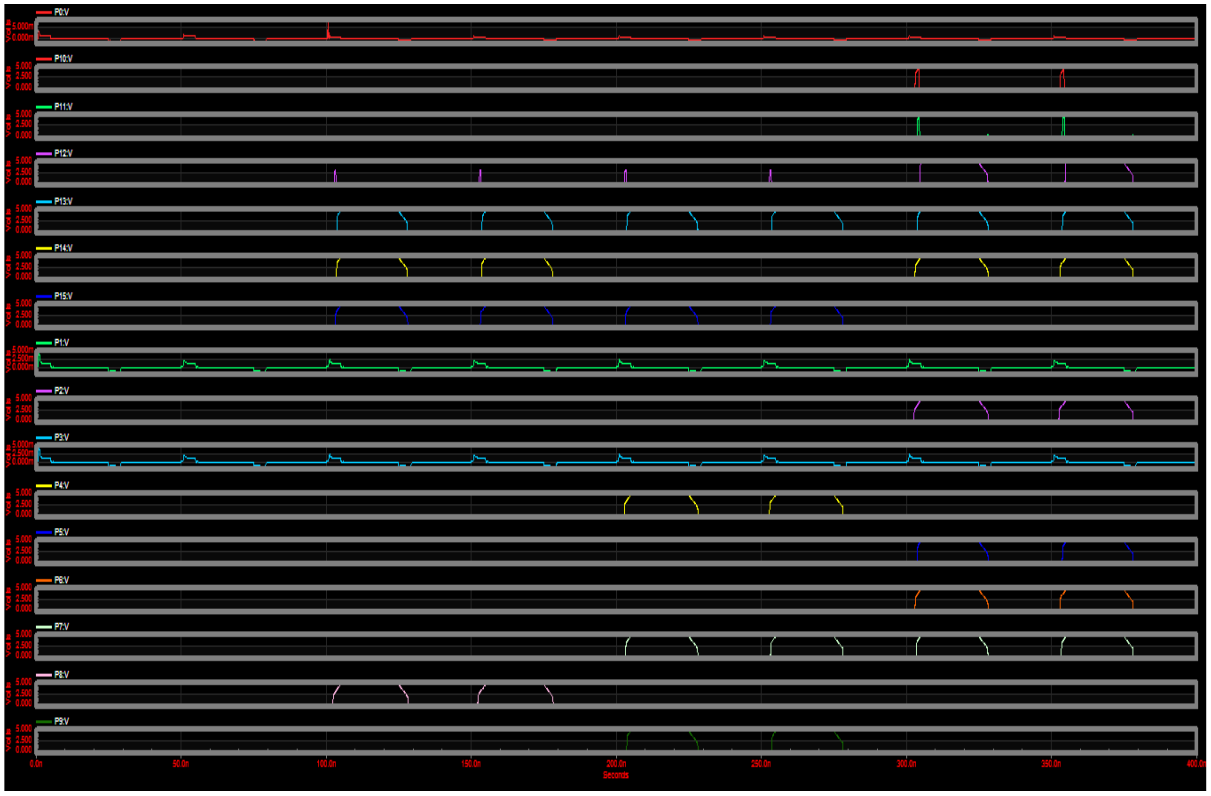

Fig. 5.6 Output Waveform of 8-bit 2N-2N2P Vedic Multiplier

5.4 Output Waveforms of ECRL Vedic Multiplier

The output waveforms for 2-bit, 4-bit and 8-bit ECRL Vedic multiplier are demonstrated in Fig. 5.7, Fig. 5.8 and Fig. 5.9 respectively. All the conditions are kept same and the practical results shows complete similarity with actual theoretical results of multiplication.

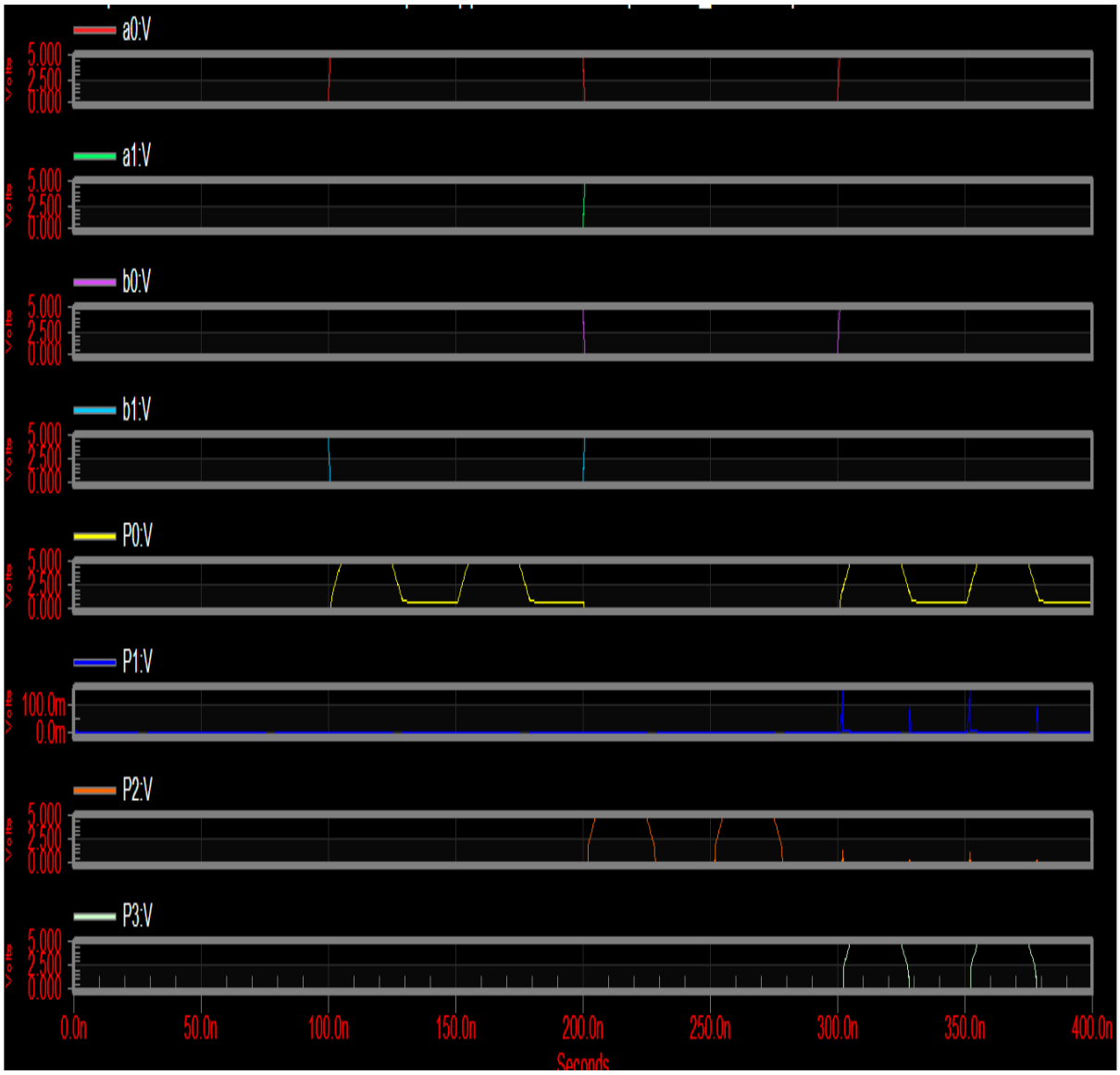

Fig. 5.7 Output Waveform of 2-bit ECRL Vedic Multiplier

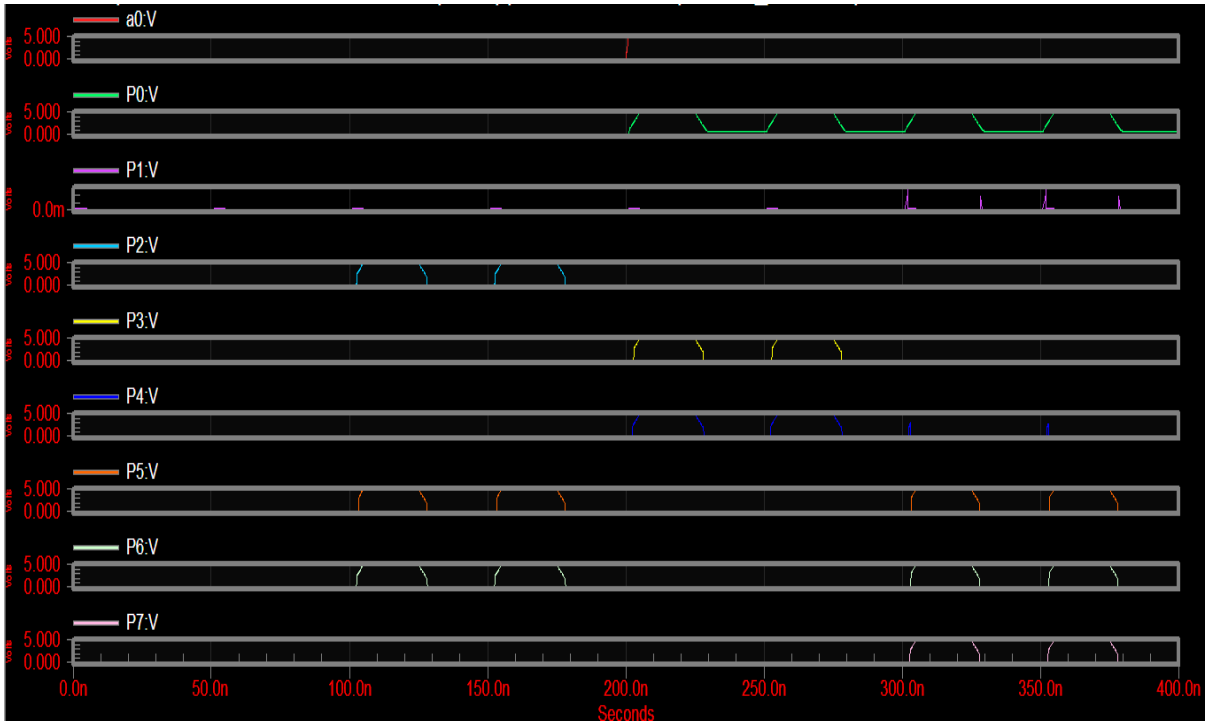

Fig. 5.8 Output Waveform of 4-bit ECRL Vedic Multiplier

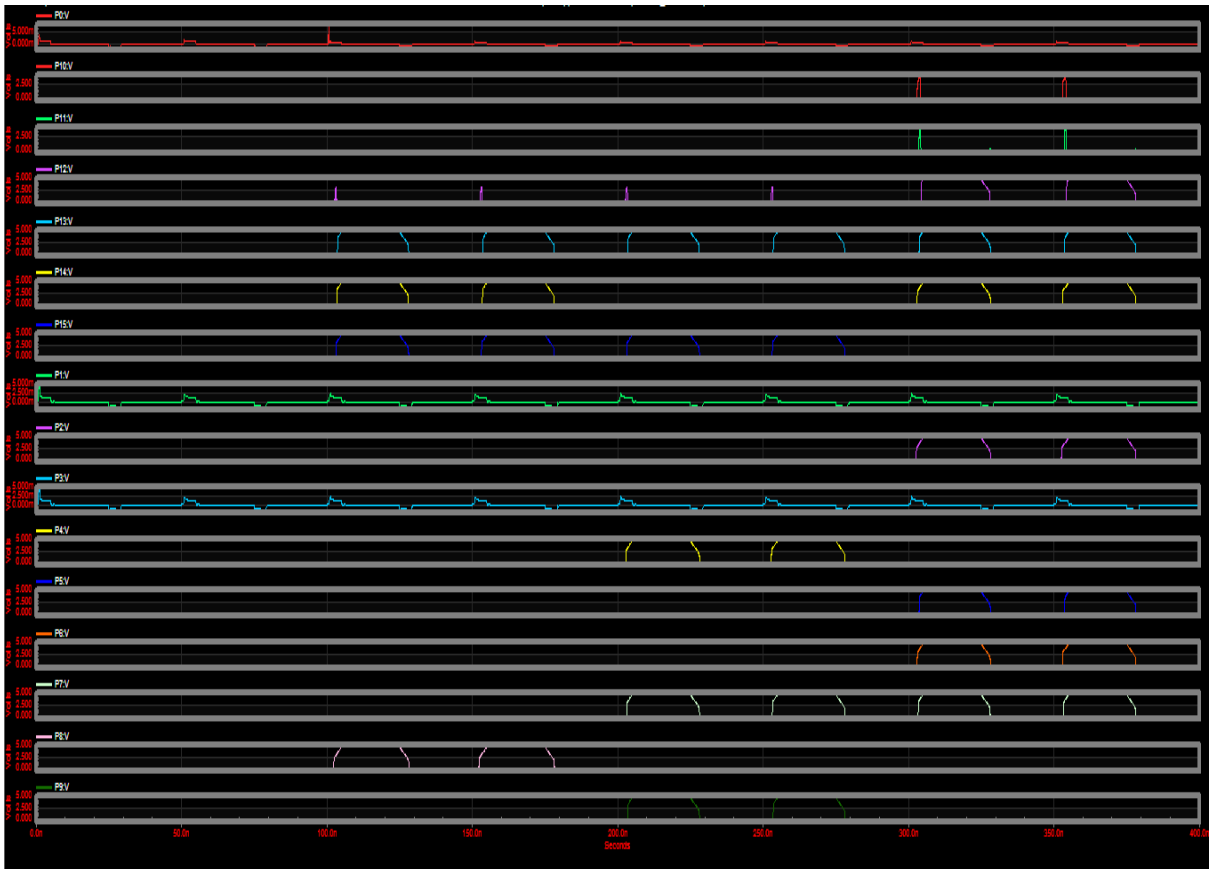

Fig. 5.9 Output Waveform of 8-bit ECRL Vedic Multiplier

5.5 Output Waveforms of CPAL Vedic Multiplier

Fig. 5.10, Fig. 5.11 and Fig. 5.12 display the output waveforms for 2-bit, 4-bit and 8-bit proposed CPAL Vedic multiplier respectively. The input combinations and the time period of analysis are similar to that of aforementioned designs. The theoretical results are verified by the practical results, which are given in Table 5.1.

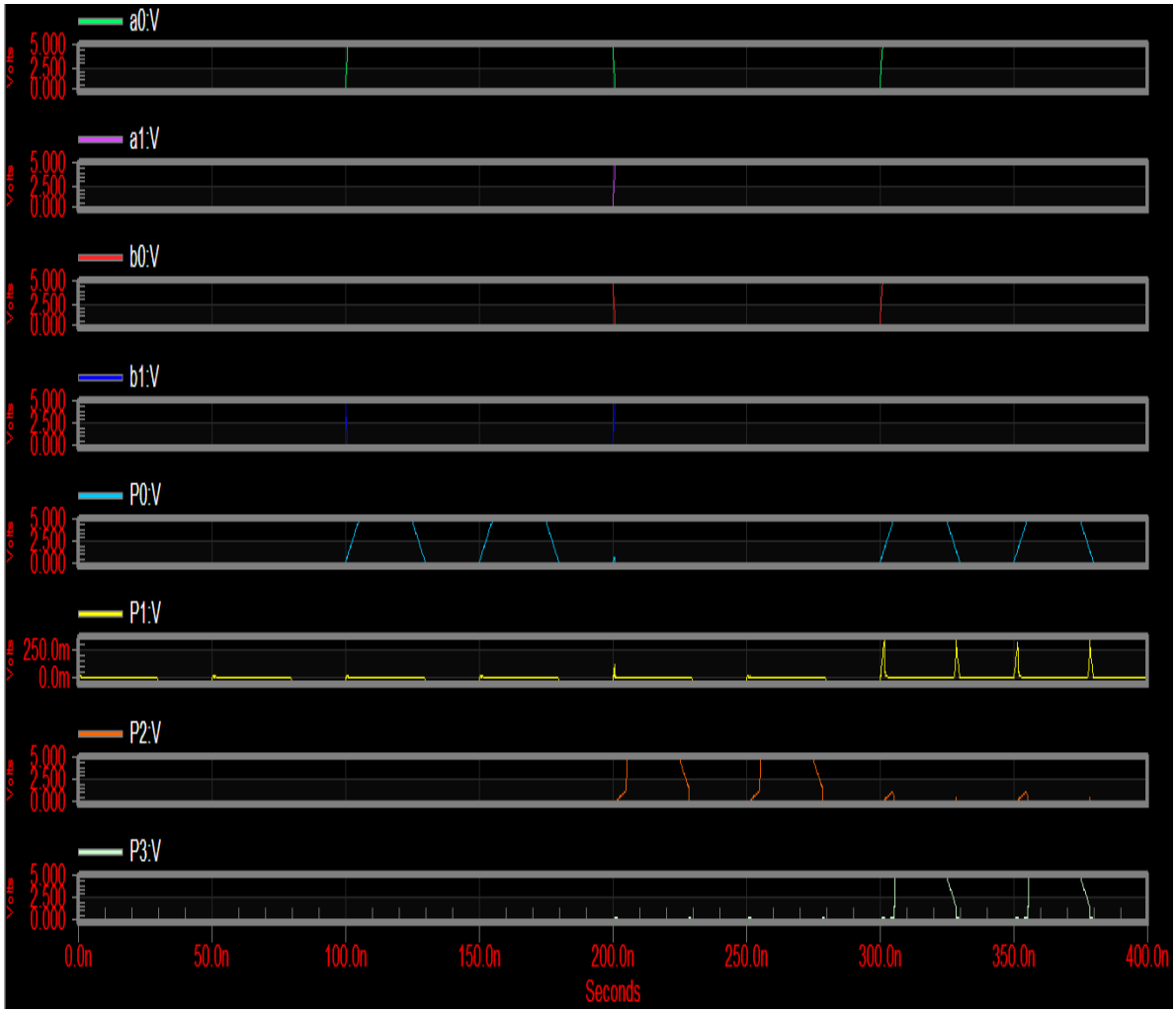

Fig. 5.10 Output Waveform of 2-bit CPAL Vedic Multiplier

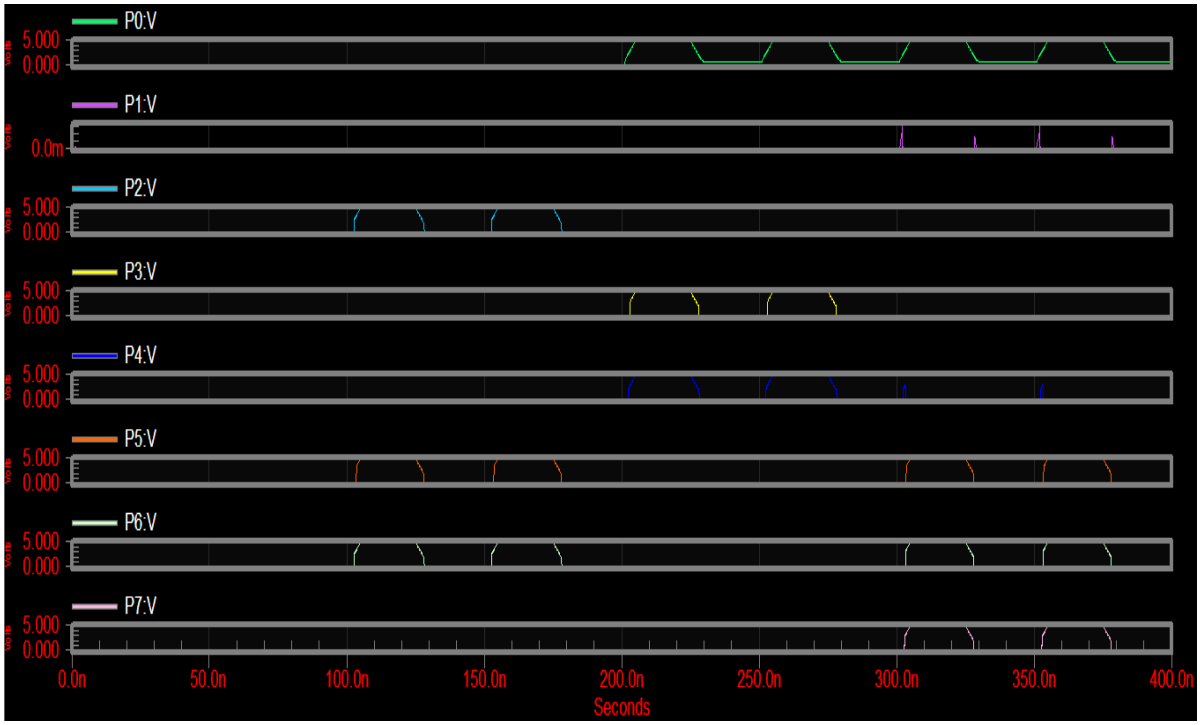

Fig. 5.11 Output Waveform of 4-bit CPAL Vedic Multiplier

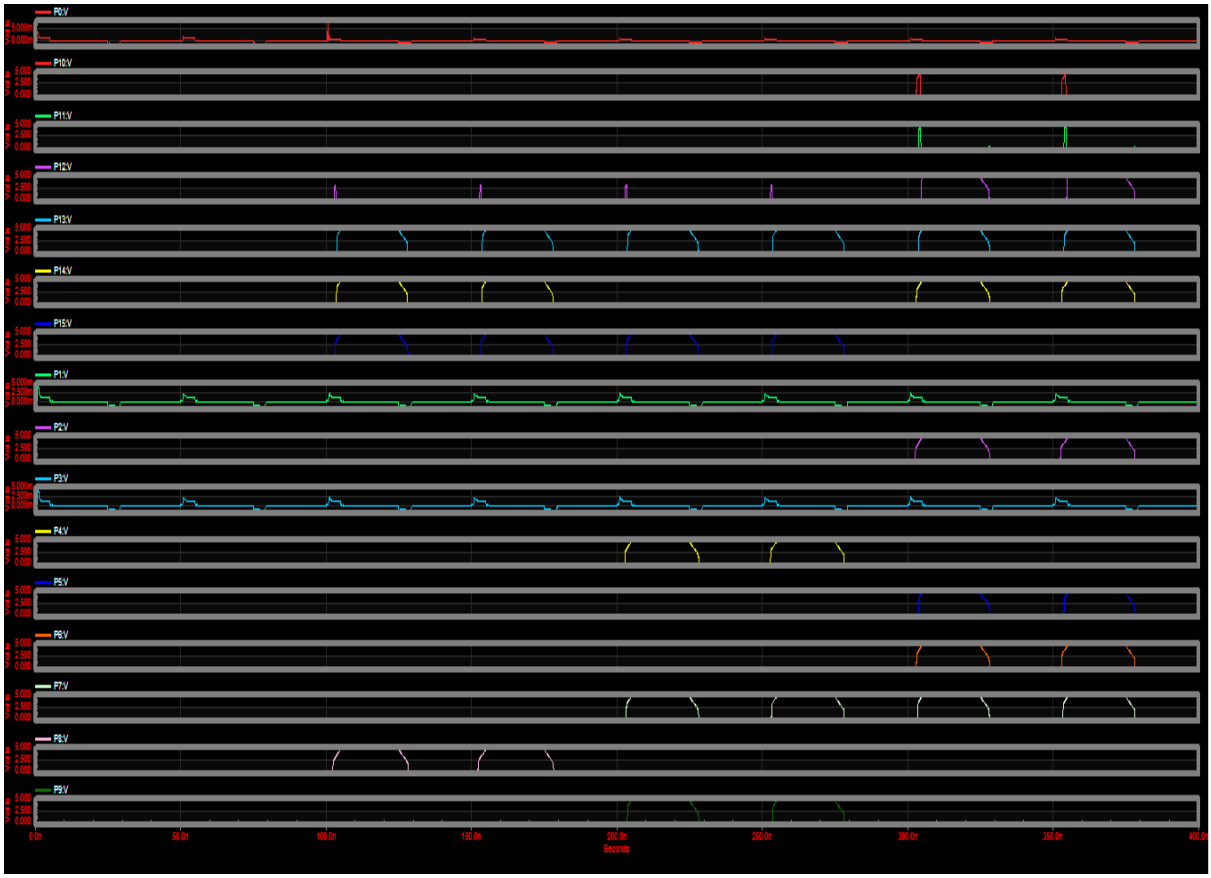

Fig. 5.12 Output Waveform of 8-bit CPAL Vedic Multiplier

Table 5.1 Different Multiplier Outputs for Different Input Conditions

Size of Multiplier	Multiplier	Multiplicand	Final Products
2-bit Vedic Multiplier	00	11	0000
	01	01	0001
	10	10	0100
	11	11	1001
4-bit Vedic Multiplier	0000	1111	00000000
	1010	1010	01100100
	0101	0101	00011001
	1111	1111	11100001
8-bit Vedic Multiplier	00000000	11111111	0000000000000000
	11110000	11110000	1110000100000000
	11001100	11001100	1010001010010000
	10101010	10101010	0111000011100100

5.6 Comparative Performance Analysis of CPAL Vedic Multiplier with other Methodologies

The performance analysis of the proposed CPAL based Vedic multiplier has been summarized in Table 5.2. The performances of the other designs, namely 2N-2N2P, ECRL and CMOS have also been included here for the purpose of comparison.

Table 5.2 Comparison of Experimental Results of 2-bit, 4-bit, and 8-bit Vedic Multiplier using Different Logic

Size of Multiplier	Logic	Average Power (watts)	Delay (ns)	PDP (J)
2-bit Vedic Multiplier	CMOS	$7.877648X10^{-7}$	0.2745	$2.162598713X10^{-16}$
	2N-2N2P	$2.964578X10^{-8}$	2.0420	$6.053668276X10^{-17}$
	ECRL	$1.717618X10^{-8}$	2.0422	$3.50771948X10^{-17}$
	CPAL	$7.093354X10^{-9}$	2.008	$1.424345483X10^{-17}$
4-bit Vedic Multiplier	CMOS	$8.942683X10^{-7}$	0.6161	$5.510283631X10^{-16}$
	2N-2N2P	$6.759878X10^{-8}$	2.0519	$1.387059367X10^{-16}$
	ECRL	$5.815385X10^{-8}$	2.0431	$1.188140288X10^{-16}$
	CPAL	$2.313647X10^{-8}$	2.010	$4.65043047X10^{-17}$
8-bit Vedic Multiplier	CMOS	$9.463201X10^{-7}$	1.5991	$1.51316584X10^{-15}$
	2N-2N2P	$2.791520X10^{-7}$	2.0521	$5.03633664X10^{-16}$
	ECRL	$1.236297X10^{-7}$	2.0432	$2.52600203X10^{-16}$
	CPAL	$4.100584X10^{-8}$	2.0120	$8.250375008X10^{-17}$

The simulation results depict that CPAL exhibits the least power consumption with respect to CMOS, 2N-2N2P, and ECRL logic methodologies. Since, recovery of energy is possible in the recovery phase of the power clock for any adiabatic logic; CPAL consumes less power than CMOS. Moreover, the CPAL is free from “non adiabatic” loss, which does exist in 2N-2N2P as well as ECRL, hence offers the least power requirement.

It has also been observed that the delay associated with the adiabatic logic families is more than that of CMOS due to the applied trapezoidal clock at the supply of the adiabatic logic. However, the overall performance of the CPAL based multiplier is superior to the aforesaid

designs as far as PDP is concerned. The percentage of improvements in average power and PDP has been shown in Table 5.3.

Table 5.3 Percentage of Improvement of CPAL as compared to CMOS, 2N-2N2P and ECRL

Size of Multiplier	Percentage improvement of CPAL over	Average Power	Delay	PDP
2-bit Vedic Multiplier	CMOS	99.03%	-86.32%	93.41%
	2N-2N2P	76.07%	1.69%	76.47%
	ECRL	58.702%	1.703%	59.39%
4-bit Vedic Multiplier	CMOS	97.41%	-69.34%	91.56%
	2N-2N2P	65.77%	2.08%	66.47%
	ECRL	60.21%	2.09%	60.86%
8-bit Vedic Multiplier	CMOS	95.67%	-20.52%	94.53%
	2N-2N2P	85.31%	1.99%	85.53%
	ECRL	66.83%	1.55%	67.33%

It has become clearly evident from Table 5.3 that CPAL based Vedic multiplier consumes 99.03%, 97.41%, and 95.67% less power for 2-bit, 4-bit, and 8-bit, respectively as compared with CMOS. The negative sign in the Table 5.3 signifies degradation of delay percentage of CPAL with respect to CMOS technology due to application of trapezoidal clock. The PDP of CPAL has also shown drastic enhancement of 93.41%, 91.56%, and 94.53% over CMOS. Moreover, CPAL also outperforms 2N-2N2P and ECRL in terms of average power, delay, and PDP. As for example, CPAL based 2-bit multiplier shows an improvement of 76.07% and 58.702% over 2N-2N2P and ECRL respectively, in terms of consumption of average power. Furthermore, the CPAL based design offers a slight improvement of 1.69% and

1.703% as compared to 2N-2N2P and ECRL respectively as far as time delay is concerned. For the same design, the improvement in PDP in CPAL multiplier is found to be 76.47% and 59.39% over 2N-2N2P and ECRL respectively. CPAL based 4-bit multiplier offers 65.77% and 60.21% improvement in terms of average power, 2.08% and 2.09% improvement in terms of delay and 66.47% and 60.86% improvement in terms of PDP with respect to 2N-2N2P and ECRL respectively. Similarly, 8-bit CPAL Vedic multiplier shows 85.31% and 66.83% progress in average power, 1.99% and 1.55% progress in delay and 85.53% and 67.33% progress in PDP.

5.7 Discussions

In this chapter, output waveforms of all the logic designs and the proposed design of "Vedic multiplier" have been displayed. From the simulated waveforms, it becomes evident that in adiabatic logic designs, logic 1 is represented by the trapezoidal clock pulse which is unlikely the CMOS logic design, where logic 1 is represented by 5 V. This is due to the application of power clock as supply instead of constant DC source. Moreover, the comparative performance analysis reveals that the proposed CPAL based "Vedic multiplier" outperforms the other logic designs.

CHAPTER 6

CONCLUSION

6.1 CONCLUDING REMARKS

Reduction of average power and delay are the two prime criteria of consideration in the design of an optimized multiplier. This has inspired the researchers to innovate various multiplication algorithms and logic styles to obtain improvement in all levels of design. In this view, "Vedic multiplication" algorithm has been proved to be efficient in terms of speed and simplicity. Moreover, it has also been established that "dynamic power consumption" can be diminished to a considerable extent by introduction of adiabatic logic style. Various adiabatic logic designs have been explored with time and their contributions in diminishing average power have been studied to attain the comparative performance analysis. Our demand of optimized multiplier can be satisfied by designing a multiplier incorporating the rules of "Vedic mathematics" along with adiabatic logic style.

In this work, an 8-bit multiplier based on "Urdhva Tiryagbham sutra" is designed using CPAL and its performances have been investigated in terms of average power, delay, and PDP. At first, basic logic gates are designed with aforementioned methodologies. These basic gates are then used to design a 2-bit Vedic multiplier which is again used to design 4-bit multiplier. The 4-bit Vedic multiplier is then used to develop the 8-bit multiplier. With the advancement of technology and an increase in the number of devices on a chip, these design parameters are of main concern to improve the performance of a circuit. In addition to this, to compare the performance of the proposed design, 8-bit Vedic multiplier has also been constructed using CMOS technology and other adiabatic logic families such as 2N-2N2P and ECRL. The experimental result indicates a considerable reduction of power consumption for CPAL based Vedic multiplier as compared to the CMOS based design. It has also been established that CPAL consumes the least power than 2N-2N2P and ECRL adiabatic designs. Due to the application of slow transition clock, which is the key reason for drastic power

saving in adiabatic circuits, the delay was more with respect to CMOS technology. But the overall PDP was remarkably satisfactory. Thus, it can be validated that the CPAL based design are economic in power consumption and can be utilized as a prominent design method in low power VLSI circuits.

6.2 Future Scope

In this thesis, "Urdhva Triyagbham sutra" of "Vedic multiplication" and partial adiabatic logic style, CPAL, has been fused to obtain an optimized multiplier. The attempt to obtain an efficient multiplier using 150 nm technology has been successfully established. The adiabatic logic style focuses on diminishing "dynamic power consumption". "Leakage current" is considered to be another important component of power consumption now a day. To minimize leakage current, certain parameters like "process parameters", "subthreshold voltage" etc. are required to be optimized. The proposed design can also be modified taking "static power consumption" into consideration.

Moreover, the proposed design can be fabricated for practical applications. The "Vedic multiplier" can also be designed using other adiabatic logic style and compared for performance analysis in terms of power consumption. Various improvements can be employed to improvise design parameters such as area and speed to obtain a further optimized outcome. Furthermore, various architectures of "parallel adder" and compressor can be adapted as an effective measure of optimization of the design in future. The above design can be further extended by adopting various structural design of MOSFET to meet the above mentioned demand. Various "bio-inspired algorithms" like "Differential Evolution", "Paddy Field Algorithm", "Particle Swarm Optimization", "Ant Colony Optimization", "Cuckoo Search Algorithm" etc. can be complied with the proposed design to handle complex computations. "Floating point multiplier" using the proposed method may be regarded as an attractive research direction in future applications.

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