A Comprehensive Study on Different Structures of TFET : Analytical Modeling and Simulation Based Validation

Thesis submitted in partial fulfillment of the requirements for the award of the degree

of

Master of Technology in

VLSI Design and Microelectronics Technology

by

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CERTIFICATE OF EXAMINATION

This is to certify that the thesis entitled "**A comprehensive study on different structures of TFET : Analytical modeling and simulation based validation**" has been carried out by **AYAN BHATTACHARYA (Roll No: 001610703006, Examination Roll No: M6VLS19014 and Registration No:137278 of 2016-17)** under my guidance and supervision and can be accepted in partial fulfilment for the degree of Master of Technology in VLSI Design and Microelectronics Technology. In my opinion the work fulfils the requirement for which it is submitted. To the best of my knowledge, the matter embodied in the thesis has not been submitted to any other organization.

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ABBREVIATIONS

CHAPTER 1

MOSFET- Metal **O**xide **S**emiconductor **F**ield **E**ffect **T**ransistor

TFET- **T**unnel **F**ield **E**ffect **T**ransistor

AMD - **A**dvanced **M**icro **D**evices

CHAPTER 2

LSI- Large **S**cale **I**ntegration

VLSI- Very **L**arge **S**cale **I**ntegration

ULSI- Ultra **L**arge **S**cale **I**ntegration

CMOS- Complementary **M**etal **O**xide **S**emiconductor

SCE- **S**hort **C**hannel **E**ffect

DIBL- **D**rain **I**nduced **B**arrier **L**owering

SD-SG TFET- Splitted-**D**rain **S**ingle-**G**ate **TFET**

TSD-SG TFET - Top- **S**plitted-**D**rain **S**ingle-**G**ate **TFET**

MSD-SG TFET- Mesial- **S**plitted-**D**rain **S**ingle-**G**ate **TFET**

BSD-SG TFET- Basal- **S**plitted-**D**rain **S**ingle-**G**ate **TFET**

CHAPTER 3

SD TFET- Splitted-**D**rain **TFET**

SS-SD TFET- Split **S**ource **S**plit **D**rain **TFET**

DSS-SD TFET- Double **S**plit **S**ource **S**plit **D**rain **TFET**

CHAPTER 4

SS-DG-TFET- **S**alient **S**ource **D**ouble **G**ate **TFET**

CHAPTER 5

DS-TFET –Double **S**ource **TFET**

ABSTRACT

The work focuses on new alternative or successor to CMOS or MOS device which can combat their disadvantages. Researchers are aiming to achieve better performing devices than MOSFET in terms of sub-threshold slope, power consumption and scalability. This work is an approach towards exploring one of such alternatives, the Tunnel Field Effect Transistor (TFET). Some application specific structures of TFET are analytically modeled and validated with the help of available simulation software during this work.

In first work the effect of source splitting in already drain splitted TFET is explored. Two different source splitted TFET geometries are critically analyzed and performance based comparison is done. During this work, the effect of source engineering in this drain engineered TFET is extensively investigated. Due to differential doping in source region, a changed behavior is expected in the modified TFET. This design modification is aimed towards achieving better performance in terms of ON/OFF current ratio.

In second work a salient source TFET structure is inquired into along with analytical expressions and simulation based results. The utility in low power application is the most striking feature of this device. In this work an attempt has been made to establish the proposed device as a better performing device than conventional double gate TFET.

The third work primarily aims to incorporate quantum mechanical models in the analysis of DS-TFET. At the age of vigorous scaling, the inclusion of quantum mechanical models are being obligatory in research works. An attempt has been made to do so to analyze the behavior of the device more accurately .In this work, quantum confinement based on non-local tunneling model along with self-consistent Schrodinger-Poisson quantum model is included.

In this work, the primary focus is on studying the effect of source engineering in TFET technology. In all three works, the geometries of source region of proposed devices are modified through engineering.

CHAPTER 1

INTRODUCTION AND OBJECTIVE

1.1. Introduction

1.2. A brief overview of TFET

1.3. Motivation of Current Research

1.4. Objective

1.5. Organization of Thesis

References

CHAPTER 1

Introduction and Objective

1.1. Introduction:

The drawbacks of the conventional MOSFET technology influence researchers to develop numerous experimental FETs which are remolding the nanoscale industry thoroughly. Reducing dimension in nano-regime is no more able to uphold Moore's law without degrading device performances. Moreover, scaled MOSFET structures with sufficiently low threshold voltage cannot be realized due to emergence of short channel effects. The swift technological advancement till date has only been possible through continuous betterment of electronic products in terms of power consumption, speed, cost, compactness, functionality and integration level. Miniaturization of device feature has been the principal impetus behind these trends and it has led to substantial improvement of quality as well as economic admissibility [1]. As enumerated by the Gordon Moore in 1965, the number of transistors per integrated chip would be roughly doubled in every 2 years. Fabrication of cheaper, faster and smaller Integrated Circuits (ICs) has been continued since last four decades to accomplish inevitable hunger for better device performance. In the early 1980's, dimension of minimum feature size in IC traversed the sub-micron limit; whereas by early 2010s, both Intel and AMD announced their commercial microchips using transistors with 32nm process. To keep pace with this implausible pace of growth, generous financial support are being invested in research and development programs. Fig 1.1 is depicting the advancement of technology in last few decades. The transistor count was exponentially increased in integrated circuits as predicted by Moore's Law. But there exists a fundamental geometrical limit which cannot be violated. At present time, semiconductor industry is facing tough challenges. With each technology node, it is getting clear that after a certain period of time, fundamental geometrical limits will be reached [2].

Therefore, to retain the performance trend, alternation of materials and innovation in geometrical structures in the field of Nanotechnology are the need of the hour. In this context the emergence of TFET took place in the field of electronics. TFETs can exhibit sub-threshold slope below 60 mV/decade due to a fundamental difference in the mechanism of current control as compared to MOSFETs. In MOSFETs, the current depends on the thermionic emission of free carriers across the potential barrier between the source and the channel. On the other hand, the current in TFETs depends on the charge carriers tunneling through a potential barrier between the source valence band and the channel conduction band. As this potential barrier is very wide in the OFF-state of the device, TFETs exhibit very low OFF-state current.

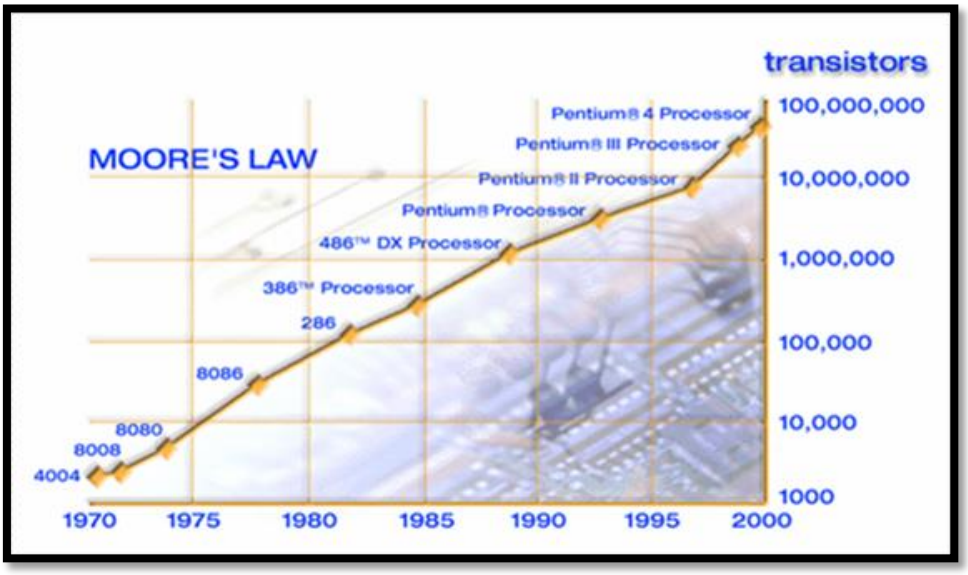


Figure 1.1: Moore's Law

Moreover TFETs have a greater immunity to these short channel effects. It may be pointed out that TFETs differ from the MOSFET only in the type of source doping. Therefore, the integration of the TFET fabrication process with the current MOSFET fabrication process would be easy.

1.2. A brief overview of TFET

Tunnel FETs use quantum-mechanical tunneling of electrons from the source to the channel as the primary carrier transport mechanism, allowing for sub-60 mV/dec subthreshold slopes.

History

The origins of three-terminal devices come from the band-to-band tunneling component in a Trench Transistor Cell [3]. A three-terminal tunnel device using this effect was proposed by Sanjay Banerjee at Texas Instruments in 1987 [4]. This device required gate overlap of the source, a situation later known as line tunneling. Later in 1992, Toshio Baba at NEC proposed a surface tunnel transistor using GaAs and AlGaAs that utilized point tunneling [5]. In 1995, William Reddick at Cambridge proposed a Silicon device using point tunneling [6]. All of these devices showed low currents and no subthreshold slope under 60 mV/dec. In 2004, Jorge Appenzeller at IBM showed experimental characteristics less than 60 mV/dec with carbon nanotube based devices [7].

Device Principles

Tunnel Field Effect Transistors (TFETs) use the tunneling of electrons as the carrier transport method for device operation. They are generally designed as gated pin diodes, where the gate is used to modulate an effective tunneling barrier height [8].

Ideally, these devices would have a very low off-state current (proportional to reverse biased diode leakage), a very low subthreshold slope, and acceptable on-current. TFETs can be generally classified as point and/or line tunneling devices [9]. In a point tunneling device, the source does not appreciably deplete, but the gate causes the channel region to invert, resulting in tunneling from the source to the channel. In a line tunneling device, the source is inverted (generally by engineering an overlapped gate with an optimized source doping profile), resulting in tunneling into the inversion layer, similar to Gate-Induced Drain Leakage (GIDL) [10-13].

Drawbacks

TFET is a relatively new technology. It is still evolving. So naturally there are some challenges and researchers are combatting it relentlessly. The primary concerns for researchers are low ON current and ambipolar conduction in TFETs. These drawbacks will be discussed elaborately in the following chapter.

1.3. Motivation of Current Research

Some of the drawbacks of TFET technology is mentioned in the previous section of this introductory chapter. The motivation behind the present research work is to overcome these drawbacks [14]. Several transistor structures are explored to achieve

(a) Better on current or better ON/OFF current ratio .
(b) Reduced ambipolar conduction

The effect of source engineering in a drain engineered TFET is analyzed in this research work. Apart from this, an attempt has been made to establish a TFET structure as a very low power consuming device. It is shown that – lower the V_{ds},better the performance .So it may be a solution for continuous degrading nano device performance in terms of power. And finally quantum mechanical characteristics are incorporated to perform the simulation in a double source single gate TFET [15-16] .As channel length is shrinked below 20 nm and source or drain thickness is scaled down to the range of 10 nm, it is important to incorporate quantum mechanical Schrodinger-Poisson model in simulation as well as analytical calculation [17-18]. An attempt has been made to do so in this research work.

1.4. Objective

The objective of this thesis work is to establish TFET as an application specific device. The present generation of low power electronics is awaiting a potential technological giant and TFET is a promising candidate to fill up the blank space [19-20]. But there are some challenges those are already mentioned. Once we can solve these issues, TFET may also be applied in commercial products. This thesis work is an attempt to demonstrate several geometrical TFET structures and their operating conditions so that it can fulfil the requirements of modern day low power electronics.

1.5. Organization of Thesis

The thesis is divided into five chapters and its outline is described as given below:

- Chapter I is an introductory chapter. In this chapter it is investigated that how the present work is relevant to other modern contemporary research works all around the globe. A very brief overview of TFET is provided here. Challenges of TFET technology are mentioned. Finally, the motivation and objective of the present work is discussed in this chapter.
- Chapter II presents the trends of various TFET technology in modern times and the theoretical background studies related to present research work in details. The drawbacks of MOSFETs are speculated and hence the emergence of TFETs are justified in this chapter. Different kind of existing TFETs are discussed. A brief literature review is presented too. A concise study of drain engineered TFET is conducted. Based on these background studies, the next footsteps are suggested in this chapter.
- In Chapter III the effect of source engineering in a drain engineered TFET is studied. This work is based on simulation in Silvaco Atlas. This is extension of the work that was already done by splitting the drain region of a TFET into two horizontal parts. In that case the ambipolar conduction is reduced. During this work, the effect of source engineering in this drain engineered TFET is extensively investigated. Due to differential doping in source region, a changed behavior is expected in the modified TFET. This design modification is aimed towards achieving better performance in terms of ON/OFF current ratio.

❖ Chapter IV contains analytical modeling and simulation based result of salient source double gate TFET structure. This salient source double gate TFET is an application specific device. Better SS is found when drain voltage is lower. Hence it is better for low power application. Moreover analytical surface potential model is verified by the help of simulation during this work. In this chapter, the proposed TFET is established as a better performing device than conventional double gate TFET.

❖ In Chapter V an attempt has been made to incorporate quantum confinement in DS-TFET (Double Source TFET) based on non-local tunneling model along with self-consistent Schrodinger-Poisson quantum model. Quantum confinement is considered in 1-D. As a result effective band gap and subsequent tunneling barrier width is increased. Hence the results obtained through quantum approach are more practical than semi-classical ones.

❖ Chapter VI is concluding chapter. Here the findings of all the works are summed up. Conclusion of the works are discussed in this chapter. The relevance of the thesis work is once again analyzed .The utility of proposed structures are justified in this chapter.

References

[1]. J. E. Lilienfeld, "Method and apparatus for controlling electric currents," U.S. Patent 1 745 175, 1930.

[2]. Pritha Banerjee, Aman Mahajan and Subir Kumar Sarkar,"3-D Analytical Modeling of Gate Engineered Tri-gate SON MOSFET", IEEE International Conference on Devices for Integrated Circuits (DEVIC-17),Kalyani Govt. Engg. College, 23-24 March, 2017

[3]. Banerjee, S., Richardson, W., Coleman, J., & Chatterjee, A. "A new three-terminal tunnel device." Electron Device Letters, IEEE, 8 347 - 349 (1987).

[4]. Baba, T. "Proposal for Surface Tunnel Transistors." Japanese Journal of Applied Physics, 31 http://jjap.jsap.jp/link?JJAP/31/L455/ L455-L457 (1992).

[5]. Reddick, W. M. & Amaratunga, G. A. J. "Silicon surface tunnel transistor." Applied Physics Letters, 67 http://link.aip.org/link/?APL/67/494/1 494-496 (1995).

[6]. Appenzeller, J., Lin, Y.-M., Knoch, J., & Avouris, P. "Band-to-Band Tunneling in Carbon Nanotube Field-Effect Transistors." Phys. Rev. Lett., 93 196805 (2004).

[7]. Nayfeh, O. M., Chleirigh, C. N., Hennessy, J., Gomez, L., Hoyt, J. L., & Antoniadis, D. A. "Design of Tunneling Field-Effect Transistors Using Strained- Silicon/Strained-Germanium Type-II Staggered Heterojunctions." Electron Device Letters, IEEE, 29 1074 -1077 (2008).

[8]. Vandenberghe, W., Verhulst, A. S., Groeseneken, G., Soree, B., & Magnus, W. "Analytical model for point and line tunneling in a tunnel field-effect transistor." Simulation of Semiconductor Processes and Devices, 2008. SISPAD 2008. International Conference on, 137 -140 (2008).

[9]. Lu, Y., Bangsaruntip, S., Wang, X., Zhang, L., Nishi, Y., & Dai, H. "DNA Functionalization of Carbon Nanotubes for Ultrathin Atomic Layer Deposition of High κ Dielectrics for Nanotube Transistors with 60 mV/Decade Switching." Journal of the American Chemical Society, 128 http://pubs.acs.org/doi/abs/10.1021/ja058836v 3518- 3519 (2006).

[10]. J.Bag,Rashmi Ranjan Sahoo, P.K.Dutta and Subir Kumar Sarkar, " Design and VLSI Implementation of Power Efficient Processor for object localization in Large WSN," Int. J. High Performance Systems Architecture, Inderscience Journal,Vol 4,No. 4,pp-204-217, 2013.

[11]. Priyanka Saha, Dinesh Kumar Dash, Subhramita Basak and Subir Kumar Sarkar, "Asymmetric Junctionless Double Gate (JLDG) Silicon on Nothing (SON) MOSFET Modified with the Concept of Work Function Engineering: A Comparative Performance Study", in 1st 'International Conference on VLSI Device, Circuit and System' (VLSI DCS 2016), 19th-20th October,2016, Meghnad Saha Institute of Technology, Kolkata, India.

[12]. B. Davari, R. H. Dennard, and G. G. Shahidi, "CMOS scaling for high-performance and low-power—the next ten years," Proc. IEEE, vol. 89, pp. 595–606, Apr. 1995.

[13]. Joyashree Bag and Subir Kumar Sarkar, "Development and VLSI implementation of a data security scheme for RFID system using programmable cellular automata" International Journal Radio Frequency Identification Technology and Applications, Vol. 4, No. 2, Pp: 197-211, 2013.

[14]. Navjeet Bagga,Saheli Sarkhel and Subir Kumar Sarkar" Exploring the Asymmetric Characteristics of a Double Gate MOSFET with Linearly Graded Binary Metal Alloy Gate Electrode for Enhanced Performance ",IETE Journal Of Research, DOI 10.1080/03772063.2016.1176542,April,2016

[15]. E. M. Conwell, "High Field Transport in Semiconductors", Solid State Physics Supplement 9 (Academic Press, New York, 1967).

[16]. Suman Basu, Samir Kumar Sarkar and Subir Kumar Sarkar, “Exploring Novel Characteristics of Strain Compensated SiGeC Nanoscale MOSFET,” Indian Journal of Physics, Volume 87, Issue 4, pp 333-338, April 2013.

[17]. Ankush Ghosh, J. Gope, T. Datta, Biplab Roy and Subir Kumar Sarkar, “Spintronic Device Based Power Efficient VLSI Chip Design for Universal Code Converter”, Canadian Journal of Pure and Applied Sciences, Vol. 2, No. 3, pp. 469-474, 2008

[18]. Sudip Dogra, Joyashree Bag, Subir Kumar Sarkar, “Development & VLSI Implementation of a new scheme for Traffic Management using RFID with least stoppage time facility to Priority Cars.”International Journal on Recent Trends in Engineering & Technology, Association of computer Electronics and Electrical Engineering. ACEEE ;pages 177-181); 2011.

[19]. V. H. Mankar, T. S. Das and Subir Kumar Sarkar,, “Cellular Automata based Robust Watermarking Architecture towards the VLSI realization” International Journal of Computer Science, VOL.2 No.3, 2008.

[20]. Navjeet Bagga, Saheli Sarkhel and Subir Kumar Sarkar, "Recent Research Trends in Gate Engineered Tunnel FET for Improved Current Behavior by subduing the Ambipolar Effects: A Review", IEEE International conference on computing, communication and automation (ICCCA2015), Galgotias University, Noida, 15th -16th May 2015.

CHAPTER 2

BACKGROUND STUDY PRIOR TO THE RESEARCH WORK AND LITERATURE REVIEW

CHAPTER 2

BACKGROUND STUDY PRIOR TO THE RESEARCH WORK AND LITERATURE REVIEW

2.1 Introduction

In previous chapter we mentioned the problem statements of TFET technology. Primarily researchers have three objectives

(a) To increase ON current

(b) To reduce ambipolar conduction.

(c) To minimize sub-threshold slope of the transfer characteristics.

In this chapter we will learn the prerequisites to conduct this research work.

2.2. Evolution of transistor

John Bardeen, William Shockley and Walter Brattain created history in 1947 at Bell Telephone Laboratories when they invented transistor. Hence an unprecedented milestone was set in the field of semiconductor industry. Thereafter we gradually entered into the era of LSI (Large–Scale–Integration), VLSI (Very–Large–Scale–Integration) and ULSI (Ultra–Large–Scale–Integration) to compensate the ungratified demand of more compact, cheaper and faster electronic devices. Incessant downscaling has made this progress possible and sustained Moore's Law till now. But currently, the semiconductor industry has reached a dipping point as further progress in traditional CMOS technology is hindered due to a bunch of challenges. These challenges will be discussed in the following sections of this chapter. Fig 2.1. indicates versatile application specific aspects of down sized transistors.

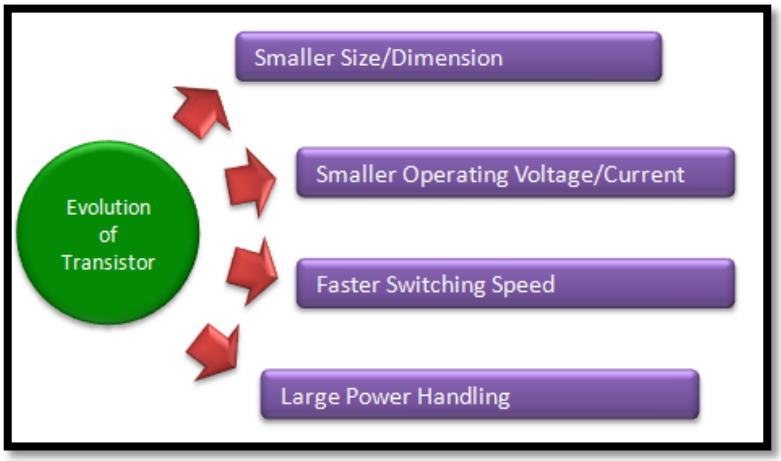


Fig.2.1. Evolution of Transistor

2.3. Timeline of electronics since 1947

1947 - First point contact transistor was invented.

1952 - Transistor was commercially used for the first time

1954 - First mass produced transistors were demonstrated.

1954 - Transistor radio was invented.

1955 – Silicon dioxide was discovered.

1958 – Integrated circuit was invented.

1962 – MOSFET was invented.

1966 – Self-aligned gate process was invented for fabrication of FETs.

1967 – First handheld calculator.

1968- Molecular beam epitaxy was developed at Bell lab.

1971- Computer on a chip was introduced by Intel.

1972- Home video games are commercially available.

1974- TMS 1000 was introduced by Texas Instruments.

1980- Built in self-testing technology in circuit board.

1998- Plastic transistors was invented.

2.4. Technological Limitations of MOSFETs

As device channel length is continuously decreased, gate control over channel deteriorates due to enhanced nearness of MOSFET's source and drain. As a result, Short–Channel–Effects (SCEs) become a serious challenge associated with downscaled MOSFETs. When the channel length is shrunk to the order of source and drain depletion-layer width SCE s emerges. SCEs lead to several reliability issues as the basic device parameters (such as threshold voltage), become dependent on channel length[3-10].

Five different short-channel effects are:

1. Drain-induced barrier lowering
2. Threshold voltage roll off,
3. Surface scattering,
4. Velocity saturation and
5. Hot electron effect

2.4.1. Drain-Induced Barrier-Lowering (DIBL):

The drain voltage is able to impact strongly on the channel region as the dimensions of a MOSFET transistor are reduced. This undesirable effect is called Drain –Induced – Barrier – Lowering (DIBL). DIBL effect takes place when the barrier height for carriers at the source end reduces due to influence

of drain electric field, upon application of a high V_{ds} (as shown in Fig. 2.2). As a result the number of charge carriers injected into channel region from the source increases leading to an enhanced off-current. Thus the drain current is not controlled only by V_{gs},but also by V_{ds} .

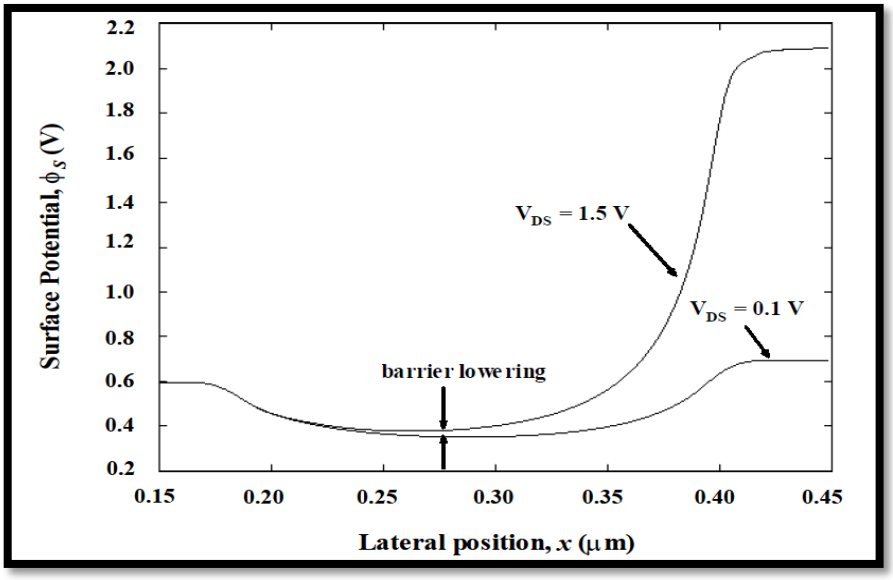


Fig 2.2. Surface potential along the position in channel for V_{DS} = 0.1 V and 1.5 V [1]

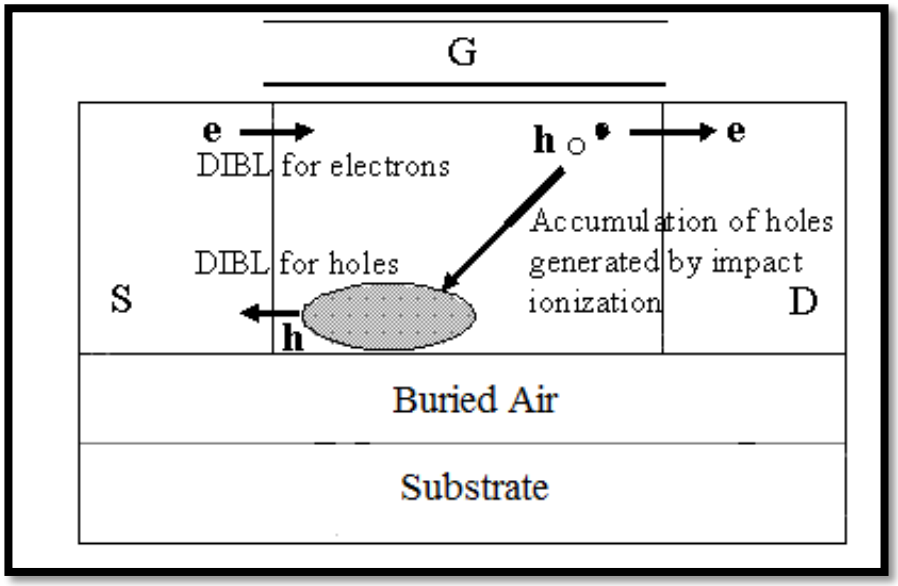


Fig 2.3. Three mechanisms determining SCEs [1]

Apart from DIBL, there are two features determining short channel effects in thin-film SON devices viz. (a) positive bias effect to device body due to accumulation of holes. These holes are generated through impact ionization near drain and (b) the DIBL effect on barrier for holes at the source edge near the bottom, as illustrated in Fig. 2.3. [1]

DIBL can be calculated as follows:

$$DIBL = \frac{V_{th}^{dd} - V_{th}^{low}}{V_{dd} - V_{dd}^{low}} \quad (2.1)$$

Where, V_{th}^{dd} is the threshold voltage measured for high drain bias (the supply voltage), and V_{th}^{low} is the threshold voltage measured for low drain bias, typically 0.05 Volt or 0.1 Volt.

V_{dd} is the supply voltage and V_{dd}^{low} is low drain voltage (for linear part of I-V characteristics).

Another process for measuring DIBL,called the Voltage-Doping Transformation model (VDT) [38] is used to evaluate the dependence of DIBL on the transistor parameters like oxide thickness, gate length or drain to source voltage. According to this model, DIBL is expressed as [39]:

$$DIBL = 0.80 \frac{\varepsilon_{Si}}{\varepsilon_{ox}} \left[1 + \frac{x_j^2}{L_{el}^2}\right] \frac{t_{ox}}{L_{el}} \frac{t_{dep}}{L_{el}} V_{DS} \quad (2.2)$$

Where L_{el} is the effective (electrical) channel length,

V_{bi} =built-in potential,

t_{ox} = oxide thickness,

x_j = source or drain junction width

t_{dep} = penetration depth of gate field in channel.

However, transistor normally does not work at a low drain bias. Hence DIBL is not a parameter, directly related to circuit operation, but rather it depicts the degradation of device characteristics such as strong threshold voltage roll-off (V_{th} roll-off) and high off current (I_{OFF}) in subthreshold region. Typically, DIBL is measured in mV/V.

2.4.2. Threshold Voltage Roll-Off

The expression of Short-Channel Effect (SCE) can be derived from the above mentioned VDT model [39]:

$$SCE = 0.64 \frac{\varepsilon_{Si}}{\varepsilon_{ox}} \left[1 + \frac{x_j^2}{L_{el}^2}\right] \frac{t_{ox}}{L_{el}} \frac{t_{dep}}{L_{el}} V_{bi} \quad (2.3)$$

From the expressions of (2.2) and (2.3), the threshold voltage (V_{th}) of MOSFET can be deduced as:

$$V_{th} = V_{th\infty} - DIBL - SCE \quad (2.4)$$

This is typically measured in mV/nm. [39]

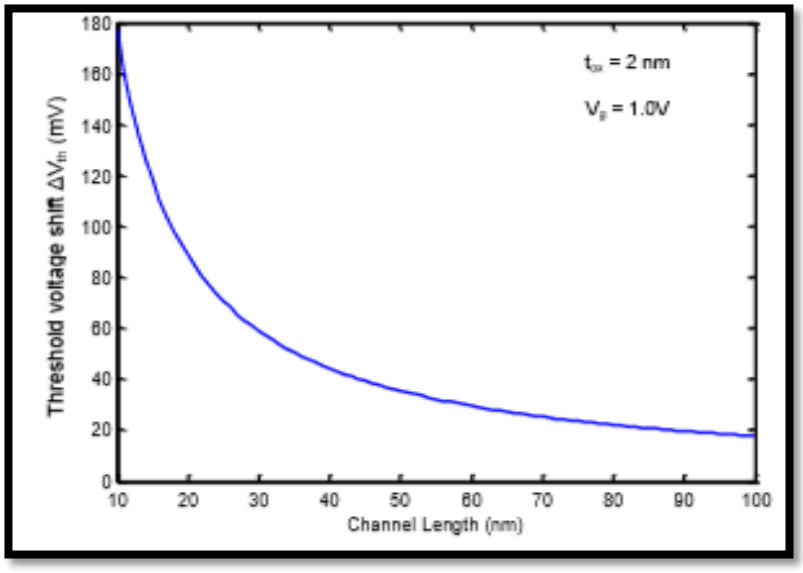


Fig. 2.4. Threshold voltage shift with channel length

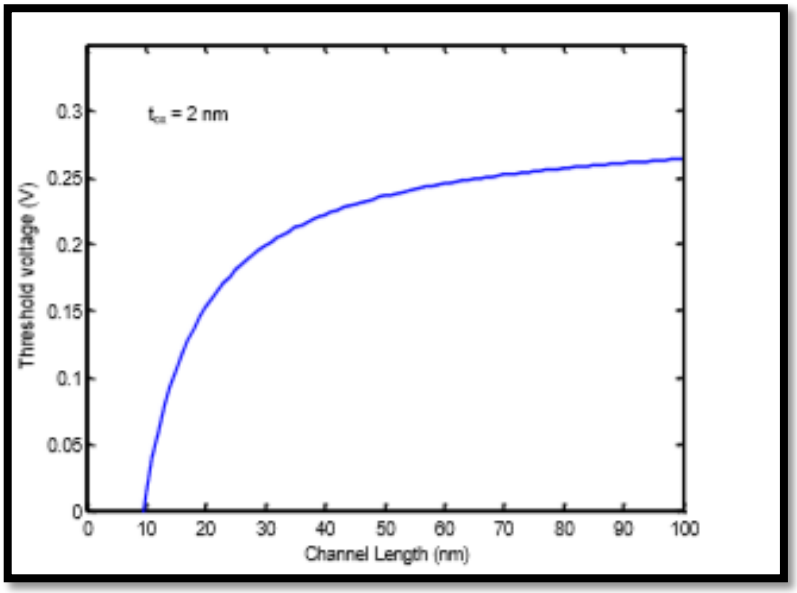


Fig. 2.5. Threshold voltage roll-off for nano scale FinFET

2.4.3. Surface scattering

Electric field's longitudinal component (ε_y) increases as the channel length shrinks as a result of lateral extension of depletion layer into channel region, and at the same time the mobility becomes electric field-dependent.[1] The collisions encountered by the electrons those are accelerated towards interface primarily due to influence of the electric field's horizontal component (ε_x), is called *surface scattering*. This phenomenon causes reduction of mobility [1]. As the carrier transport in MOSFET is confined within narrow inversion layer, the electrons face greater trouble in moving parallel to the interface. Therefore, even for small ε_y, the average surface mobility is roughly half of the bulk mobility. We can get an idea of the mutual dependence of mobility , gate voltage and the threshold voltage from Fig 2.7.

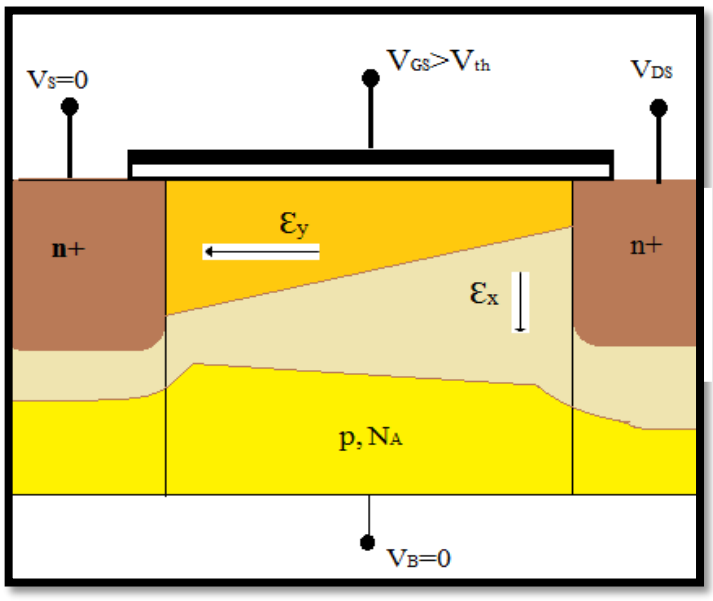


Fig. 2.6. Cross section view of MOSFET

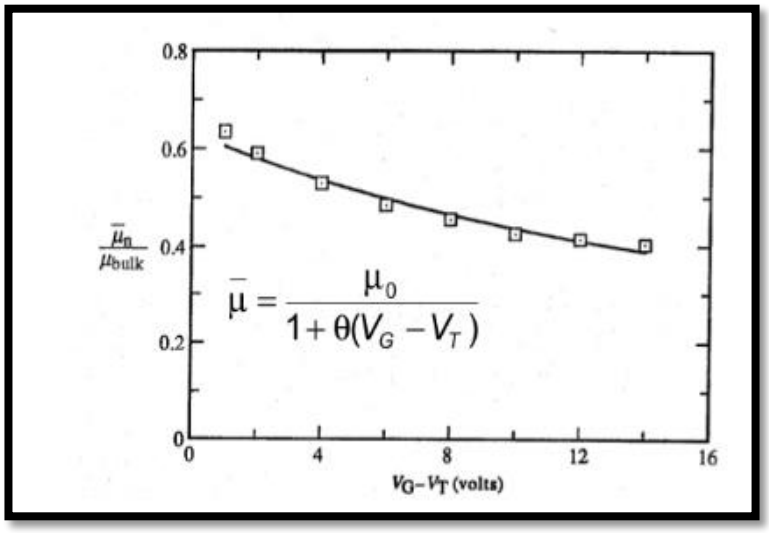


Fig. 2.7. Mobility dependence on gate voltage

2.4.4. Velocity saturation

The next important SCE that we will cover in this chapter is "velocity saturation" which is the consequence of a high lateral electric field ($\mathcal{E}_y$) along the scaled channel. At low $\mathcal{E}_y$, the drift velocity of mobile carriers in the channel region varies linearly with the intensity of electric field. However, as $\mathcal{E}_y$ raises above 10^4 V/cm, the drift velocity increases more slowly, and approaches to the saturation limit of 10^7 cm/s around $\mathcal{E}_y=10^5$ V/cm at 300 K. Here, the drain current is limited by velocity saturation

leading to reduction of the transconductance in saturation mode. After incorporating velocity saturation, the maximum transconductance (g_m) achievable by a MOSFET is given as

$$g_m = WC_{ox}V_{de(sat)} \quad (2.5)$$

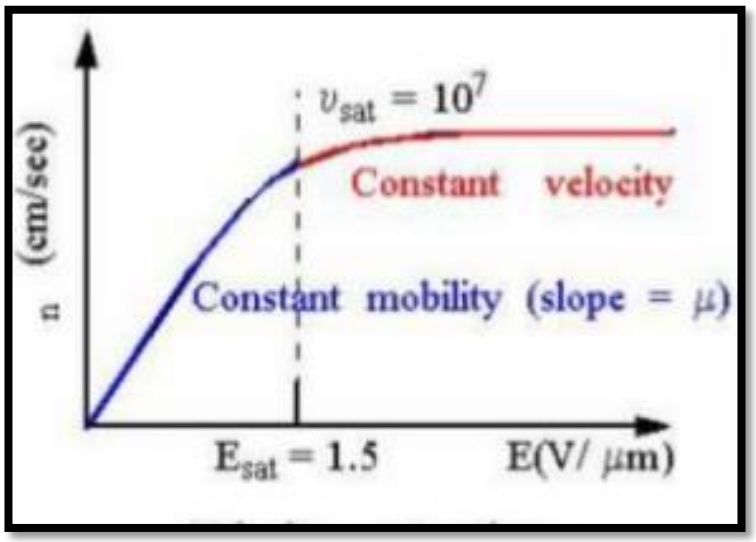


Fig. 2.8. Velocity Saturation

2.4.5. Hot Electron Effect

Another problem originated from the high electric field and short channel, that degrades the behavior of MOSFET devices is called "hot electron effect" (Fig. 2.9). Electrons acquire a large amount of energy from that electric field and they forcefully enter the oxide. In this oxide region the electrons can be trapped; hence the charge density is increased .These charges can accumulate with time. Moreover these charges can degrade the performance of the device by increasing threshold voltage and reducing the gate's control on drain current. In case of semiconductor devices, the *hot electron effect* occurs where the electrons can rise above the conduction band. Instead of being conducted to a collector through the material or recombining with holes, these 'hot' electrons can penetrate the semiconductor material. These electrons generally give away their excess energy as phonons. Also, in MOSFETs, the hot electrons may jump from the drain to the gate or the substrate. Therefore, consequent effects of this phenomenon include heating of the device, and increased leakage current.

Apart from short channel effects MOSFET has limitation in terms of Sub-threshold swing. Maximum SS achievable in MOSFET is 60 mV/decade. To overcome these shortcomings researchers carried on their research vigorously and as a result Tunneling Field Effect Transistor came into the picture. In the next section, we will look into basics of TFET.

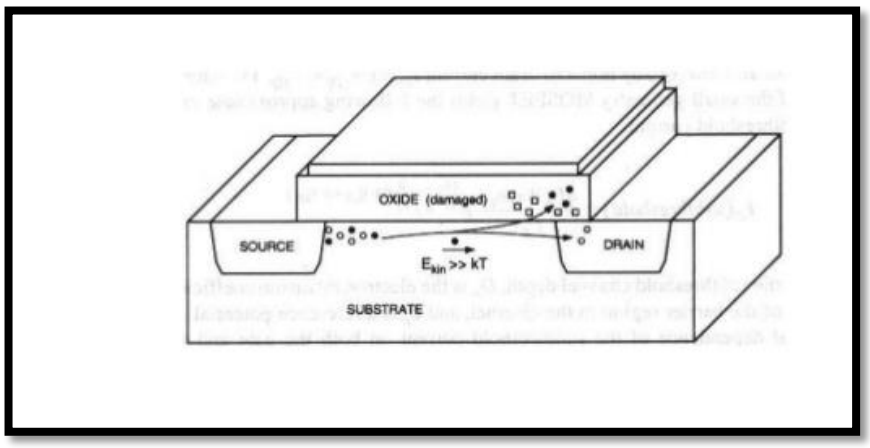


Fig. 2.9. Hot electron effect

2.5. Introduction to TFET

Researchers' relentless efforts made us move towards the era of low power and high-speed with enhanced device packing density [1] This introduces devices with dimensions in nano metre range as well as better RF performance.In previous section we studied that MOSFET s have major disadvantages like high leakage, more power dissipation, various short channel effects and threshold voltage roll off when we move towards nano-regime . Hence emergence of technologies like TFET was inevitable. It is found that TFET devices performs better than MOSFET devices when channel length is scaled down. The predominant advantage of TFET is current conduction through modulation of quantum mechanical Band-to-Band Tunneling (BTBT), which is a result of finite, but non-zero, probability of tunneling through a potential barrier, a process in which electrons tunnel from the valence band through the semiconductor bandgap to the conduction band or vice versa without any trap assistance. This merit carries forward the advantages over the thermionic injection across an energy barrier for carrier transport in MOSFET. Thus, due to its built-in tunnel barrier, where the channel current in TFET is controlled by tunneling mechanism from the source, the TFET device is immuned to short channel effect and the subthreshold swing of conventional TFET is usually under 60 mV/decade at 300 K, allowing TFETs to have SS as low as 20 mv/decade, which is the main reason to design low voltage, less power consuming operating devices in this technology.

Basic Operation of TFET

(i) **Thermal Equilibrium**

Band diagram of a TFET with no external bias (i.e *Vgs*=*Vds*= 0) in thermal equilibrium is shown in Figure 2.10. Two depletion regions are formed in this case, one each at the source–channel junction and the channel–drain junction [1].

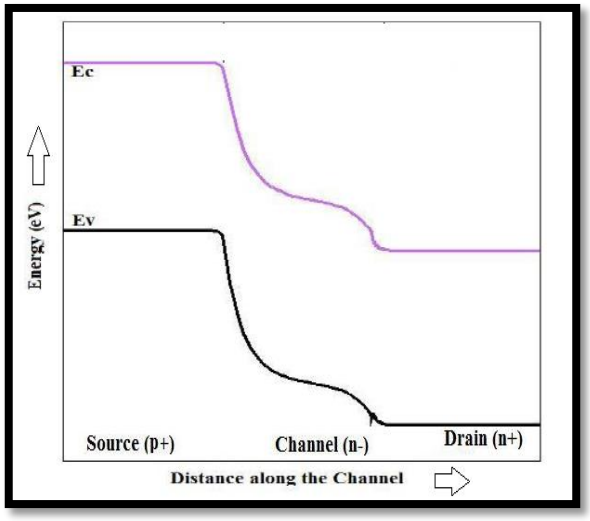


Figure 2.10. Band diagram of a n-channel TFET at zero bias[1].

(ii) Off State

The TFET stays OFF when *Vds*> 0 and *Vgs*= 0. The energy band diagram for OFF state is shown in Figure 2.11. Current is generated in off state due to the existence of carriers in the conduction band. These carriers drift towards drain and hence current is generated. But in n-channel TFET the source is p-type. Therefore, very few free electrons is present in conduction band unlike MOSFET s. This causes negligible OFF current.

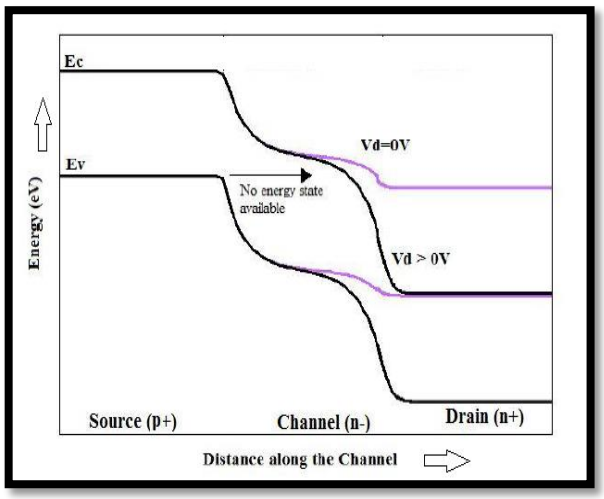


Figure 2.11. Band diagram of a TFET in the OFF-state at V_{gs}= 0 V [1].

(iii) On State

As *Vgs* is increased the energy band level varies as shown in Fig. 2.12. At a certain value of the gate voltage *Vgs*, the valence band in the source gets aligned with the conduction band in the channel. Now the electrons can conduct tunneling from valence band to conduction band through the barrier caused by the band gap. As *Vgs* is further increased, the bands present in the channel region are further lowered in energy resulting more electrons to tunnel This leads to a steep increase in the current because of the increase of tunneling probability.

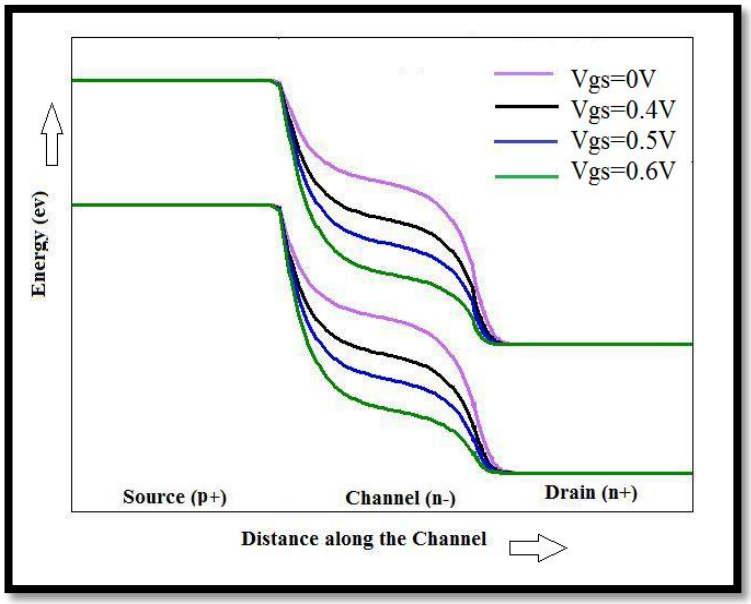


Figure 2.12. Band diagram along the surface of the TFET for (Vgs= 0, 0.4, 0.5, 0.6) in the ON-state [1].

2.6. Major shortcomings of TFET

There are several shortcomings in TFET technology. Two of them are most predominant and are the area of interest for present day researcher scholars. Those are following

2.6.1. Low on current

2.6.2. Ambipolar current conduction

2.6.1. Low on current in TFET

In n channel TFET the source is of p type. Hence the carriers present in conduction band is much less than MOSFET s. As a result lesser number of current carriers are injected into the channel. This phenomenon leads to low on current in TFET devices.

In MOSFET devices current is achievable in milli-ampere range whereas in TFET devices normally current is achieved in microampere range that is thousand times smaller .

2.6.2 Ambipolar current conduction

As *Vgs* is decreased below 0 V, the valence band of the channel is aligned with the conduction band of the drain, and the electrons from the valence band of the channel tunnels into the conduction band of the drain, resulting in a current flow. The electrons tunnel in same direction as in the case of positive gate bias. This phenomenon results in the device current having the same polarity even at a negative gate bias.This is called ambipolar conduction and is shown in Figure 2.13.

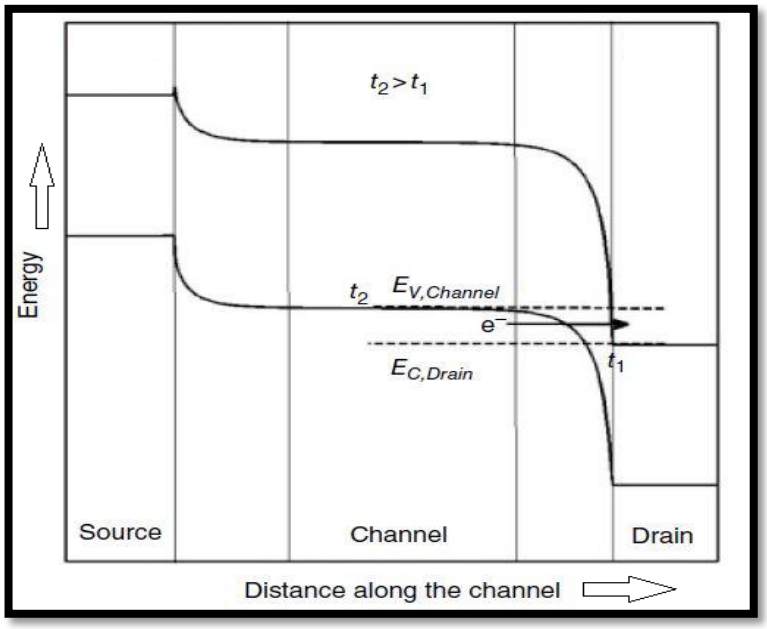


Figure 2.13. Band diagram along the surface of a TFET for a negative gate voltage (Vgs) and a positive drain voltage (Vds) [1].

2.7. Structural difference of TFET and MOSFET

As shown in Fig.2.14 and Fig. 2.15, N- channel MOSFET has n-type source and n-type drain unlike TFET. This is why carrier injection rate is higher in MOSFET than in TFET. Consequently, both leakage current and operating on current is much less in TFET than in MOSFET. Moreover, carrier transport mechanism is different in MOSFET and TFET. In MOSFETs current is generated through thermionic emission mechanism whereas in TFET tunneling takes place [1].

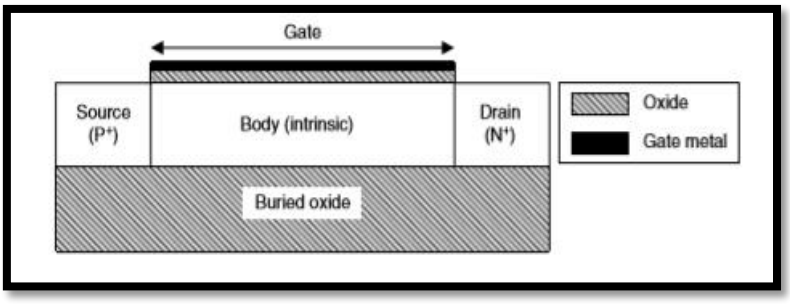


Figure 2.14. N-channel TFET

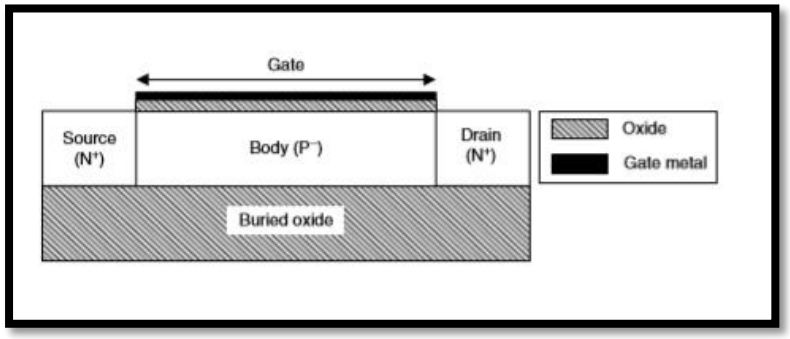


Figure 2.15. N-channel MOSFET

2.8. Performance dependence on several parameters of device

Device parameters like doping, gate work function, gate oxide permittivity etc. cause variation in TFET performance. Researchers have to optimize these parameters. Now, we will study these performance dependences briefly.

2.8.1 Doping

If we dope source region heavily, a narrower depletion region is formed in the source side. Hence tunneling width is lesser than in the case of low doped source region as shown in Fig. 2.16. This is the reason why larger on current is achievable in case of heavily doped source region. Similarly drain region should be doped moderately to curb ambipolar conduction as tunneling in the channel-drain junction is an unwanted phenomena in TFET.

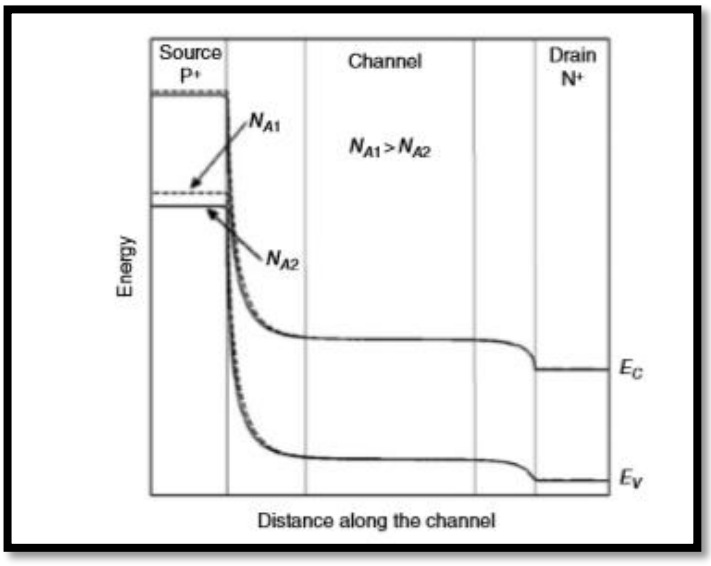


Figure 2.16. Band diagrams along the surface of an n-channel TFET with different values of source doping concentration. [1]

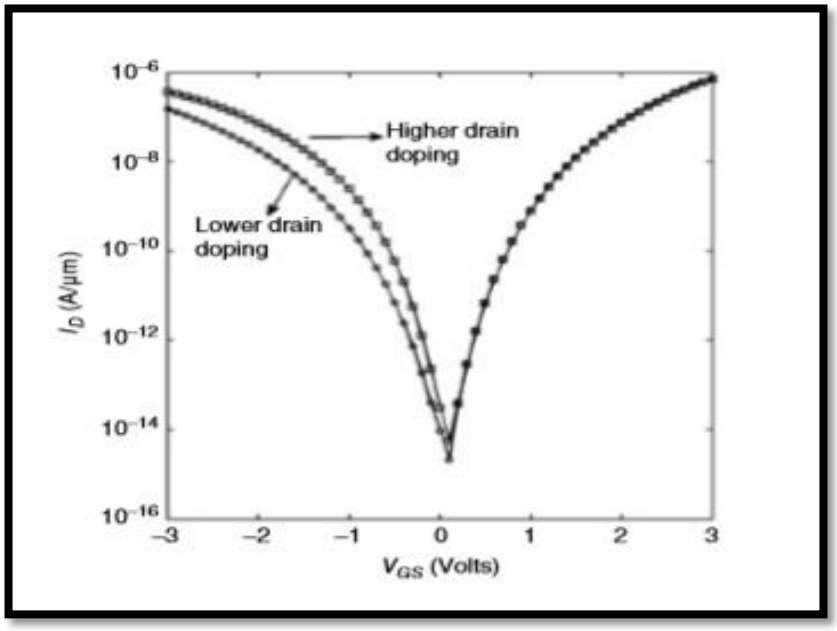


Figure 2.17. Transfer characteristics of an n-channel TFET with different drain doping concentrations for a fixed drain voltage (VDS). [1]

2.8.2. Gate work function

From fig. 2.18 and 2.19. we can understand that if we decrease the gate work function,source channel tunneling is increased and channel drain tunneling is decreased. .Consequently right hand curve of the transfer chracteristics is raised whereas the left hand curve of the transfer characteristics is lowered along current-axis. Hence,curve's central point is shifted towards left.

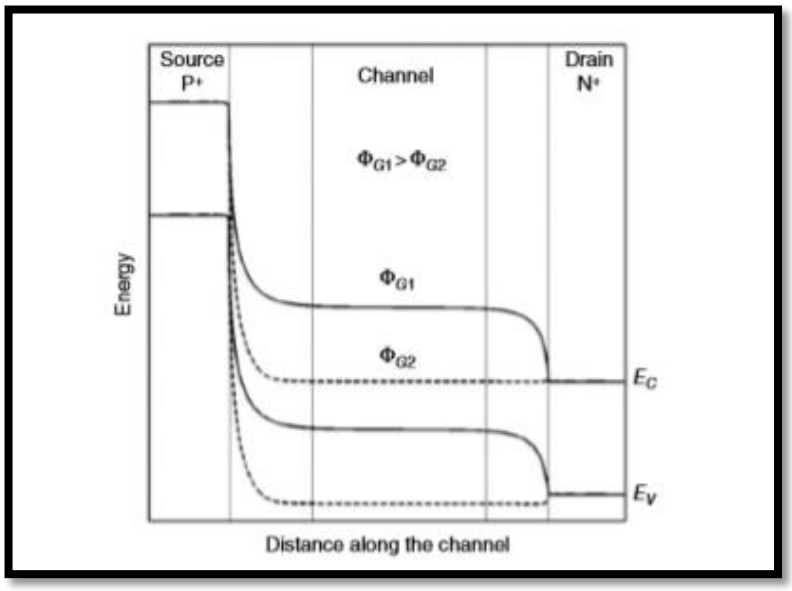


Figure 2.18. Band diagram along the surface of an n-channel TFET for different values of the gate work function.

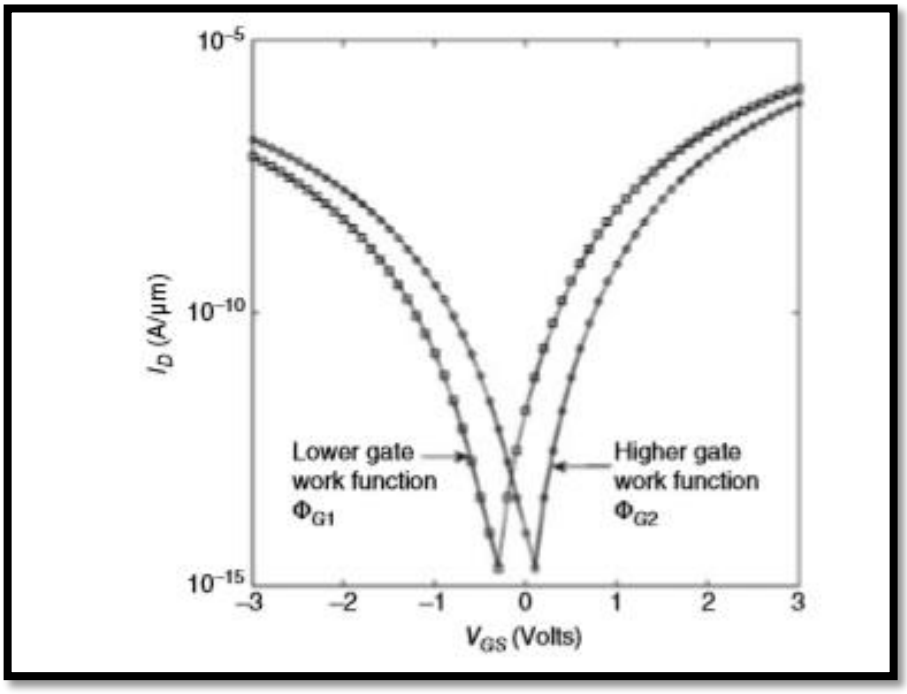


Figure 2.19. Transfer characteristics of an n-channel TFET with different values of the gate work function.

2.8.3. Gate Oxide

We know $C_{ox} = \varepsilon_{ox}/t_{ox}$. More the oxide capacitance, more the gate-control over channel. To increase oxide capacitance we can use oxides with higher permittivity and also we can reduce the thickness of the oxide layer. But in latter case, more leakage current will be present as tunneling probability is more due to the thin oxide layer. Gate leakage is shown in Fig. 2.20.

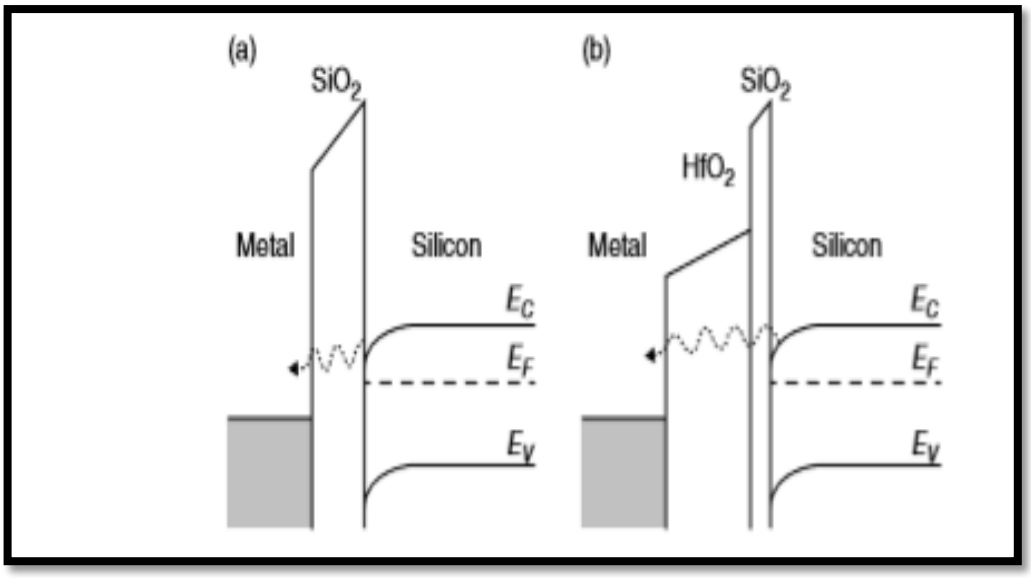


Figure 2.20. Gate leakage in a TFET through (a) SiO2 and (b) HfO2/SiO2 gate stack [2].

2.9. Different types of existing TFET

Broadly we can classify TFET in two categories

(a) Planar TFET – Here current carrying surface is planar .

(b) Three dimensional TFET – In this case current carrying surface is three dimensional.

2.9.1 Planar TFET

Generally in SOI TFET a thin silicon layer (in order of 10 nm) is grown on a thick buried oxide layer (in order of 100 nm).This buried oxide layer blocks leakage currents through the bulk region .

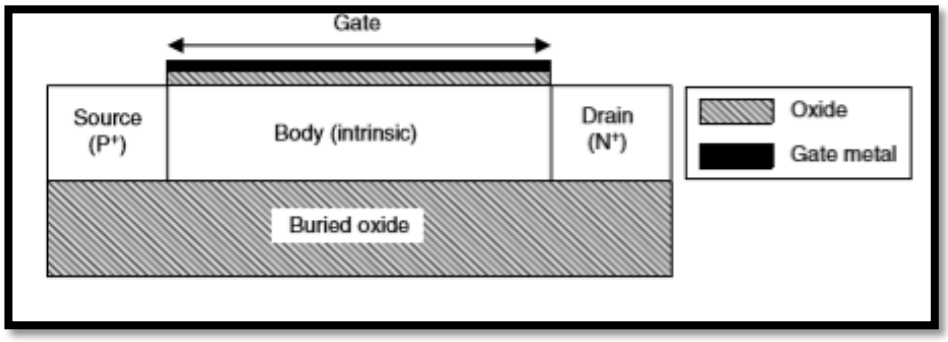


Figure 2.21. P-channel SOI TFET

Different types of already existing planar TFETs are as follows

(a) Double gate TFET

This TFET structure consists of two gates. One at the top end and is known as front gate .Other one is at the bottom end and is called back gate. The presence of two gates increases the controllability over the channel

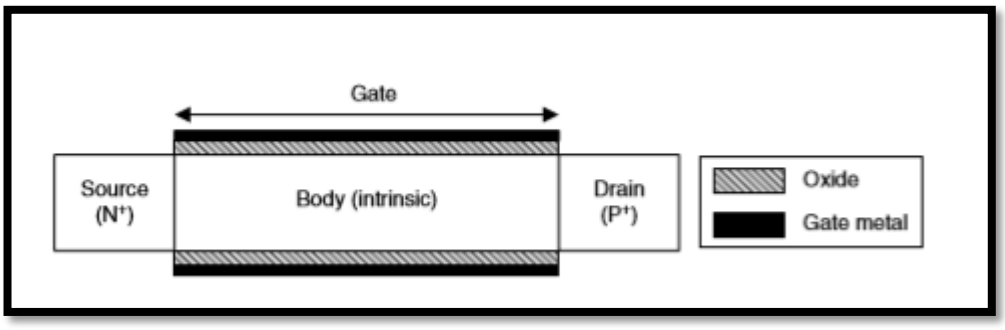


Figure 2.22. P-channel double gate TFET

(b) Dual material gate TFET

A schematic of dual material gate TFET is shown in fig. 2.23 In this structure gate consists of two materials. Gate near the source end is called tunneling gate and the gate near the drain end is called auxiliary gate. The fabrication of this device is possible using sidewall spacer technique. [3]-[5]

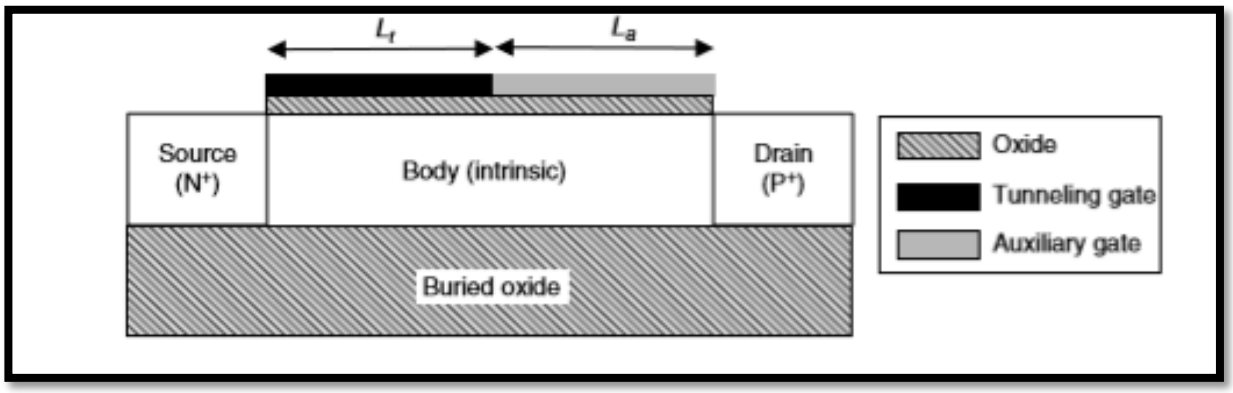


Figure 2.23. P-channel dual material gate TFET

(c) p-n-p-n TFET

A schematic of p-n-p-n TFET structure is shown in figure 2.24. The narrow P+ pocket near the source-channel junction results to narrower tunneling width. Hence, this structure can provide larger ON current than the conventional one.

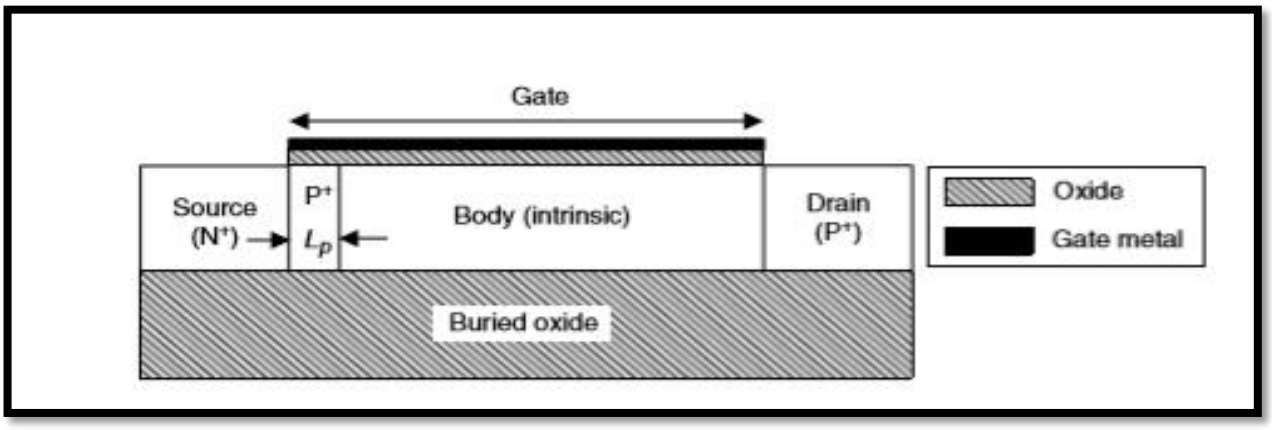


Figure 2.24. p-n-p-n TFET

(d) Raised Ge-source TFET

Silicon TFETs have a limitation of low on current . To overcome this limitation low bandgap material germanium is used. Moreover the advantage of raised source structure is that more tunneling area is provided. Hence, more on current can be achieved. Apart from that,this structure provides steeper subthreshold swing than the conventional TFET.

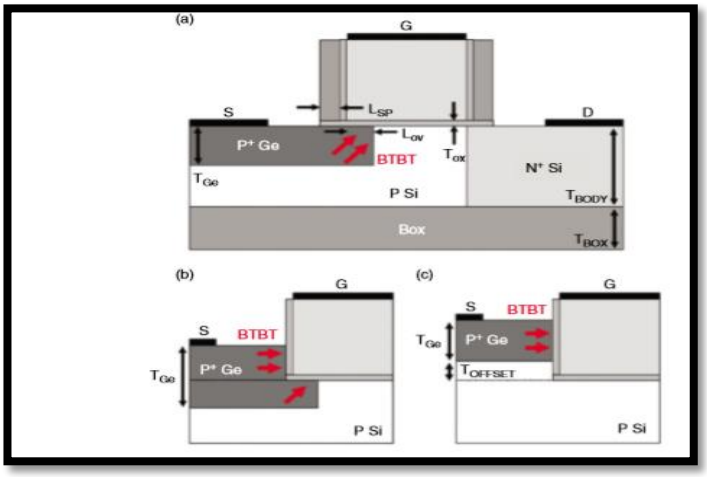


Figure 2.25. Schematic of (a) planar, (b) partially raised and (c) fully raised Ge-source TFETs. Directions of tunneling in each case are shown by arrows [6].

(e) **Heterojunction TFET**

Heterojunction TFET consists of III-V materials instead of silicon. As shown in fig. 2.26. (b) band diagram is staggered near the source-channel junction. Consequently tunneling width becomes less and large on current is achievable.

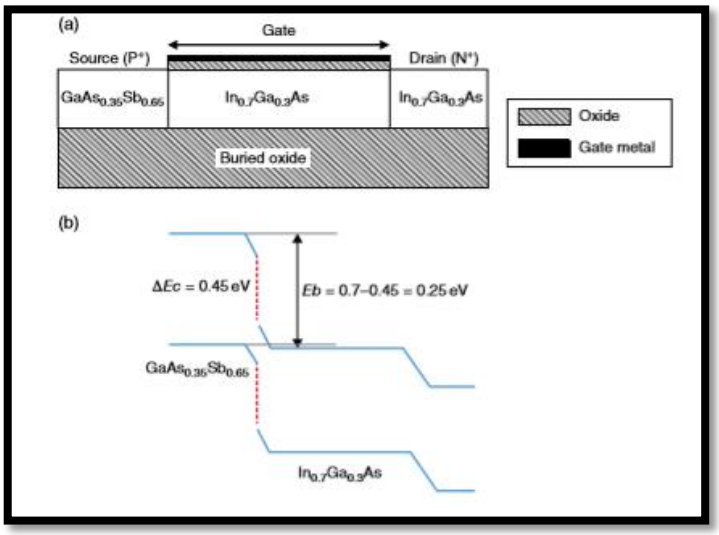


Figure 2.26. (a) Schematic view of an n-channel heterojunction TFET. (b) Band diagram of the heterojunction TFET shown in (a) [7].

(f) Ferroelectric TFET

In ferroelectric TFET a ferroelectric stack material is used between gate metal and oxide. When Gate voltage is applied ,effective gate voltage is increased due to the polarization of ferroelectric material [8] .Hence on current is increased in this type of TFET than conventional ones.

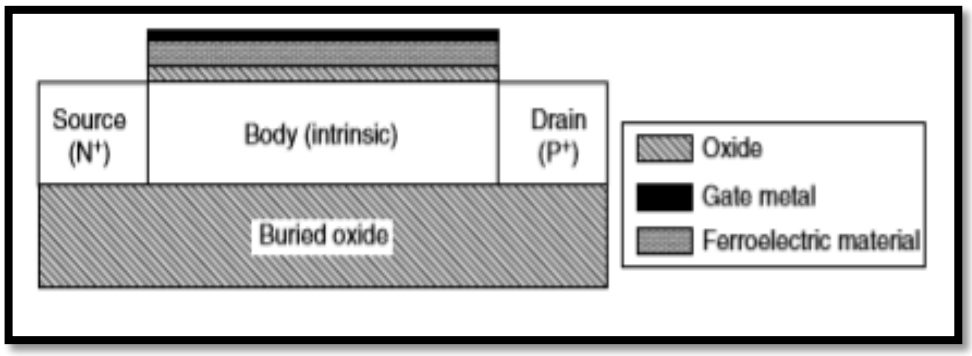


Figure 2.27. P-channel ferroelectric TFET

Moreover,ferroelectric TFET also gives better performance in terms of subthreshold swing. This is depicted in figure 2.28.

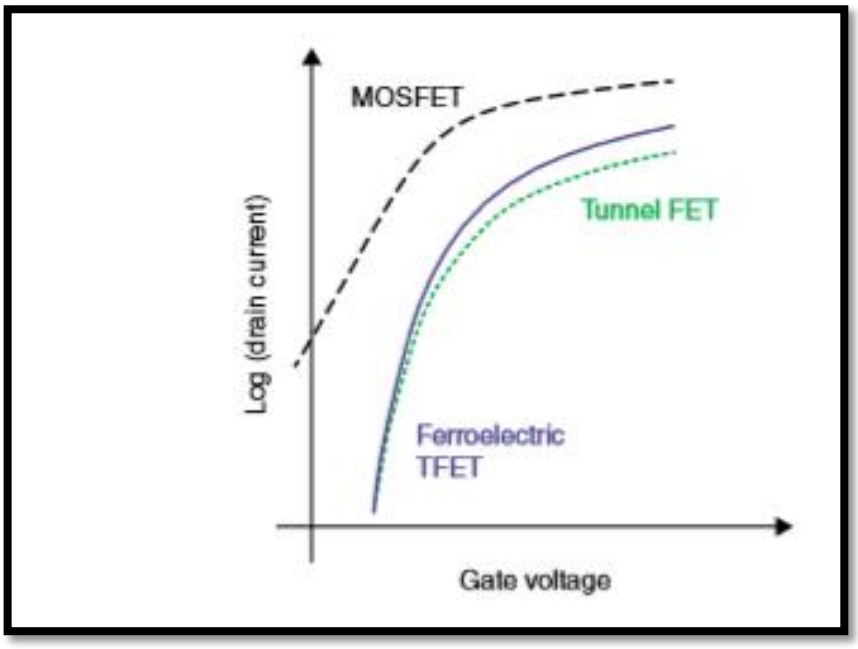


Figure 2.28. Comparison of the ID–VGS curves of a ferroelectric TFET with that of a MOSFET and a conventional TFET [8]

2.9.2 Three dimensional TFET

In three dimensional TFET s current carrying surface exists along three dimension. Most popular 3D TFET s are gate all around nano-wire TFET and tri-gate TFET.

(a) Gate all around nano-wire TFET

In this structure 2 nm thick gate oxide surrounds silicon nanowire of radius 10 nm .And oxide is covered all around by gate metal. This TFET achieves better gate control over channel than double gate TFET [9]-[15].

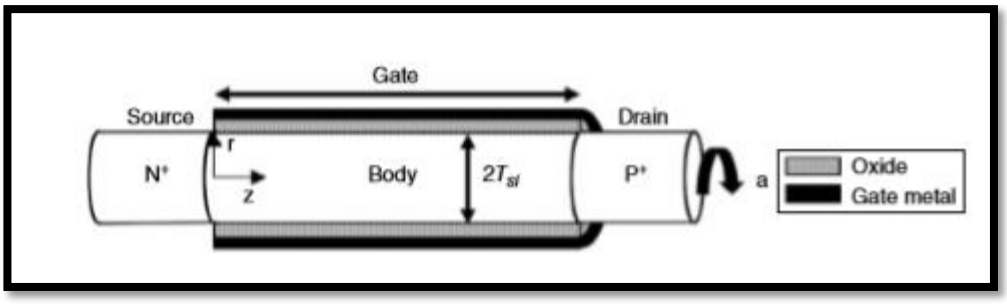


Figure 2.29. Gate all around nanowire TFET

(b) Tri-gate TFET

Tri-gate TFET s are being produced commercially by Intel. It is simpler to fabricate than gate all around nanowire TFET. Short channel effects are done away with in this structure. It also performs better in terms of on current and subthreshold swing.

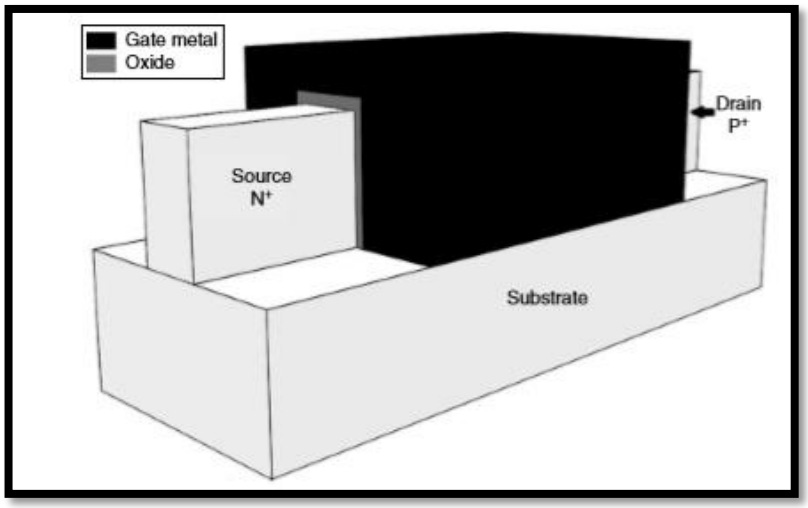


Figure 2.30. Tri-gate TFET

2.10. Drain Engineered TFET

Splitted drain structure displays considerable reduction in ambipolar conduction due to increase of the tunneling width at the channel-drain junction [17]. Based on this a research work was conducted .[18]. In this extended work four TFET structures are considered.

(a) Splitted-Drain Single-Gate TFET (SD-SG TFET: total drain is splitted),

(b) Top-Splitted-Drain Single-Gate TFET (TSD-SG TFET: splitted-drain in upper location),

(c) Mesial-Splitted-Drain Single-Gate TFET (MSD-SG TFET: splitted-drain in middle location),

(d) Basal-Splitted-Drain Single-Gate TFET (BSD-SG TFET: splitted-drain in bottom location).

2.10.1 Device structure and parameter

The 2-D cross-sectional view of the p-channel TFET structures are given in Fig. 2.31. (a) Splitted-Drain Single-Gate TFET (SD-SG TFET), (b) Top-Splitted-Drain Single-Gate TFET (TSD-SG TFET), (c) Mesial-Splitted-Drain Single-Gate TFET (MSD-SG TFET) and (d) Basal-Splitted-Drain Single-Gate TFET (BSD-SG TFET). The structures contain two separate drain regions of different concentration instead of a single doped drain region present in a conventional TFET. The highly-doped drain region is above the lightly doped region. The Doping specification of the TFET models are: P+ type source region ($1\times10^{20}cm^{-3)}$ and P channel region (1×10^{17} cm^{-3}), which are kept constant for all the simulations. Such doping concentration create a tunnel junction between source and channel where the phenomenon of inter-band tunneling occur for the TFET to conduct in N-mode. The doping specification of the upper N+ doped drain region is 5×10^{18} cm^{-3}, drain electrode has the Ohmic contact with this higher doped drain region. The lower N doped drain region is 1×10^{17} cm^{-3}. Both disparate drain regions are variably doped to attain an optimal doping profile after analyzing the simulated graphs of all the characteristics. The device is simulated with lateral dimensions of 70nm, 50nm, 70nm for source, gate and drain respectively and a total device length of 250nm. A 30nm oxide overlapped depletion region is present in both side of source and drain, this region is to reduce impact ionization and improve ON current. The vertical dimensions of Si ground plane andSiO_2 spacer is 20 nm and 20nm respectively. The length of the both parted drain regions D1 and D2 are varied to get the optimal dimensions for better characterizations and in these structures, both drain parts vertical lengths are 30nm each for SD-SG TFET and 5nm for other three TSD-SG TFET, MSD-SG TFET, BSD-SG TFET. The dielectric used for gate electrode is SiO_2, which has a thickness of t_{ox} = 1nmand dielectric constant is 3.9. Table 2.1 summarizes all the parameters for all the structures [19]-[26].

Table 2.1 Device Parameters

Parameters name/unit	Symbol	SD-SG TFET	TSD-SG TFET	MSD-SG TFET	BSD-SG TFET
Source doping (cm^{-3})	N_s	1×10^{20}	1×10^{20}	1×10^{20}	1×10^{20}
Channel doping(cm^{-3})	N_{ch}	1×10^{17}	1×10^{17}	1×10^{17}	1×10^{17}
Drain doping (cm^{-3})	N_{D1}	5×10^{18}	5×10^{18}	5×10^{18}	5×10^{18}
	N_{D2}	1×10^{17}	1×10^{17}	1×10^{17}	1×10^{17}
Substrate doping (cm^{-3})	n_i	1×10^{17}	1×10^{17}	1×10^{17}	1×10^{17}
source length (nm)	X_s	100	100	100	100
Channel Length (nm)	L	50	50	50	50
Effective Channel Length (nm)	L_{eff}	50	50	60	70
Drain Length (nm)	X_d	100	100	100	100
source width (nm)	Y_s	60	60	60	60
Channel width (nm)	W	60	60	60	60
Drain width (nm)	Y_{d1}, Y_{d2}	30, 30	5,5	5,5	5,5
Length of electrical drain (nm)	L_{ED}	70	5	5	5
Silicon body thickness	T_{si}	60	60	60	60
Oxide thickness (nm)	T_{ox}	1	1	1	1
Work function of control gate (eV)	$\emptyset ms$	4.1	4.1	4.1	4.1
Substrate, box thickness (nm)	T_{box}	20	20	20	20

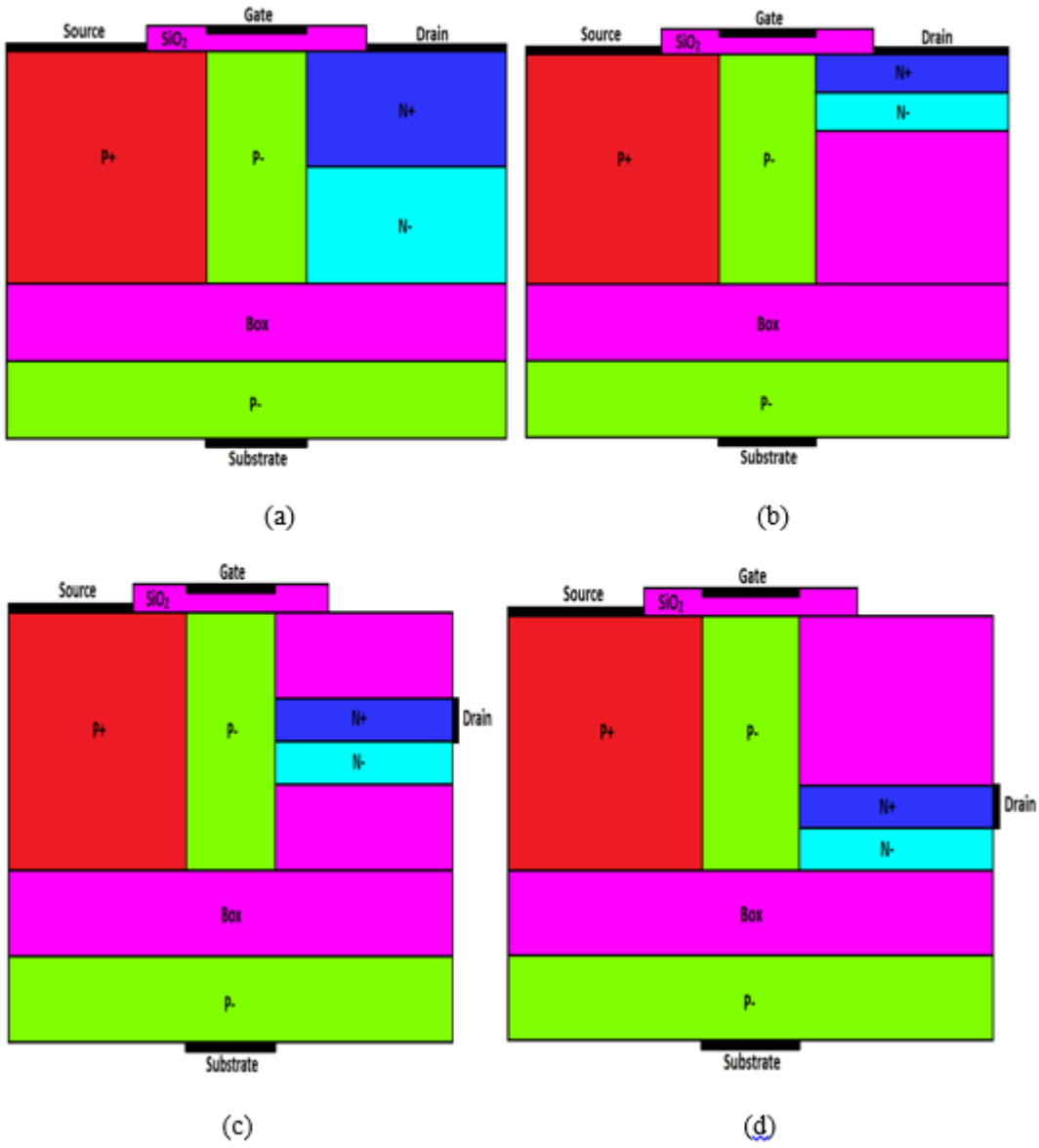


Figure 2.31. Device Structure of (a) Splitted-Drain Single-Gate TFET (SD-SG TFET), (b) Top-Splitted-Drain Single-Gate TFET (TSD-SG TFET), (c) Mesial-Splitted-Drain Single-Gate TFET (MSD-SG TFET) and (d) Basal-Splitted-Drain Single-Gate TFET (BSD-SG TFET)

2.10.2. Observations

Analytical and simulation based study was conducted during the research work. Following are some observations found .From Fig.2.32 we can understand the potential profile performance is the best in case of BSD-SG TFET. A comparative graphical result is demonstrated in Fig. 2.32. As the potential is higher in BSD-SG TFET, the drain current is also is the highest in the proposed structure. The comparison between transfer characteristics of several structures is graphically represented in Fig, 2.33.

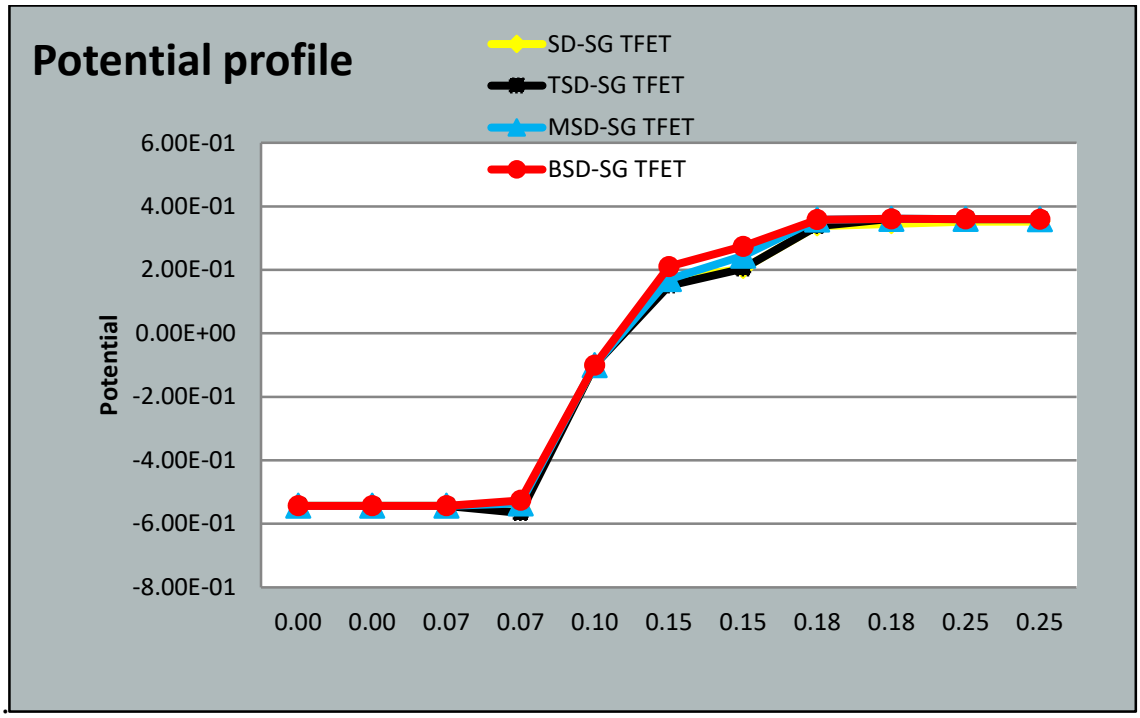


Figure 2.32. Comparison of potential profile

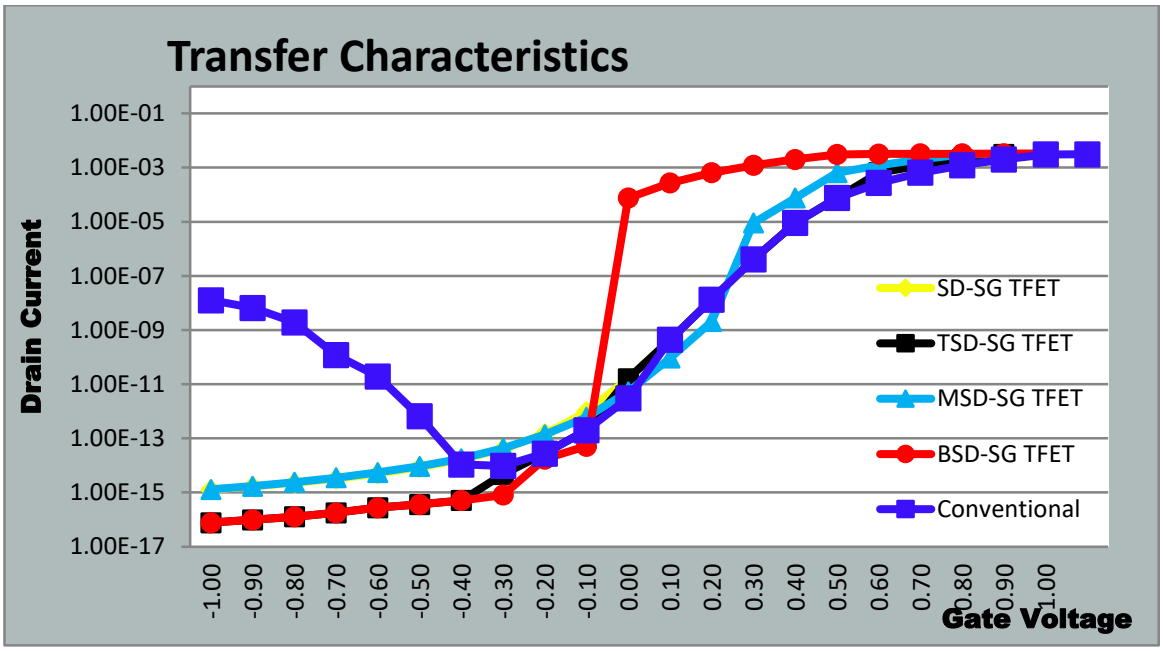


Figure 2.33. Comparison of transfer characteristics

From Fig. 2.33. we can make out that ambipolar current is considerably reduced in this drain-engineered TFET structures. All the proposed structures are better than conventional TFET as shown in Fig. 2.33.

2.11. Literature Review:

❖ Saurav Roy et al. demonstrated a vertical ultra-thin body TFET [28] in 2017. A dielectric body wall or STI wall is used as an isolating material in this device. In this study it is revealed that the proposed device structure works identically to a SOI-MOS without using SOI wafer. As STI wall is used instead of buried oxide layer, it overcomes the high cost factor and complex fabrication procedures in case of SOI wafers. Moreover, it is claimed that proposed FET structure can be scaled down extensively.

❖ Zheng Chen et al. have introduced a new concept of energy efficiency by varying source doping gradient of TFET [29]. A relationship has been established between switching activity factor, nominal SDG and σ-SDG. Based on this relationship the optimal design technique is investigated during this research work with the view point of source doping gradient variation.

❖ In [30] a two source TFET is demonstrated by Navjeet Bagga et al. In this study introduction of two sources ensures increased tunneling area that leads to better device performance in terms of on current. In a nutshell the utility of this TFET structure primarily depends on the enhanced BTBT obtained by the structural modification.

❖ In [31] Jang Hyun Kim et al. has conducted a research work regarding sandwiched vertical lightly doped Si- channel in double gate TFET. This structure exhibits excellent tunnel controllability. An improved performance in terms of SS and ON/OFF ratio are also achieved in this VS-TFET.

❖ Bijoy Goswami et al. demonstrated a TFET design with a T-shaped channel in one of their studies [32]. In this device better tunneling profile is noticed than conventional TFET. The emphasis is given on reduction of ambipolar current during the research work. Furthermore, better ON/OFF current ratio is achieved in this T-Channel TFET than traditional TFET device.

❖ Bijoy Goswami et al. also demonstrated another TFET structure to study the effect of differentially doped drain on the device output characteristics and its ambipolar behavior [33]. Here ambipolar current is surprisingly found much more suppressed than popular TFET structures. So,the proposed structures in this study are proved to be power efficient and application oriented in the field of emerging TFET technology.

❖ Fan Chen et al. have conducted a study on the scalability and switching mechanism of Vertical-TFETs [34]. The interrelation between switching mechanism and energy filtering has been the centre of attention here . Based on this relationship, several optimizations in device dimensions are done.

❖ Cem Alper et al. have simulated several TFET devices incorporating quantum mechanical models [35]. This work has taken care of the sub band quantization .Similar approach is observed in a research work conducted by J.L. Padilla et al [36]. The primary motivation behind these two works is to look into the degradation of output current behavior due to sub band quantization. The quantum mechanical models deviate the device characteristics from the ideal one. As we are moving towards ultra-nano regime ,we need to take care of quantum mechanical effects. Hence these works are invaluable in the field of TFET technology.

❖ Pritha Banerjee et al. have demonstrated a 3D Silicon on Nothing MOSFET in one of their academic explorations [37]. Physics based several models are incorporated in this research work. An analytical model is also formulated in the work. This work explains some major drawbacks of MOSFETs so that emergence of better performing TFET is necessary right now.

2.12. Next footstep

We have already looked into the effect of drain engineering in previous section. Our present research work is motivated to study the effects of source engineering in several TFET structures. [21-26]
In following three chapter we will make an attempt to do so.

❖ In chapter 3 we will study the effect of differentially doped source region.
❖ In chapter 4 we will study the effect of source extension in both sides. (i.e salient source TFET)
❖ In chapter 5 we will make an attempt to model a double source TFET structure

So in this research work,we are trying to have a clear idea about the effects of source engineering in TFET structures.

2.13. Simulation software

All the simulations during the research work is done in Silvaco ,Atlas.[27]
ATLAS provides general capabilities for physically-based two (2D) and three-dimensional (3D) simulation of semiconductor devices. It predicts the electrical behavior of specified semiconductor structures and provides insight into the internal physical mechanisms associated with device operation.

2.14. Quantum simulation

Several local and non-local tunneling models can be incorporated in quantum simulation [27] Moreover density gradient model and self-consistent Schrodinger –Poisson model is also included in simulation Variation of several parameters are also analyzed in these quantum models in that study. Following that research work we have also attempted the same in the double source TFET structure.

References

[1] Tunnel Field-Effect Transistors (TFET) Modelling and Simulation
Jagadesh Kumar Mamidala ,Rajat, Pratyush Pandey

[2] R. Vishnoi and M. J. Kumar, "Compact Analytical Model of Dual Material Gate Tunneling Field Effect Transistor using Interband Tunneling and Channel Transport," IEEE Transactions on Electron Devices, vol. 61, no. 6, pp. 1936– 1942, June 2014.

[3] R.Vishnoi and M.J.Kumar,"Compact Analytical Drain Current Model of Gate-All Around Nanowire Tunneling FET",IEEE Transactions on Electron Devices,vol.61, no. 7, pp. 2599–2603, July 2014.

[4] R.Vishnoi and M.J.Kumar, "Two Dimensional Analytical Model for the Threshold Voltage of a Tunneling FET with Localized Charges", IEEE Transactions on Electron Devices, Vol. 61, no. 9, pp. 3054 – 3059, September 2014.

[5] R.Vishnoi and M.J.Kumar, "An Accurate Compact Analytical Model for the Drain Current of a TFET from Sub-threshold to Strong Inversion", IEEE Transactions on Electron Devices, vol. 62, no. 2, pp. 478–484, February 2015.

[6] R.Vishnoi and M.J.Kumar, "Two Dimensional Analytical Model for the Threshold Voltage of a Gate All Around Nanowire Tunneling FET with Localized Charges", IEEE International Conference on Nanotechnology, Rome, Italy, July 2015.

[7] C. Chen, S.-L. Ong, C.-H. Heng, G. Samudra and Y.-C. Yeo, "A Variational Approach to the Two-Dimensional Nonlinear Poisson's Equation for the Modelling of Tunneling Transistors", IEEE Electron Device Letters, vol. 29, pp. 1252–1255, November 2008.

[8] L. Komzisk, Applied Calculus of Variations for Engineers, CRC Press, 2009.

[9] X. Liang and Y. Taur, "A 2-D Analytical Solution for SCEs in DG MOSFETs", IEEE Trans. on Electron Devices, vol. 51, pp. 1385–1391, August 2004.

[10] E. Kreyszig, Advanced Engineering Mathematics, 8th edn, John Wiley & Sons, 1999.

[11] N. Cui, R. Liang, J. Wang and J. Xu, "Si-based Hetero-Material-Gate Tunnel Field Effect Transistor: Analytical Model and Simulation," 12th IEEE International Conference on Nanotechnology (IEEE-NANO), 2012, pp. 1–5.

[12] N. Cui, R. Lianga, J. Wang and J. Xu, "Two-dimensional analytical model of hetero strained Ge/strained Si TFET", International Silicon–Germanium Technology and Device Meeting (ISTDM), 2012, pp. 1–2.

[13] M. Lee and W. Choi, "Analytical Model of Single-Gate Silicon-on-Insulator Tunneling Field-Effect Transistors", Solid State Electron., vol. 63, no. 1, pp. 110–114, 2011.

[14] M.Gholizadeh and S.E.Hosseini, "A2-DAnalyticalModelforDouble-GateTunnel FETs", IEEE Trans. on Electron Devices, vol. 61, pp. 1494–1500, May 2014.

[15] L.Liu,D.Mohanta,and S.Datta, "Scaling Length Theory of Double-Gate Interband Tunnel Field-Effect Transistors", IEEE Trans. Electron Devices, vol. 59, no. 4, pp. 902–908, April 2012.

[16] S. Lin and J. Kuo, "Modeling the Fringing Electric Field Effect on the Threshold Voltage of FD SOI nMOS Devices with the LDD/Sidewall Oxide Spacer Structure", IEEE Trans. Electron Devices, vol. 50, no. 12, pp. 2559–2564, December 2003.

[17] B. Raad, K. Nigam, D. Sharma, and P. Kondekar, "Dielectric and work function engineered TFET for ambipolar suppression and RF performance enhancement," Electron. Lett., vol. 52, no. 9, pp. 770–772, Apr. 2016.

[18] Disha Bhattacharjee, Bijoy Goswami, Dinesh Kumar Dash, Ayan Bhattacharya, Subir Kumar Sarkar "Analytical Modelling and Simulation of Drain Doping Engineered Splitted Drain Structured TFET and its Improved Performance in Subduing Ambipolar Effect" Solid State Electronics

[19]. Subir Kumar Sarkar: "Spintronics Device Based VLSI Chip for Error Correction in Wireless Cellular Communication"AIUB Journal of Science and Engineering.Volume 8 Number 1 August 2009.

[20]. Saheli Sarkhel, Navjeet Bagga and Subir Kumar Sarkar, "Compact 2D Modeling and Drain Current Performance Analysis of a Work Function Engineered Double Gate Tunnel Field Effect Transistor." Journal of Computational Electronics, Springer, Vol. 15, Issue 1, pp. 104-114, March 2016.

[21]. Amit Jain and Subir Kumar Sarkar "Design and Reliability analysis of a 4 :1 Mux using Single Electron Tunneling technology based Threshold Logic Gate", Journal of Electron Devices, Vol-15, Pp-1241-1248,2012.

[22]. N. Basanta Singh, Sanjoy Deb, Asish Kumar De and Subir Kumar Sarkar, 'Design and Simulation of 2–to-4 Decoder Using Single Electron Tunneling Technology based Threshold Logic Gate' Journal of Electron Devices, Vol. 9, pp. 342-351 , 2011.

[23].Sanjoy Deb, N. Basanta Singh,D Das, A K De and Subir Kumar Sarkar, “Analytical model of threshold voltage and sub-threshold slope of SOI and SON MOSFETs: A Comparative study, Journal of electron devices, Vol.8, pp-300- 309, 2010.

[24].Tiya Dey Malakar, Partha Bhattacharyya and Subir kumar Sarkar, "Quantum Analytical Modelling of Threshold Voltage for Linearly Graded Alloy Material Gate Recessed S/D SOI MOSFET" IEEE International Conference on Devices for Integrated Circuits (DEVIC-17),Kalyani Govt. Engg. College, 23-24 March, 2017

[25].Bibhas Manna, Saheli Sarkhel, Ankush Ghosh, S S Singh and Subir Kumar Sarkar,“Dual Material Gate Nanoscale SON MOSFET: For Better Performance”, International Journal of Computer Application (IJCA), ISBN: 973-93-80875-27-15, 2013

[26].Tripty Kumari and Subir Kumar Sarkar,"Performance Analysis and Comparative Study of Triple Metal Double Gate TFET with SOI equivalent", IEEE International Conference on Devices for Integrated Circuits (DEVIC-17), Kalyani Govt. Engg. College, 23-24 March, 2017. [28] Atlas User’s Manual, Silvaco Int., Santa Clara, CA, May 26, 2006.

[27] Doctoral thesis , “Study and simulation of advanced Si-based Nano-devices” – J.L.Padilla de la Torre

[28] Saurav Roy, Amitabh Chatterjee, Dheeraj Kumar Sinha, Rimma Pirogova, and Srimanta Baishya,” 2-D Analytical Modeling of Surface Potential and Threshold Voltage for Vertical Super-Thin Body FET”, IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 64, NO. 5, MAY 2017

[29] Cheng Chen, Zhixuan Wang, Yang Zhao,” New Insights into Energy Efficiency of Tunnel FET with Awareness of Source Doping Gradient Variation”, IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 65, NO. 5, MAY 2018

[30] Navjeet Bagga, Anil Kumar, and Sudeb Dasgupta ,” Demonstration of a Novel Two Source Region Tunnel FET”, IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 64, NO. 12, DECEMBER 2017

[31] Jang Hyun Kim, Sangwan Kim and Byung-Gook Park,” Double-Gate TFET With Vertical Channel Sandwiched by Lightly Doped Si”, IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 66, NO. 4, APRIL 2019

[32] Bijoy Goswami, Disha Bhattacharjee, Dinesh Kumar Dash, Ayan Bhattacharya, Subir Kumar Sarkar “Demonstration of T-shaped channel Tunnel Field-Effect Transistors” 2nd International Conference on Electronics, Materials Engineering and Nano-Technology (IEMENTech 2018) , 4-5th May 2018, IEM Gurukul Campus, Kolkata, West Bengal, IEEE.

[33] Bijoy Goswami, Disha Bhattacharjee, Dinesh Kumar Dash, Ayan Bhattacharya, Subir Kumar Sarkar “Drain Doping Engineering and its influence on Device Output Characteristics and Ambipolar

Conduction on a Splitted-Drain TFET model" International Conference in Communication, Devices and Networking (ICCDN 2018) Sikkim Manipal Institute of Technology, Sikkim, 2-3rd June 2018,Springer

[34] Fan Chen , Hesameddin Ilatikhameneh , Yaohua Tan, Gerhard Klimeck , and Rajib Rahman," Switching Mechanism and the Scalability of Vertical-TFETs", IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 65, NO. 7, JULY 2018

[35] Cem Alper, Pierpaolo Palestri,Livio Lattanzio, Jose L. Padilla and Adrian M. Ionescu," Two Dimensional Quantum Mechanical Simulation of Low Dimensional Tunneling Devices"

[36] J. L. Padilla, F. Gámiz, and A. Godoy," A Simple Approach to Quantum Confinement in Tunneling Field-Effect Transistors", IEEE ELECTRON DEVICE LETTERS, VOL. 33, NO. 10, OCTOBER 2012

[37] Pritha Banerjee and Subir Kumar Sarkar," 3-D Analytical Modeling of Dual-Material Triple-Gate Silicon-on-Nothing MOSFET"," IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 64, NO. 2, FEBRUARY 2017"

[38]. Baba, T. "Proposal for Surface Tunnel Transistors." Japanese Journal of Applied Physics, 31 http://jjap.jsap.jp/link?JJAP/31/L455/ L455-L457 (1992).

[39]. Reddick, W. M. & Amaratunga, G. A. J. "Silicon surface tunnel transistor." Applied Physics Letters, 67 http://link.aip.org/link/?APL/67/494/1 494-496 (1995).

CHAPTER 3

IMPACT OF SOURCE ENGINEERING IN SPLIT DRAIN TUNNEL FIELD EFFECT TRANSISTOR

Chapter 3: Impact of Source Engineering in Split Drain Tunnel Field Effect Transistor

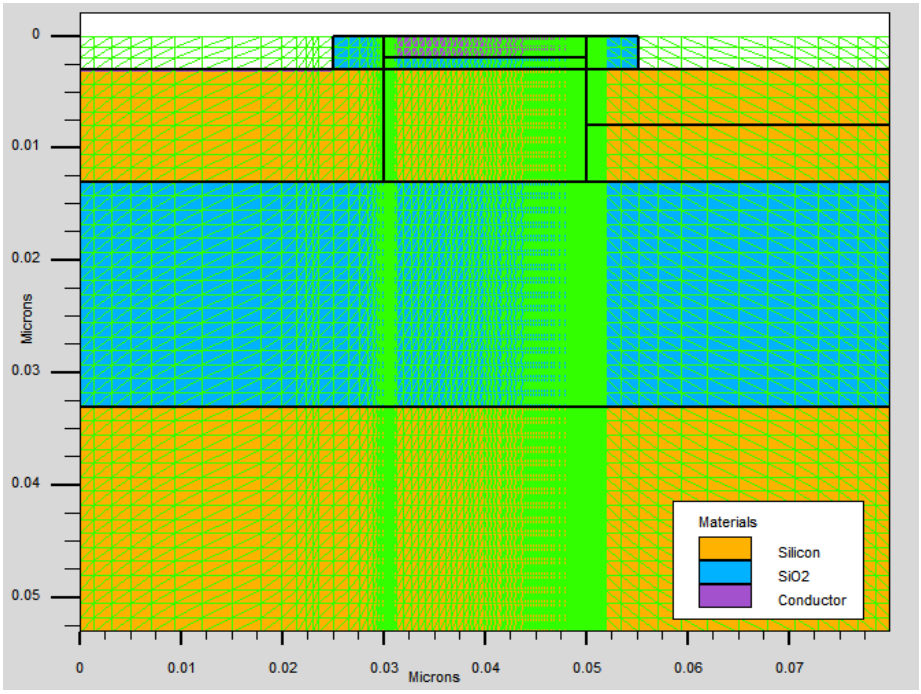
3.1. Introduction and proposed work

This chapter confers the results of the analysis of source and drain doping engineering for a 2D TFET model. Two different models have been extensively studied that are composed of split source and split drain region with varying doping concentration. Both the models consist of split drain, one with split source and another with double split source and are specified as Split Source Split Drain TFET (SS-SD TFET) and Double Split Source Split Drain TFET (DSS-SD TFET).The device characteristics are compared with Split Drain (SD TFET) model [1-3] and the improvements are registered that exhibits reduction in ambipolar conduction (OFF current) along with the increase of tunneling effect.

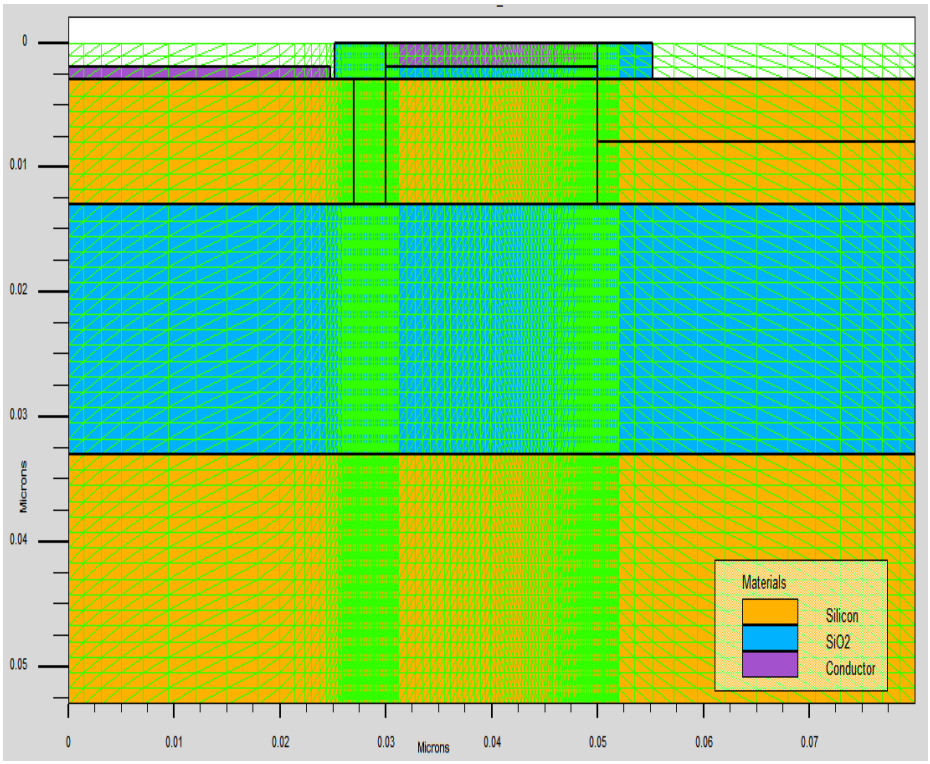
Ambipolar conduction [3-9] is the foremost curtailment in case of TFET at the drain channel junction in addition to low ON current than MOSFET [10]. To overcome this shortcoming, gate-drain underlap structure [13] is suggested that reduces the ambipolar conduction significantly along with the current driving capability [12] which is not acceptable. Therefore an alternative perspective is considered in this paper where source as well as drain doping engineering [11] is included in 2D TFET devices. The structures are investigated by simulation to study the influence of the split drain and split source regions. The structures are named after the split regions at source and drain such as Split Source Split Drain TFET (SS-SD TFET) and Double Split Source Split Drain TFET (DSS-SD TEFT). In the first case source is split into lightly doped followed by a heavily doped p type region and in the second case it is split into three regions where an additional heavily doped n type region accompanies the previous case. This structure offers many advantageous outcome such as low OFF current and low ambipolar conduction. The study consists of comparison of I_d-V_{gs} and I_d-V_{ds} characteristics among the three different structures. The band diagram considering different conditions of gate and drain bias are also analyzed.

Simulations are performed using Silvaco, Atlas.

3.2. Device structure and parameters



(a)



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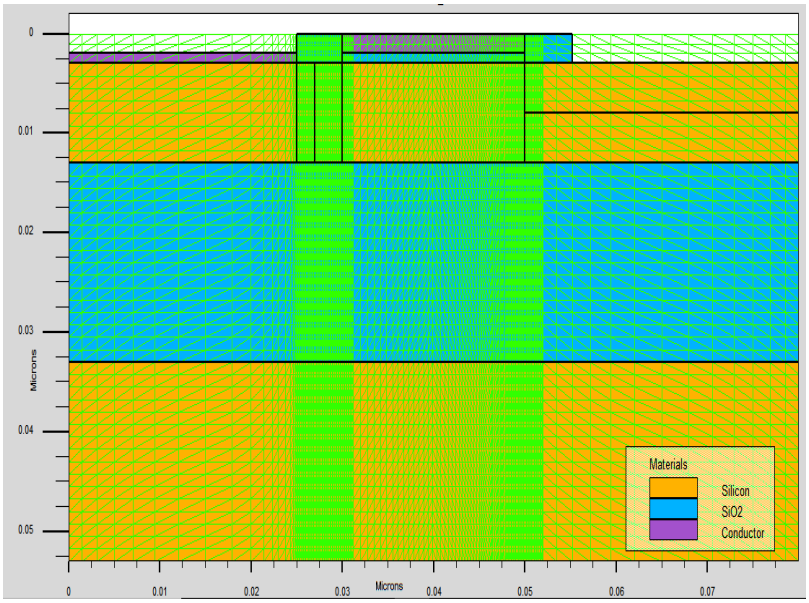


(c)

Fig 3.1: Structures along with corresponding doping profiles of (a) Split Drain TFET (SD TFET) , (b) Split Source Split Drain TFET (SS-SD TFET) (c) Double Split Source Split Drain TFET (DSS-SD TFET)

The structures in Fig 3.1 are 2D cross sectional view of (a) Split drain TFET (SD TFET) , (b) Split source split drain TFET (SS-SD TFET) and (c) Double split source split drain TFET (DSS-SD TFET) derived by the simulation in Silvaco, Atlas. The drain regions of all the structures considered here are split regions having different doping concentrations in comparison with conventional single doping drain region TFET. The other two variants of structure includes split source region along with split drain with different doping profile. The drain doping specifications are given as follows: highly doped n type drain region ($5x10^{18}cm^{-3}$) above lightly doped n type drain region ($10^{17}cm^{-3}$).The source doping specification for double split source is: lightly doped p type region at left side ($10^{17}cm^{-3}$), highly doped p type region in the middle ($10^{18}cm^{-3}$) and highly doped n type region at the right side ($10^{18}cm^{-3}$). The split source structure has source doping specification similar to double split structure except the right side highly doped n type region. Channel is n type and body of the device is p type with both having concentration of $10^{15}cm^{-3}$.The doping concentrations are kept constant throughout the simulation process including the tunnel region which is responsible for the interband tunneling phenomenon. The lateral dimension of the device is considered as follows: the total length of the device is 80nm which is divided into 30nm, 20nm and 30nm for source, channel under gate and drain regions respectively. Above both source and drain regions some oxide overlap regions having length 5nm and thickness of 3nm is present to prevent impact ionization and to increase the conductance during ON

time. The vertical length of both the oxide and bottom semiconductor plane is 20nm each. The effective vertical dimension of each of the parts of the split drain is 5nm. The drain contact is made at the lower lightly doped drain region only. For split source the length of the left part is of 27nm and the right part is 3nm whereas for double split source the lateral dimension of the left part is of 25nm, middle part is 2nm and right part is 3nm. SiO2 is used as the gate dielectric having dielectric constant of 3.9 and thickness of tox=2nm and n-type polysilicon is used as the gate material.

Fig. 4.1 displays the mesh points at the source channel and channel drain junctions are more closely spaced in order to obtain better accuracy of the results.

3.3. Simulation setup

Silvaco, Atlas version 5.20.2.R is used for simulation considering the following models: Lombardi mobility model (CTV), Fermi Dirac statistics and the Shockley-Read-Hall and Auger recombination models, bandgap narrowing model , nonlocal BTBT.

3.4. Results and discussion:

(a) Electron Mobility

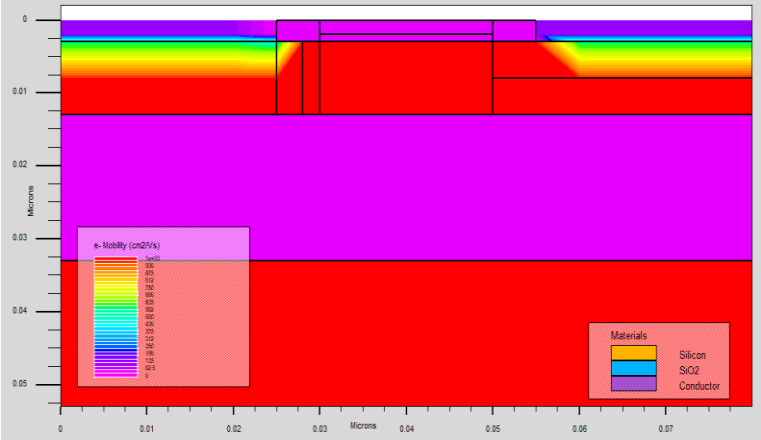


Fig 3.2: Electron Mobility profile of the carriers for the DSS-SD-TFET structure.

Fig. 3.2 exhibits the mobility of electron for the DSS-SD TFET structure. It is evident from the figure that the red colored areas have highest mobility that is present along the channel from source to drain. As the mobility is greater for the lower part of the split drain therefore the drain contact is taken at the lower part only.

(b) Drain Output Characteristics

Drain output characteristics are depicted in the following Fig.3.3 for the above discussed three structures such the SD TFET model, the SS-SD TFET model and the DSS-SD TFET model. In all the three cases the channel length is taken as 20nm. The range of Vds is upto 1V along with Vgs value of 0.5V. It is evident from the figure that the drain current is maximum for DSS-SD TFET among the three structures considered here suggesting it as the best in this case.

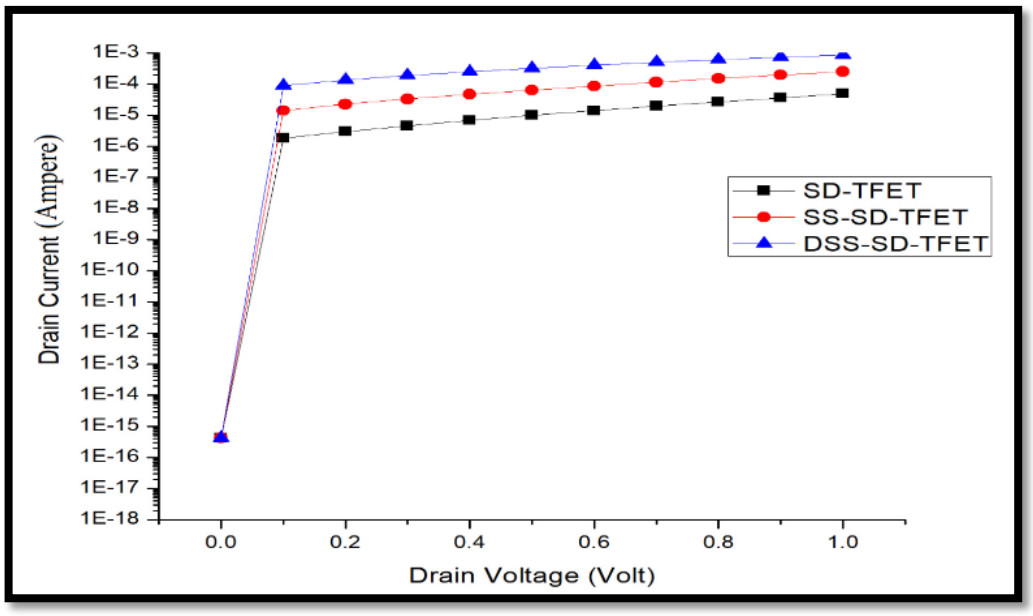


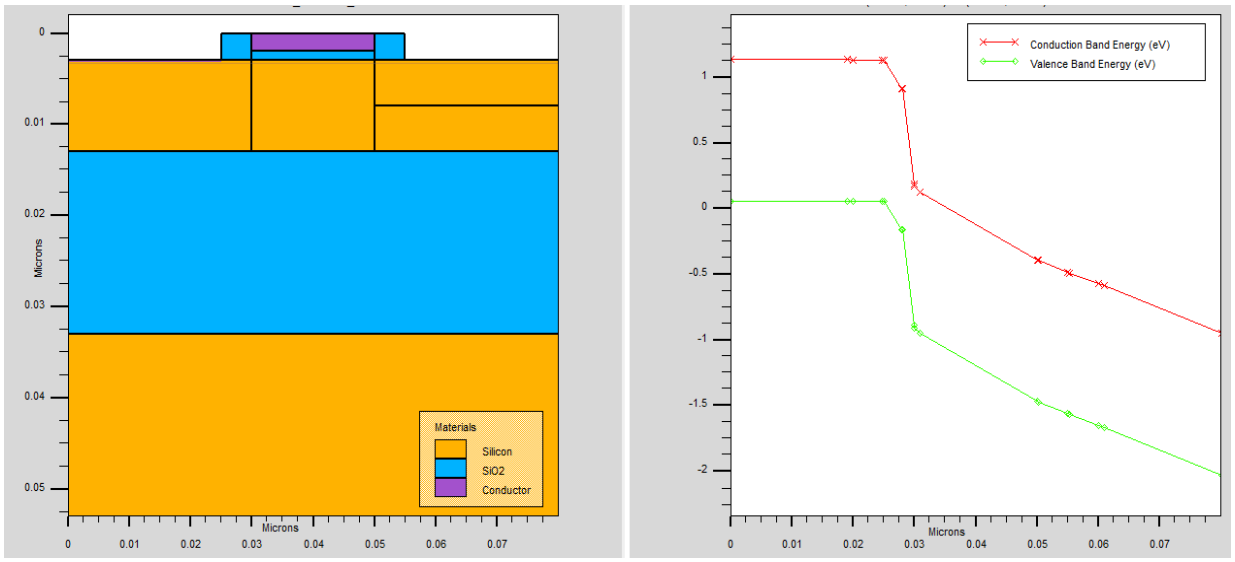
Fig.3.3: Comparison of Drain current vs Vds characteristics for three structures such as SD-TFET, SS-SD TFET and DSS-SD TFET.

(c) Band Diagram Analysis

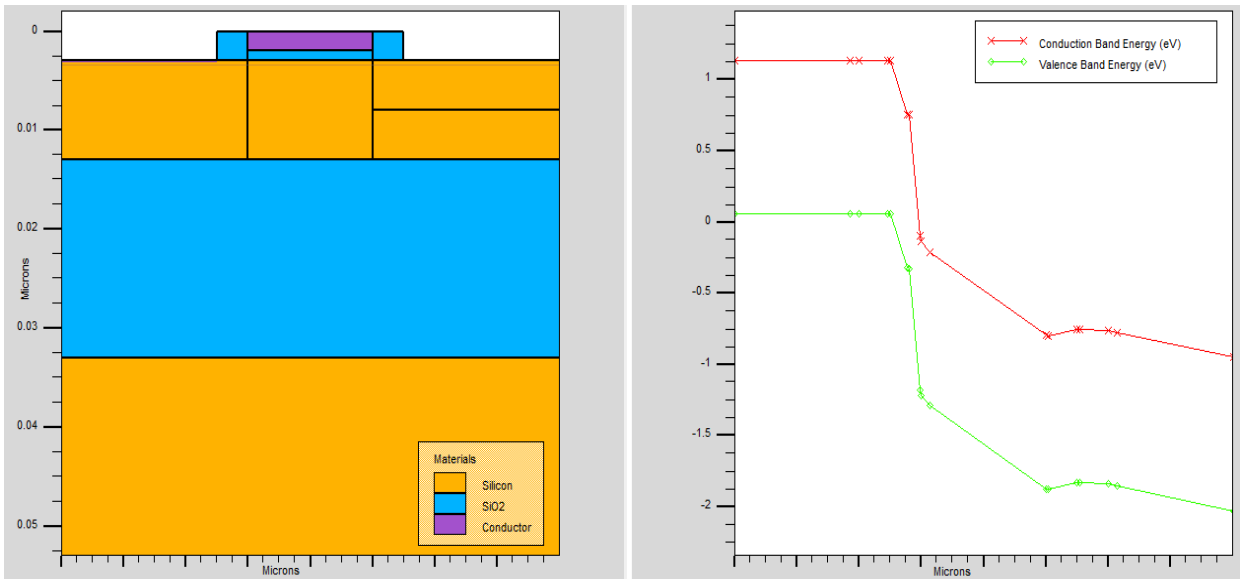
The band diagrams of the above three models are analyzed for two conditions such as: V_{gs} =V_{ds} =1V and V_{gs}>V_{ds} where V_{gs} =1.5V and V_{ds} =1V. Keeping V_{ds} =1V at constant value when V_{gs} =1V, TFET will be just ON and when V_{gs} =1.5V, TFET will be in ON condition.

In comparison with the SD TFET structure we observe that SS-SD TFET structure provides improvement in terms of source tunneling and significant reduction in ambipolarity.The outcome of DSS-SD TFET structure additionally exhibits drastic reduction in ambipolar conduction because of reverse band bending at the drain end. The tunnel width is also minimum in DSS-SD TFET structure among all the three presented here depicting better ON current[14-15].

Band diagrams for the SD TFET model are shown below.



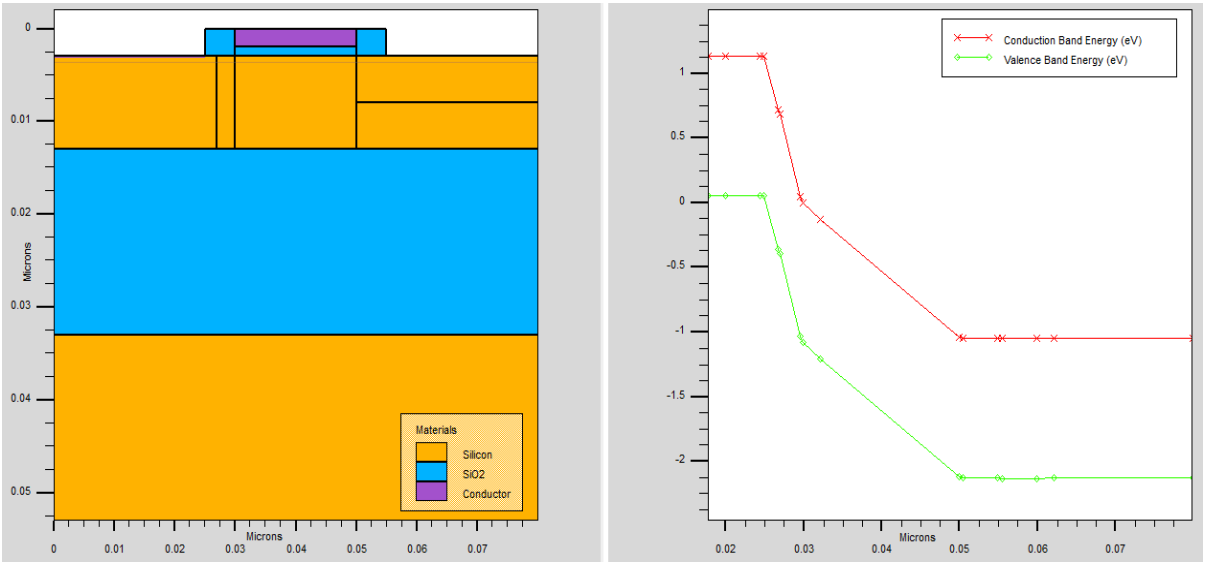
(a)



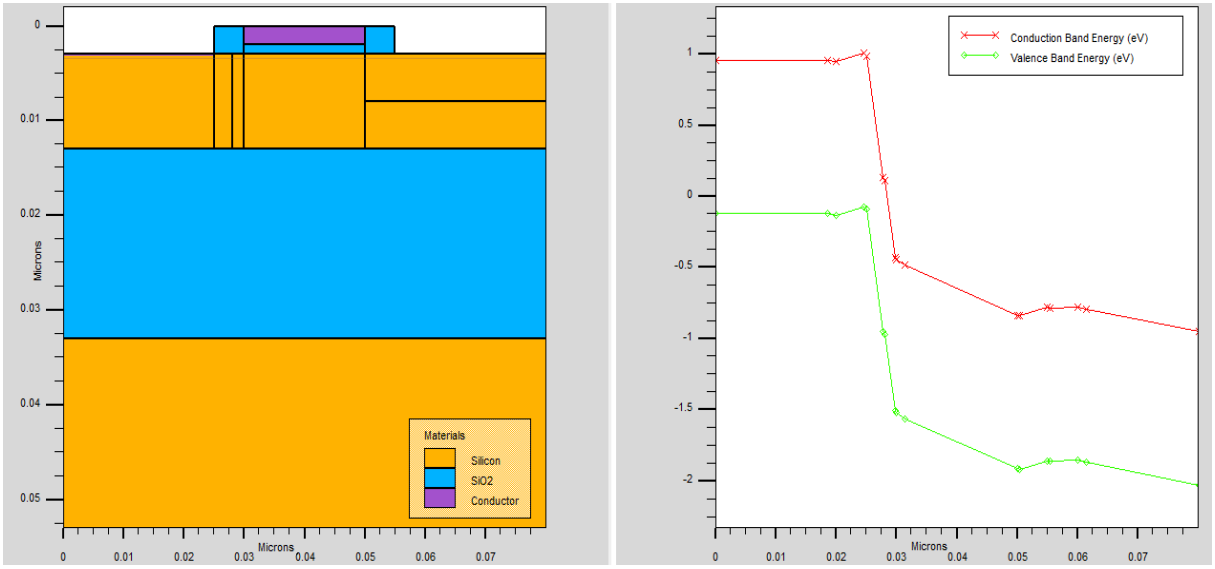
(b)

Fig 3. 4: Band diagram of the SD TFET structure for (a) Vgs = Vds (Just ON) and (b) Vgs > Vds (ON).

Band diagrams for SS-SD TFET is shown below.



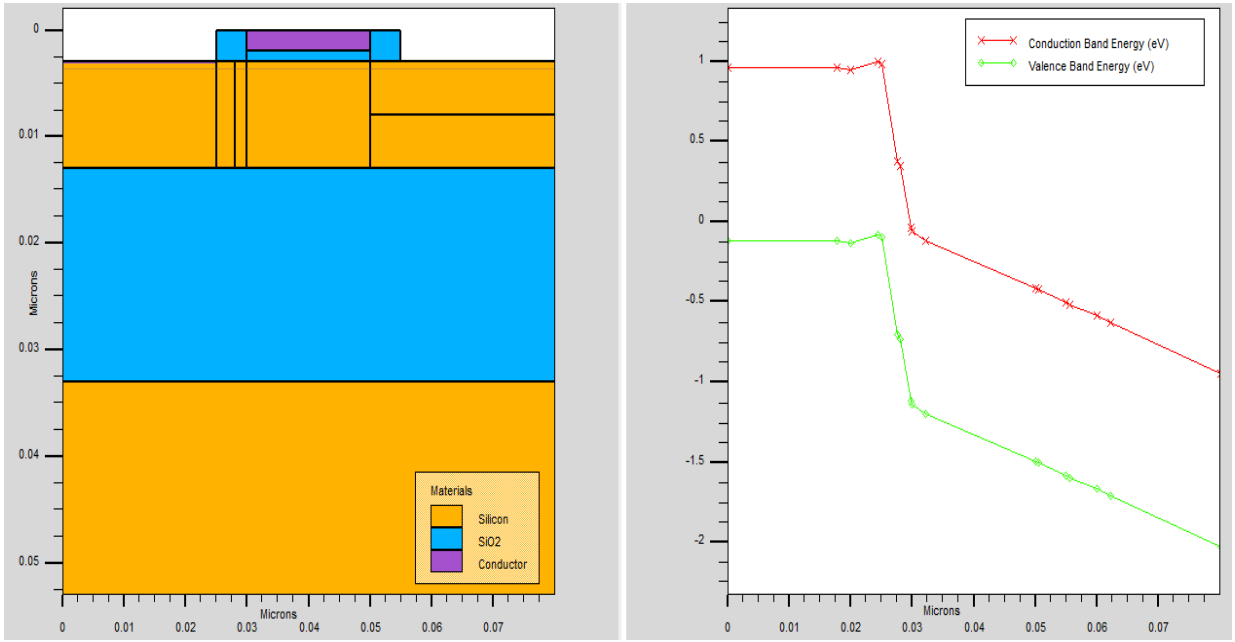
(a)



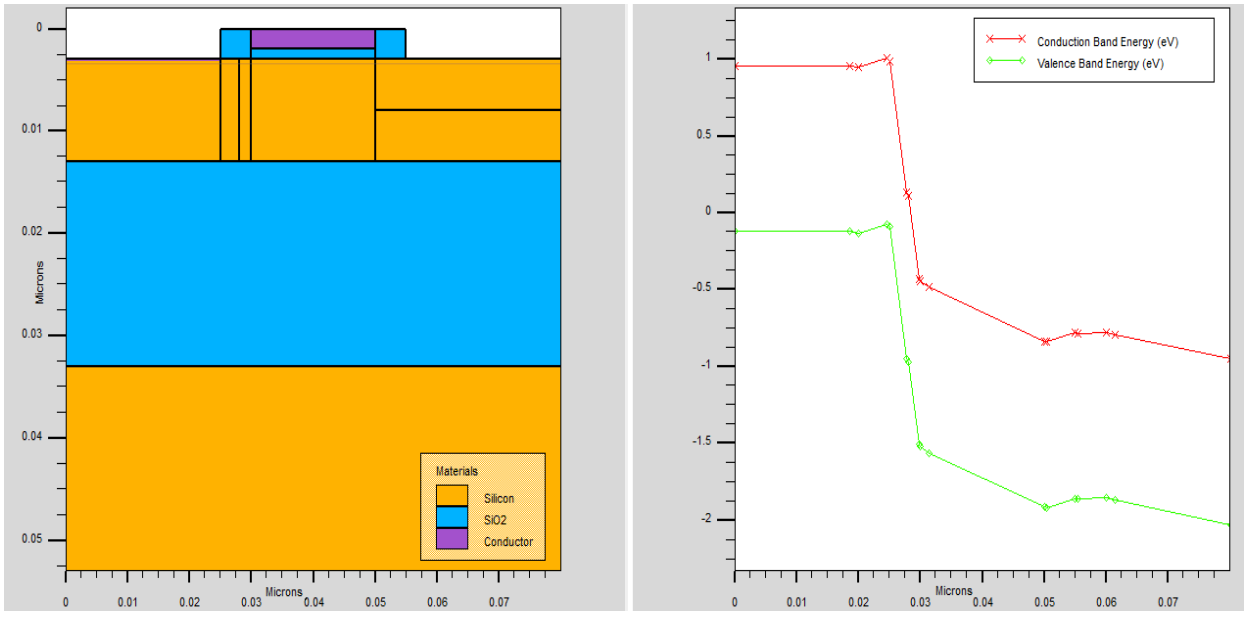
(b)

Fig 3.5: Band diagrams of SS-SD TFET structure for (a) Vgs = Vds (Just ON) and (b) Vgs > Vds (ON)

Band diagrams for DSS-SD TFET are shown below.



(a)



(b)

Fig 3.6: Band diagram for DSS-SD TFET structure for (a) Vgs = Vds (Just ON) and (b) Vgs > Vds (ON)

(d) Transfer Characteristics

The transfer characteristics of the three structures are compared for the V_{gs} sweep from -0.5V to 2V for V_{ds}=1V.

The graph of Fig.3.7 depicts that the device ON current for SD-TFET is lower than SS-SD TFET and DSS-SD TFET due to broader tunnel width. In addition to this the DSS-SD TFET exhibits lowest OFF current among the three structures[16-18]. Table.1 contains the ratio of ON-OFF current for three structures and it is evident that DSS-SD TFET has the best I_{on}/I_{off} ratio among the three. This characteristics proves the effectiveness of the structure.

TABLE 3.1. COMPARISON OF ON-OFF CURRENT RATIO FROM SIMULATION

STRUCTURE	DSS-SD TFET	SS-SD TFET	SD TFET
I_{on}/I_{off}	5×10^{10}	1.49×10^{10}	5.6×10^{8}

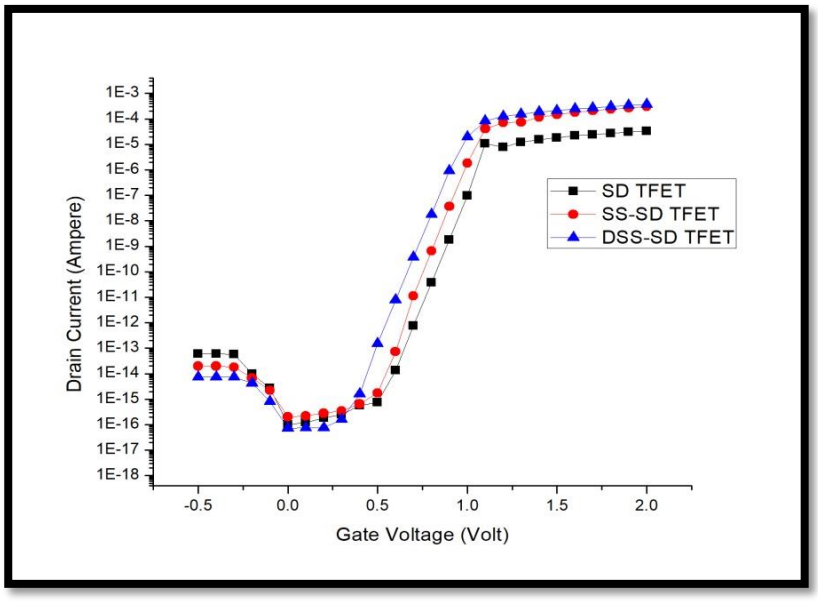


Fig 3.7: Transfer characteristics of SD TFET, SS-SD TFET and DSS-SD TFET structures.

References

[1]Y. Khatami and K. Banerjee, "Steep subthreshold slope n-and p-type tunnel-FET devices for low-power and energy-efficient digital circuits," *IEEE Transactions on Electron Devices,* vol. 56, pp. 2752-2761, 2009.

[2]A. M. Ionescu and H. Riel, "Tunnel field-effect transistors as energy efficient electronic switches", Nature, vol. 479, no. 7373, pp. 329–337, Nov. 2011.

[3]A. C. Seabaugh and Q. Zhang, "Low-voltage tunnel transistors for beyond CMOS logic", Proc. IEEE, vol. 98, no. 12, pp. 2095–2110, Dec.2010.

[4]S. Saurabh and M. J. Kumar, "Novel attributes of a dual material gate nanoscale tunnel field-effect transistor," *IEEE Trans. Electron Devices,* vol. 58, no. 2, pp. 404–410, Feb. 2011.

[5]B. Ghosh and M. W. Akram, "Junctionless tunnel field effect transistor," *IEEE Electron Device Lett.*, vol. 34, no. 4, pp. 584–586, May 2013.

[6]L. Lattanzio, L. De Michielis, and A. M. Ionescu, "Complementary germanium electron–hole bilayer tunnel FET for sub-0.5-V operation," *IEEE Electron Device Lett.*, vol. 33, no. 2, pp. 167–169, Feb. 2012.

[7]J. Appenzeller, Y.-M. Lin, J. Knoch, and P. Avouris, "Band-to-band tunneling in carbon nanotube field-effect transistors," *Phys. Rev. Lett.*, vol. 93, no. 19, p. 196805, Nov. 2004.

[8]N. Bagga, S. Sarkhel and Subir Kumar Sarkar, "Recent research trends in gate engineered tunnel FET for improved current behavior by subduing the ambipolar effects: A review," In *Computing, Communication & Automation (ICCCA), 2015 International Conference on IEEE*, pp. 1264-1267, May 2015.

[9]S. Sarkhel, N. Bagga, and Subir Kumar Sarkar, " Compact 2D modeling and drain current performance analysis of a work function engineered double gate tunnel field effect transistor," *Journal of Computational Electronics*, vol. 15, issue 1, pp. 104-114, Dec. 2015.

[10] K. K. Bhuwalka, J. Schulze, and I. Eisele, "Scaling the vertical tunnel FET with tunnel band gap modulation and gate work function engineering," *IEEE Trans. Electron Devices*, Vol. 52, No. 5, pp. 909-917, May.2005.

[11] Ahmed Shaker, Mona El Sabbagh, and Mohammed M. El-Banna, " Influence of Drain Doping Engineering on the Ambipolar Conduction and High-Frequency Performance of TFETs" ieee transactions on electron devices, vol. 64, no. 9, september 2017.

[12] B. Raad, K. Nigam, D. Sharma, and P. Kondekar, "Dielectric and work function engineered TFET for ambipolar suppression and RF performance enhancement," Electron.Lett., vol. 52, no. 9, pp. 770–772, Apr. 2016.

[13] A. S. Verhulst, W. G. Vandenberghe, K. Maex, and G. Groeseneken, “Tunnel field-effect transistor without gate-drain overlap,” Appl. Phys. Lett., vol. 91, no. 5, p. 053102, Jul. 2007.

[14] Bibhas Manna, Saheli Sarkhel, Ankush Ghosh, S S Singh and Subir Kumar Sarkar,“Dual Material Gate Nanoscale SON MOSFET: For Better Performance”, International Journal of Computer Application (IJCA), ISBN: 973-93-80875-27-15, 2013

[15] Tripty Kumari and Subir Kumar Sarkar,"Performance Analysis and Comparative Study of Triple Metal Double Gate TFET with SOI equivalent", IEEE International Conference on Devices for Integrated Circuits (DEVIC-17), Kalyani Govt. Engg. College, 23-24 March, 2017.

[16] Bijoy Goswami, Disha Bhattacharjee, Dinesh Kumar Dash, Ayan Bhattacharya, Subir Kumar Sarkar “Demonstration of T-shaped channel Tunnel Field-Effect Transistors” 2nd International Conference on Electronics, Materials Engineering and Nano-Technology (IEMENTech 2018) , 4-5th May 2018, IEM Gurukul Campus, Kolkata, West Bengal, IEEE.

[17] Bijoy Goswami, Disha Bhattacharjee, Dinesh Kumar Dash, Ayan Bhattacharya, Subir Kumar Sarkar “Drain Doping Engineering and its influence on Device Output Characteristics and Ambipolar Conduction on a Splitted-Drain TFET model” International Conference in Communication, Devices and Networking (ICCDN 2018) Sikkim Manipal Institute of Technology, Sikkim, 2-3rd June 2018,Springer

[18] Disha Bhattacharjee, Bijoy Goswami, Dinesh Kumar Dash, Ayan Bhattacharya, Subir Kumar Sarkar “Influence of Drain Doping Engineering in Triple Splitted-Drain TFET model”International Conference on Recent innovations in Electrical, Electronics & Communication Engineering - ICRIEECE”. July 27th and 28th 2018 School of Electrical Engineering, Kalenga institute of Industrial Technology (KIIT), Bhubaneswar, India, IEEE

CHAPTER 4

ANALYTICAL MODELING AND SIMULATION OF LOW POWER SALIENT SOURCE DOUBLE GATE TFET

Chapter 4: Analytical Modeling and Simulation of Low Power Salient Source Double Gate TFET

4.1. Introduction and Proposed Work

The analytical surface potential model of 22nm salient source Double Gate TFET(SS-DG-TFET) is presented in this paper. The surface potential is analyzed as the performance parameter along with assessment of improved ON/ OFF current ratio. The variation of tunnel current is examined under same front and back gate bias together with identical oxide thickness [1]-[4]. The source region has been extended symmetrically in both direction in order to enhance the conductivity of the channel region and it has been efficiently deployed in the proposed model[5]-[11]. The execution of low power functionality and lower sub-threshold slope is also established in this model. Performance study [12]-[14] has been conducted previously along with the development of analytical models for the description of TFET devices [15]-[24]. The deficiency of proper drain current model [21],[22] and in some of the models [23],[24] the influence of depletion region on the drain current is limited to the source side only and ambipolar conduction at the channel drain interface [25] has been overlooked. Previously the tunnel current was determined by numerical integration of carrier generation rate upon depletion region rather than tunneling length[18],[20],[21],[24],[26]. We consider the tunneling process at the source channel interface in the proposed design . The boundary conditions are estimated considering the maximum and minimum tunneling length at the interfaces for the bias conditions [27].

The most attractive feature of the proposed structure is low power friendliness. Several results are compared by applying different drain voltages. Transfer characteristics comparison is presented in this work. Further tunneling phenomenon is analyzed from energy band diagrams of the device under different operating conditions.Thereafter electric field and potential study has been conducted. An analytical model of surface potential is derived. At last a comparison is done between the proposed structure and the conventional double gate TFET.

All the simulations are executed by Silvaco, Atlas.

4.2. Device structure with optimized parameters

The 2D cross sectional view of the proposed SS-DG-TFET structure has been depicted in Fig. 4.1. The structure contains an extended source region which is symmetric on both vertical sides resulting into the vertical dimension of the source to be 28nm whereas the drain region as well as the channel region

are restricted to 14nm of height. The channel length is considered to be 22nm for best performance and length of both the source and drain regions are taken as 10nm each. So the total device length is determined to be 42nm. The optimum doping concentration after investigation is found to be $1x10^{21}$ cm^{-3}, $1x10^{15} cm^{-3}$ and $1x10^{19}$ cm^{-3}in source, channel and drain regions respectively. It can be clearly identified in Fig.2 where y axis indicates doping concentration in logarithmic scale. The source region is heavily doped P+ type, channel is lightly doped N type and drain is heavily doped N+ type silicon. The oxide region is extended laterally as well as vertically at source side to avoid contact of the gate with source region as the source is also extended and the same technique is adopted at the drain side as well to maintain the symmetric structure. The lateral dimension of extended oxide on both side of gate is 1nm each which results into the total oxide length of 22nm whereas the optimum gate thickness is found to be 4nm with 20nm length. So the vertical dimension of oxide regions are t_{ox} = 1nm under gate and 5nm at the extended parts. This oxide and gate structure is followed in both the upper and lower gates of the dual gate structure for symmetry. The dielectric used for gate oxide is SiO_2 with dielectric constant 3.9 and N type polysilicon is used as gate material.

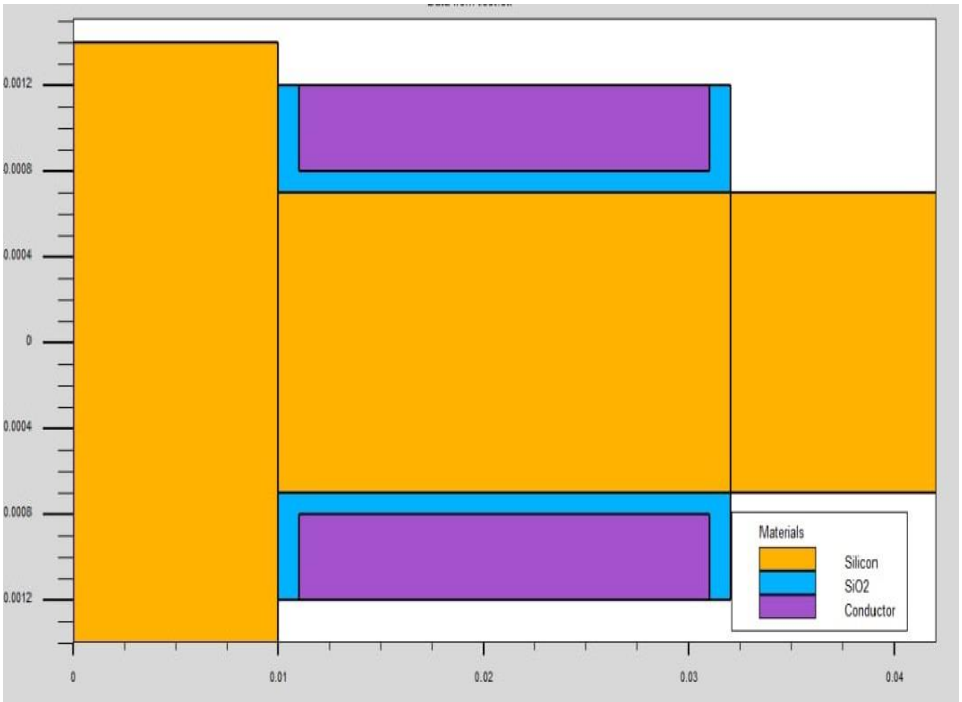


Fig. 4.1: 2D cross sectional view of salient source DG-TFET

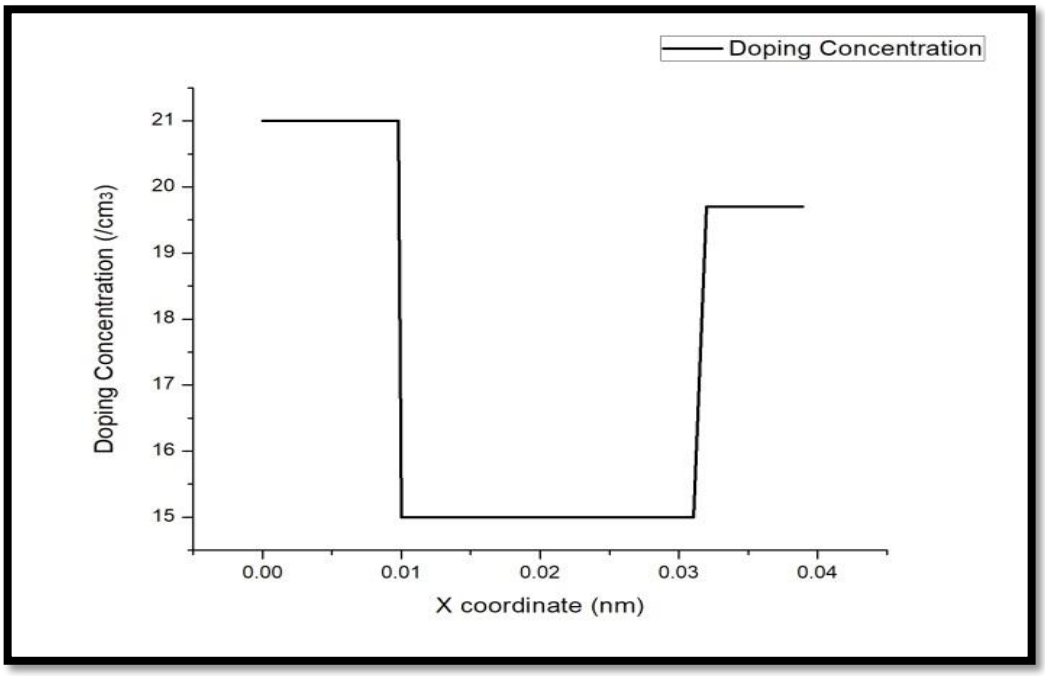


Fig. 4.2: Doping concentration along the device

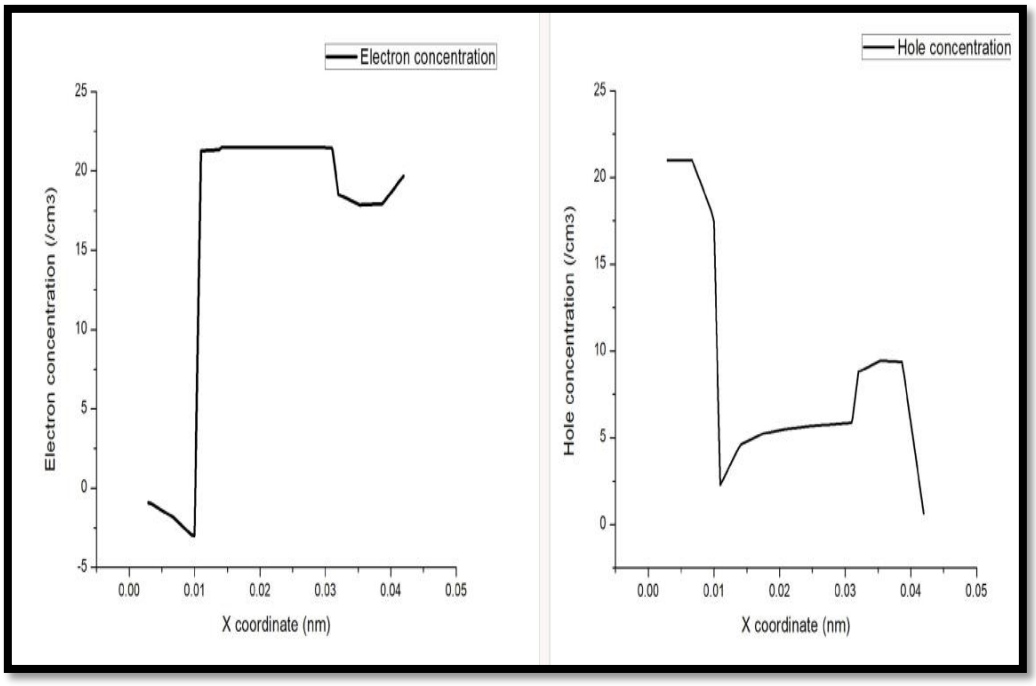


Fig. 4.3: Electron and hole concentration in SS-DG-TFET

Further we can estimate the behavior of charge carriers (i.e. electrons and holes) in SS-DG-TFET along the length of source, channel and drain region from Fig. 4.3. As source region doping is p-type Si whereas

channel and drain consist of n-type Si, hence electron and hole concentration along the length (x-coordinate) of the device is self-explanatory from the figure.

4.3. Results and Discussions:

(a) Study of Gate Voltage-Drain Current Characteristics

From the curves of drain current with respect to gate to source voltage it is prominent that the OFF current decreases resulting into lowering of ambipolar conduction with respect to conventional TFET. Thus in low power also the ON to OFF current ratio is in the order of 10^{10} that depicts good performance characteristics of the proposed model. We have investigated the gate current for three different drain to source voltages such as 0.4V, 0.5V and 0.6V. It is evident from Fig. 4.4 that sub-threshold slope (SS) decreases with the decrease of Vds . This phenomenon is striking .It can be concluded that the device works as better TFET in lower drain-to-source voltage. When Vds = 0.4 Volt that is at the lowest voltage among the three compared here, SS is lowest which exhibits the best performance of the proposed model. It indicates that the structure operates as the best in low power.

TABLE 4.1

VALUES OF SUB-THRESHOLD SLOPE CORRESPONDING TO V_{ds}

Gate Voltage	**Sub-threshold Slope**
0.4 Volt	39 mv/decade
0.5 Volt	48 mv/decade
0.6 Volt	54 mv/decade

Table 4.1 suggests that the proposed TFET is low power friendly device in terms of subthreshold slope ,hence it is faster in low power operations than conventional double gate TFET.

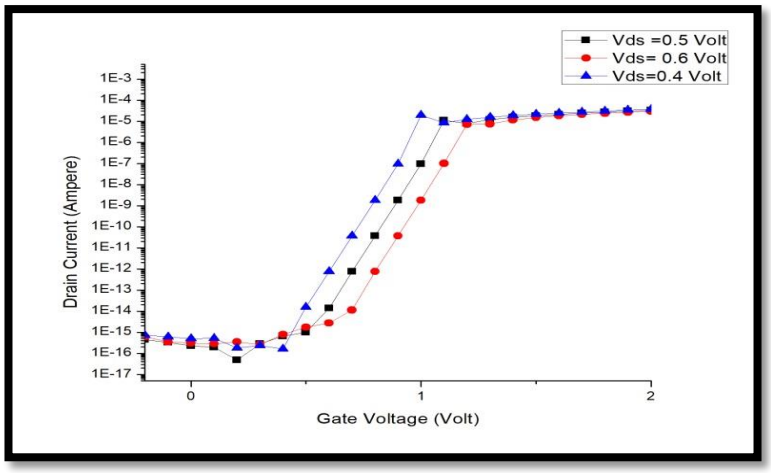
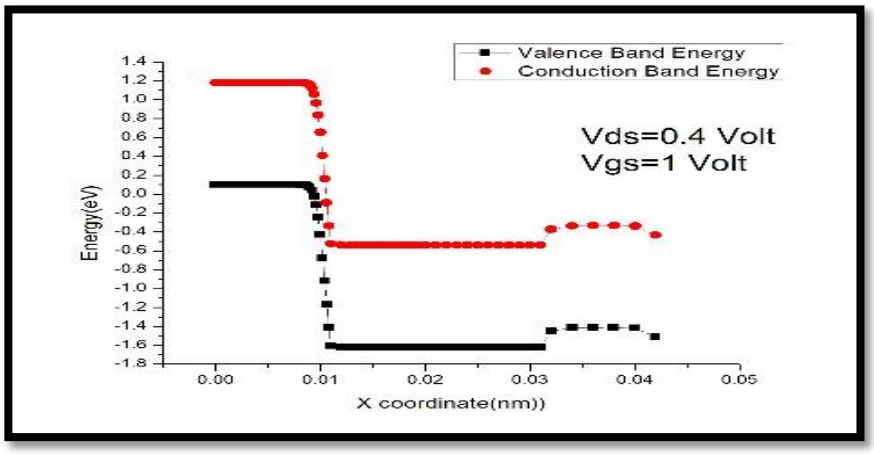


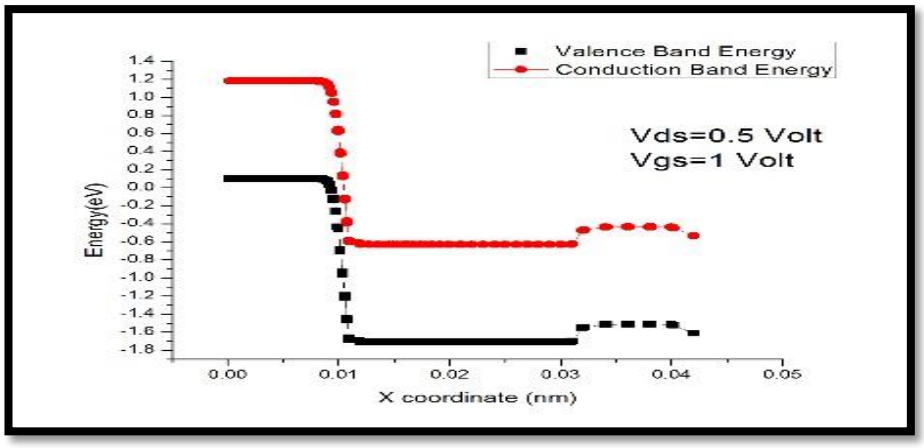
Fig. 4.4: I_{ds} –V_{gs} characteristic at V_{ds}=0.4V, 0.5V and 0.6V

(b) Band Diagram Analysis

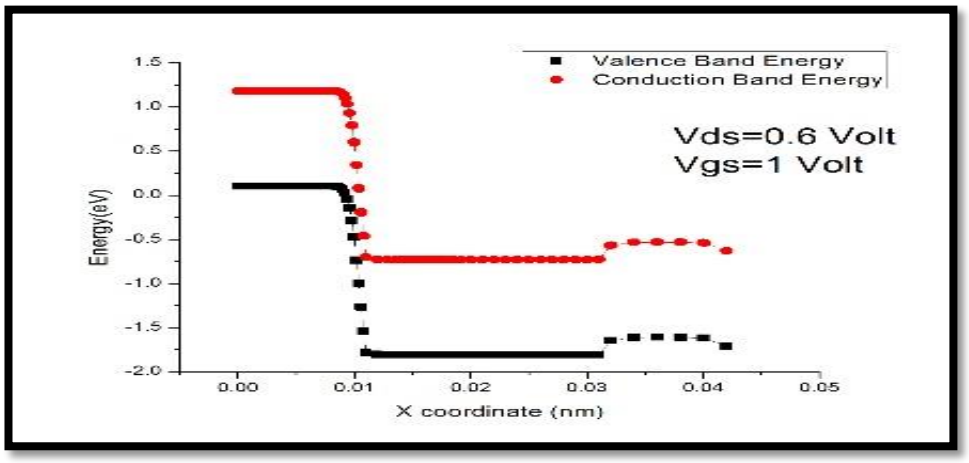
Fig. 4.5 depicts the band diagram of the SS-DG-TFET for three different V_{ds} conditions specifically (a)V_{ds}=0.4V, (b)V_{ds}=0.5V and (c)V_{ds}=0.6V. From Fig. 4.5 it is evident that the tunneling at the source side is almost similar in all the three cases considered here despite of drain to source voltage variation. As the tunnel width is very less so the tunneling effect is predominant at source side. This improved tunneling behavior is the consequence of the extension of source in vertical dimension that provides the piping effect from the source to channel with increased conductivity. For Fig. 4.5(c) V_{ds}=0.6V.As the voltage is more so tunneling probability is high but for Fig.4.5(a),where V_{ds}=0.4V, tunneling is not significantly less compared to Fig. 4.5(c). If we consider SS then also the characteristics of the device at V_{ds}=0.4V is quite appreciable.



(a)



(b)

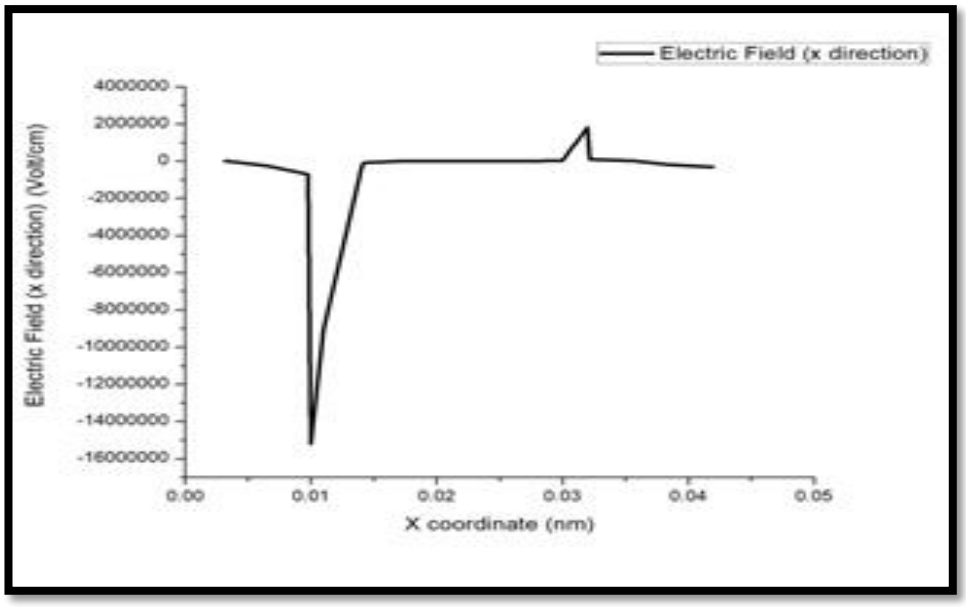


(c)

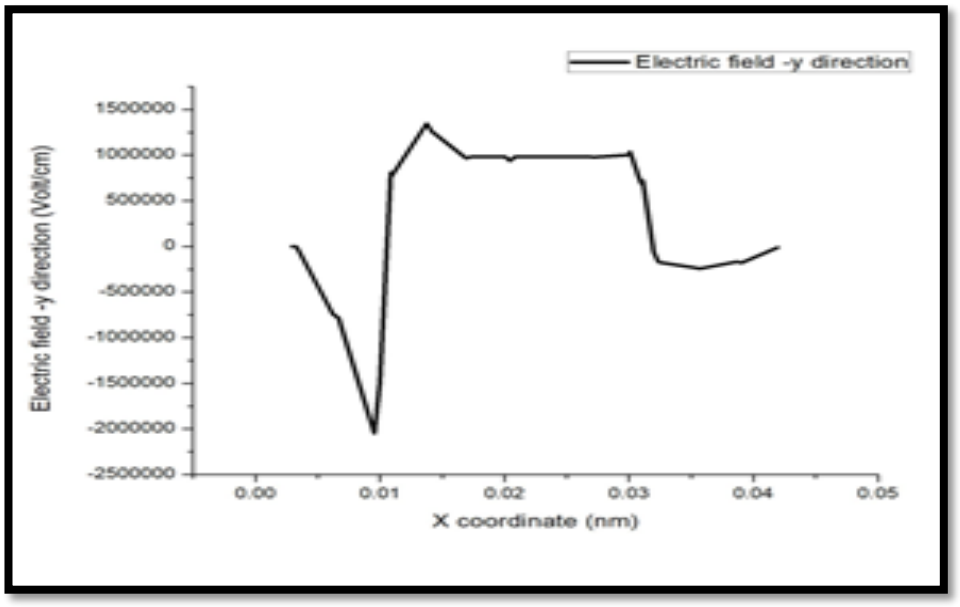
Fig. 4.5: Band diagram of SS- DG-TFET structure for (a)V_{ds}=0.4V, (b)V_{ds}=0.5V and (c)V_{ds}=0.6V.

(c) Electric Field Study

The electric field along the channel length is observed for three different drain to source bias conditions. We have studied that the electric field for V_{ds}= 0.4V, V_{ds}= 0.5V and V_{ds}= 0.6V are almost similar and close to the conventional TFET electric field. So it can be concluded that there is no degradation of electric field profile in lower voltages thus the model is suited for low power application. Fig. 6 shows the electric field along and X and Y direction. As the channel is n-type so the electric field in X direction has a peak in downward direction in source-channel intersection. And for same reason a much smaller peak in opposite direction is achieved in channel-drain intersection.



(a)



(b)

Fig. 4.6: Electric field along (a) X and (b) Y direction

(d) Surface Potential

In this section we will examine analytical modeling as well as simulation based outcome of the surface potential.

Analytical Modeling

The analytical surface potential model of the proposed structure is presented in this section. The 2D

Poisson's equation is solved for the channel region for calculating the surface potential that is to be verified with the simulation results.

From Fig.1 it is evident that the channel thickness is y ($0 \le y \le t_{si}$) and L denotes the channel length that varies along the X direction. The channel region is affected by both the front and back gate bias so the equation is applied to the channel region only. The Poisson equation at the 2D channel region is

$$\frac{\partial^2\phi(x,y)}{\partial x^2}+\frac{\partial^2\phi(x,y)}{\partial y^2}=\frac{qN_c}{\varepsilon_{si}} \qquad (1)$$

Where Φ(x,y) is electrostatic potential, q is electronic charge, N_c is the channel concentration and ε_{si} is defined as permittivity of silicon. Now potential profile is considered as Young's parabolic approximation:

$$\phi(x,y)=\phi_s(x)+c_1(x)y+c_2(x)y^2 \qquad (2)$$

Where $\phi_s(x)$ is surface potential, c_1 and c_2 are functions of x. The boundary conditions at the source channel and channel drain interface for the electrostatic potential; is defined as described in [27],

$$\left.\frac{d\phi(x,y)}{dy}\right|_{y=0}=\frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{\phi_s(x)-V_{GS1}}{t_f} \qquad (3)$$

$$\left.\frac{d\phi(x,y)}{dy}\right|_{y=t_{si}}=\frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{V'_{GS1}-\phi_B(x)}{t_B} \qquad (4)$$

Where $V_{GS1}=V_{GS}-V_{FB}$, Flat band voltage $V_{FB}=\phi_M-\phi_{Si}$, $\phi_{Si}=\chi+\frac{E_g}{2q}+\phi_B$ and $\phi_B=V_T\ln\frac{N_c}{n_i}$.

Differentiating (2) with respect to y we get ,

$$\frac{d\phi(x,y)}{dy}=c_1(x)+2c_2(x)y \qquad (5)$$

and applying the boundary condition (3) , the values of c1(x) is found to be

$$c_1(x)=\frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{\phi_s(s)-V_{GS1}}{t_f} \qquad (6).$$

Applying the boundary condition (4) and replacing the value of V'_{GS1} with V_{GS1} as are same for both gates and putting the value of $y=t_{si}$ in (2) the value of $c_2(x)$ is found to be

$$c_2(x)=\frac{\varepsilon_{ox}}{2t_{si}\varepsilon_{si}}\frac{2V_{GS1}-\phi_B(x)-\phi_s(s)}{t_f} \qquad (7)$$

and here in the proposed structure $t_B=t_f$.

Where the parameters of the equations are as follows:

χ =electron affinity

E_g = band gap energy

N_c = doping concentration at the channel region

ϕ_{Si} = silicon work function

ϕ_B = built-in potential

ϕ_M = metal work function

To solve $\phi_s(s)$, the values of $c_1(x)$ and $c_2(x)$ is put into (2) and as $\phi(x,y)|_{y=t_{si}} = \phi_B(x)$ therefore from (2) it is found that

$$\phi_B(x) = \phi_S(x) \qquad (8).$$

Now considering (8) and replacing the values of $c_1(x)$ and $c_2(x)$ from (6) and (7) into (2), the modified expression is found to be

$$\phi(x,y) = \phi_S(x) + \frac{\varepsilon_{ox}}{\varepsilon_{si}}\left(\frac{\phi_s(x) - V_{GS1}}{t_f}\right)y + \frac{\varepsilon_{ox}}{\varepsilon_{si}t_{si}}\left(\frac{V_{GS1} - \phi_s(x)}{t_f}\right)y^2 \qquad (9)$$

Differentiating (9) with respect to x and y and replacing in equation (1) the differential equation of the surface potential is found to be

$$\frac{\partial^2\phi_S(x)}{\partial x^2} - \phi_S(x)\,\mathrm{k}_1 = k_2 \qquad (10)$$

where $k_1 = \dfrac{2\varepsilon_{ox}}{t_{si}\varepsilon_{si}t_f}$ (11)

and $k_2 = -\dfrac{qN_c}{\varepsilon_{si}} - \dfrac{2\varepsilon_{ox}}{t_{si}\varepsilon_{si}t_f}V_{GS1}$ (12).

Solving the above mentioned second order differential equation the surface potential is found to be

$$\phi_s(x) = A\exp(\sqrt{k_1}y) + B\exp(-\sqrt{k_1}y) - \delta \qquad (11)$$

Where the expression of A , B and δ is as follows [28],

$$A = \frac{k_2\left(e^{\sqrt{k_1}L} - 1\right)}{k_1\left(e^{2\sqrt{k_1}L} - 1\right)} + \frac{\left[V_{bi}\left(e^{\sqrt{k_1}L} - 1\right) + V_{Ds}e^{\sqrt{k_1}L}\right]}{\left(e^{2\sqrt{k_1}L} - 1\right)} \qquad (13)$$

$$B = \frac{k_2e^{\sqrt{k_1}L}\left(e^{\sqrt{k_1}L} - 1\right)}{k_1\left(e^{2\sqrt{k_1}L} - 1\right)} + \frac{e^{\sqrt{k_1}L}\left[V_{bi}\left(e^{\sqrt{k_1}L} - 1\right) - V_{Ds}\right]}{\left(e^{2\sqrt{k_1}L} - 1\right)} \qquad (14)$$

$$\delta = \frac{k_2}{k_1} \qquad (15)$$

TABLE 4.2
VALUES OF DIFFERENT PARAMETERS

Different parameters	**Symbol**	**Values**
Channel doping concentraition	N_C	$10^{15}/cm^3$
Energy band gap	E_g	1.1 eV
Oxide permittivity	ε_{ox}	3.9
Silicon permittivity	ε_{si}	11.7
Electron Affinity	χ	1.39 ev
Channel Length	L	22 nm
Thermal Voltage	V_T	26 mV
Drain to source voltage	V_{DS}	0.4 Volt
Metal work function	$\emptyset_M$	4.15 Volt

The surface potential of the salient source TFET and analytical model has been plotted along the channel length .In Fig 4.7 it is depicted that both the curves are in close proximity with maximum potential of 1V at the channel region. This suggests that surface potential for proposed simulated model and its analytical output are analogous.

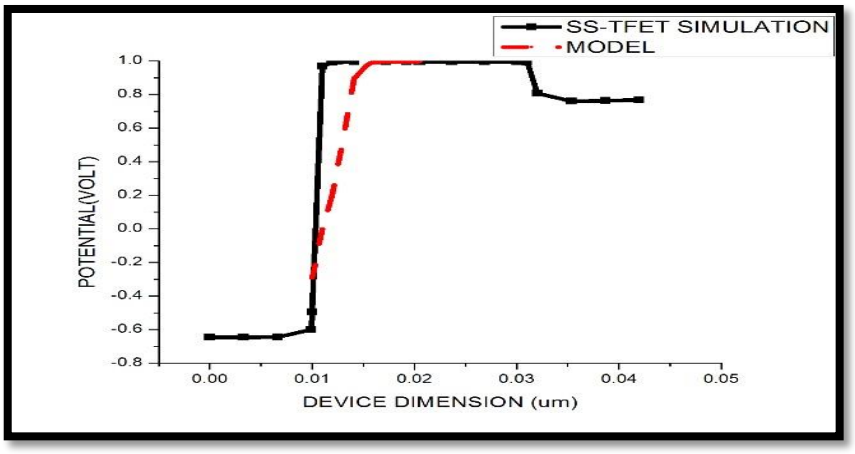


Fig. 4.7: Surface potential of SS-DG-TFET

Simulation Based Study :

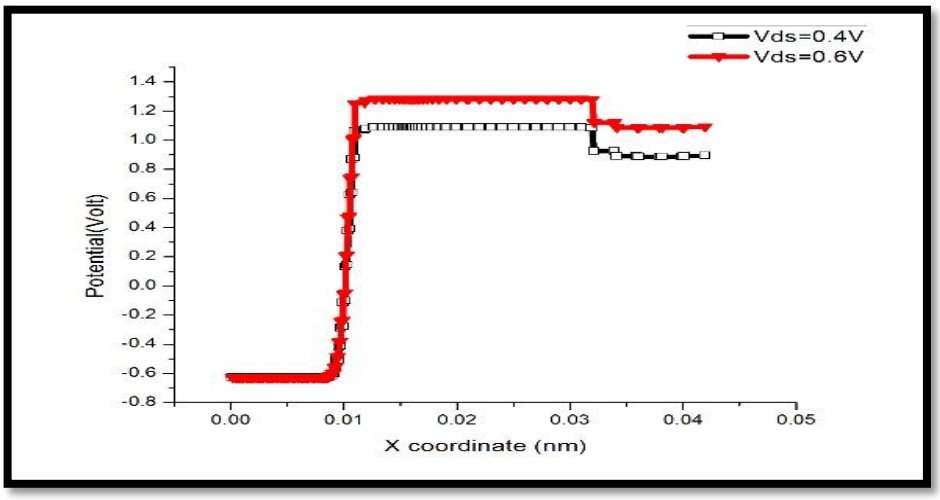


Fig. 4.8**:** Comparison of surface potential for V_{ds}=0.4V and V_{ds}=0.6V

It is evident from the Fig.4.8 that for greater voltage (V_{ds}=0.6V) the surface potential is intuitively more compared to V_{ds}= 0.4V. For both the cases V_{gs} is considered to be 1V. It can be easily determined that power consumption is more for 0.6V but if we consider the previous analysis, specifically SS, then it establishes the fact that the device is useful enough for low power applications[29-30].

(e) Comparison with already existing structure

Further we have also studied that our proposed structure is better in terms of ON current to OFF current ratio than the conventional double gate TFET. Our model has symmetrical extended source that gives a piping effect through channel .Hence more current is flown through channel of SS-DG-TFET compared to conventional double gate TFET [31-32]. A comparison graph is presented in Fig. 4.9.

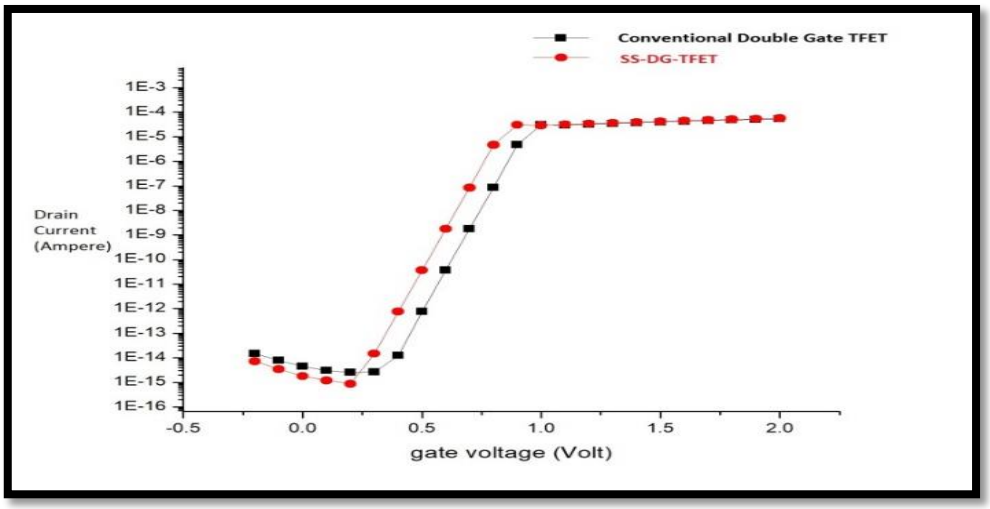


Fig.4.9: Comparison of gate-voltage drain-current characteristic of SS-DG-TFET and conventional double gate TFET at Vds=0.4 volt

References

[1] B. Razavi,Design of Analog CMOS Integrated Circuits.NewYork,NY, USA: McGraw-Hill, 1999.

[2] W. Y. Choi, B.-G. Park, J. D. Lee, and T.-J. K. Liu, "Tunneling field-effect transistors (TFETs) with subthreshold swing (SS) less than 60 mV/dec ,"IEEE Electron Device Lett., vol. 28, no. 8, pp. 743–745, Aug. 2007.

[3] N. Patel, A. Ramesha, and S. Mahapatra, "Drive current boosting of n-type tunnel FET with strained SiGe layer at source,"Microelectron. J., vol. 39, no. 12, pp. 1671–1677, Dec. 2008.

[4] W. Hansch, C. Fink, J. Schulze, and I. Eisele, "A vertical MOS-gated Esaki tunneling transistor in silicon,"Thin Solid Films, vol. 369, nos. 1–2, pp. 387–389, Jul. 2000.

[5] K. Boucart and A. M. Ionescu, "Double-gate tunnel FET with high-κ gate dielectric ," IEEE Trans. Electron Devices, vol. 54, no. 7, pp. 1725–1733, Jul. 2007.

[6] K. Boucart and A. M. Ionescu, "Threshold voltage in tunnel FETs: Physical definition, extraction, scaling and impact on IC design," inProc. IEEE 37th Eur. Solid State Device Res. Conf. (ESSDERC), Sep. 2007, pp. 299–302.

[7] K. Boucart and A. M. Ionescu, "Double gate tunnel FET with ultrathin silicon body and high-k gate dielectric," inProc. 36th Eur. Solid-State Device Res. Conf. (ESSDERC), Sep. 2006, pp. 383–386.

[8] A. M. Ionescu and H. Riel, "Tunnel field-effect transistors as energyefficient electronic switches,"Nature, vol. 479, no. 7373, pp. 329–337, Nov. 2011.

[9] C. Huet al., "Prospect of tunneling green transistor for 0.1 V CMOS," in Proc. IEEE Int. Electron Devices Meeting, Dec. 2010, pp. 16.1.1–16.1.4.

[10] L. Liu, D. Mohata, and S. Datta, "Scaling length theory of double-gate interband tunnel field-effect transistors," IEEE Trans. Electron Devices, vol. 59, no. 4, pp. 902–908, Apr. 2012.

[11] A. C. Seabaugh and Q. Zhang, "Low-voltage tunnel transistors for beyond CMOS logic," Proc. IEEE, vol. 98, no. 12, pp. 2095–2110, Dec. 2010.

[12] K. K. Bhuwalka, J. Schulze, and I. Eisele, "A simulation approach to optimize the electrical parameters of a vertical tunnel FET,"IEEE Trans. Electron Devices, vol. 52, no. 7, pp. 1541–1547, Jul. 2005.

[13] E.-H. Toh, G. H. Wang, L. Chan, G. Samudra, and Y.-C. Yeo, "Device physics and guiding principles for the design of double-gate tunneling field effect transistor with silicon-germanium source heterojunction, " Appl. Phys. Lett., vol. 91, no. 24, pp. 243505-1–243505-3, Dec. 2007.

[14] K. Boucart and A. M. Ionescu, “A new definition of threshold voltage in tunnel FETs,” Solid-State Electron., vol. 52, no. 9, pp. 1318–1323, Sep. 2008.

[15] A. S. Verhulst, W. G. Vandenberghe, K. Maex, and G. Groeseneken, “Boosting the on-current of a n-channel nanowire tunnel field-effect transistor by source material optimization,” J. Appl. Phys., vol. 104, no. 6, pp. 064514-1–064514-10, Sep. 2008.

[16] W. G. Vandenberghe, A. S. Verhulst, G. Groeseneken, B. Soree, and W. Magnus, “Analytical model for a tunnel field-effect transistor,” in Proc. 14th IEEE Medit. Electrotech. Conf. (MELECON), May 2008, pp. 923-928.

[17] J. Knoch, S. Mantl, Y.-M. Lin, Z. Chen, P. Avouris, and J. Appenzeller, “An extended model for carbon nanotube field-effect transistors,” in 62nd DRC, Conf. Dig. Device Res. Conf., vol. 1. Jun. 2004, pp. 135-136.

[18] M. G. Bardon, H. P. Neves, R. Puers, and C. Van Hoof, “Pseudotwo- dimensional model for double-gate tunnel FETs considering the junctions depletion regions,” IEEE Trans. Electron Devices, vol. 57, no. 4, pp. 827–834, Apr. 2010.

[19] P. M. Solomon, D. J. Frank, and S. O. Koswatta, “Compact model and performance estimation for tunneling nanowire FET,” in Proc. 69th Annu. Device Res. Conf. (DRC), Jun. 2011, pp. 197–198.

[20] N. Cuiet al., “A two-dimensional analytical model for tunnel field effect transistor and its applications, ” Jpn. J. Appl. Phys., vol. 52, no. 4R, pp. 044303-1–044303-6, 2013.

[21] N. Bagga and Subir Kumar Sarkar, "An Analytical Model for Tunnel Barrier Modulation in Triple Metal Double Gate TFET," in *IEEE Transactions on Electron Devices*, vol. 62, no. 7, pp. 2136-2142, July 2015.

[22] F. Villani, E. Gnani, A. Gnudi, S. Reggiani, and G. Baccarani, “A quasi 2D semianalytical model for the potential profile in hetero and homojunction tunnel FETs,” in Proc. 44th Eur. Solid State Device Res. Conf. (ESSDERC), Sep. 2014, pp. 262–265.

[23] B. Manna, S. Sarkhel, N. Islam, S. Sarkar and Subir Kumar Sarkar, "Spatial Composition Grading of Binary Metal Alloy Gate Electrode for Short-Channel SOI/SON MOSFET Application," in *IEEE Transactions on Electron Devices*, vol. 59, no. 12, pp. 3280-3287, Dec. 2012

[24] S. Deb, N. B. Singh, N. Islam and Subir Kumar Sarkar, "Work Function Engineering With Linearly Graded Binary Metal Alloy Gate Electrode for Short-Channel SOI MOSFET," in *IEEE Transactions on Nanotechnology*, vol. 11, no. 3, pp. 472-478, May 2012.

[25] C. Anghel, Hraziia, A. Gupta, A. Amara, and A. Vladimirescu, “30-nm tunnel FET with improved performance and reduced ambipolar current,” IEEE Trans. Electron Devices, vol. 58, no. 6, pp. 1649–1654, Jun. 2011.

[26] S. Naskar and Subir Kumar Sarkar, "Quantum Analytical Model for Inversion Charge and Threshold Voltage of Short-Channel Dual-Material Double-Gate SON MOSFET," in *IEEE Transactions on Electron Devices*, vol. 60, no. 9, pp. 2734-2740, Sept. 2013.

[27] Bagga, N., Dasgupta S.: "Surface Potential and Drain Current Analytical Model of Gate All Around Triple Metal TFET"*IEEE Transactions on Electron Devices*, 2017, **64**, (2), pp. 606–613.

[28] S. Roy, A. Chatterjee, D. K. Sinha, R. Pirogova and S. Baishya, "2-D Analytical Modeling of Surface Potential and Threshold Voltage for Vertical Super-Thin Body FET," *IEEE Transactions on Electron Devices*, vol. 64, no. 5, pp. 2106-2112, May 2017.

[29] Amit Jain and Subir Kumar Sarkar "Design and Reliability analysis of a 4 :1 Mux using Single Electron Tunnelling technology based Threshold Logic Gate", Journal of Electron Devices, Vol-15, Pp-1241-1248,2012.

[30] Saheli Sarkhel, Priyanka Saha and Subir Kumar Sarkar, "Exploring the Threshold Voltage Characteristics and Short Channel Behavior of Gate Engineered Front Gate Stack MOSFET with Graded Channel", Silicon, Springer, DOI 10.1007/s12633-018-9950-9, pp-1-8, August 2018

[31] Priyanka Saha and Subir Kumar Sarkar, "Threshold Voltage Modeling of Linearly Graded Binary Metal Alloy Gate Electrode with DP MOSFET", IETE Journal of Research, Taylor & Francis , DOI 10.1080/03772063.2018.1508374,2018

[32] Priyanka Saha, Pritha Banerjee and Subir Kumar Sarkar, "2D modeling based comprehensive analysis of short channel effects in DMG strained VSTB FET", Superlattices and Microstructures, Elsevier, doi.10.1016/j.spmi.2018.03.070, vol. 118, pp-16-28, March 2018

Chapter 5

Double Source TFET : A quantum confinement based approach

5.1. Introduction and Proposed Work

5.2. Device structures and optimized parameters

5.3. Description of the model

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(b) Schrodinger-Poisson model

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5.4.3 Variation of oxide thickness

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Chapter 5:
Double Source TFET : A quantum confinement based approach

5.1. Introduction and Proposed Work

Tunnel field effect transistors are being extensively studied due to their excellent sub threshold behavior and low power applications [1-5].At the same time scalability is the need of the hour in semiconductor industry. Quantum confinement needs to be taken care of in scaled devices having dimensions in the range of 15 to 20 nm. In this work, an attempt has been made to incorporate quantum confinement in DS-TFET (Double Source TFET) based on non-local tunneling model along with self-consistent Schrodinger-Poisson quantum model. Quantum confinement is considered in 1-D. As a result effective band gap and subsequent tunneling barrier width is increased [6]. Hence the results obtained through quantum approach are more practical than semi-classical ones. In this chapter we will gather basic knowledge regarding the models . Thereafter a comparative study is done between results of quantum model and non-local BTBT model. The change in transfer characteristics of the proposed TFET model is analyzed for different channel length and different source dimensions. Variation of oxide thickness is studied during the work. Results for different gate work function is also studied for proposed DS-TFET. The channel lengh is optimized based on transconductance. After that band diagram analysis is performed incorporating the self-consistent Schrodinger-Poisson quantum model.

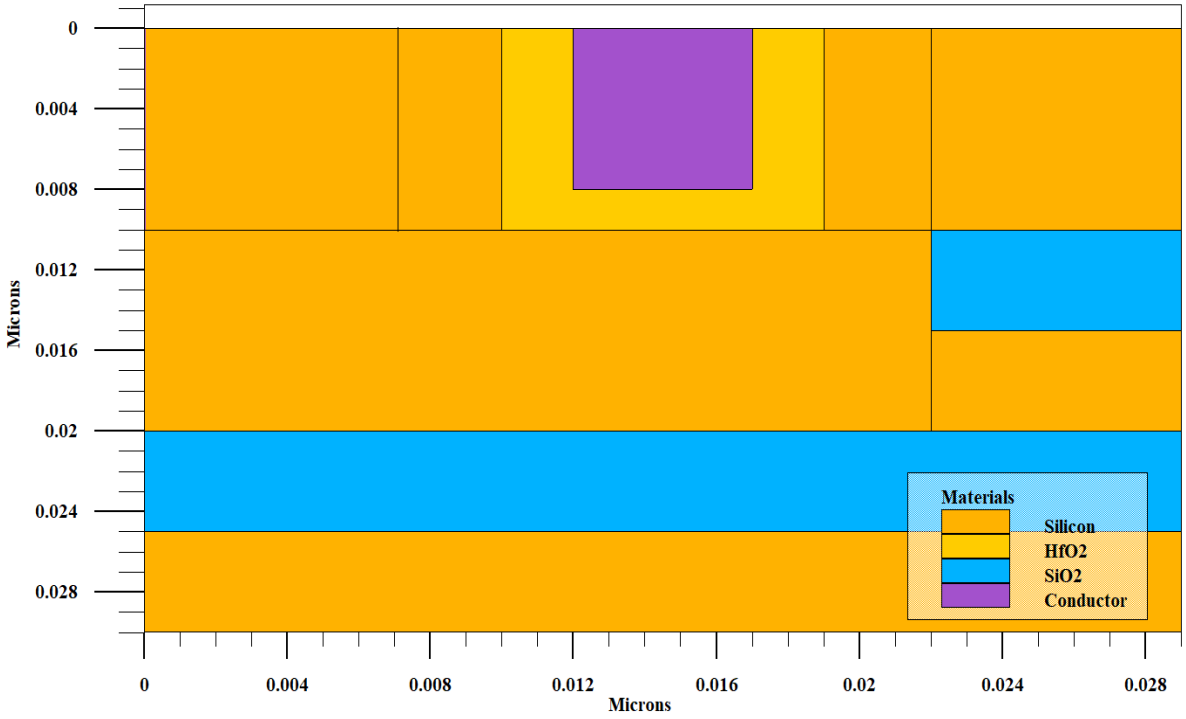
At last the potential and electric field profile is obtained for DS-TFET.

All simulation is performed in Silvaco,Atlas.

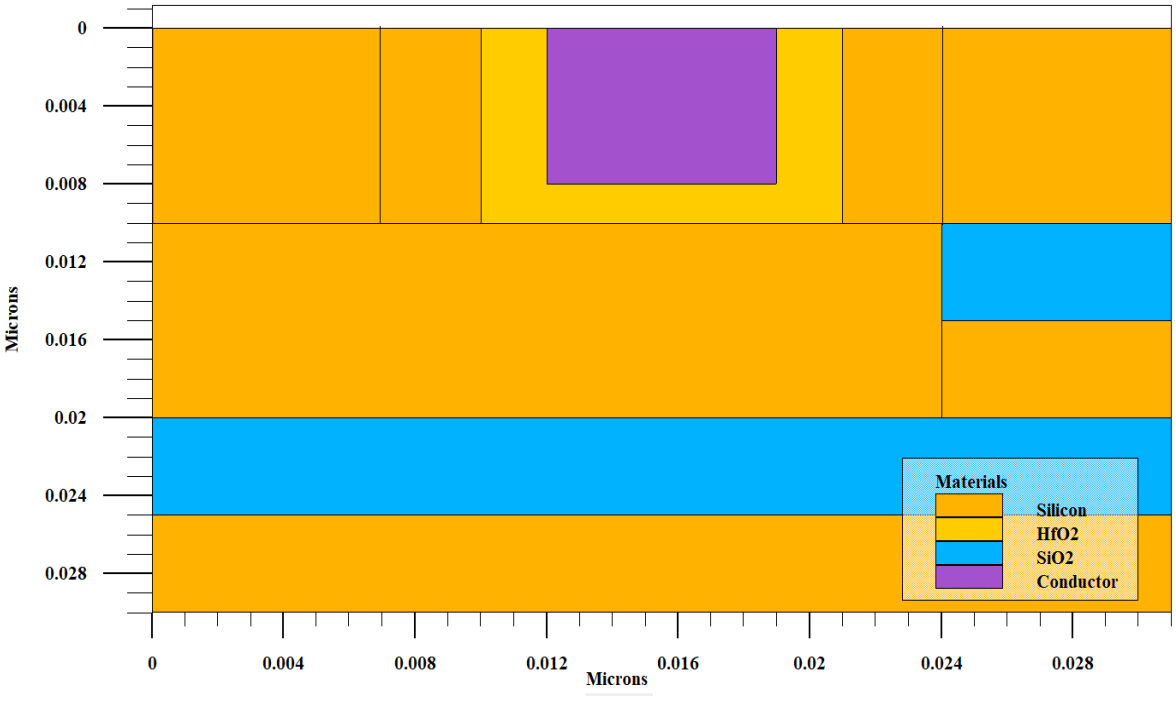
5.2. Device structure and optimized parameters:

The 2D cross sectional view of the proposed DS-TFET structure has been depicted in Fig. 5.1.this structure has two sources in extreme left top and right top. Adjacent to sources there exist two narrow channel regions just beside the gate oxide HfO_2 layer. They are named left channel and right channel respectively for the sake of our convenience. Below this layer there exists a n-type silicon layer that helps channel to transport carrier. A spacer SiO_2 region is present between right source and the drain region just below it. Effective channel length is varied by changing gate length. Gate length is varied from 5 nm to 7 nm, 9 nm, 13 nm and 20 nm .A BOX layer and p-type substrate is present at the bottom of the structure. Source electrodes are connected at top of the two sources and drain contact is made at

the right end of the drain region. Doping concentrations and dimensions of different regions of the device are provided in table 5.1 and 5.2.



(a)



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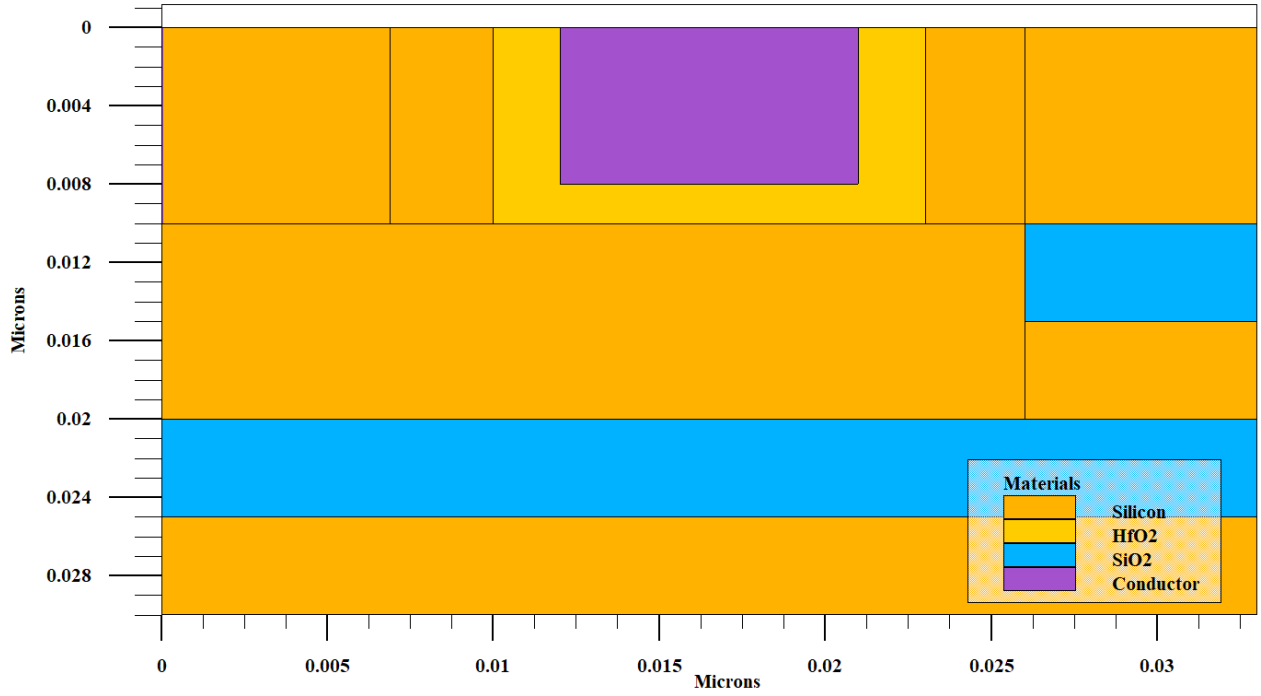
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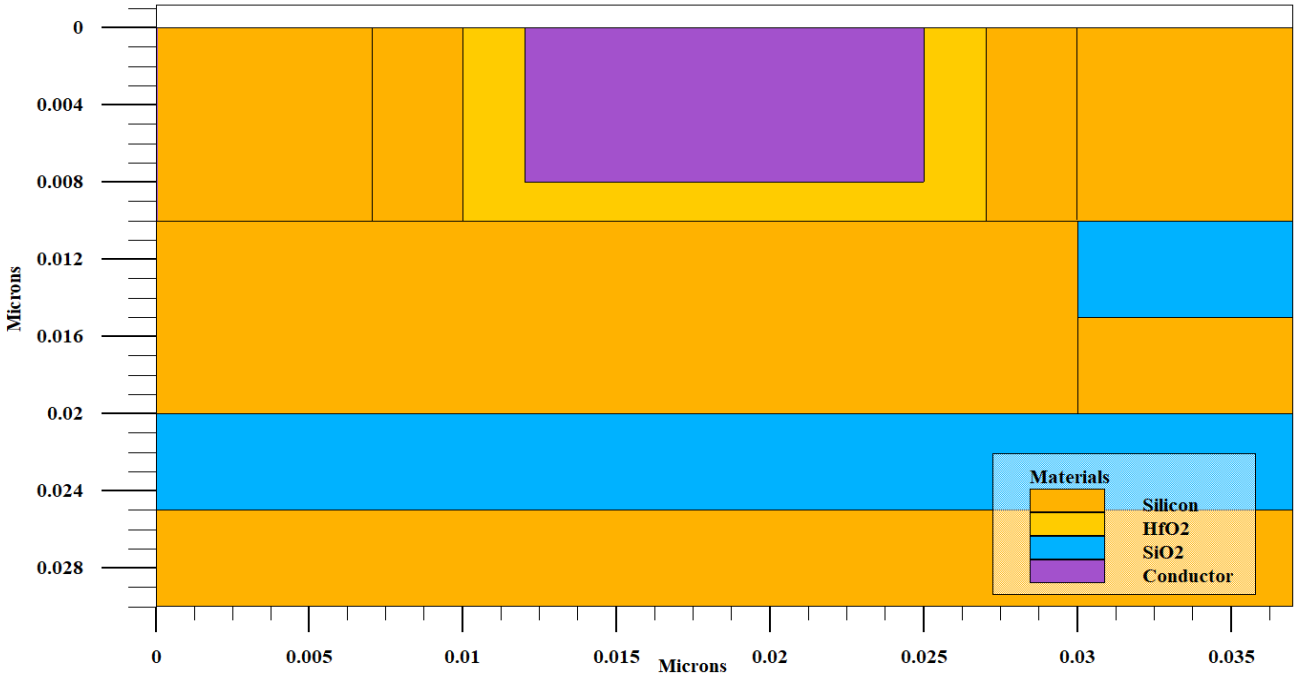
Conductor

(c)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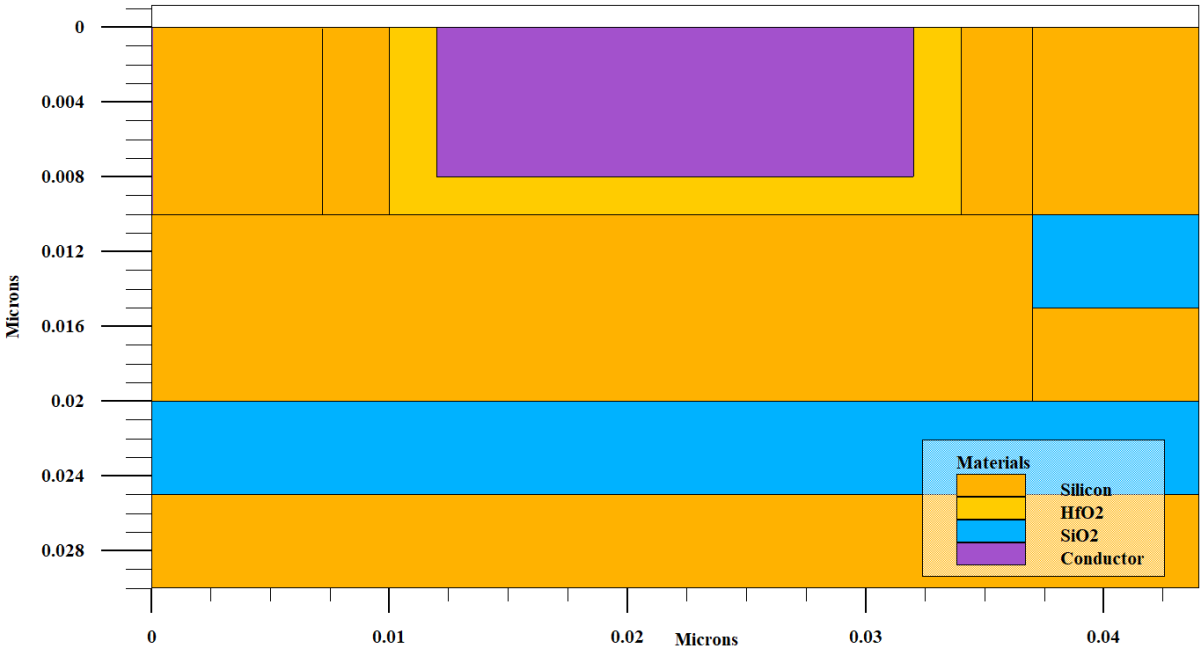

(e)

Figure 5.1. 2D cross sectional view of DS-TFET with effective channel length (a) 5nm (b) 7nm
(c) 9nm (d) 13 nm and (e) 20 nm

Table 5.1
Doping concentration of different regions

Region	**Doping type**	**Doping Concentration (/cm^3)**
Left Source	p-type	10^{21}
Right Source	p-type	10^{21}
Drain	n-type	5 X 10^{18}
Channel	n-type	10^{17}
Substrate	p-type	5 X 10^{16}

From Table 5.1 we have had a clear idea about the doping concentrations of different regions in the proposed DS-TFET. Source regions are highly doped whereas drain region is lightly doped with respect to source. Substrate region consists of p-type silicon.

Table 5.2.
Dimensions of different regions of DS-TFET

Different regions	Material	Dimensions
Left Source	Silicon	7 nm x 10 nm
Right Source	Silicon	7 nm x 10 nm
Drain	Silicon	7 nm x 5 nm
Spacer	SiO_2	7 nm x 5nm
Left channel	Silicon	3 nm x 10 nm
Right channel	Silicon	3 nm x 10 nm
Middle layer	Silicon	Width is varied according to varied channel length. Height is 10 nm
Gate	Aluminium	Variation is made in width as 5 nm,7 nm,9 nm,13 nm and 20 nm. Height is 8 nm.
Gate Oxide	HfO_2	Uniform thickness of 2 nm is maintained.
BOX	SiO_2	Height is 5 nm. Length is carried according to varied effective channel length.
Substrate	Silicon	Height is 5 nm. Length is carried according to varied effective channel length.

5.3. Description of the model

(a) Non local BTBT model

An attempt has been made to incorporate quantum mechanical quantization along with non-local BTBT model to analyze the performance of the device more practically. Electric field is hence non uniform. Transmission probabilities are given as [7] Wentzel–Kramer–Brillouin approximation :

$$T(E_{\|},y)= \exp[-2\int_{x_{start}}^{x_{end}} k(x,y)dx] \quad (5.1)$$

$E_{\|}$ is longitudinal energy level. x_{start} and x_{end} are the limits of definite integral. The simulator considers BTBT to take place in 1D and then derives 2-D BTBT by dividing tunneling width into multiple parallel slices in the direction of tunneling. k (x,y) is wave vector of carrier given by [8] :

$$k(x,y)= \frac{k_e k_h}{k_e^{\,2}+k_h^{\,2}} \quad (5.2)$$

where $k_e = \frac{1}{ih}\sqrt{2m_e^{\,*}(x,y)\{E-E_c(x,y)\}}$ (5.3)

and $k_h = \frac{1}{ih}\sqrt{2m_h^{\,*}(x,y)\{E_v(x,y)-E\}}$ (5.4)

E_c and E_v are nothing but conduction and valance band energy level. $m_e^{\,*}$ and $m_h^{\,*}$ are tunneling effective masses of electron and hole respectively.The current density in x direction then calculated as in [6] :

$$J_{BTBT}(y)= \frac{q}{\pi h}\iint T(E_{\|},y)[f_l(E_y+E_t)-fr(E_y+E_t)]\times\rho(E_T)dE_{\|}dE_T \quad (5.5)$$

Where 2D density of states is given by [10][12] :

$$\rho(E_T)= \frac{m_e^{\,T} m_h^{\,T}}{2\pi h^2} \quad (5.6)$$

(b) Schrodinger-Poisson model

This model is self-consistent because it self-consistently solves the Poisson's equation for potential and at the same time Schrodinger's equation for bound state energy of valence and conduction band both. From [10] we can find that quantum electron density depends on 1D Schrodinger's equation's solution which has to be solved for eigen state value E_{il} and wave function $\psi_{il}(x,y)$ at each slice formed and for each individual electron valley l .

$$-\frac{\hbar^2}{2}\frac{\partial}{\partial y}[\frac{1}{m_y^{\,l}(x,y)}\frac{\partial\psi_{il}}{\partial y}]+E_c(x,y)\psi_{il}=E_{il}\psi_{il} \quad (5.7)$$

Where $m_y^{\,l}(x,y)$ is spatially dependent effective mass of l^{th} valley in y direction.

This equation can be written down for holes also .The concentration of electrons (or holes) in 1D can be obtained after this using Fermi-Dirac statistics, wave functions and eigen values.

$$n(x,y)=\frac{2kT}{\pi\hbar^2}\sum_l m_x^{\,l}(x,y)m_y^{\,l}(x,y)\sum_{i=0}^{\infty}|\ \psi_{il}(x,y)\ |^2\times\ln[1+\exp(-\frac{E_{il}-E_F}{kT})]$$

After calculating electron concentration we can substitute Poisson's equation's charged part by it to derive the potential.

(c) Limitation of the model

As non-local BTBT and Schrodinger-Poisson model cannot be taken care of at the same time, the solution is obtained by the method mentioned in [7] and [10].

5.4. Results and Discussions

Several comparisons are done in this study. Those are provided in the following sections.

5.4.1 Comparison of transfer characteristics for different channel length

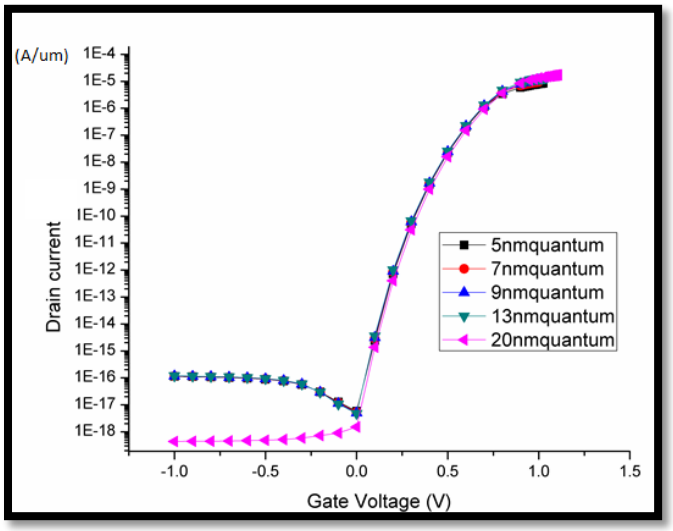

Figure 5.2. Transfer characteristics comparison for different effective channel length

From fig. 5.2. we can see that if channel length is brought below 20 nm ,current remains almost same once we incorporate quantum model . Only performance based on ambipolarity is degraded, that too is negligible. From this curve we can come to the conclusion that this device has excellent scalability.

5.4.2 Comparison of transconductance

Transconductance is one of the most important parameters in device physics. A comparison chart of transconductance with the variation of effective channel length is provided in table 5.3 and fig. 5.3.

Table 5.3.

Comparison of transconductance

Channel Length	**Transconductance**
5 nm	3.14 x 10^{-15} siemens
7nm	3.38 x 10^{-15} siemens
9nm	3.55 x 10^{-15} siemens
13 nm	3.79 x 10^{-15} siemens

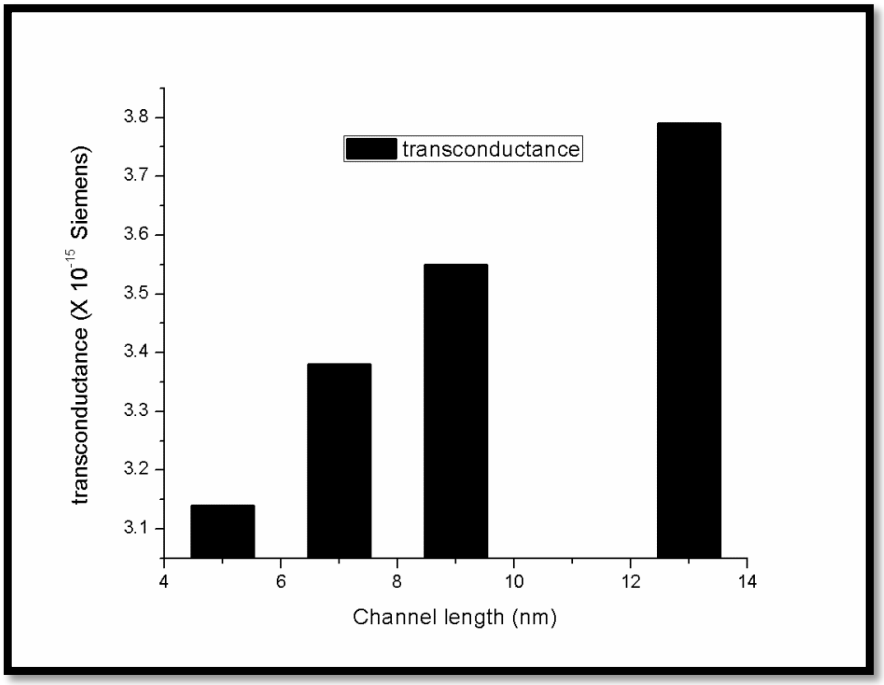

Figure 5.3. Comparison of transconductance

From fig. 5.3 and table 5.3. we can come to the conclusion that 13 nm channel length will perform better in terms of transconductance in the case of DS-TFET. The subthreshold slope is found to be 36 db/decade for 13nm channel length, which is satisfactory. So, we continued our study with DS-TFET shown in fig.5.1.(d) that has 13 nm gate length, and hence effective channel length is 13 nm.

5.4.3. Variation of oxide thickness

We analyzed the DS-TFET with 1nm,2 nm and 3 nm uniform gate oxide thickness**.** The outcomes are depicted in figure 5.4 and 5.5.

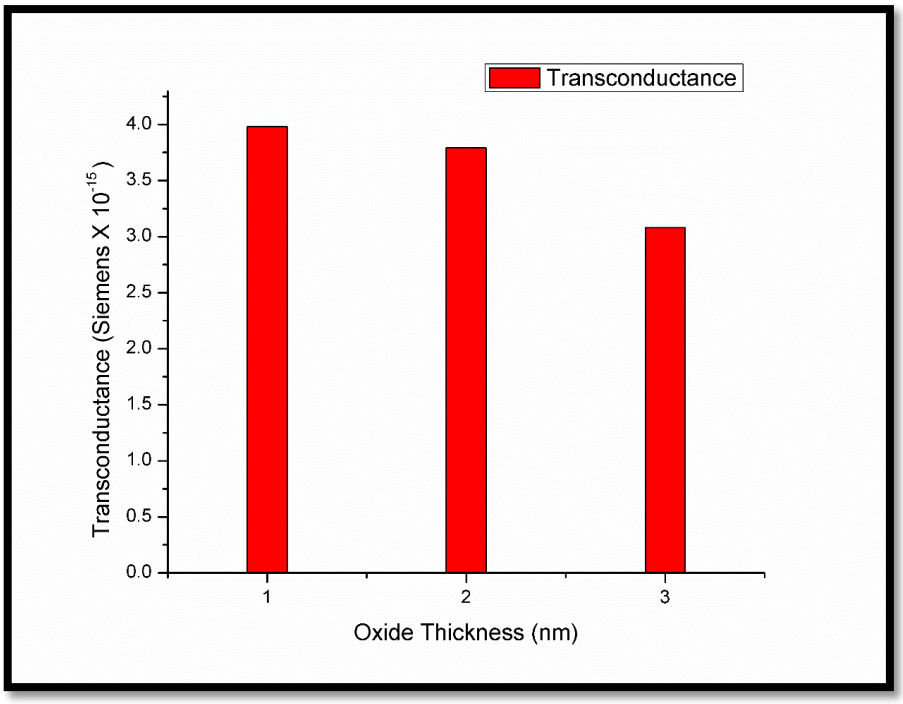

Figure 5.4. Comparison of transconductance for different oxide thickness

From fig. 5.4. and 5.5. we can make out that DS-TFET with 1 nm uniform gate oxide thickness performs better in terms of transconductance and output characteristics. But there is a possibility of leakage when oxide is too thin . That is the reason why we opted for 2 nm gate oxide thickness for further investigation of device performances.

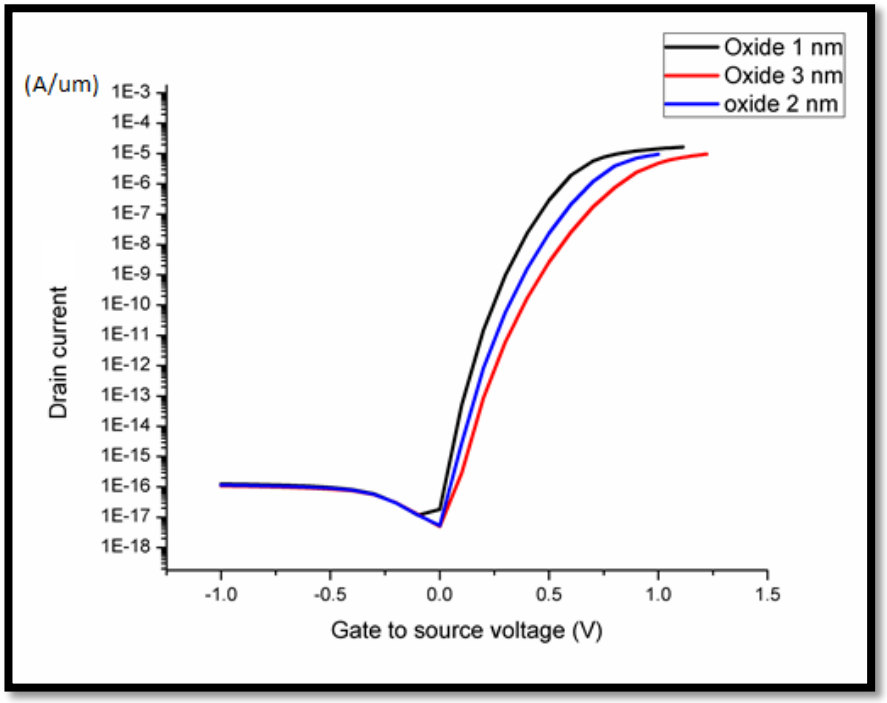

Figure 5.5. Comparison of transfer characteristics for different gate oxide thickness

5.4.4. Variation of gate work function

The effect of gate work function variation in DS-TFET is depicted in fig.5.6.

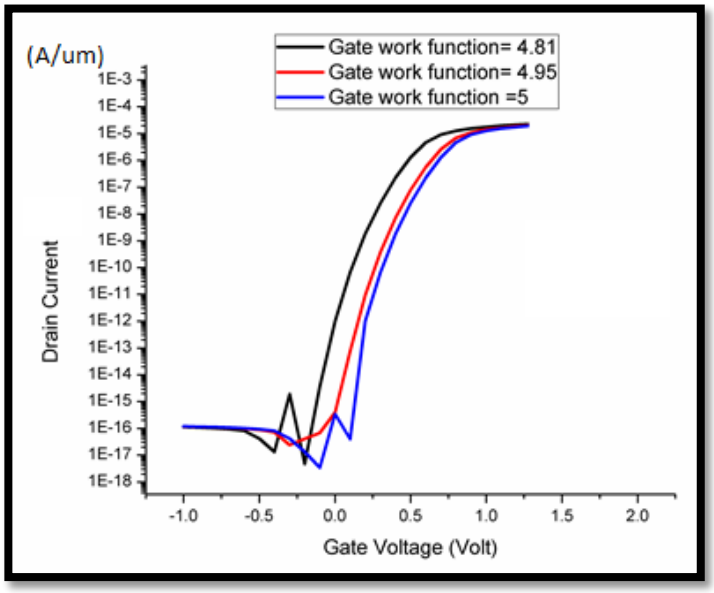

Figure 5.6. Gate work function variation in DS-TFET

Like conventional TFET, here also decreasing gate work function leads to increased source-channel tunneling and decreased drain channel tunneling [11]. This phenomenon raises the right hand curve and lowers the left-hand curve along Y axis. , thereby shifts the central point more leftwards.

5.4.5. Difference with Semi-classical model

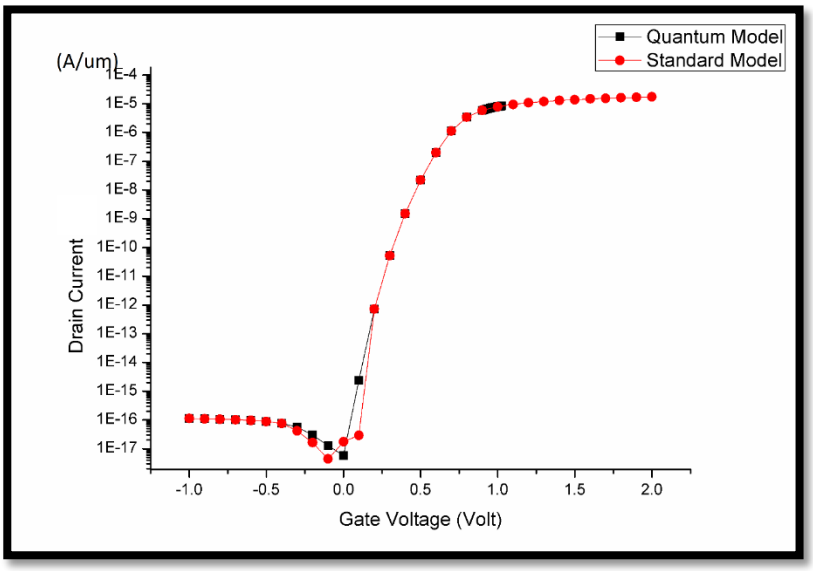

Figure 5.7. Comparison of quantum model with standard semi-classical model

From fig. 5.7. it is clearly understood that in quantum model the slope is little bit more than the standard one. This result is quite natural because we are moving towards practical

implementation of device. Output characteristics will differ naturally from the ideal case because now we are considering sub band quantization and this deviation is acceptable.

Table 5.4. Comparison of SS

Model	Sub threshold slope
Semi-Classical	23 db/decade
Quantum	36 db/decade

5.4.6. Effect of drain voltage on output characteristics

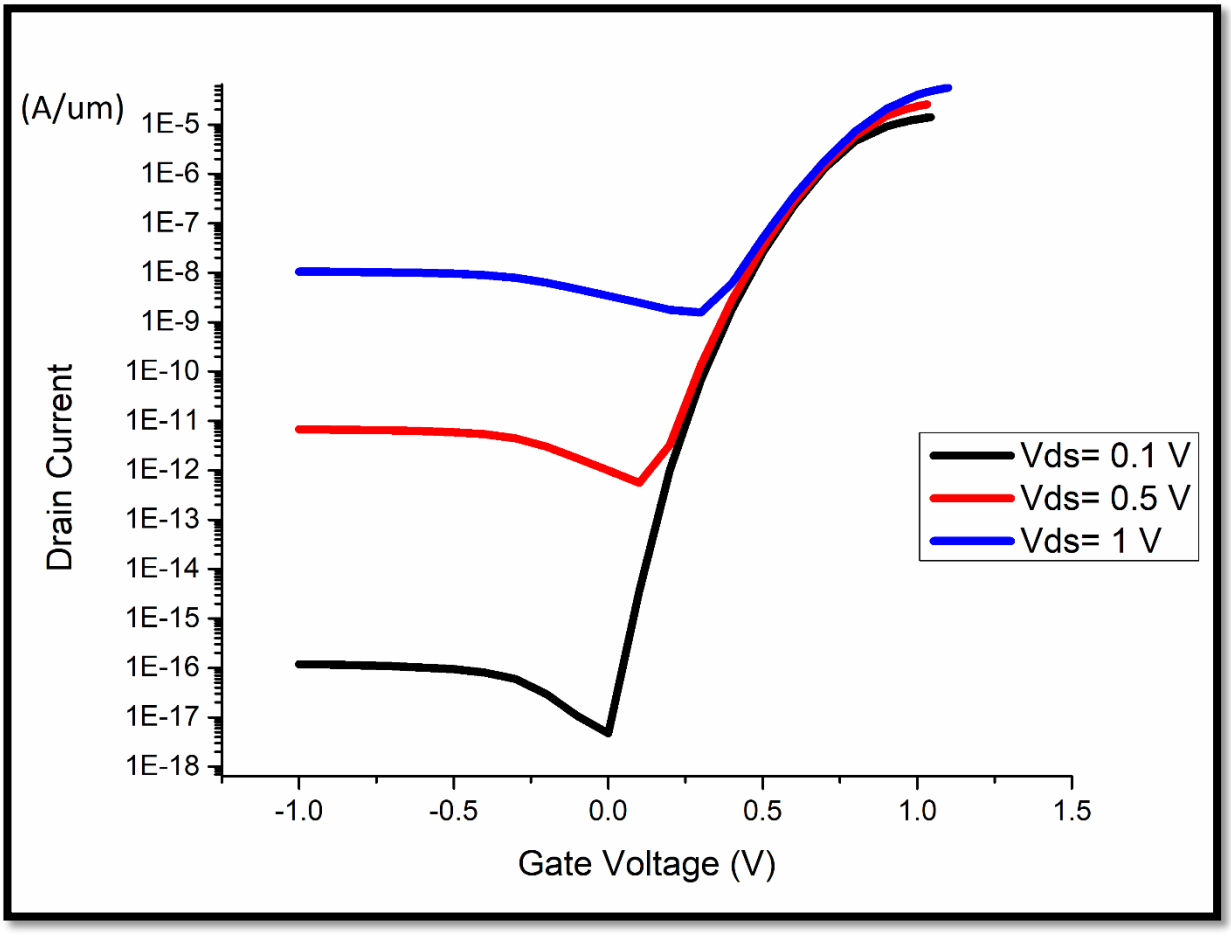

Figure 5.8. Effect on output characteristics for Drain voltage variation

This result is quite similar to that of [12]. From this curve it is clear that DS-TFET is suitable for low power application as for high drain voltage the SS and Current performance degrades. So, lower the drain to source voltage, better the device performance.

5.4.7. Source length variation

From fig. 5.9 and 5.10 it is clear that DS-TFET works most efficiently when lengths of both [13-16] sources are 10 nm each. The output characteristics are investigated by making each source 5 nm,7 nm and 10 nm by keeping the length of other source constant at 10 nm. Below 10 nm, further scaling starts to degrade the performance of DS-TFET. So length of both sources are optimized at 10 nm.

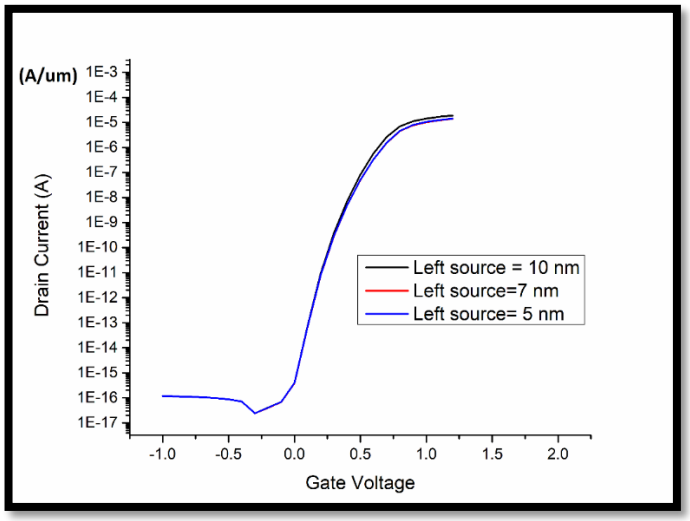

Figure 5.9. Effect on output characteristics for left source length variation

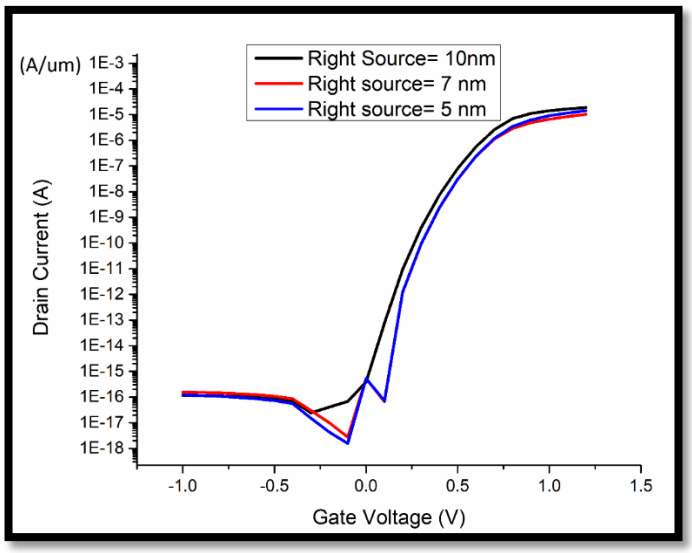

Figure 5.10. Effect on output characteristics for right source length variation

5.4.8. Band diagram analysis

As we have considered quantization of both valence and conduction band , the valence and conduction bands has to be considered as a discrete energy level spectrum that makes the tunneling possible between first bound states for holes and electrons only. This effective increment in the band gap[17-20] drastically reduces BTBT probability. This is depicted in fig. 5.11.

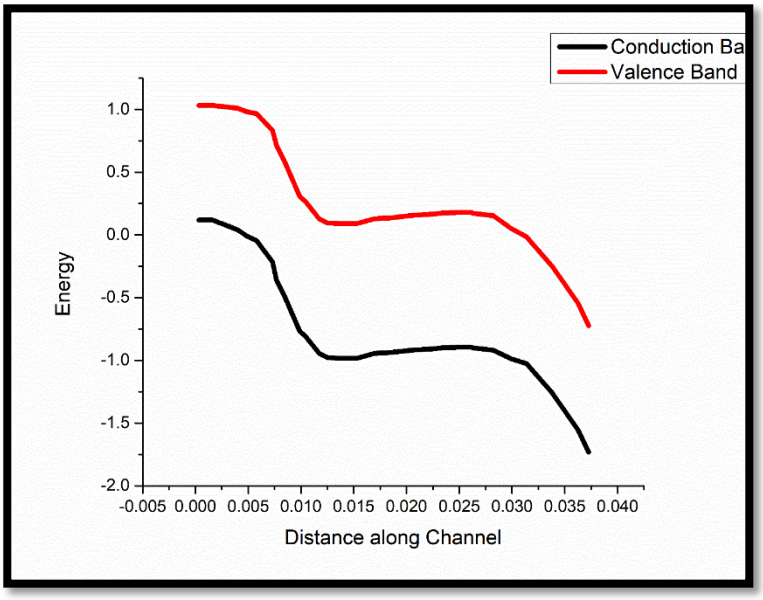

Figure 5.11. Band diagram for Vds = 0.1 volt

5.4.9. Electric Field and Potential

Electric Field and potential curve of DS-TFET is shown in fig. 5.12. and fig. 5.13. respectively. The deviation of these curves from conventional TFET is primarily due to the [21-22] presence of the right source. Also as the cutline is taken through a pseudo-surface, the ,curves are not depicting the most accurate behavior.

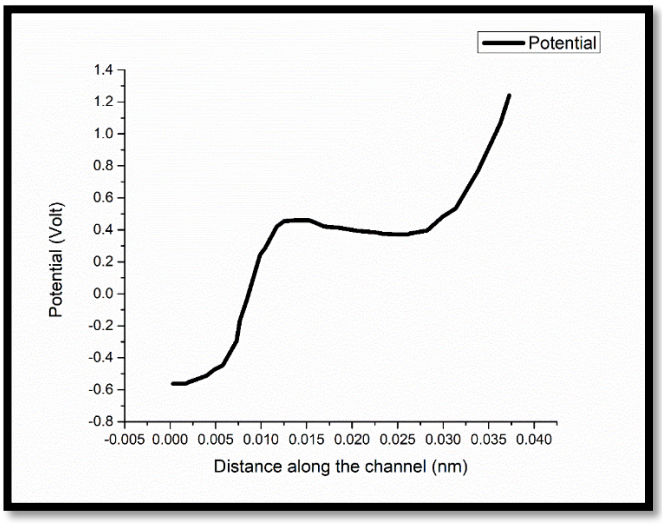

Figure 5.12. Potential curve of DS-TFET

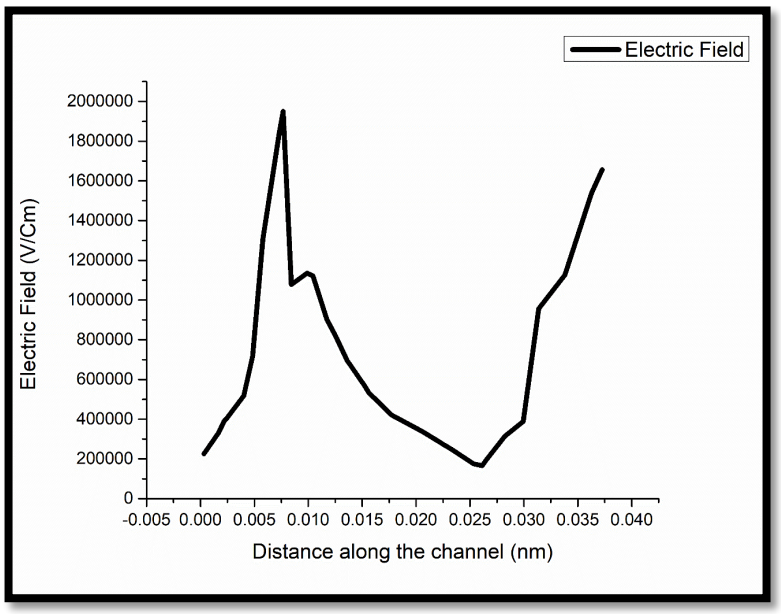

Figure 5.13.Electric Field of DS-TFET

In Fig.5.13. we can see there is a peak in left source and channel junction and again a peak is observed in the right source and channel junction too. This dual source structure exhibits interesting results.These two peaks generate a considerable current through the device. Hence DS-TFET is a highly efficient nano structure that operates satisfactorily in low power operating conditions. Fig. 5.12. can also be understood easily after analyzing electric field profile as we all know potential and electric fields are inter related .

References

[1] W. Y. Choi, B.-G. Park, J. D. Lee, and T.-J. K. Liu, "Tunneling field-effect transistors (TFETs) with subthreshold swing (SS) less than 60 mV/dec," IEEE Electron Device Lett., vol. 28, no. 8, pp. 743–745, Aug. 2007. doi: 10.1109/LED.2007.901273.

[2] P.-Y. Wang and B.-Y. Tsui, "Band engineering to improve average subthreshold swing by suppressing low electric field band-to-band tunneling with epitaxial tunnel layer tunnel FET structure," IEEE Trans. Nanotechnology., vol. 15, no. 1, pp. 74–79, Jan. 2016. doi: 10.1109/ TNANO.2015.2501829.

[3] S. W. Kim, W. Y. Choi, H. Kim, M.-C. Sun, H. W. Kim, and B.-G. Park, "Investigation on hump effects of L-shaped tunneling filed-effect transistors," in Proc. IEEE Silicon Nanoelectron. Workshop (SNW), Honolulu, HI, USA, Jun. 2012, pp. 1–2. doi: 10.1109/ SNW.2012.6243306.

[4] A. Mishra, M. Pattanaik, and V. Sharma, “Double gate vertical tunnel FET for hybrid CMOS-TFET based low standby power logic circuits,” in Proc. Annu. Int. Conf. Emerg. Res. Areas, Int. Conf. Microelectron., Commun. Renew. Energy, Kanjirapally, India, Jun. 2013, pp. 1–4. doi: 10.1109/AICERA-ICMiCR.2013.6575992.

[5] P. Wang, K. Hilsenbeck, T. Nirschl, M. Oswald, C. Stepper, M. Weiss, D. Schmitt-Landsiedel, and W. Hansch, “Complementary tunneling transistor for low-power applications,” Solid State Electron., vol. 48, no. 12, pp. 2281–2286, Dec. 2004

[6] J. L. Padilla, F. Gámiz, Senior Member, IEEE, and A. Godoy “A Simple Approach to Quantum Confinement in Tunneling Field-Effect Transistors” , IEEE ELECTRON DEVICE LETTERS, VOL. 33, NO. 10, OCTOBER2012

[7]] S. Sze, Physics of Semiconductor Devices. Hoboken, NJ: Wiley, 2007.

[8] José L. Padilla, Francisco Gámiz, “Impact of Quantum Confinement on Gate Threshold Voltage and Subthreshold Swings in Double-Gate Tunnel FETs”, IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 59, NO. 12, DECEMBER 2012

[9] S.Agarwal and E.Yablonovitch,“Using dimensionality to achieve a sharp tunneling FET (TFET) turn-on,” in Proc. 69th Annu. DRC, Jun. 20–22, 2011, pp. 199–200.

[10] Silvaco, Santa Clara, CA, ATLAS Users Manual, 2012.

[11] Jagadesh Kumar Mamidala ,Rajat, Pratyush Pandey
“Tunnel Field-Effect Transistors (TFET) Modelling and Simulation”

[12] Jang Hyun Kim,Sangwan Kim,Byung-Gook Park,” Double-Gate TFET With Vertical Channel Sandwiched by Lightly Doped Si” IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 66, NO. 4, APRIL 2019

[13] Pritha Banerjee ,Priyanka Saha and Subir Kumar Sarkar, "Analytical Modelling and Performance Analysis of Gate Engineered Tri-gate SON MOSFET", IET Circuits, Devices & Systems, DOI: 10.1049/iet-cds.2017.0473, March 2018

[14]Pritha Banerjee and Subir Kumar Sarkar, "Comprehensive analysis of subthreshold short channel behavior of a Dual-material gate strained Trapezoidal FinFET", Superlattices and Microstructures, Elsevier, doi.org/10.1016/j.spmi.2018.02.034, February 2018

[15] Priyanka Saha, Pritha Banerjee, Dinesh Kumar Dash and Subir Kumar Sarkar, "Exploring the short channel characteristics of Asymmetric Junctionless Double Gate Silicon On Nothing MOSFET", Journal of Materials Engineering and Performance, Springer, DOI: 10.1007/s11665-018-3281-2, March 2018.

[16] Aman Mahajan ,Dinesh Kumar Dash, Pritha Banerjee and Subir Kumar Sarkar ,“Analytical Modeling of Triple Metal Hetero Dielectric DG SON TFET”, Journal of Materials Engineering and Performance, Springer, vol:27, Issue 3, February 2018.

[17]Tripty Kumari, Priyanka Saha, Dinesh Kumar Dash and Subir Kumar Sarkar, " Modeling of Dual Gate Material Hetero-dielectric Strained PNPN TFET for Improved ON Current", Journal of Materials Engineering and Performance, Springer, vol:27, Issue 3, January 2018.

[18] Pritha Banerjee, Tripty Kumari and Subir Kumar Sarkar, "2-D modeling and analysis of short-channel behavior of a front high-K gate stack triple-material gate SB SON MOSFET",Applied Physics A, Springer, https://doi.org/10.1007/s00339-018-1567-8, January, 2018

[19] Pritha Banerjee and Subir Kumar Sarkar, “3D Analytical Modeling of Dual Material Triple Gate Silicon-on Nothing MOSFET”, IEEE Transactions on Electron Devices, Vol.64, Issue 2, pp-368-375, February 2017

[20] Dinesh Kumar Dash, Priyanka Saha and Subir Kumar Sarkar, "Analytical modeling of asymmetric hetero-dielectric engineered dual-material DG-TFET", in Journal of Computational Electronics, Springer, DOI 10.1007/s10825-017-1102-8 , November 2017

[21] Priyanka Saha, Tripty Kumari & Subir Kumar Sarkar, "Analytical Modelling and Performance Analysis of Dielectric Pocket-Induced Double-Gate Tunnel Field-Effect Transistor", IETE Technical Review, Taylor & Francis , DOI: 10.1080/02564602.2017.1381049, December 2017

[22] Pritha Banerjee, Priyanka Saha and Subir Kumar Sarkar,"Two dimensional analytical modeling of a high-K gate stack triple-material double gate strained silicon-on-nothing MOSFET with a vertical Gaussian doping", in Journal of Computational Electronics, Springer, DOI 10.1007/s10825-017-1089-1, November 2017

Chapter 6:
Concluding Remarks and Future Scope

6.1. Conclusion

6.2. Scopes for Future Work

6.1 Conclusion

In this work, several TFET structures are analyzed. The prominent emphasis has been given on various aspects of source engineering. Some striking features of TFET are noticed during this research work. Especially the low power friendliness of DS-TFET and salient source double gate TFET is a promising phenomenon. Scalability performance of DS-TFET is also showing interesting and superlative results. On the other hand, experimentally splitted source TFET structures are taking care of ambipolar current reduction. As we all know, ambipolar current is one of the major drawbacks of TFET technology along with low on current. Moreover all three structures discussed in chapter 3,4 and 5 encounter much lower sub-threshold slope and much higher current ON/OFF ratio than conventional TFET s. Hence these TFETs are the promising candidates to conquer future age of advanced electronics.

Chapter 3: This study recommends the influence of the drain and source engineering incorporated into drain engineered TFET structure. The doping concentration of upper drain region is higher than the lower drain region. The source regions are double spilt and single split in two models with different doping concentration. From table 3.1. a conclusion can be drawn that proposed models show better I_{on}/I_{off} ratio compared to drain engineered TFET due to higher ON current and prominently lower OFF current. Among all the structures investigated here in this work, the double split source structure shows the best performance in terms of ON current and ambipolar conduction.As evident from fig. 3.7., The device can be used for further advancements in low power, RF and analog applications.

Chapter 4: The proposed structure of this study, SS-DG-TFET displays good performance in low power operating conditions as reflected in fig. 4.4. The performance has been characterized in terms of lower SS, increased ON to OFF current ratio, along with improved tunneling at the source end of the channel. Fig. 4.7 indicates that proposed model exhibits analogous result with the analytical model in terms of surface potential. The performance parameters are compared for three different V_{ds} conditions and a rigorous examination determines that the device operates well enough in low power. Table 4.1 establishes the claim firmly. It is evident from the Fig.4.8 that for greater voltage (V_{ds}=0.6V) the surface potential is intuitively more compared to V_{ds}= 0.4V. For both the cases V_{gs} is considered to be 1V. It can be easily determined that power consumption is more for 0.6V but if we consider the previous analysis, specifically SS, then it establishes the fact that the device is useful enough for low power applications Moreover from fig. 4.9. we can understand the proposed device is better than conventional Double Gate TFET.

Chapter 5: This study aimed to incorporate quantum mechanical effects in the behavior of DS-TFET. This device is acceptable for low power applications. For high power application, the device structure should be adjusted accordingly based on the power requirement. Quantum models other than Schrodinger-Poisson are yet to be included in this study. Fig. 5.2 reveals that DS-TFET has ON/OFF ratio in the range of 10^{10} which is better than conventional TFET . From table 5.4. it is found that DS-TFET's SS is also much better than conventional one. Apart from channel length gate oxide thickness, gate work function, drain voltage and source length are also varied to find the optimum operating conditions of the device proposed in this study. Fig. 5.11, fig. 5.12 and fig 5.13 reveal the electrostatic behavior of previously optimized DS-TFET in terms of energy band,electric field and potential . In conclusion, we can say that DS-TFET is one of the most promising candidates to rule the market of low power electronics in future.

6.2. Scopes for Future Work

There are some issues which could be considered to enhance the accuracy of the present model. Some scopes for future extension of the present work are as follows:

I. Quantum mechanical effect is not considered in splitted source TFET and salient source double gate TFET structures. So, it should be included in future model for better functionality.

II. Ambipolar conduction increases in DS-TFET when dimensions are scaled down .This phenomenon needs to be taken care of.

III. The OFF current should be lowered further in TFET structures to achieve better ON/OFF current ratio,

IV. Research works should be conducted to bring down the threshold voltage of TFET further. So that it can work in lower voltages, and hence become more suitable for low power applications.

Research publications of Ayan Bhattacharya relevant to the current thesis

Journals :

1. Disha Bhattacharjee,Bijoy Goswami,Dinesh Kumar Dash,**Ayan Bhattacharya**,Subir Kumar Sarkar "**Analytical Modelling and Simulation of Drain Doping Engineered Splitted Drain Structured TFET and its Improved Performance in Subduing Ambipolar Effect** ", IET Circuit ,Device and System (Accepted)

2. Bijoy Goswami, Debadipta Basak, **Ayan Bhattacharya**, Sutanni Bhowmick, Koelgeet Kaur and Subir Kumar Sarkar, "**Analytical Modelling and the Impact of Quantum Confinement Effect on Subthreshold Swing of Salient Source DG-TFET**",IOP,May,2019

3. Subhashis Roy, Bikram Biswas, Anup Dey, **Ayan Bhattacharya**, Sudhabindu Ray, Subir Kumar Sarkar, **" Comparison of Annealing Temperature and Heterostructure Effects on ZnO based Thin Film H2 Sensor**",Sensor Letters (Accepted)

Conferences

1. Bijoy Goswami, Sutanni Bhowmick ,Debadipta Basak, **Ayan Bhattacharya**, Arindam Halder, Sutanni Bhowmick, Subir Kumar Sarkar **"2-D Analysis of a Centrally Aligned PNPN-DG TFET to Preclude Ambipolar Conduction" ,** ECTI CON 2019,Thailand . (Abroad)

2. Bijoy Goswami, Disha Bhattacharjee, Dinesh Kumar Dash, **Ayan Bhattacharya**, Subir Kumar Sarkar "**Demonstration of T-shaped channel Tunnel Field-Effect Transistors**" 2nd International Conference on Electronics, Materials Engineering and Nano-Technology (IEMENTech 2018) , 4-5th May 2018, IEM Gurukul Campus, Kolkata, West Bengal, IEEE.

3. Bijoy Goswami, Disha Bhattacharjee, Dinesh Kumar Dash, **Ayan Bhattacharya**, Subir Kumar Sarkar "**Drain Doping Engineering and its influence on Device Output Characteristics and Ambipolar**

Conduction on a Splitted-Drain TFET model" International Conference in Communication, Devices and Networking (ICCDN 2018) Sikkim Manipal Institute of Technology, Sikkim, 2-3rd June 2018,Springer

4. Disha Bhattacharjee, Bijoy Goswami, Dinesh Kumar Dash, **Ayan Bhattacharya**, Subir Kumar Sarkar "**Influence of Drain Doping Engineering in Triple Splitted-Drain TFET model**"International Conference on Recent innovations in Electrical, Electronics & Communication Engineering - ICRIEECE". July 27th and 28th 2018 School of Electrical Engineering, Kalenga institute of Industrial Technology (KIIT), Bhubaneswar, India, IEEE
5. **Ayan Bhattacharya**, Debadipta Basak,S Reddy,Subir Kumar Sarkar "**Impact of Source Engineering in Split Drain Tunnel Field Effect Transistor**" IEEE EDKCON 2018 , Pride Hotel, Kolkata
6. Bijoy Goswami, Debadipta Basak, **Ayan Bhattacharya**, Koelgeet Kaur, Sutanni Bhowmick, Subir Kumar Sarkar "**Analytical Modeling and Simulation of Low Power Salient Source Double Gate TFET** " ,Kalyani University,23-24 March,2019