Analytical Modeling and Simulation Based Validation for Some Renovated Nano TFET Device Structures

THESIS SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE AWARD OF THE DEGREE OF

MASTER OF TECHNOLOGY IN

VLSI DESIGN AND MICROELECTRONICS TECHNOLOGY BY

DEBADIPTA BASAK

Roll No: 001610703005

Examination Roll No: M6VLS19013

Registration No: 137277 of 2016-17

Under the Esteemed Guidance of

PROF. SUBIR KUMAR SARKAR

Department of Electronics and Tele-Communication Engineering

Jadavpur University

Kolkata-700032, West Bengal, India

MAY 2019

Faculty of Engineering & Technology

Jadavpur University

CERTIFICATE OF EXAMINATION

This is to certify that the thesis entitled "**Analytical Modeling and Simulation Based Validation for Some Renovated Nano TFET Device Structures**" has been carried out by **DEBADIPTA BASAK (Roll No: 001610703005, Examination Roll No: M6VLS19013 and Registration No: 137277 of 2016-17)** under my guidance and supervision and can be accepted in partial fulfilment for the degree of Master of Technology in VLSI Design and Microelectronics Technology. In my opinion the work fulfils the requirement for which it is submitted. To the best of my knowledge, the matter embodied in the thesis has not been submitted to any other organization.

_____

Prof. Subir Kumar Sarkar

Project Supervisor

Course Coordinator of VLSI Design and Microelectronics Technology

Department of Electronics and Tele-Communication Engineering

Jadavpur University, Kolkata-700032

_____

Prof. Sheli Sinha Chaudhuri

Head of the Department

Department of Electronics and

Tele-Communication Engineering

Jadavpur University, Kolkata-700032

_____

Prof. Chiranjib Bhattacharjee

Dean

Faculty Council of Engineering

and Technology (FET)

Jadavpur University, Kolkata-700032

Faculty of Engineering & Technology

Jadavpur University

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NAME: **DEBADIPTA BASAK**

EXAMINATION ROLL NUMBER: **M6VLS19013**

DEPARTMENT: **Electronics and Tele-Communication Engineering (ETCE)**

Thesis Title: "**Analytical Modeling and Simulation Based Validation for Some Renovated Nano TFET Device Structures"**

_____

(DEBADIPTA BASAK)

Signature with Date

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Debadipta Basak

M.Tech VLSI Design and Microelectronics Technology

Department of ETCE, Jadavpur University

Kolkata-700032, West Bengal, India

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Abbreviations

Chapter 1

MOSFET – Metal Oxide Semiconductor Field Effect Transistor

SCE – Short Channel Effect

FET – Field Effect Transistor

TFET – Tunnel Field Effect Transistor

DIBL – Drain Induced Barrier Lowering

CLM – Channel Length Modulation

SS – Subthreshold Slope

CMOS – Complementary Metal Oxide Semiconductor

SOI – Silicon on Insulator

LDD – Low Doped Drain

BTBT – Band to Band Tunneling

SPICE – Simulation Program with Integrated Circuit Emphasis

Chapter 3

2D TFET – 2 Dimensional Tunnel Field Effect Transistor

DG TFET – Double Gate Tunnel Field Effect Transistor

PNPN-DG TFET – PNPN Double Gate Tunnel Field Effect Transistor

Chapter 4

2D SOI TFET – 2 Dimensional Silicon on Insulator Tunnel Field Effect Transistor

GCES SOI TFET – Gate Centric Extended Source Silicon on Insulator Tunnel Field Effect Transistor

Abstract

This work contains the analytical modeling along with validation by commercially available simulation on software for some of the TFET structures as alternatives to conventional TFET devices and focuses on the improvement of the alternative TFET structures. The limitations and the constraints of the conventional TFET devices are overcome by the proposed alternative structures in terms of device performance. The characteristics, integrity and application of such TFET devices contribute to the subsequent IC technology.

In the first work a novel source pocket doping in PNPN-DG TFET has been explored. Two dimensional analytical modeling of surface potential together with its validation by simulation has been carried out to preclude ambipolar current. The gate length has been varied and the surface potential of each of them has been compared with the simulated results. Transfer characteristics of the proposed structure with three different gate lengths have been intensively studied and it exhibits that reduction of the gate length reduces ambipolar conduction.

The second work demonstrates another alternative structure of TFET device that includes analytical current modeling considering point and line tunneling mechanism of classical approach and validation of the same by simulation. The gate length of Gate Centric Extended Source SOI TFET (GCES SOI TFET) has been altered while performing the simulation that has been carried out using Silvaco, Atlas. The device parameters such as I_{on}/I_{off}, subthreshold slope, threshold voltage are analyzed and comparatively studied. The structure has been optimized to get suitable V_{DS} for operation, dimension of source extension, and drain contact position. Considering these optimum configurations, the structure is simulated taking into account both quantum mechanical effects and classical behavior and the evaluated outcomes indicate 10nm gate length as the best structure in terms of SS and V_{th} amongst the three. The structure exhibits large ON current due to effects of line and point tunneling at the source and gate overlap region which is the combined effect of trench gate and extended source. The comparative study between the transfer characteristics considering classical and quantum effects exhibits that ON current is greater and SS is lesser in case of classical approach compared to quantum confinement effects due to discretization of energy bands in quantum confinement.

Chapter 1
Introduction and Thesis Outline

1.1 Introduction

Gordon Moore postulated that in every 18 months the number of transistors will be doubled for a particular unit of chip area in order to incorporate more functionality and speed. However the miniaturization of the devices raised concern towards achieving low power and low latency during the operation. MOSFET [1]-[7] devices experience some drawbacks like power dissipation, short channel effects (SCEs) etc. The saturation of Moore's estimation and also in order to overcome the disadvantages of MOSFET, alternative FET structures such as Tunnel Field Effect Transistor or TFET has been proposed in the field of Nano devices.

In low dimensions MOSFET [8] devices face severe issues related to device performance due to excessive scaling. Smaller channel lengths of the device cause short channel effects like Drain Induced Barrier Lowering (DIBL), Hot carrier effects, Channel length modulation (CLM), Threshold voltage roll-off etc. Also the leakage current is a major issue during the OFF state of the device that increases power consumption. Low power device has much demand in semiconductor industry alongside low area requirements. Thus to overcome these hindrances faced by MOSFET devices alternative device structures are developed and TFET

is one the major improvement in the field of nano devices. TFET works on different principle for carrier transport than MOSFET because of its structural difference. Electrons tunnel from source to channel in case of TFET whereas thermionic injection is the major cause of carrier flow in MOSFET. TFET also provides faster operation as subthreshold slope for the same can be reduced below 60mV/dec.

The following works are focused towards some advanced structures of TFET compared to conventional TFET. In addition to this, TFET structures are advantageous in case of fabrication as it can be fabricated using CMOS process technology like the MOSFET structures. So the TFET structures and its applications in Nano scale industry are promising for future endeavours. For low dimensional device, quantum confinement occurs which is also considered in one of the works and compared with classical outcomes.

1.2 Literature Survey and State-of-the-Art

Tunnel Field Effect Transistor (TFET) is a promising device structure in the field of low power electronics and semiconductor devices. TFET devices have opposite source and drain doping types unlike MOSFET devices and the carriers follow tunneling mechanism from source to channel that leads to current conduction in the device. To increase the ON current of the device along with low power operation by lowering subthreshold slope is accomplished with several structural modifications. A compendious study of different TFET structures are presented in this section which mainly includes dual gate TFETs and SOI TFETs.

In the year 2006 a novel double gate TFET structure has been proposed [9] where for the first time double gate operational advantages over single gate structures are demonstrated. The structure also included high K dielectric materials instead of SiO_2 and a current of about 1mA was achieved for a gate voltage of 1.2V. Also the OFF current for the device was observed to be as low as 0.1fA that increased I_{on}/I_{off} along with a subthreshold slope of 52mV/dec.

A source gate overlapped TFET [10]-[11] structure is analyzed in 2008 and 2011 at nanometer dimension. The model is analytically derived considering line tunneling and point tunneling at the source channel interface due to the overlap region. The generation rate for Kane's model is considered and integrated in order to determine drain current of the device and

this work has been done separately by taking into account of point tunneling as well as line tunneling. Thickness of gate oxide and source doping concentrations are key factors upon which these two tunneling mechanism are dependent on.

A source-pocket TFET structure has been thoroughly investigated in the year 2011[12] where current flow in the device is depended on band to band tunneling at the source channel interface. Because of the presence of n+ pocket region at the source side, a different fabrication methodology and annealing mechanism has been adopted. The advantage of highly doped source side pocket region in this structure is examined in terms of device performance parameters such as higher ON current, lower subthreshold slope(SS) in comparison with conventional TFET. Low doped drain (LDD) extension along with this structure reduces ambipolar conduction. The structure also has been examined in temperature fluctuations that display very less temperature dependence of the device.

A 2D SOI TFET structure is modeled in [13] where drain and source depletion regions have also been considered. This structure is also analytically modeled and verified with simulated results for surface potential, band to band carrier generation rate and electric field. From the electric field and band to band generation rate, drain current is derived which describes the effect of gate voltage and predicts the nature of ambipolar conduction. The model has included several effects precisely gate work function, silicon thickness, thickness of the gate oxide etc. and the results of the analytical models are compared with simulated outcomes to establish accuracy.

In 2012 the impact of quantum confinement has been studied [14]-[15] for very low dimensional DG-TFET structure. The impression up on the device performance due to quantum effects are investigated and compared with conventional device behaviors such as electrical parameters, SS and threshold voltages. Here it has been observed that the inclusion of quantum confinement causes discretization of the energy bands and that eventually reduces band to band tunneling in the device. Thus much impact has been created on device characteristics mentioned above for incorporating non local BTBT tunneling effects along with quantum confinement.

In 2015 an SOI TFET with back gate control [16] has been analyzed using TCAD simulations. The structure also incorporates two different gate oxide materials namely HfO_2

and SiO_2. The device performance parameters such as band to band generation rate, ON and OFF current are examined for different thickness of body layers, gate oxides and back gate voltages. The device offered better ON current, better ON current to OFF current ration and less subthreshold swing. It has been observed that ON current is independent of the back gate bias for that particular structure.

In the year 2018 a source channel overlapped TFET structure [17] along with trench gate has been investigated. I_{on}/I_{off}, transfer characteristics, subthreshold slope (SS), BTBT rate has been rigorously examined and it has been found from the results that the structure exhibits I_{on}/I_{off} ratio of around 10^{10} and an ON current of 10^{-5} A/um. The structure offers better switching characteristics and the device is included in an inverter circuit and it has been characterized by SPICE simulation that provides high frequency of about 1GHz at the gate voltage of about 1V.

1.3 Thesis Outline

This thesis focuses on analytical modeling and validation of the same by simulation of some modified nano TFET device structures.

Chapter 1: This chapter presents a brief introduction of the thesis work. It provides a concise description of the Nano device specifically TFET and the objective of the work. The outline of the thesis has also been given in this chapter.

Chapter 2: This chapter presents literature survey and previous research works regarding the Nano devices and their applications. An introduction to the Tunnel Field Effect Transistor and its operation has also been elaborately analyzed in this chapter.

Chapter 3: An alternative 2D TFET structure precisely Source Pocket Doping in PNPN-DG TFET has been demonstrated in this chapter. The chapter includes overview of the proposed structure, the specific structural description. Analytical modelling of the surface potential has been accomplished to validate the simulated results. A comparative study of the results are illustrated in this chapter which eventually concludes the privilege of the proposed work over the conventional TFET structures.

Chapter 4: In this chapter another variation of TFET structure has been analytically modeled and validated by simulation. The work presents a Gate Centric Extended Source SOI TFET, its analytical current modeling using classical line and point tunneling approach and validation of the same by simulation. Also the same structure has been simulated considering quantum confinement and compared to classical outcomes. The results are analyzed and a rigorous discussion has been presented in this chapter that leads to the conclusion regarding benefits and application areas along with future endeavors of the proposed work.

Chapter 5: This final chapter includes the conclusion drawn for the entire thesis work along with future scopes of Nano devices.

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Chapter 2
Introduction to Nano Devices and TFET

2.1 Introduction to Nano Devices and Applications

The concept of Nano technology and Nano device came from Richard Feynman who described a process by which scientists can control and be able to manipulate nano scale particles including atoms and molecules.

For insurgence of the nano industry along with the field of electronics comprises of the advancement of Nano devices. Nano devices consist of the study of devices with structural dimension from 1nm to 100nm that is the technology operates in nanometer range only. Nanotechnology encompasses development of nanoscale physical, chemical and biological systems and also assimilates them for larger systems. There are some differences between the nano particles of materials and the larger ones of the same materials and the difference lies in surface area per weight of the material. As the nano particles consist of larger surface area

therefore are more susceptible to reactions with other particles. Reduction of dimension to nano scale also incorporates the properties of quantum realm that supersedes the classical behaviors.

Nano devices revolutionize the electronics industry and research domains with extensively prevalent ideas that results into smart devices such as phones, appliances, and gadgets etc. Nano devices have enormous future prospects in different fields [1][2][3] in terms of energy conservation, more functionally active but compact machines along with great reliability.

Application of nano devices and nano technology are widespread through enormous fields such as medicine, energy, electronics and other industries. In the field of medicine nano electronic devices such as biosensors are extensively used. Nano devices can be used for low power applications for energy conservation as well. Nano devices are useful for other electronics applications such as memory devices where a large memory can be fit into very small area in space.

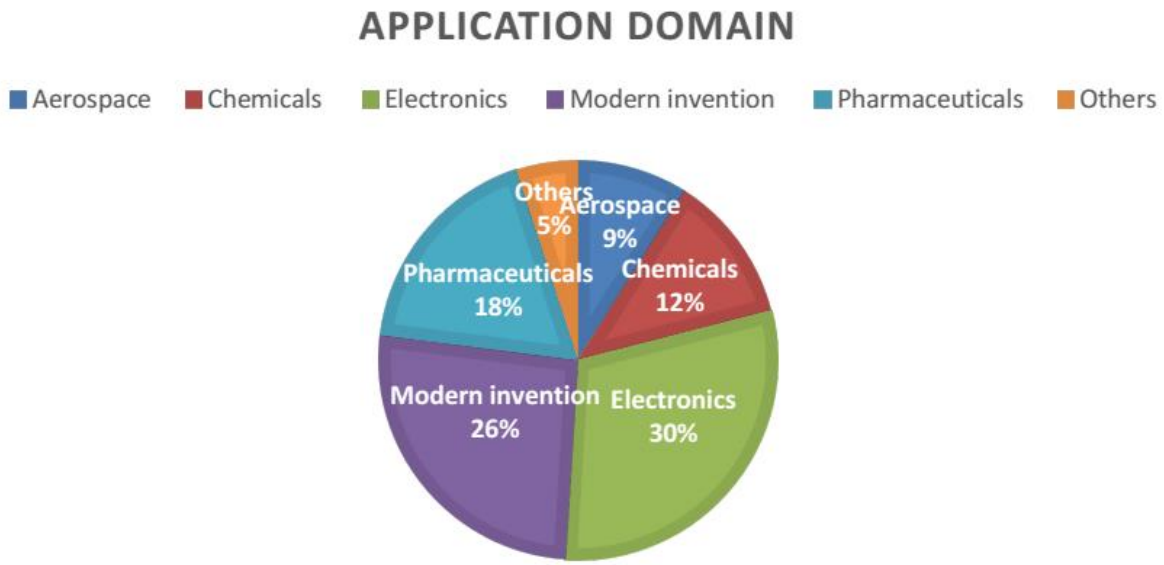


Fig2.1: Application areas of Nano devices.

2.2 Introduction to Tunnel Field Effect transistors

The main focus of semiconductor technology is to accommodate more functionality in smaller area and to achieve this goal scaling of device dimension has become a continuous process in this field. It has been a long journey from the period of vacuum tubes to MOSFETs [4]-[8] of

micrometer range. The technology defined by the gate length of the transistors are further reduced and this process has been predicted by Moore's law which predicted that number of transistors will be doubled in a particular unit of area in every 18 months. Eventually the reduction of dimensions of MOSFET devices have reached some limit and are constrained by short cannel effects(SCEs)[9], minimum subthreshold slope of 60mV/dec[10] etc. Scaling includes voltage scaling which reduces power consumption but after a certain dimension (50nm), off state power consumption becomes a major issue for low dimensional devices. Another significant criteria of semiconductor devices is low power application [11]-[12]. To overcome the constraints such as larger leakage current [13] and subthreshold slope met by MOSFET [14]-[18] devices, an alternative structure became important in this field.

Subthreshold slope is defined as

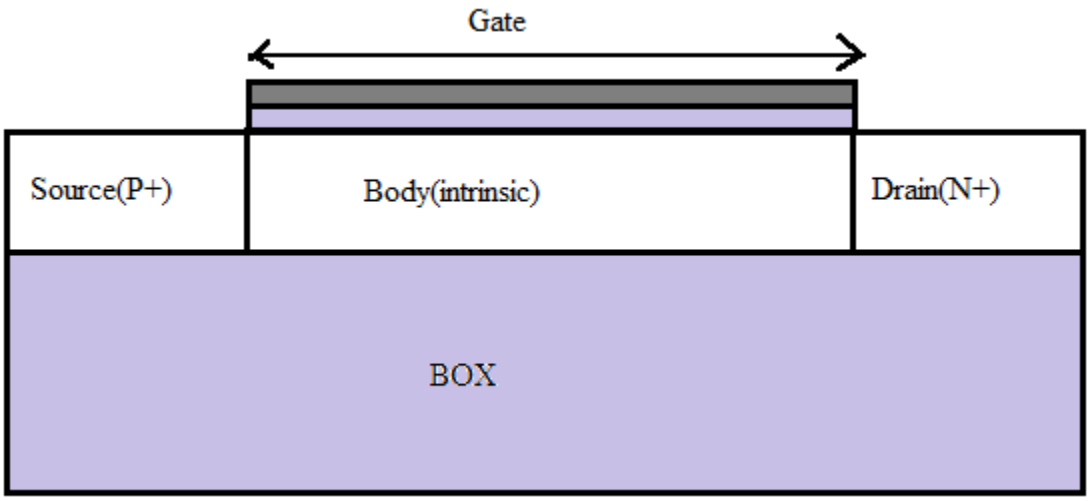
$$SS = \left(\frac{d(\log_{10} I_{DS})}{dV_G} \right)^{-1}$$

The alternative device that could face the challenges of MOSFET is Tunnel Field Effect Transistor (TFET). The mechanism of current flow is different in case of MOSFET and TFET devices which elaborately could be explained by stating that current in MOSFET is the cause of thermionic emission of carriers from source to channel whereas current in TFET is caused by tunneling of carriers at the source channel interface. Also subthreshold slope below 60mV/dec can be achieved by TFET devices and are more immune to SCEs such as threshold voltage roll-off, drain induced barrier lowering (DIBL) etc.

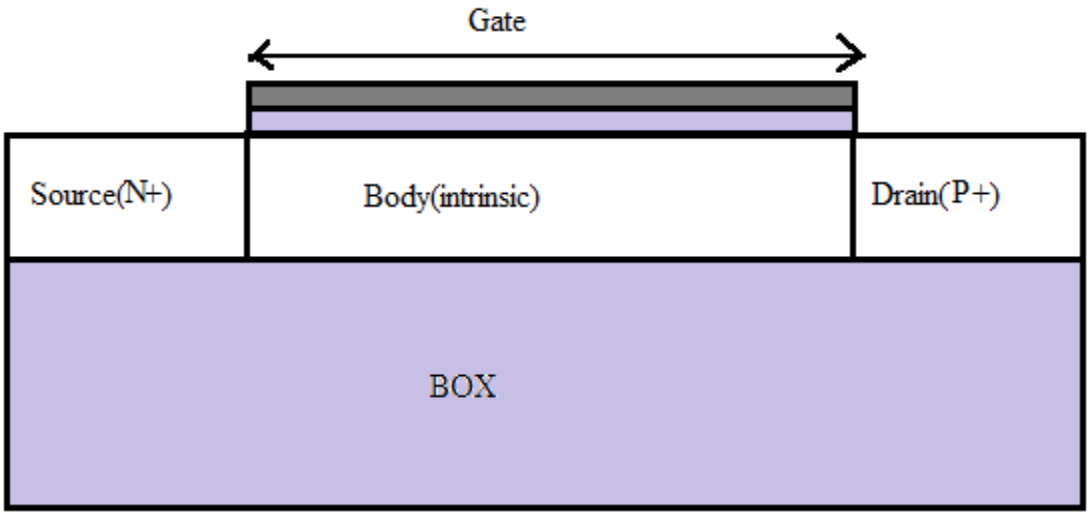
The difference in structure of MOSFET and TFET lies in type of source doping and therefore fabrication steps of TFET devices can be assimilated with that of the MOSFET. The details of TFET structures are explored below:

2.2.1 Basic Structure of TFET

Basic structure of TFET includes different regions along with their doping type and contacts that controls the operation of the device. Two types of basic TFET structures are examined below each of which contains three regions namely source, channel and drain. N-channel and P-channel TFET are similar to NMOS and PMOS except for the source doping type that differs in TFET from MOSFET. The structures are illustrated below:



(a)



(b)

Fig2.2: (a) n-channel TFET and (b) p-channel TFET structure

For NMOS source and drain are of n-type whereas for n-channel TFET source doping is of p-type while drain is n-type. Similarly in case of PMOS source and drain doping are p-type but for p-channel TFET drain is p-type while source doping is opposite that is n-type. The channel region for both the variations of TFET are generally either intrinsic or very lightly doped. This conventional TFET structure is varied to achieve better performance in terms of device

parameters. Next we will study the band diagrams of n-channel TFET for different state of the device.

2.2.2 Band diagram analysis

Band diagram during thermal equilibrium can be observed when there is no external bias is applied ($V_G=V_S=V_D=0$).

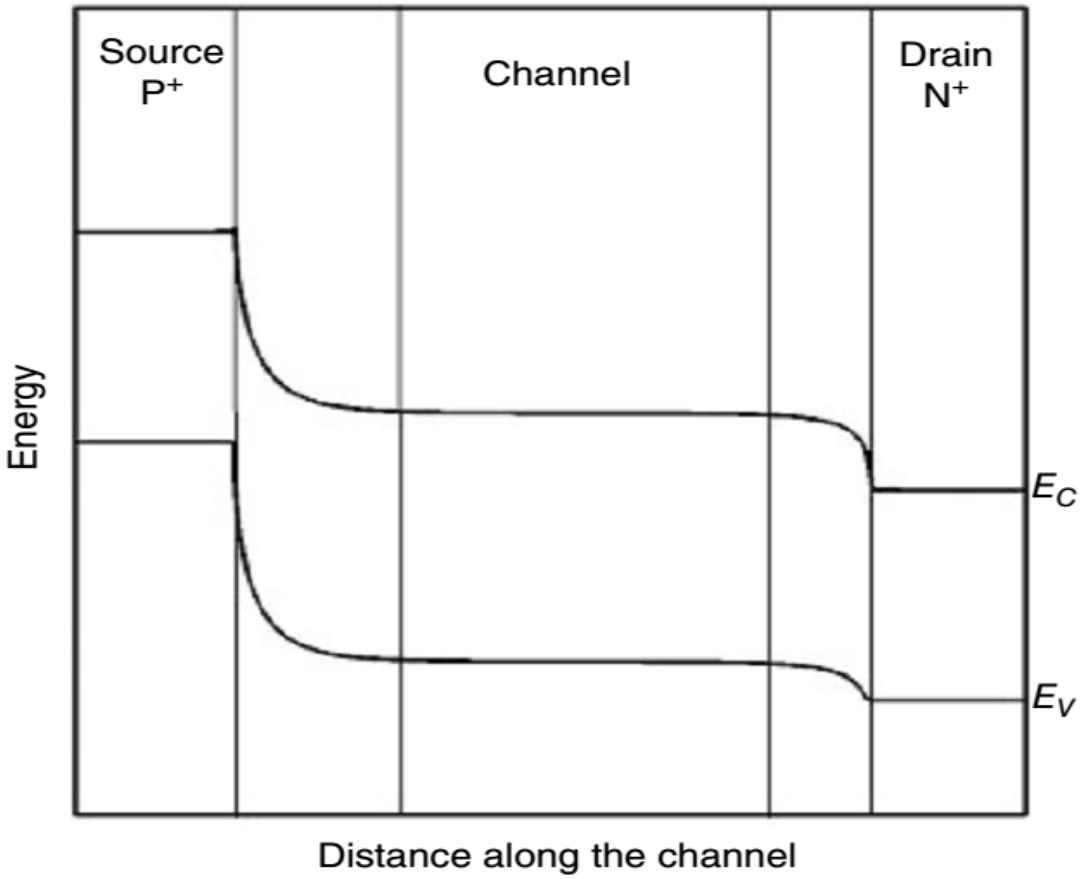


Fig2.3 Band diagram of n-channel TFET in zero bias condition

During OFF state that is when $V_{GS}=0$ but $V_{DS}>0$, the carriers from the channel will have little tendency to drift to drain current while as the source is of p-type therefore very few electrons in the conduction band can be injected to the channel leading to negligible OFF state current. Comparatively as MOSFET has n-type source so greater number of electrons from the conduction band can be injected to the channel due to thermionic emission resulting into greater OFF current than TFET.

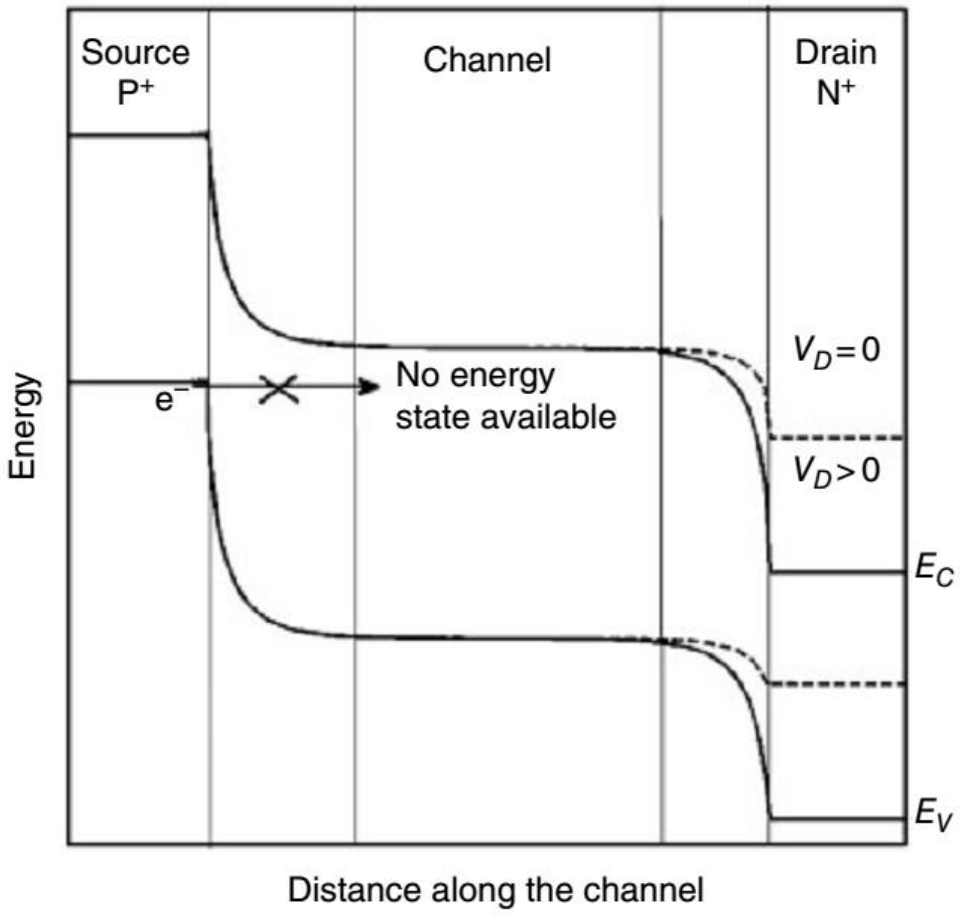
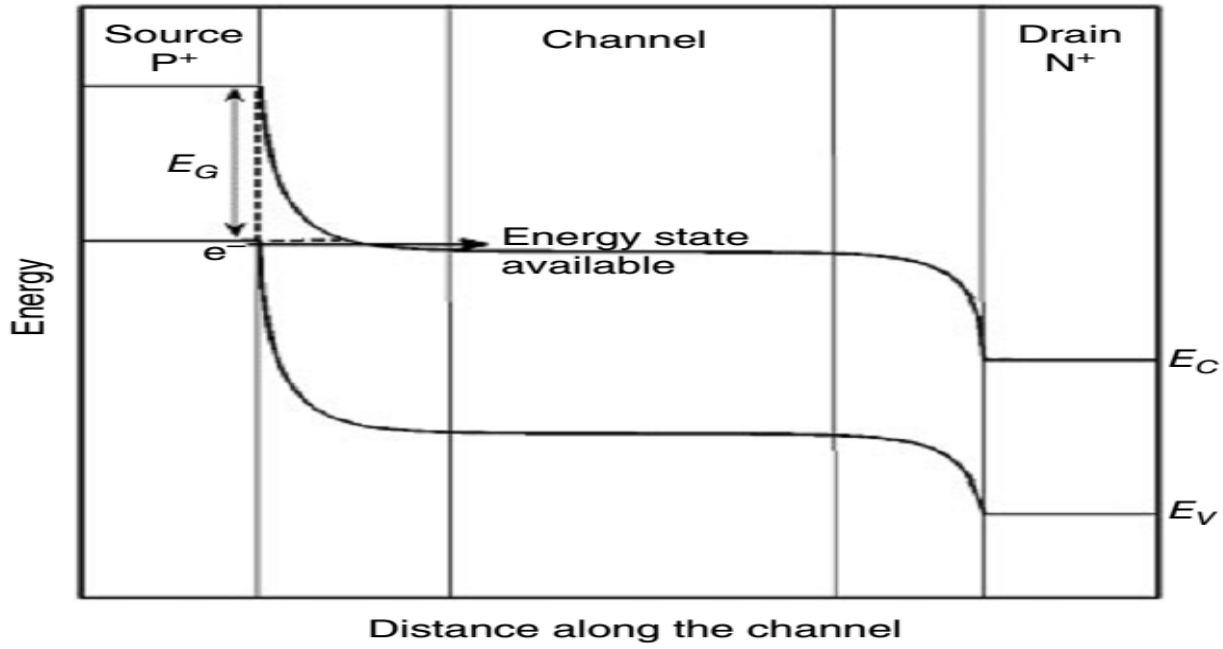
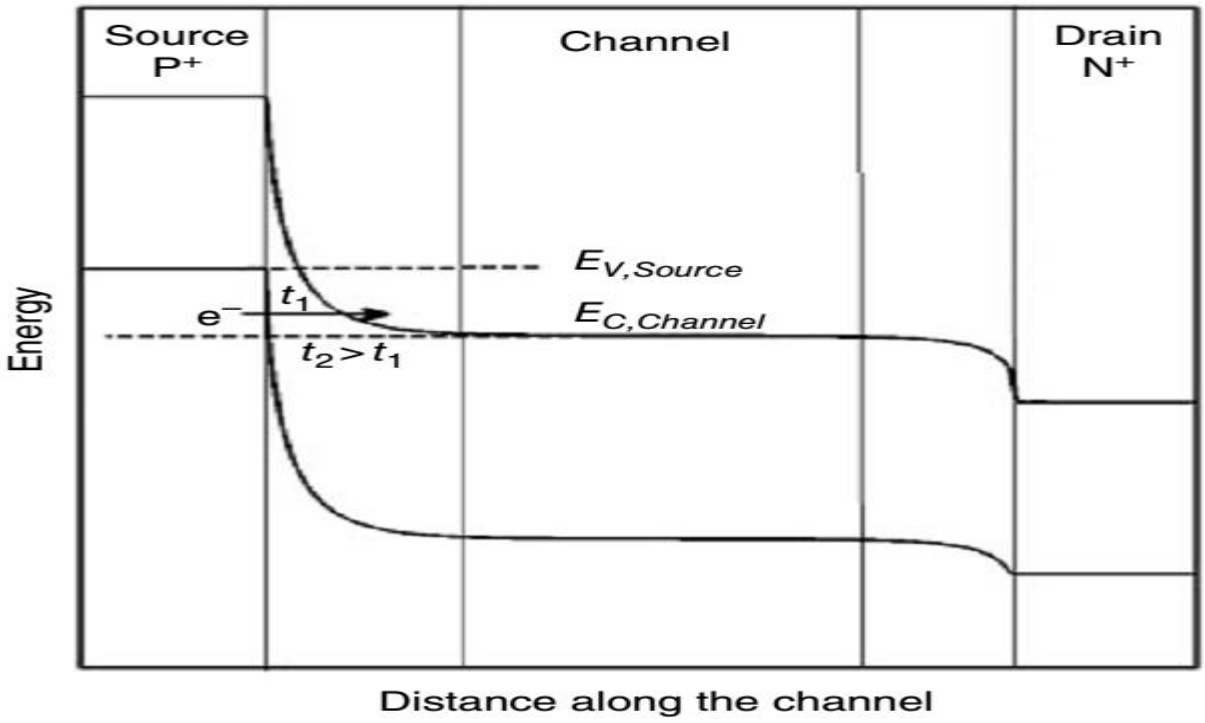


Fig2.4 Band diagram of n-channel TFET in OFF state (V_{GS}=0)

In order to turn the device into ON-state the carriers should be injected from the valence band of the source to the conduction band of the channel as there are negligible amount of electrons in the conduction band of p-type source. To achieve this state V_{GS} in increased and the bad at the interface of source and channel starts bending. At a certain value of V_{GS}>0 there will be available empty energy state in the conduction band of channel that are aligned to energy states in valence band of source. Thus electrons will tunnel from source valence band to channel conduction band driving the device into ON state. Further increase of gate potential decreases the tunneling length and increases electron tunneling probability which eventually results into higher ON current. Further increase in gate voltage causes pinning of channel potential to drain potential and therefore increase of drain current does not depend on gate voltage increase anymore. It mostly depends on tunneling length and also the rate of increase of drain current reduces.



(a)



(b)

Fig2.5: Band diagram of n-channel TFET (a) at the starting of ON state and (b) deep into the ON state when $V_{GS}>0$

2.2.3 Ambipolar Conduction

When negative gate voltage is applied the channel potential moves up and a tunneling path is created between channel and drain interface. Electrons from valence band of the channel moves to conduction band of the drain as the both gets aligned. Thus current can flow in same polarity when positive gate voltage was applied. This is known as ambipolar conduction [19-20]. Increasing negative gate voltage increases this current but after a certain point the channel potential gets pinned to source potential and the current becomes solely dependent on tunneling length rather than gate voltage. Also the rate of increase of current decreases.

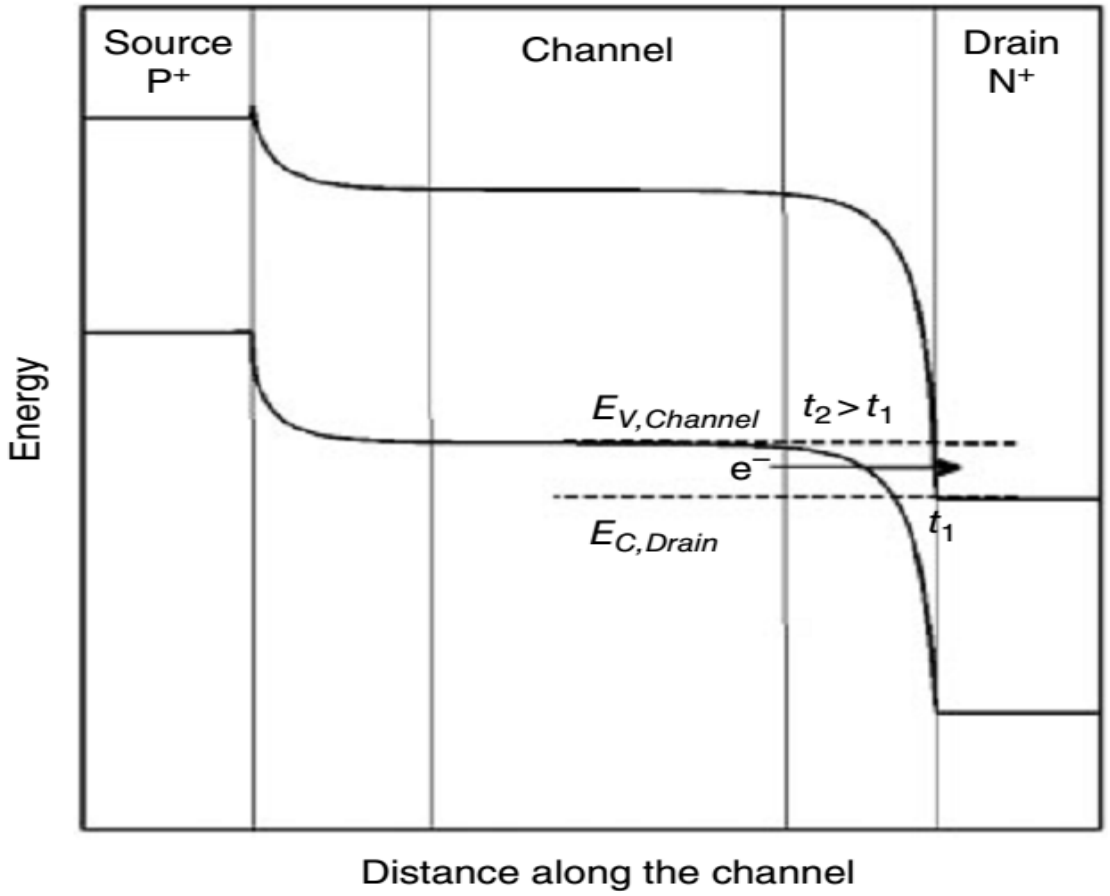
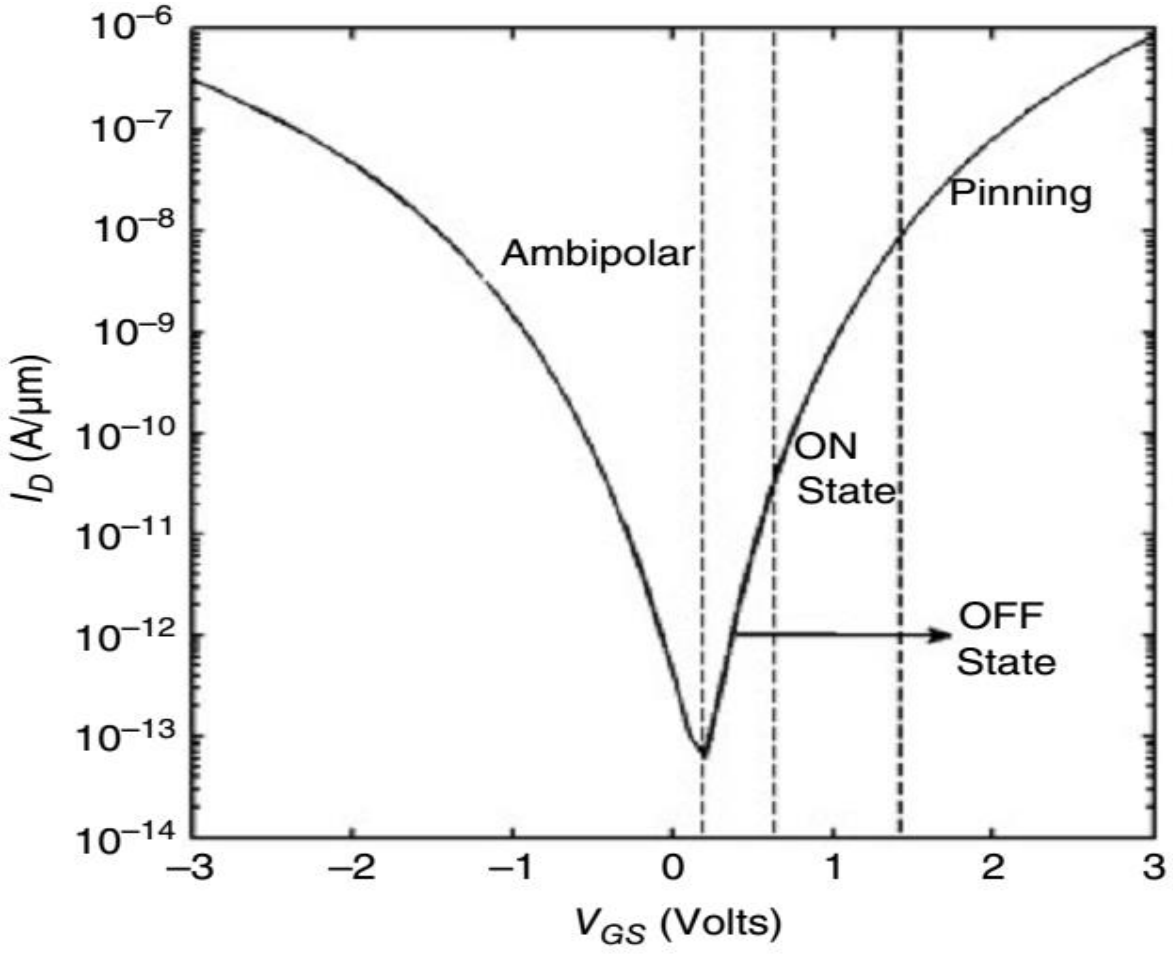


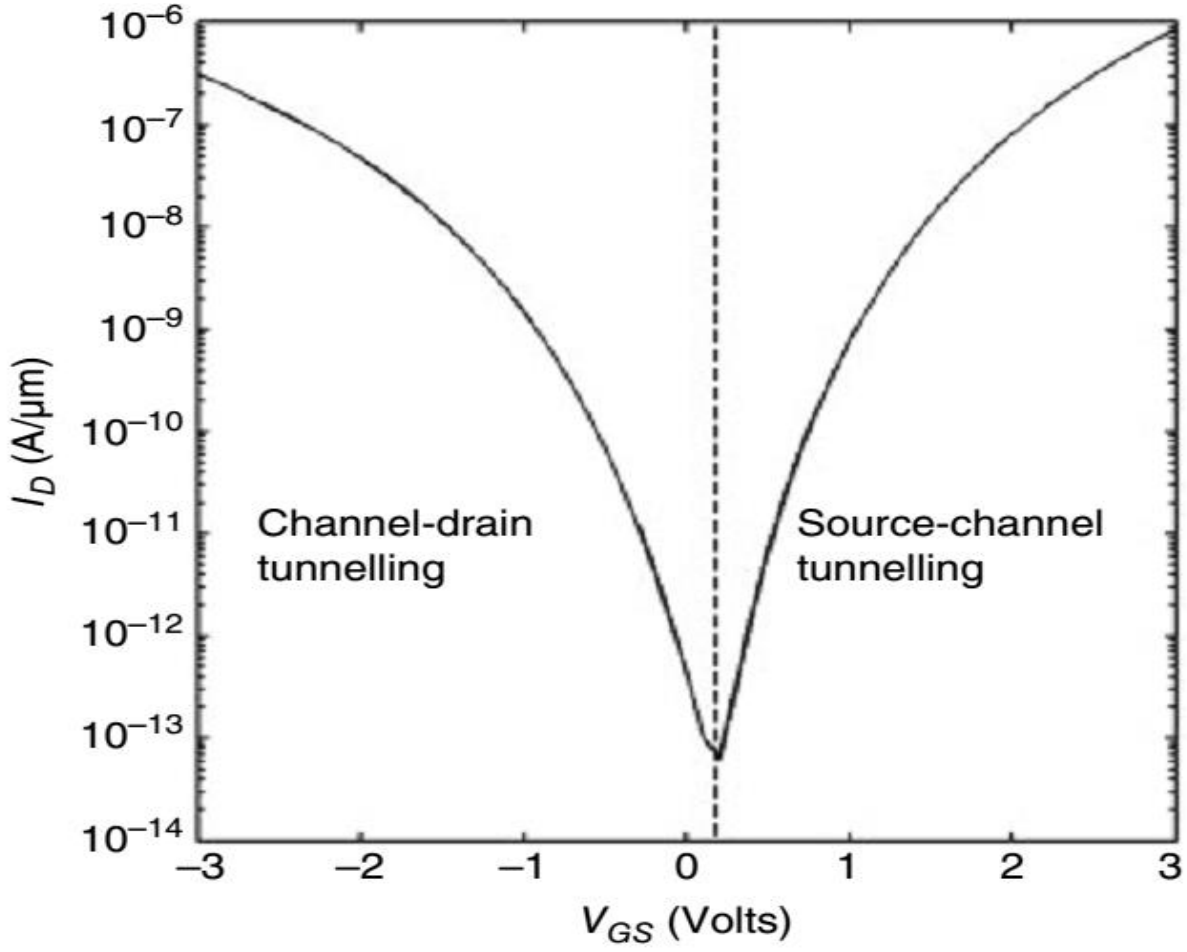
Fig2.6: Ambipolar conduction at channel drain junction when $V_{GS}<0$.

2.2.4 Device Transfer Characteristics

The following figure demonstrates transfer characteristics of TFET [21]-[23] with equal source and drain doping. For positive gate voltage energy states of source valence band and channel conduction band get aligned and electrons tunnel from source valence band to channel conduction band resulting into drain current. During OFF condition negligible OFF current flows through source channel interface. For negative gate bias the energy states of channel valence band and drain conduction band get aligned and electrons tunnel from channel valence band to vacant energy states of drain conduction band. This causes ambipolar conduction in negative gate bias.



(a)



(b)

Fig2.7: Transfer Characteristics of n-channel TFET showing (a) different regions of operation and (b) ON state and OFF state current due to source-channel and channel-drain tunneling.

2.2.5 Device Output Characteristics

Initially when $V_{GS} > V_{DS}$, drain current increases due to increase in gate bias. Gradually the channel potential is pinned to drain potential and after that increase in drain potential increases channel potential which results into enhancement of drain current. When drain and gate potential become equivalent, the drain current does not increase anymore with the increase in drain potential and eventually gets saturated.

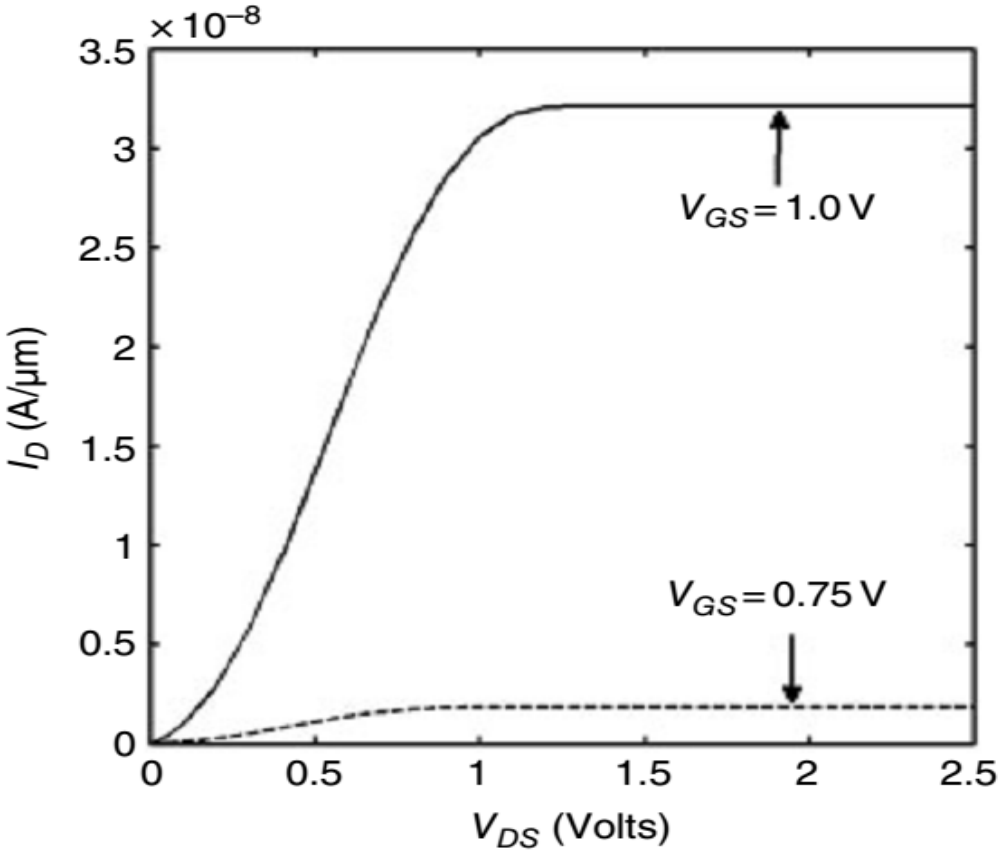


Fig2.8: Output characteristics of n-channel TFET for different V_{GS}

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Chapter 3

Source Pocket Doping in Nano PNPN-DG TFET

3. Source Pocket Doping in Nano PNPN-DG TFET

3.1 Introduction to the proposed work

An analytical model for a 2D TFET with two symmetrical source pocket doping is presented in this chapter. The structure of TFET proposed here is symmetric having double gate along with two heavily doped pocket regions at the source that enhances the source tunnelling which in turn increases the ON current and provides negligible ambipolar conduction which is the ramification

of conventional TFET structures along with its suitability for low power applications. The gate length is varied to 24nm, 14nm and 7nm and these three structures are compared. Nevertheless, in all the three cases, Silvaco Atlas-based simulation is performed where the channel length is considered to be 24nm. The proposed structure(s) is analytically modelled and suitably validated with simulated outcomes. All the simulations in this work are accomplished with Silvaco, Atlas.

The improvement of performance of the devices is achieved by scaling of the device size, modification of device structure with new material incorporation and structure varieties. MOSFET structures have their limitation over betterment of performance due to the short channel effects and therefore researchers opted for TFET devices[1]-[4] which contribute to the new ways of developing advanced device structures [5]-[9]. The TFET devices are capable of achieving lower subthreshold swing of less than 60mV/decade than MOSFET[10]-[14] due to the BTBT mechanism that leads to higher I_{on}/I_{off} ratio [15].

The cross-section of double gate (DG) TFET structure [16]-[17] with two heavily doped source pocket regions [18], [19-20] is shown in Fig3.1. The two source pocket regions enhance the source tunneling thereby increasing the ON current. Also it has been seen that when the gate length is reduced to 7nm, these pocket regions help in minimizing the ambipolar current to negligible amount hence making the proposed structure suitable for low power applications.

Analytical studies [21] on TFET modeling are increasing because a physics-based analytical model provides an insight on the device physics and facilitates compact modeling for circuit-level studies.

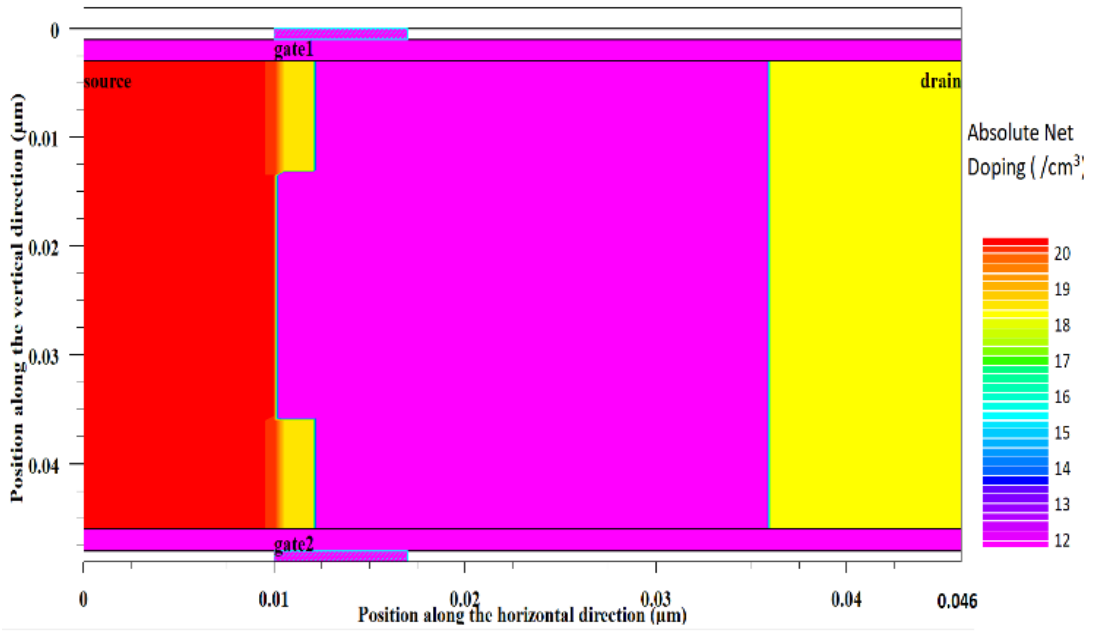
In this work, a 2-D analytical model for DG TFETs with two source pocket doping regions is presented. Based on the 2-D Poisson's equation solution, analytical expression for the surface potential is derived. This work is structured as follows: In Section 2 the device structure has been discussed. In Section 3 analytical expression for the surface potential has been derived. Then in section 4, the analytical model is validated by comparing it with simulation results. Also, graphs for potential distribution, total current density, electric field for different gate lengths has been shown.

3.2 Device Structure and Parameters

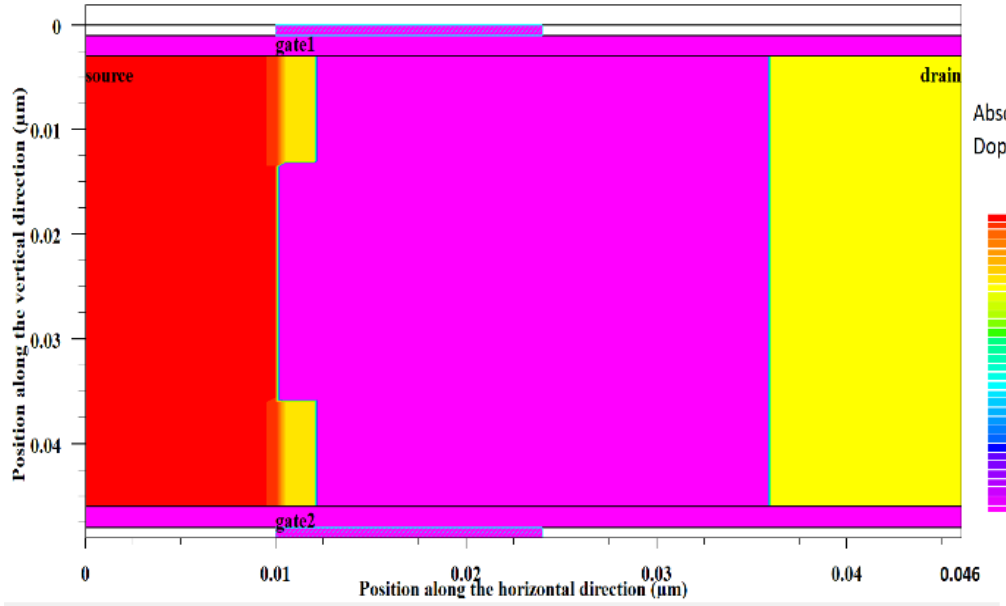
The proposed 2D structure of the double gate TFET consists of two symmetric gates on both top and bottom of the device. The device length is considered to be 46nm along with the vertical dimension of 49nm. The gate length is varied [22] to 24nm, 14nm and 7nm whereas the effective channel length is examined to be 24nm.

SiO2 is applied as the oxide material on both side of the device having length as same as the device and thickness of t_{ox}=2nm. The 10nm long drain region is of N+ type with doping concentration of $5x10^{18}$ cm^{-3}. The source region has P+ type doping concentration of $5x10^{20}$ cm^{-3} having the dimension of 10nm length and 43nm of depth.

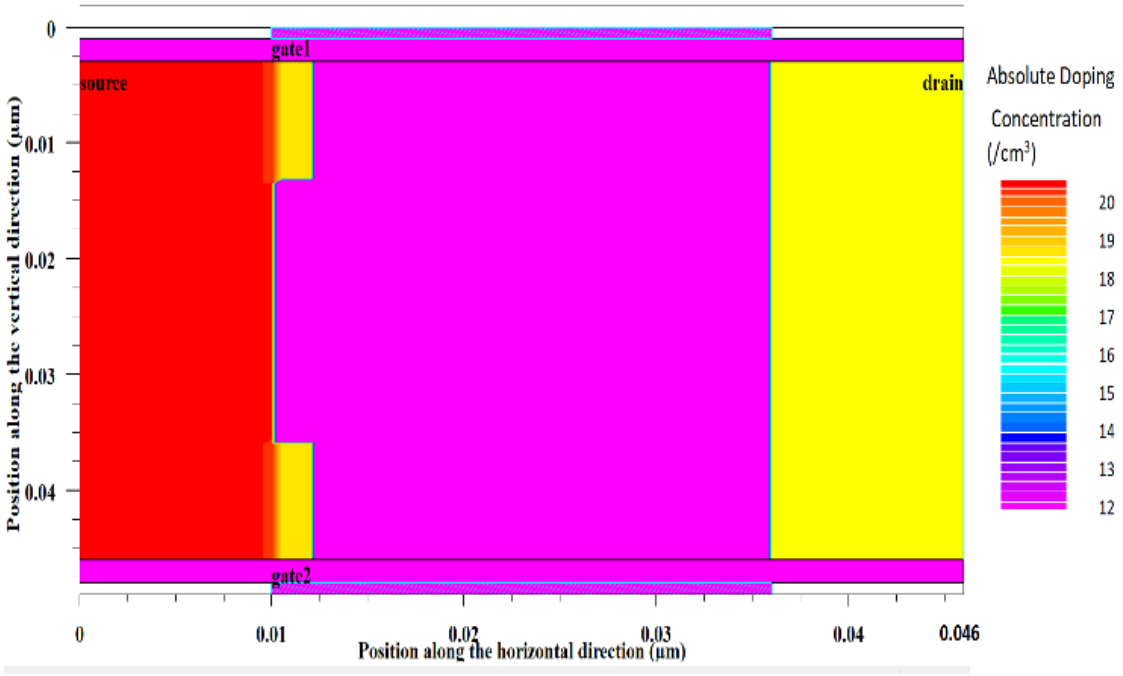
In addition to this the source region consists of two symmetric pockets of N+ type doped regions having concentration of 10^{19} cm^{-3} with each having the dimension of 2nm length and 10nm of depth. Both the gate contacts have work function of 5.1eV and the source and drain contacts are considered to be in vertical direction on two opposite sides of the proposed structure.



(a)



(b)



(c)

Fig3.1: Structure of PNPN-DG TFET for gate length of (a)7nm , (b)14nm and (c) 24nm.

3.3 Analytical Modelling

The analytical modelling of the surface potential has been verified with the simulated results.

3.3.1 Surface Potential

2-D Poisson's equation is used to administer the surface potential of the proposed structure which is given by

$$\frac{\partial^2\phi(x,y)}{\partial x^2}+\frac{\partial^2\phi(x,y)}{\partial y^2}=-\frac{qN_{cn}}{\varepsilon_{si}} \tag{3.1}$$

where $0\le x\le L$ and $0\le y\le t_{si}$

Here N_{cn} is the doping concentration at the channel region and the channel length L is divided into three regions. Thus the total length L = L1+L2+L3. The surface potential profile has been approximated using the parabolic polynomial function such as

$$\phi(x,y)=\phi_s(x)+C_1(x)y+C_2(x)y^2 \tag{3.2}$$

Where C1 and C2 are arbitrary functions of x and $\phi_s(x)$ is surface potential. As the channel is divided into three regions of aforementioned length therefore the surface potential under different regions as considered here can be represented in the following way

$$\phi_j(x,y)=\phi_{sj}(x)+C_{j1}(x)y+C_{j2}(x)y^2 \tag{3.3}$$

for $L_{j-1}\le x\le L_j$, $0\le y\le t_{si}$ and j=1,2 ,3.

The surface potential can be achieved by solving the Poisson's equations with the application of the boundary conditions as follows.

The electric field is continuous at y=0 that is for the front–gate oxide interface which leads to the three expressions corresponding to three regions below:

$$\left.\frac{d\phi_1(x,y)}{dx}\right|_{y=0}=\frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{\phi_{s1}(x)-V_{GS1}}{t_f} \tag{3.4}$$

$$\left.\frac{d\phi_2(x,y)}{dx}\right|_{y=0}=\frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{\phi_{s2}(x)-V_{GS1}}{t_f} \tag{3.5}$$

$$\left.\frac{d\phi_3(x,y)}{dx}\right|_{y=0}=\frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{\phi_{s3}(x)-V_{GS1}}{t_f} \tag{3.6}$$

Here $V_{GS1} = V_{GS} - V_{FB,L1}$ and $V_{FB,L1} = \phi_{MS1} = \phi_M - \phi_{si}$ where $V_{FB,L1}$ is the flat band potential, ϕ_M and ϕ_{si} are the metal and silicon work functions respectively. Also, $\phi_{si} = \chi + \frac{E_g}{2q} + \phi_B$ where χ is electron affinity, E_g is bandgap of silicon, ϕ_B is built-in potential and is given by $\phi_B = V_T \ln \frac{N_{cn}}{n_i}$.

The electric field is continuous at $y=t_{si}$ that is for the back–gate oxide interface which leads to the three expressions corresponding to three regions below:

$$\left.\frac{d\phi_1(x,y)}{dx}\right|_{y=t_{si}} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{V'_{GS,b1} - \phi_{B1}(x)}{t_b} \tag{3.7}$$

$$\left.\frac{d\phi_2(x,y)}{dx}\right|_{y=t_{si}} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{V'_{GS,b1} - \phi_{B2}(x)}{t_b} \tag{3.8}$$

$$\left.\frac{d\phi_3(x,y)}{dx}\right|_{y=t_{si}} = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{V'_{GS,b1} - \phi_{B3}(x)}{t_b} \tag{3.9}$$

where $V'_{GS1,b} = V_{GS} - V_{FB,L1}$

Using these three boundary conditions mentioned above solution for the arbitrary functions of the parabolic approximation are found to be

$$C_{11}(x) = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{\phi_{s1}(x) - V_{GS1}}{t_f} \tag{3.10}$$

$$C_{21}(x) = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{\phi_{s2}(x) - V_{GS1}}{t_f} \tag{3.11}$$

$$C_{31}(x) = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{\phi_{s3}(x) - V_{GS1}}{t_f} \tag{3.12}$$

$$C_{12}(x) = \frac{1}{2C_{si}t_{si}^2}\left[C_b(V'_{GS,b1} - \phi_{B1}(x)) - C_f(\phi_{s1}(x) - V_{GS1})\right] \tag{3.13}$$

$$C_{22}(x) = \frac{1}{2C_{si}t_{si}^2}\left[C_b(V'_{GS,b1} - \phi_{B2}(x)) - C_f(\phi_{s2}(x) - V_{GS1})\right] \tag{3.14}$$

$$C_{32}(x) = \frac{1}{2C_{si}t_{si}^2}\left[C_b(V'_{GS,b1} - \phi_{B3}(x)) - C_f(\phi_{s3}(x) - V_{GS1})\right] \tag{3.15}$$

The values of these constants are put into (2) and solving for (1), the surface potential is achieved in the following format corresponding to the three regions considered in the structure,

$$\frac{\partial^2 \phi_{s1}(x)}{\partial x^2} - \alpha \phi_{s1}(x) = \beta_1 \tag{3.16}$$

$$\frac{\partial^2 \phi_{s2}(x)}{\partial x^2} - \alpha \phi_{s2}(x) = \beta_2 \tag{3.17}$$

$$\frac{\partial^2 \phi_{s3}(x)}{\partial x^2} - \alpha_3 \phi_{s3}(x) = \beta_3 \tag{3.18}$$

where α , α_3, β_1, β_2 and β_3 are given by:

$$\alpha = \frac{2C_f}{C_{si}t_{si}^2\left(1+\frac{C_{ox}}{C_{si}}-\frac{C_f}{C_{si}}\right)} \tag{3.19}$$

$$\beta_1 = \left[-\frac{qN_{cn}}{\varepsilon_{si}} - \frac{2V_{GS1}C_f}{C_{si}t_{si}^2}\right]\left[\frac{1}{1+\frac{C_{ox}}{C_{si}}-\frac{C_f}{C_{si}}}\right] \tag{3.20}$$

and

$$\beta_2 = \left[-\frac{qN_{cn}}{\varepsilon_{si}} - \frac{2V_{GS1}C_f}{C_{si}t_{si}^2}\right]\left[\frac{1}{1+\frac{C_{ox}}{C_{si}}-\frac{C_f}{C_{si}}}\right] = \beta_1 \tag{3.21}$$

$$\alpha_3 = \frac{2C_f^{'}}{C_{si}t_{si}^2\left(1+\frac{C_{ox}}{C_{si}}-\frac{C_f^{'}}{C_{si}}\right)} \tag{3.22}$$

and

$$\beta_3 = \left[-\frac{qN_{cn}}{\varepsilon_{si}} - \frac{2V_{GS1}C_f^{'}}{C_{si}t_{si}^2}\right]\left[\frac{1}{1+\frac{C_{ox}}{C_{si}}-\frac{C_f^{'}}{C_{si}}}\right] \tag{3.23}$$

Where $c_f^{'} = c_{if} + c_{of}$ and the values of inner fringing capacitance (C_{if}) and outer fringing capacitance (C_{of}) are taken from [23].

Solving those three differential equations i.e. (15), (16) and (17) using C.F. and P.I. and combining the two, solution for surface potential of the three regions are found such as

$$\phi_{s1}(x) = Ae^{\sqrt{\alpha}x} + Be^{-\sqrt{\alpha}x} - \frac{\beta_1}{\alpha} \tag{3.24}$$

$$\phi_{s2}(x) = Ce^{\sqrt{\alpha}(x-L1)} + De^{-\sqrt{\alpha}(x-L1)} - \frac{\beta_2}{\alpha} \tag{3.25}$$

$$\phi_{s3}(x) = Ee^{\sqrt{\alpha}(x-L1-L2)} + Fe^{-\sqrt{\alpha}(x-L1-L2)} - \frac{\beta_3}{\alpha_3} \tag{3.26}$$

where the values of the constants A, B , C, D , E and F are found to be :

$$A = \frac{\beta_1\left(e^{\sqrt{\alpha}L_1} - 1\right)}{\alpha\left(e^{2\sqrt{\alpha}L_1} - 1\right)} + \frac{\left[V_{bi}\left(e^{\sqrt{\alpha}L_1} - 1\right) + (\mathrm{V}_{ds}(\frac{L_2}{L}) + V_{bi})e^{\sqrt{\alpha}L_1}\right]}{\left(e^{2\sqrt{\alpha}L_1} - 1\right)} \tag{3.27}$$

$$B = \frac{\beta_1 e^{\sqrt{\alpha}L_1}\left(e^{\sqrt{\alpha}L_1} - 1\right)}{\alpha\left(e^{2\sqrt{\alpha}L_1} - 1\right)} + \frac{e^{\sqrt{\alpha}L_1}\left[V_{bi}\left(e^{\sqrt{\alpha}L_1} - 1\right) + (\mathrm{V}_{ds}(\frac{L_2}{L}) + V_{bi})\right]}{\left(e^{2\sqrt{\alpha}L_1} - 1\right)} \tag{3.28}$$

$$C = \frac{\beta_2\left(e^{\sqrt{\alpha}L_2} - 1\right)}{\alpha\left(e^{2\sqrt{\alpha}L_2} - 1\right)} + \frac{\left[(V_{ds}(\frac{L_2}{L}) + V_{bi})\left(e^{\sqrt{\alpha}L_2} - 1\right) + (V_{ds}(\frac{L_3}{L}) + V_{bi})e^{\sqrt{\alpha}L_2}\right]}{\left(e^{2\sqrt{\alpha}L_2} - 1\right)} \tag{3.29}$$

$$D = \frac{\beta_2 e^{\sqrt{\alpha}L_2}\left(e^{\sqrt{\alpha}L_2} - 1\right)}{\alpha\left(e^{2\sqrt{\alpha}L_2} - 1\right)} + \frac{e^{\sqrt{\alpha}L_2}\left[(V_{ds}(\frac{L_2}{L}) + V_{bi})\left(e^{\sqrt{\alpha}L_2} - 1\right) + (V_{ds}(\frac{L_3}{L}) + V_{bi})\right]}{\left(e^{2\sqrt{\alpha}L_2} - 1\right)} \tag{3.30}$$

$$E = \frac{\beta_3\left(e^{\sqrt{\alpha_3}L_3} - 1\right)}{\alpha_3\left(e^{2\sqrt{\alpha_3}L_3} - 1\right)} + \frac{\left[(V_{ds}(\frac{L_3}{L}) + V_{bi})\left(e^{\sqrt{\alpha_3}L_3} - 1\right) + (V_{ds} + V_{bi})e^{\sqrt{\alpha_3}L_3}\right]}{\left(e^{2\sqrt{\alpha_3}L_3} - 1\right)} \tag{3.31}$$

$$F = \frac{\beta_3 e^{\sqrt{\alpha_3}L_3}\left(e^{\sqrt{\alpha_3}L_3} - 1\right)}{\alpha_3\left(e^{2\sqrt{\alpha_3}L_3} - 1\right)} + \frac{e^{\sqrt{\alpha_3}L_3}\left[(V_{ds}(\frac{L_2}{L}) + V_{bi})\left(e^{\sqrt{\alpha_3}L_3} - 1\right) + (V_{ds}(\frac{L_3}{L}) + V_{bi})\right]}{\left(e^{2\sqrt{\alpha_3}L_3} - 1\right)} \tag{3.32}$$

Where , L_1, L_2 and L_3 are considered as

$$L_1 = l_p$$
$$L_2 = l_g - l_p$$
$$L_3 = L - l_g - l_p$$

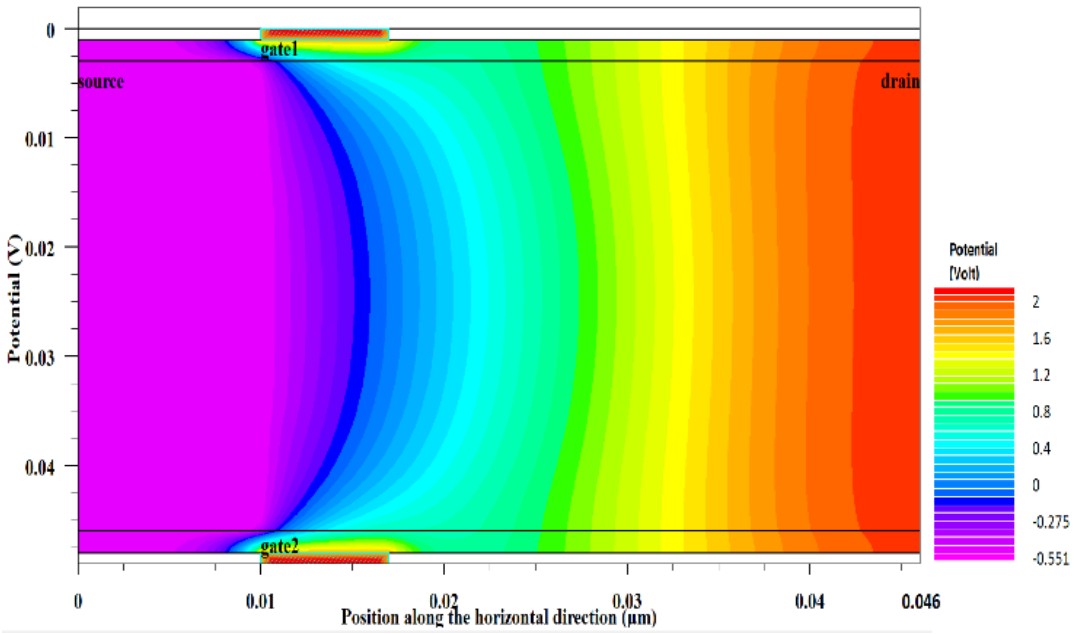
and l_p, l_g are defined as the length of the source pocket region and gate respectively.

3.4 Results and Discussions

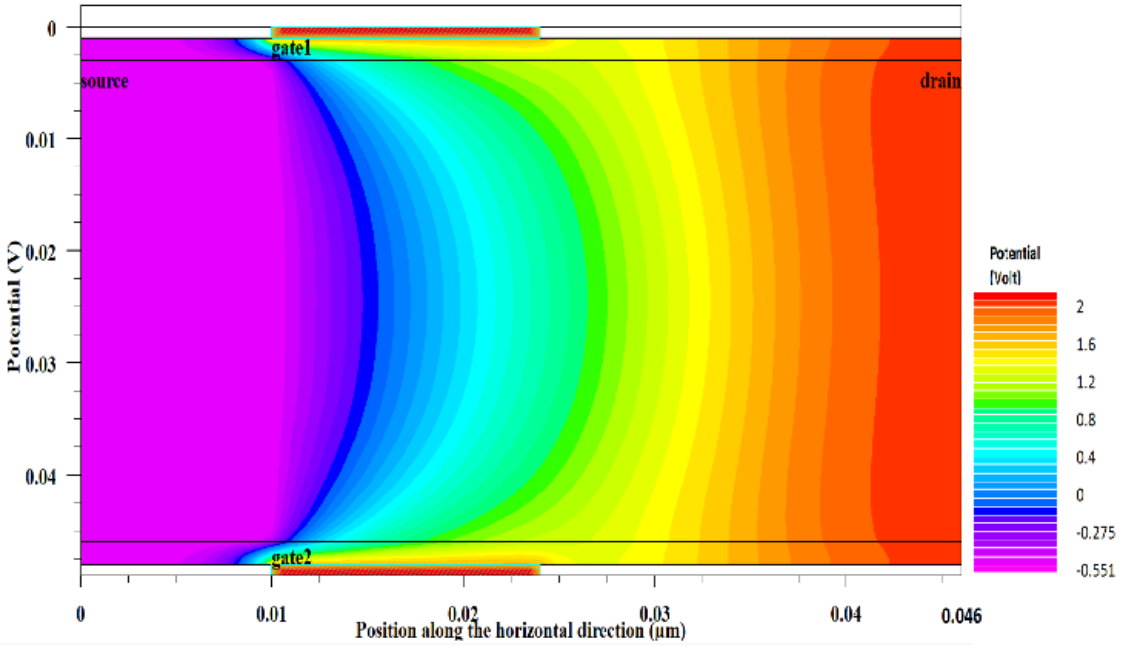
Attempts are made for Analytical modelling and simulation based validation studies of the proposed device structures. The simulation results along with visual graphical plots of potential profiles, electric field, electron current, hole current, total current etc. for different gate lengths of the structure are depicted in this section.

3.4.1. Potential Distribution

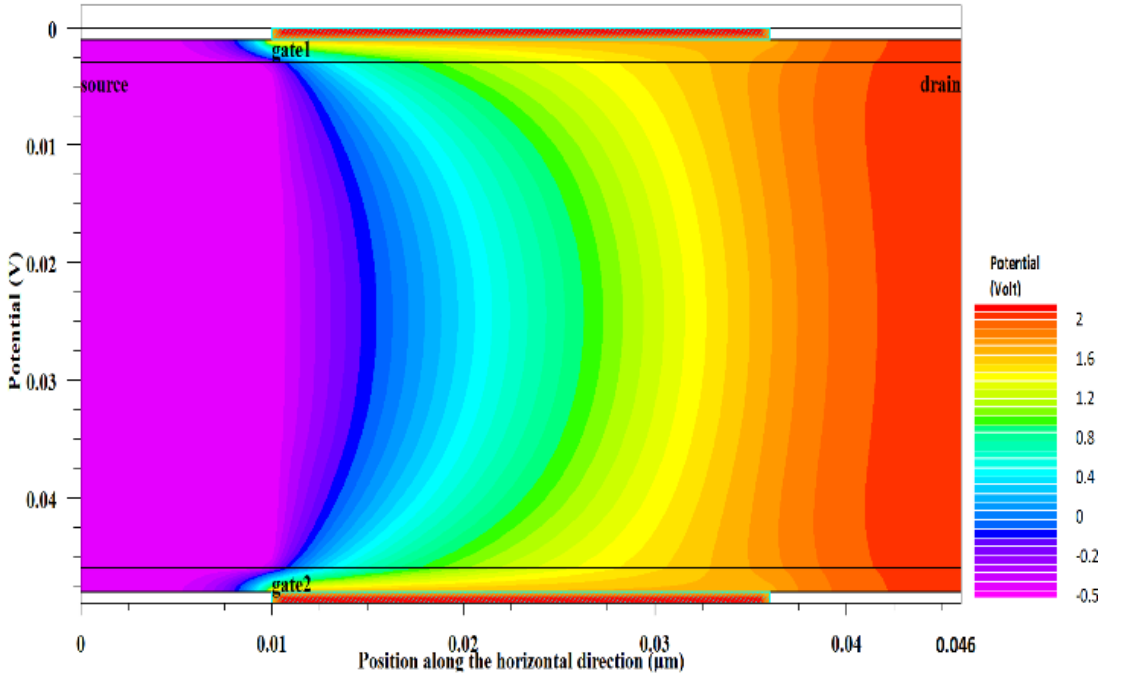
The potential distribution for different gate lengths have been shown in Fig3.2. For gate length 7nm depicted in Fig3.2.(a) the variation of potential along the vertical dimension at any vertical line is almost nil whereas for gate length of 14nm and 24nm as shown in Fig3.2.(b) and Fig3.2.(c) the potential varies in vertical dimension which is clear from the curvature of the distributions. So it signifies that the 7nm structure exhibits negligible ambipolarity and also is more stable.



(a)



(b)

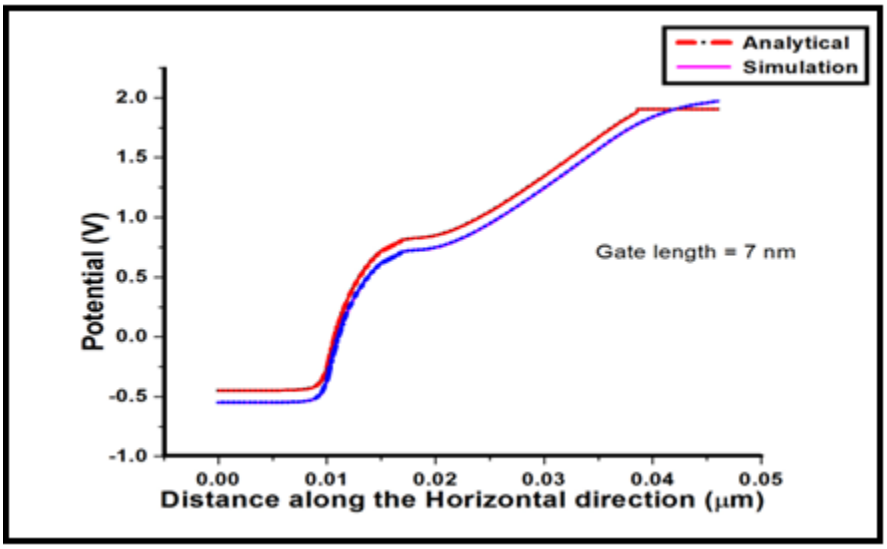


(c)

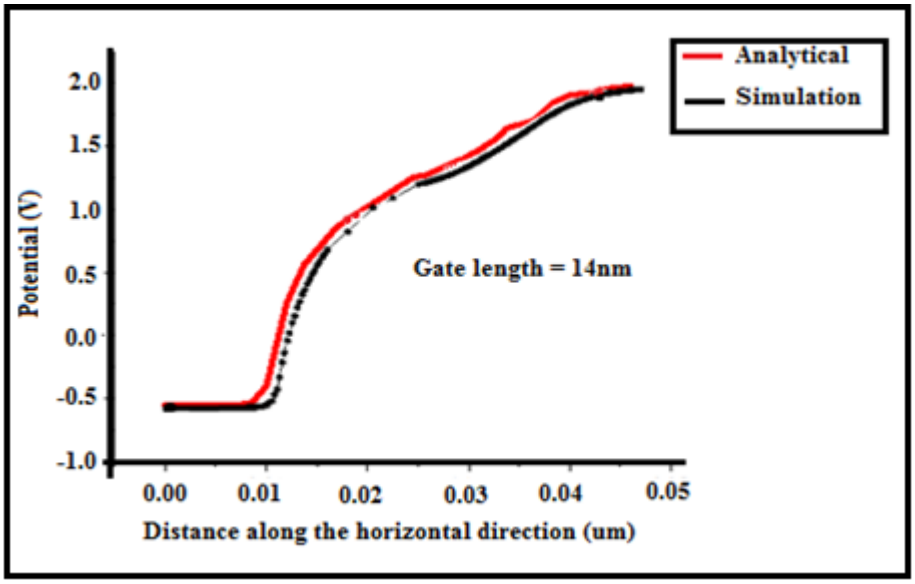
Fig3.2. The Potential distribution for different gate lengths (a) 7nm, (b) 14nm , (c) 24nm.

Comparison between simulated results of surface potential along device length for 7nm, 14nm and 24nm gate length PNPN-DG TFET and the corresponding analytical models have been plotted in Fig.3.3 It is manifested in the figures that the two outcomes are congruent.

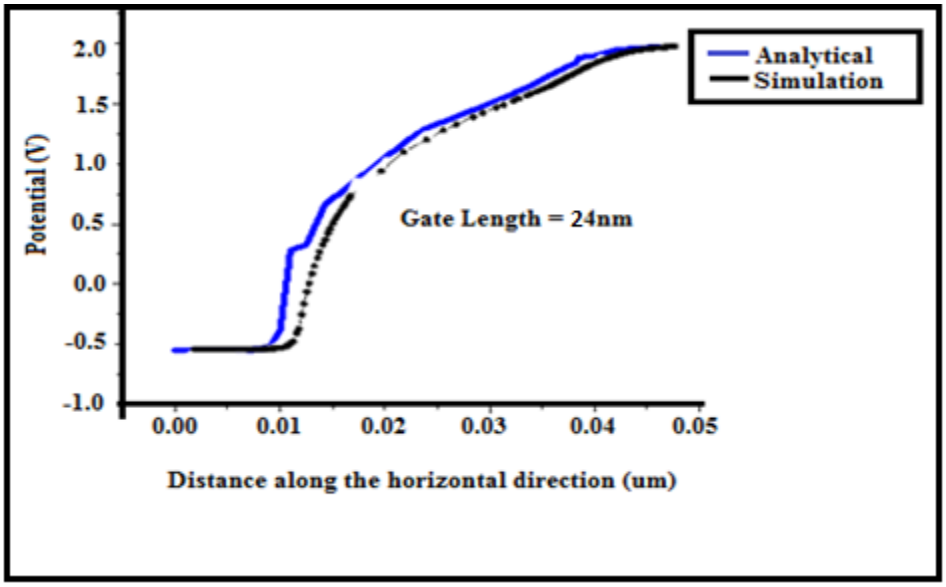
Fig3.4. exhibits the surface potential distribution along the length of the device for three different gate lengths of 7nm, 14nm and 24nm.



(a)



(b)



(C)

Fig.3.3 Comparison of analytical result of the surface potential distribution and simulation outcome for (a)7nm, (b) 14nm and (c) 24nm gate length.

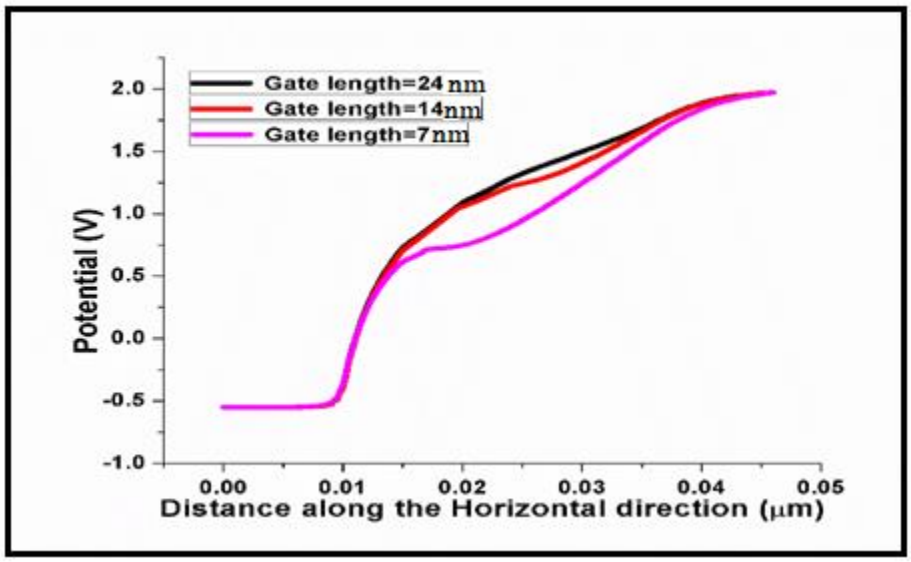
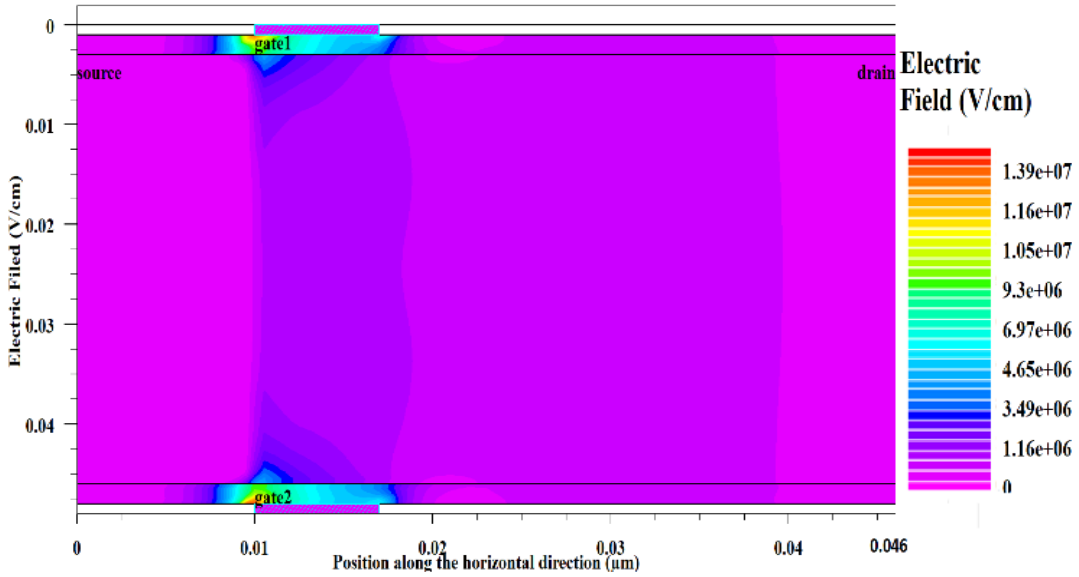


Fig3.4. Simulation based results of surface potential distribution for 7nm, 14nm and 24nm gate lengths.

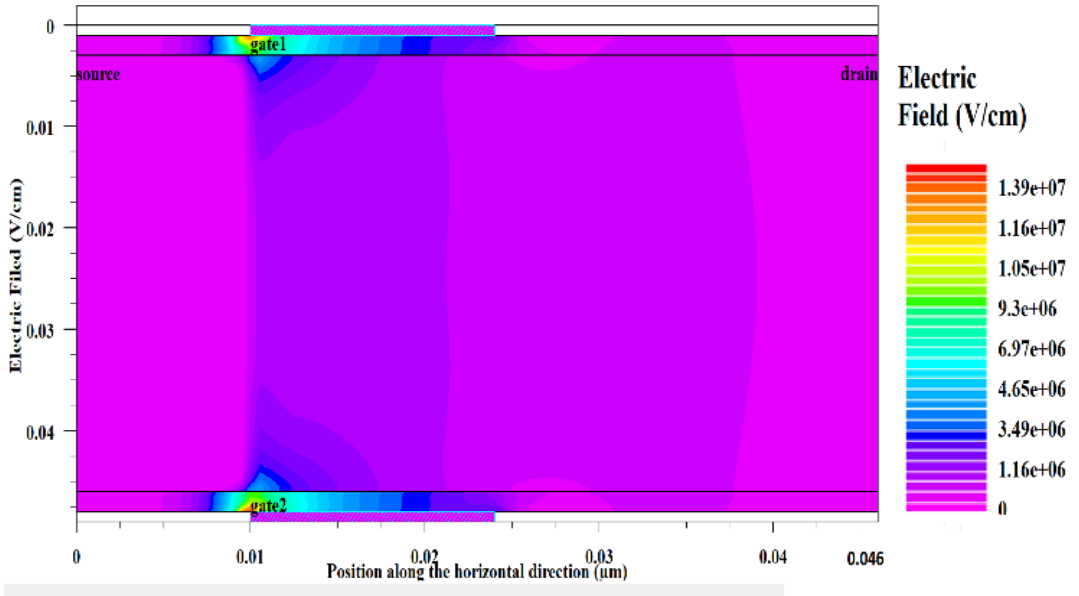
3.4.2 Electric Field Distribution

The electric field distribution profiles for different gate lengths have been illustrated in Fig3.5. For 14nm and 24nm gate length shown in Fig3.5(b) and Fig3.5(c) the electric field is non uniform at the drain side which is evident from the distribution curvature. Along with that two symmetrical zero electric field regions are formed towards the drain side of the channel for these

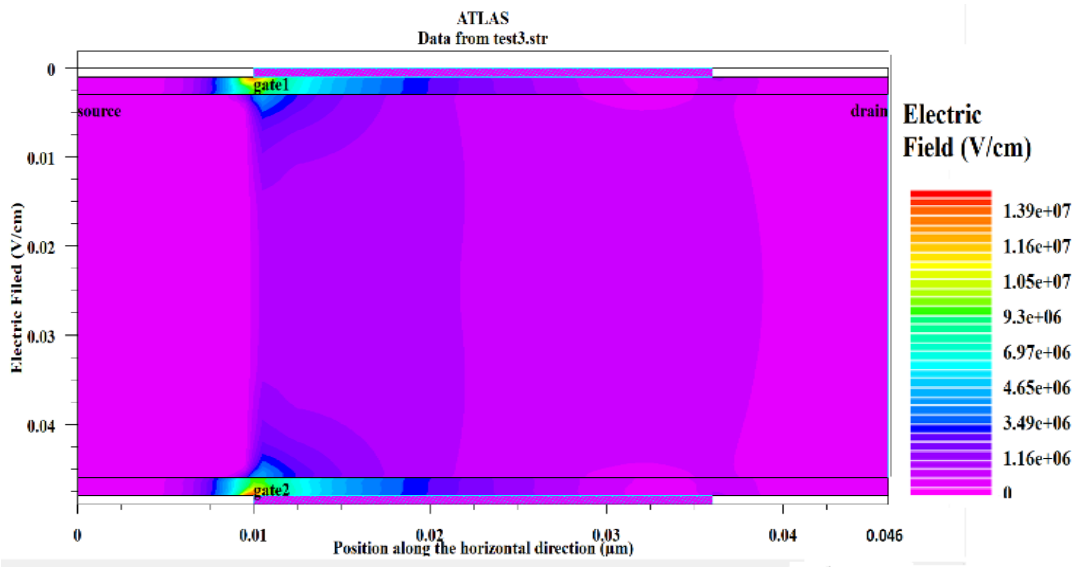
two cases. Considering Fig3.5(a) 7nm gate length structure it is visible that the electric field is uniform at the drain side and the zero field regions are almost absent.



(a)



(b)



(c)

Fig3.5. Electric field distribution profile for gate length (a) 7nm, (b) 14nm and (c) 24nm.

3.4.3 Conduction and Valence Band Energy

The comparison of conduction and valence band energy for the structures with three different gate lengths is illustrated in Fig3.6. It is evident from the graph that the tunnelling is almost similar for the three cases but 7nm gate length structure exhibits reverse band bending at channel drain junction side which manifests the cause of reduced ambipolar conduction for the same. Also it is evident that valence and conduction bands are getting parallel to each other along the drain region which negates the further possibility of ambipolar conduction.

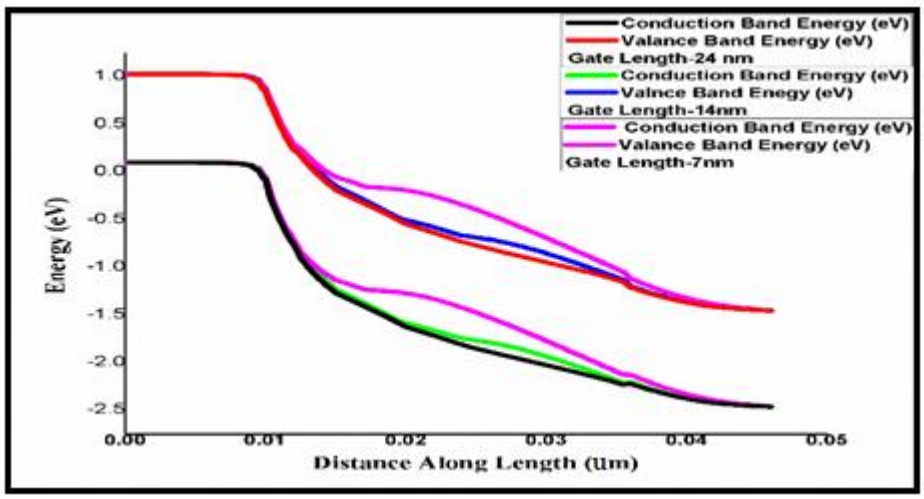


Fig3.6. Comparison of valence and conduction band energy for 7nm, 14nm and 24nm gate lengths.

3.4.4 Electric Field

The electric field along the length of the PNPN-DG TFET for 7nm, 14nm and 24nm gate lengths have been depicted in Fig3.7. The high electric field at the source channel junction explains the tunnelling phenomenon whereas the increase of electric field at the channel drain junction demonstrates the fact that the electrons from drain side cannot tunnel to the channel i.e. in reverse direction. This in turn helps to reduce the ambipolarity of the device.

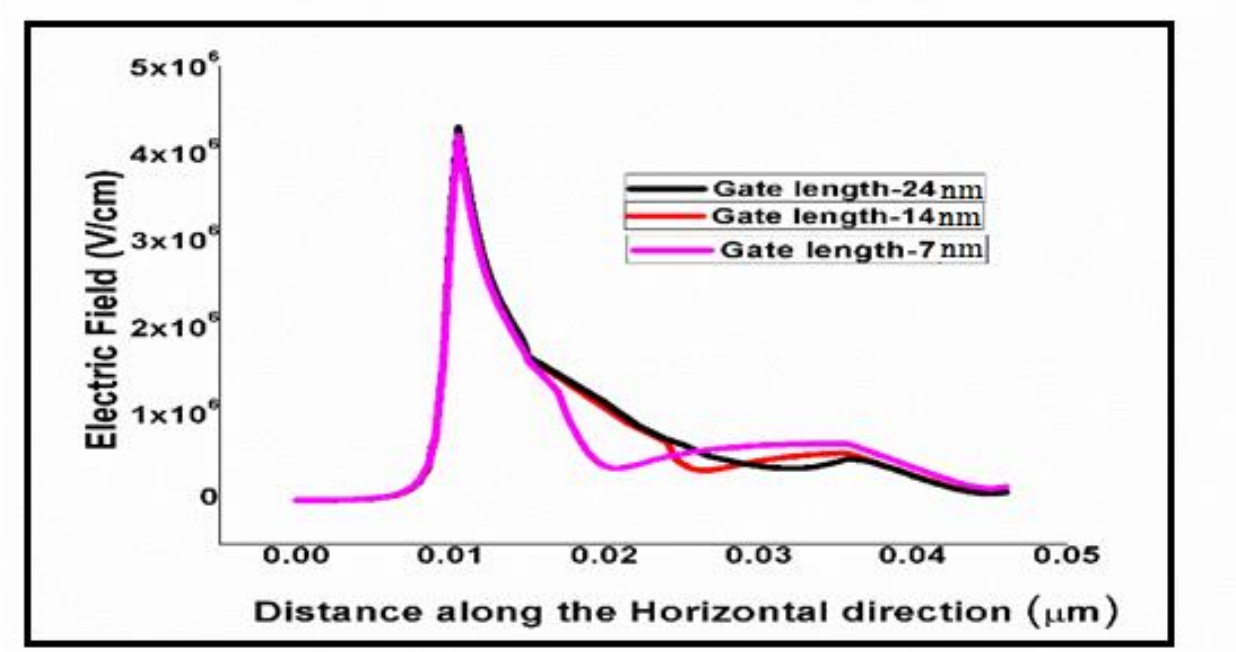


Fig3.7. Electric field along the length of PNPN-DG TFET for 7nm, 14nm and 24nm gate lengths.

3.4.5 Band to Band Tunnelling Rate

Comparison of BTBT tunnelling rate for PNPN-DG TFET of three different gate lengths 7nm, 14nm and 24nm have been illustrated in Fig3.8. The curves of 14nm and 24nm have been completely overlapped showing the same rate of band to band tunnelling whereas the 7nm gate length curve shows better tunnelling rate to some extent at the source channel junction. This explains the reason behind better performance of 7nm gate length structure that manifests best I_{on}/I_{off} amongst the three.

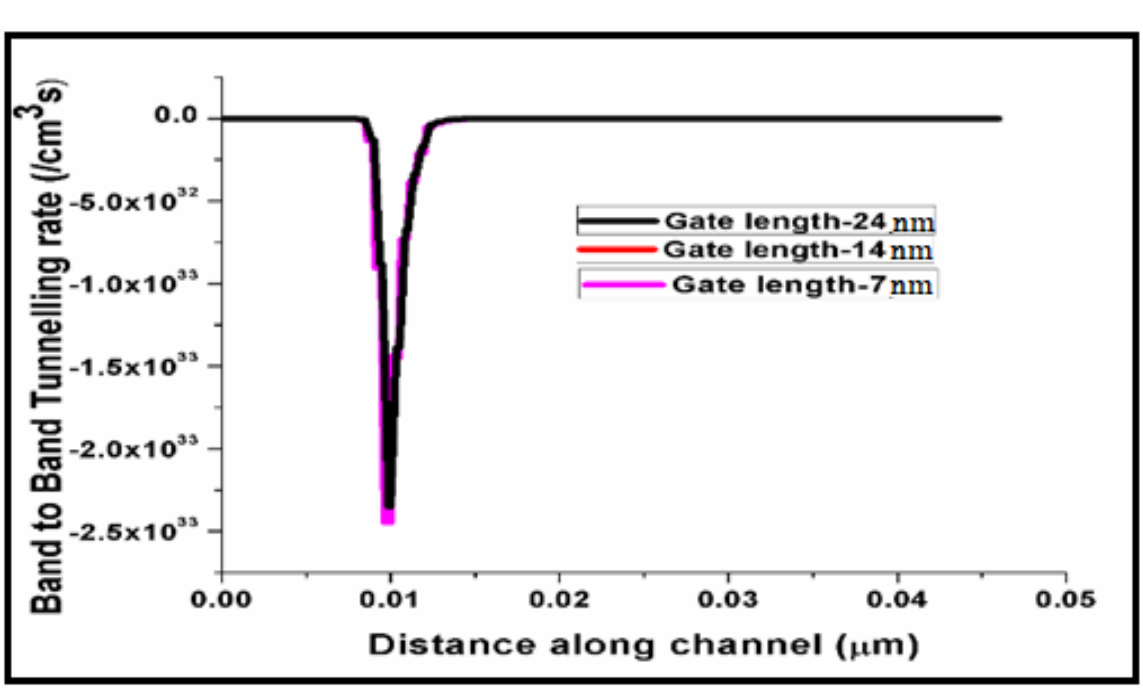


Fig3.8. BTBT tunnelling rate along the channel length of PNPN-DG TFET for 7nm, 14nm and 24nm gate lengths.

3.4.6 Transfer Characteristics

The transfer characteristics of PNPN-DG TFET for three different gate lengths of 7nm, 14nm and 24nm have been demonstrated in Fig3.9. All the structures considering three gate length variations show almost similar ON current which is depicted in the Fig3.9 but the structure with smallest gate length of 7nm exhibits OFF current of the order of 10^{-16} to 10^{-17}. It elucidates that the smaller gate length enhances the performance of the device and hence 7nm structure is the best amongst the three considered in this work. Also it is evident from the transfer characteristics that this structure is suitable for low power applications as it displays negligible ambipolar conduction.

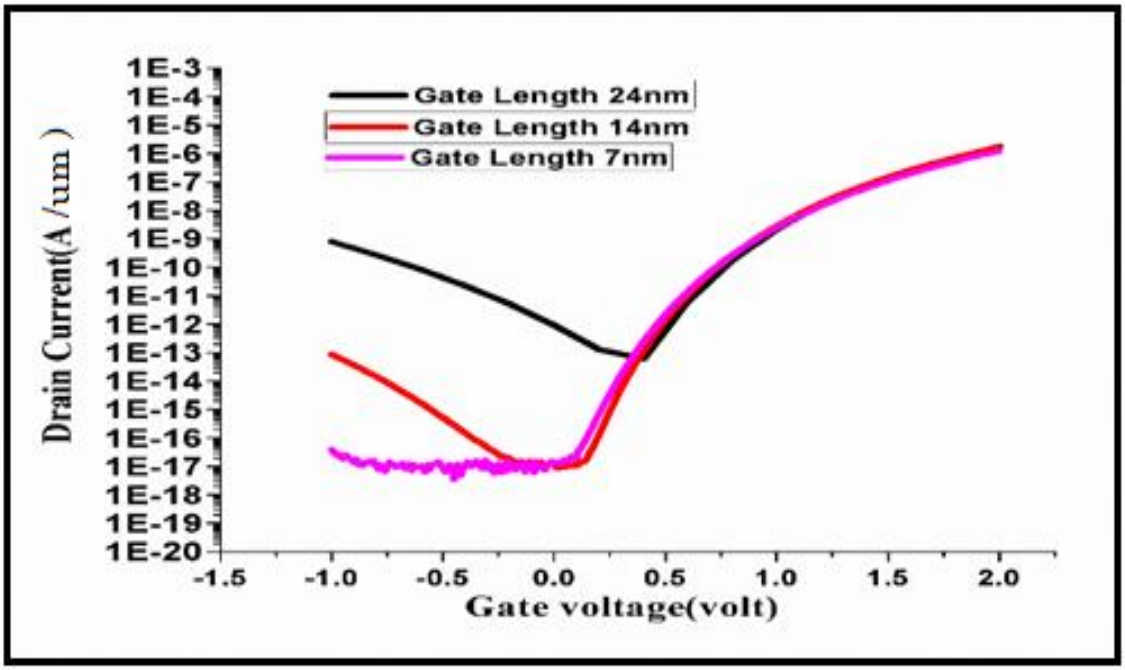


Fig3.9. Transfer Characteristics of PNPN-DG TFET for 7nm, 14nm and 24nm gate lengths.

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Chapter 4

Gate Centric Extended Source Nano SOI TFET

4.1 Introduction to the proposed work

Tunnel Field Effect Transistors are promising devices for future that can supersede MOSFET [1]-[4] devices in terms of device performance and overcome the limitations posed by MOSFETs. TFET devices [5]-[8] can be modified achieve low power applications [9]-[12]. Also TFET devices fabrication can be integrated with CMOS process technology and therefore similar to MOSFET fabrication. Conventional TFET devices exhibit low ON current which can be improved by modifying the structures, device dimension, doping concentration etc. Si based TFET structures are advantageous over other new material [13]-[17] variations as they are consistent and can be integrated with CMOS processes. Thus novel TFET structures are developed in order to increase ON current of the device by enhancing area of tunneling.

In the proposed work a trench gate SOI structure has been suggested along with source extension [18]-[19] and intrinsic region at the lower portion of drain that works as LDD. The source extension increases tunneling area incorporating line tunneling along with point tunneling due to source gate overlap. Also the intrinsic region at the lower left portion of drain increases effective channel length. Hence the possibility of source depletion region to overlap with drain reduces and eventually results into greater ON current for the device. The lower left portion of the drain mirrors the extended source region in opposite direction with low doping concentration to avoid the depletion region of both source and drain to overlap. This overlap in low dimensional device may cause SCE like DIBL and to avoid the same such specific region variation has been considered. The gate length of the proposed structure has been varied and output characteristics have been examined by performing simulation using Silvaco, Atlas. Simulations are performed considering both with quantum and without quantum effects and a comparative study of the both has been presented in this work.

Source and gate overlap region creates modification in the understanding of tunneling at source and channel junction. The area covered includes line tunneling as well as point tunneling [20]-[21] at the mentioned interface.

When quantum effects [22] are considered in device operation, the conduction and valence energy bands no more remain continuous and become discrete spectrum of energy. Therefore tunneling will only be possible between the first energy states available for electrons and holes.

This results into increase in tunneling width that causes reduction in BTBT probability along with reduction in ON current.

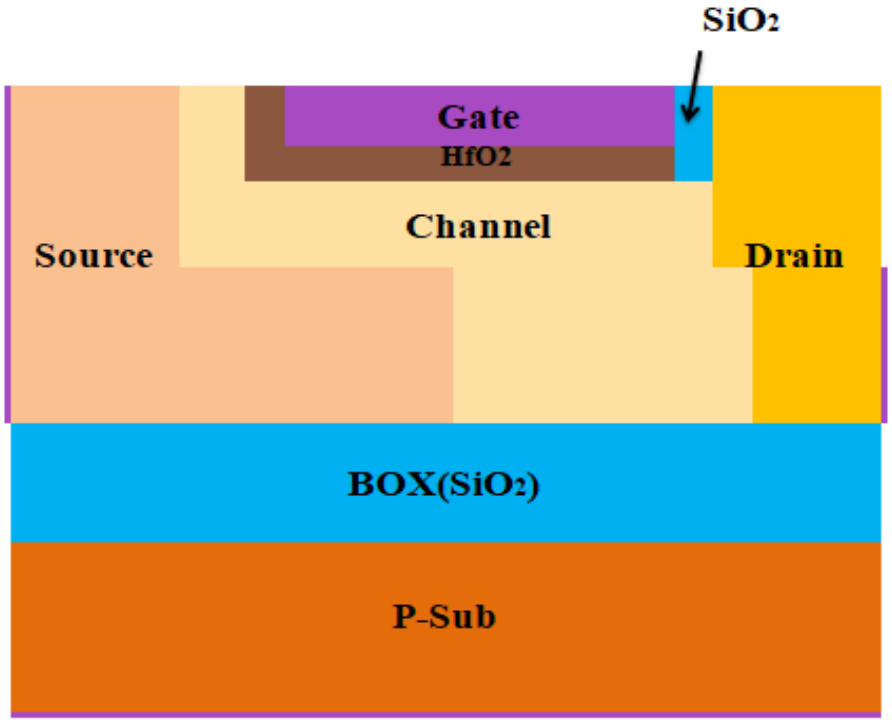


Fig4.1: Schematic of Gate Centric Extended Source SOI TFET

In this chapter section wise the work is described in the following manner. In the next section the detail structural description along with device parameters are provided. In the following section after this, simulation setup and the models used for simulations have been described. A comparative investigation of the outcome considering quantum and without quantum are presented in the next segment of this chapter followed by the conclusion that has been achieved from the results.

4.2 Device Structure, Parameters and Fabrication Steps

An SOI TFET precisely Gate Centric Extended Source SOI TFET structure has been considered in this chapter. The proposed structure has an extended source part which overlaps under the trench gate. This expansion of part of source is up to the middle position of gate. Drain on the other hand has an intrinsic part at the lower left portion that mirrors the extended part of source in opposite direction. Channel region is intrinsic and the effective channel length increases due to

the LDD at the lower left corner. Two different oxides namely HfO_2 and SiO_2 have been used as gate dielectric. As the proposed structure has a trench gate therefore the dielectric covers three sides of gate. SiO_2 is used at the left side as well as underneath the gate whereas HfO_2 is used at the right side on gate only. The source along with its extended portion is of P+ type with doping concentration of $10^{20}cm^{-3}$ whereas drain doping is of N type with concentration of $10^{17}cm^{-3}$. The channel region as well as the lower left part of drain is kept intrinsic ($10^{12}cm^{-3}$). A P type substrate below the buried oxide (SiO2) layer is considered for the proposed SOI structure in order to ease the process of fabrication as well as to avail other advantages offered by SOI such as less parasitic capacitance, less leakage current, more firm and stable structure. The work function of gate of the device has been considered as 4.85eV.

The device has three variations in gate length specifically 10nm, 7nm and 5nm. The regional dimensions are varied according to the gate length and the details of structural doping concentration are specified in the following Table 4.1.

Region	**Doping Type**	**Doping Concentration (cm^{-3})**
Source	P+	10^{20}
Extended Source	P+	10^{20}
Channel	i	10^{12}
Drain	N	10^{17}
LDD	i	10^{12}

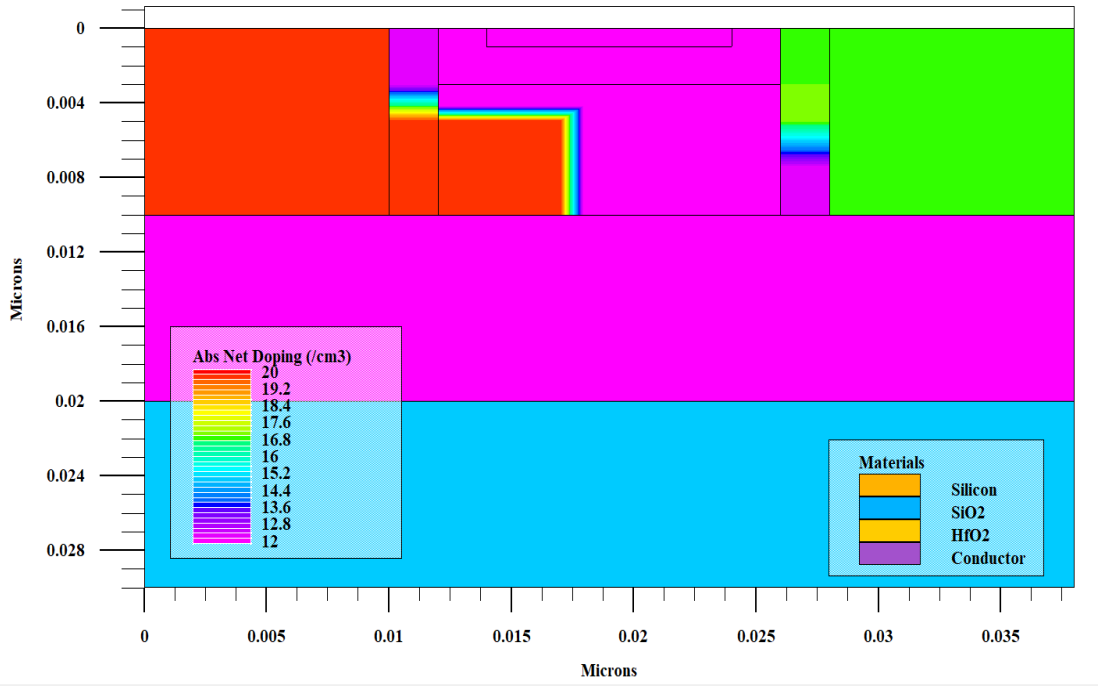
Table 4.1: Details of doping type and concentration for different regions of the structure.

For 10nm gate length source region has a dimension of 12nmX10nm with an extended part of area 7nmX5nm. The drain has a low doped intrinsic segment at the lower left part with dimension of 2nmX5nm whereas the upper part of this segment has higher doping concentration and dimension same as the lower one. The rest of the drain has a dimension of 10nmX10nm. Channel starts from the left side of trench gate, goes underneath the gate till the low doped intrinsic drain segment. Gate oxide SiO_2 is 2nm thick and has a dimension of 2nmX2nm at the left part of gate and 10nmX2nm under the gate. HfO_2 on the other hand is present at the right of

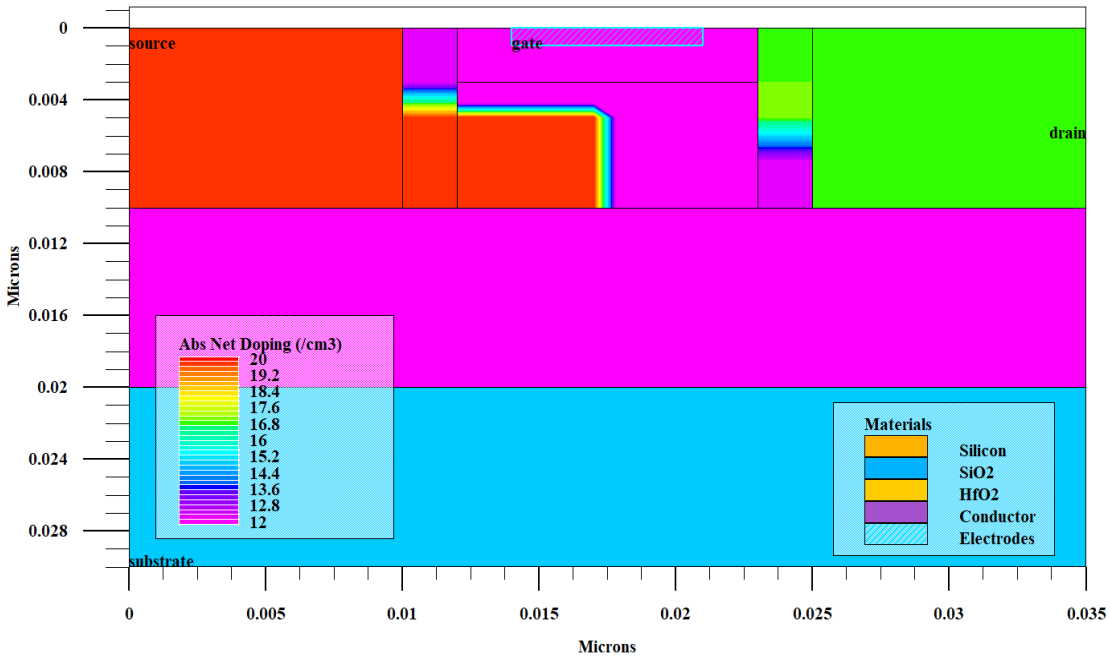
gate having dimension of 2nmX2nm.The trench gate is 1nm deep and has a variation in length of 10nm, 7nm and 5nm. The objective of this gate length variation is to investigate the suitable gate length for such small dimensional device structure. The buried oxide layer underneath the device has a length similar to device length and a depth of 10nm. In addition, the P substrate below BOX also has a length of device length along with a 10nm depth. Total device length is varied in accordance with gate length and is described in the table 4.2 below:

Gate length (nm)	Device length(nm)
10	38
7	35
5	33

Table 4.2: Total device length for different gate length of the structure.



(a)



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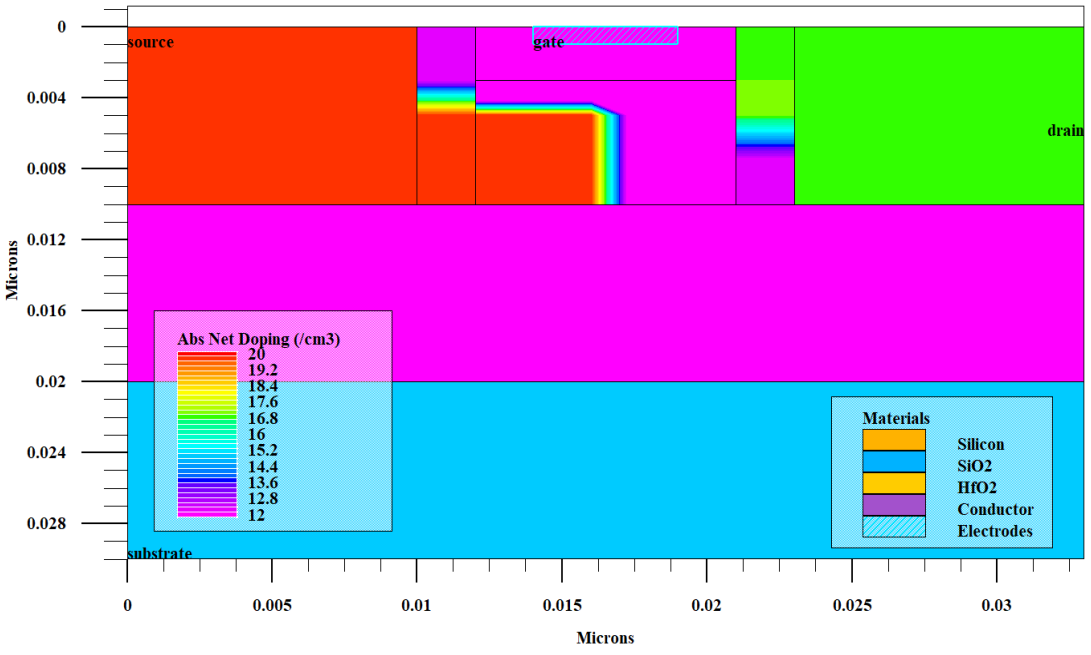


(c)

Fig4.2: Absolute net doping concentration of GCES SOI TFET for (a)10nm, (b)7nm and (c)5nm gate lengths.

Fabrication of the proposed device requires growing the structure layer by layer on top of silicon substrate. SiO_2 (BOX) layer can be grown on P type Si substrate by the method of oxidation. An intrinsic layer of Si is deposited on top of it. This layer is doped (left side P type for source and right side N type for drain) by the process of proper masking according to specific regions followed by diffusion of dopants. The same procedures of Si deposition, masking and diffusion could be carried out in accordance with specific region definition that would work as source, channel and drain. The channel region is then etched by photolithographic process and oxides (HfO2 and SiO2) are deposited in the etched area. The oxide is then etched according to its thickness required and gate metal is deposited in the etched area forming a trench gate structure. Source and drain contacts are at the two sides of the device along with one body contact below the substrate. Gate contact is taken from the top of the device on the gate metal. The fabrication steps are briefly illustrated in the Fig4.3.

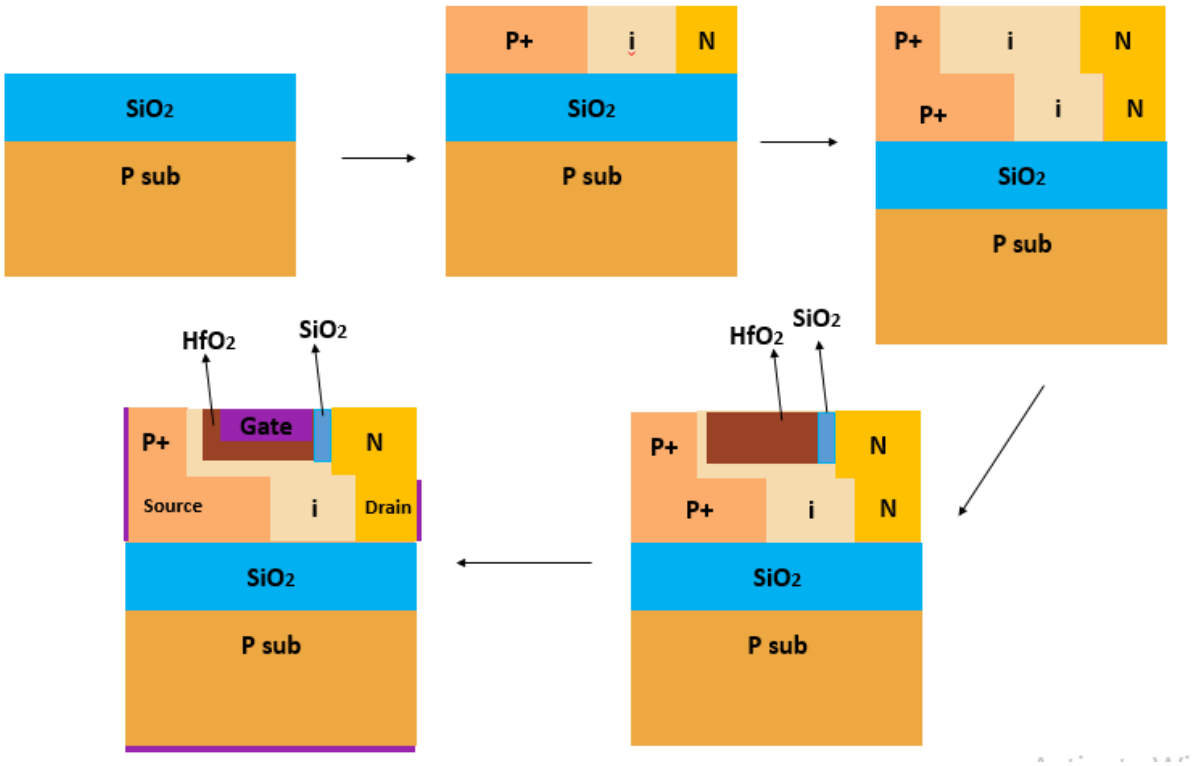


Fig4.3: Fabrication steps of the proposed GCES SOI TFET structure

4.3 Simulation Setup and Model Descriptions

Simulation is performed considering quantum mechanical description along with quantization in subband transition using self-consistent Schrodinger Poisson model and classical model simulation that includes non-local BTBT, bandgap narrowing model, Fermi Dirac statistics, Auger and SRH (Shockley Read Hall) recombination models . Silvaco, Atlas has been used for performing this simulation operation where inside the bandgap, electric field is considered as non-uniform. Carrier concentration is determined considering Fermi Dirac statistics whereas Auger and SRH (Shockley Read Hall) recombination models are accounted for determining carrier energy. Carrier generation rate is deduced by accounting Non local BTBT model.

4.4 Analytical Modeling

The rate of generation can be calculated using Kane's model for known tunneling distance and is given by

$$G = A\frac{E_G^{D-1/2}}{q^D l^D}\exp(-Bq\sqrt{E_G}l) \tag{4.1}$$

where A,B and D are Kane's Model parameters that are material independent, q and E_G are the elementary charge and band gap respectively.

Integrating this generation rate over the entire volume we get the total current as

$$I = q\int GdV \tag{4.2}$$

4.4.1 Point Tunneling

Now for the proposed structure we assume the following boundary conditions:

Also the charge density $\rho = 0$ at the gate oxide and intrinsic semiconductor. Hence the Poisson's equation $\nabla^2\psi = -\frac{\rho}{\varepsilon_s}$ reduces to Laplace equation $\nabla^2\psi = 0$

For an applied gate voltage we have $\psi_g = V_{gs} - V_{FB}$ and we considered $\psi_s = 0$ where V_{FB} is Flat band voltage. We assume the semiconductor extending to infinity by taking x>0 and z>0 and

hence potential for pont tunneling can easily be calculated using polar coordinates as it is evident from the curved electric field lines from source edge to gate depcted in Fig4.4.

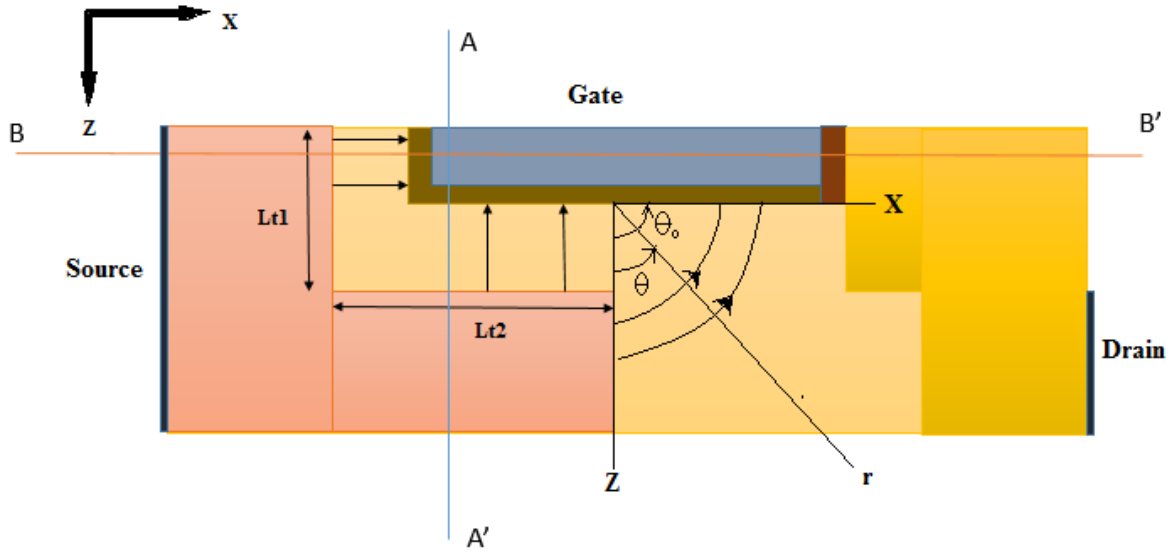


Fig4.4 Line and Point tunneling

Incorporating polar coordinates we assume x=rsinθ and z=rcosθ where θ ranges from 0 to $\pi/2$ (evident from Fig4.4)

Hence $\psi(x,z)=\psi_g(\frac{2}{\pi}\theta)$ and tunneling path length can be calculated along the arc of electric field lines $l=r\theta_0$ where angle between equipotential lines $\theta_0=\frac{\pi}{2}(\frac{E_g}{q})\frac{1}{\psi_g}$ as $\frac{E_g}{q}$ is the potential difference.

Now the total current for point tunneling can be calculated by integrating the generation rate from Kane's model over the entire tunneling area depicted in Fig4.3 and the same is given by

$$I=qW\int_{r_0}^{\infty}\int_{\theta_0}^{\cos^{-1}\frac{t_{ox}'}{r}}G(r)rd\theta dr \qquad (4.3)$$

or,

$$I = qW\int_{r_0}^{\infty}\int_{\theta_0}^{\cos^{-1}\frac{t_{ox}^{'}}{r}} A\frac{E_G^{D-1/2}}{q^D(r\theta_0)^D}\exp(-Bq\sqrt{E_g}r\theta_0)rd\theta dr \qquad (4.4)$$

Where $r_0 = t_{ox}^{'}/\cos\theta_0$,

$G(r) = A\frac{E_G^{D-1/2}}{q^D(r\theta_0)^D}\exp(-Bq\sqrt{E_g}r\theta_0)$ and equivalent thickness of semiconductor

$t_{ox}^{'} = t_{ox}(\frac{\varepsilon_s}{\varepsilon_{ox}})$.

Integrating (4.4) over θ as polar coordinate is considered we get

$$I = qW\int_{r_0}^{\infty} A\frac{E_G^{D-1/2}}{q^D(r\theta_0)^D}\exp(-Bq\sqrt{E_g}r\theta_0)\,\theta\Big|_{\theta_0}^{\cos^{-1}\frac{t_{ox}^{'}}{r}} rdr$$

$$I = qW\int_{r_0}^{\infty} A\frac{E_G^{D-1/2}}{q^D(r\theta_0)^D}\exp(-Bq\sqrt{E_g}r\theta_0)(\cos^{-1}\frac{t_{ox}^{'}}{r}-\theta_0)rdr$$

$$I = W\int_{r_0}^{\infty} A\frac{E_G^{D-1/2}}{q^{D-1}(r\theta_0)^{D-1}}\exp(-Bq\sqrt{E_g}r\theta_0)(\cos^{-1}\frac{t_{ox}^{'}}{r}-\theta_0)dr$$

$$I = AW\int_{r_0}^{\infty}\frac{E_G^{D-1/2}\,e^{(-Bq\sqrt{E_g}r\theta_0)}}{q^{D-1}r^{D-1}{\theta_0}^D}(\cos^{-1}\frac{t_{ox}^{'}}{r}-\theta_0)dr \qquad (4.5)$$

Now first order Taylor expansion is performed to solve this integration around $r = r_0$ and we have

$$f(r) = f(r_0) + f'(r_0)(r-r_0) \qquad (4.6)$$

Assume

$$f(r) = (\cos^{-1}\frac{t_{ox}^{'}}{r}-\theta_0)\frac{E_G^{D-1/2}\,e^{(-Bq\sqrt{E_g}r\theta_0)}}{q^{D-1}r^{D-1}{\theta_0}^D} \qquad (4.7)$$

and

$$f(r_0) = (\cos^{-1}\frac{t_{ox}^{'}}{r_0} - \theta_0)\frac{E_G^{D-1/2}\, e^{(-Bq\sqrt{E_g}r_0\theta_0)}}{q^{D-1}r_0^{D-1}\theta_0^{D}} \tag{4.8}$$

Differentiating $f(r_0)$ with respect to r_0 we get

$$f'(r_0) = \begin{bmatrix} -\frac{1}{\sqrt{1-\left(\frac{t_{ox}^{'}}{r_0}\right)^2}}\frac{E_G^{D-1/2}\, e^{(-Bq\sqrt{E_g}r_0\theta_0)}}{q^{D-1}r_0^{D-1}\theta_0^{D}} \\ +(\cos^{-1}\frac{t_{ox}^{'}}{r_0} - \theta_0)\frac{e^{(-Bq\sqrt{E_g}r_0\theta_0)}(-Bq\sqrt{E_g}\theta_0)E_G^{D-1/2}}{q^{D-1}r_0^{D-1}\theta_0^{D}} \\ +(\cos^{-1}\frac{t_{ox}^{'}}{r_0} - \theta_0)\frac{e^{(-Bq\sqrt{E_g}r_0\theta_0)}E_G^{D-1/2}}{q^{D-1}r_0^{D}\theta_0^{D}}(1-D) \end{bmatrix} \tag{4.9}$$

Now multiplying the same with $(r - r_0)$ we get

$$(r-r_0)\times f'(r_0) = \begin{bmatrix} -\frac{1}{\sqrt{1-\left(\frac{t_{ox}^{'}}{r_0}\right)^2}}\frac{E_G^{D-1/2}\, e^{(-Bq\sqrt{E_g}r_0\theta_0)}}{q^{D-1}r_0^{D-1}\theta_0^{D}} \\ +(\cos^{-1}\frac{t_{ox}^{'}}{r_0} - \theta_0)\frac{e^{(-Bq\sqrt{E_g}r_0\theta_0)}(-Bq\sqrt{E_g}\theta_0)E_G^{D-1/2}}{q^{D-1}r_0^{D-1}\theta_0^{D}} \\ +(\cos^{-1}\frac{t_{ox}^{'}}{r_0} - \theta_0)\frac{e^{(-Bq\sqrt{E_g}r_0\theta_0)}E_G^{D-1/2}}{q^{D-1}r_0^{D}\theta_0^{D}}(1-D) \end{bmatrix} \times (r-r_0) \tag{4.10}$$

Putting the values of (4.7) and (4.10) in (4.6) we get

$$f(r)=\frac{WAE_G^{D-1/2}}{q^{D-1}r^{D-1}{\theta_0}^D}\left[\begin{array}{l}(\cos^{-1}\frac{t_{ox}^{'}}{r_0}-\theta_0)\,\mathrm{e}^{(-Bq\sqrt{E_g}r_0\theta_0)}\\ -\frac{1}{\sqrt{1-\left(\frac{t_{ox}^{'}}{r_0}\right)^2}}\mathrm{e}^{(-Bq\sqrt{E_g}r_0\theta_0)}(r-r_0)\\ +(\cos^{-1}\frac{t_{ox}^{'}}{r_0}-\theta_0)\,\mathrm{e}^{(-Bq\sqrt{E_g}r_0\theta_0)}(-Bq\sqrt{E_g}\theta_0)(r-r_0)\\ +(\cos^{-1}\frac{t_{ox}^{'}}{r_0}-\theta_0)\,\mathrm{e}^{(-Bq\sqrt{E_g}r_0\theta_0)}(r-r_0)\end{array}\right]$$

$$=\frac{WAE_G^{D-1/2}}{q^{D-1}r^{D-1}{\theta_0}^D}\left[\begin{array}{l}-\theta_0\,\mathrm{e}^{(-Bq\sqrt{E_g}r_0\theta_0)}-\frac{1}{\sqrt{1-\left(\frac{t_{ox}^{'}}{r_0}\right)^2}}(r-r_0)\,\mathrm{e}^{(-Bq\sqrt{E_g}r_0\theta_0)}\\ +\theta_0^2Bq\sqrt{E_g}(r-r_0)\,\mathrm{e}^{(-Bq\sqrt{E_g}r_0\theta_0)}-\theta_0(r-r_0)\,\mathrm{e}^{(-Bq\sqrt{E_g}r_0\theta_0)}\end{array}\right] \tag{4.11}$$

Here we have assumed $\cos\theta_0$=1 and therefore $\cos^{-1}\frac{t_{ox}^{'}}{r_0}$ is 0. Again this implies θ_0=0 and the equation for I reduces to

$$I\approx\frac{WAE_G^{D-1/2}}{q^{D-1}r^{D-1}{\theta_0}^D}\int_{r_0}^{\infty}\left[\frac{t_{ox}^{'}(r-r_0)\,\mathrm{e}^{(-Bq\sqrt{E_g}r_0\theta_0)}}{\sqrt{1-\left(\frac{t_{ox}^{'}}{r_0}\right)^2}\,r_0}dr\right] \tag{4.12}$$

The integration with respect to dr is solved and simplified as

$$I \approx \frac{WAE_G^{D-1/2}}{q^{D-1}r^{D-1}\theta_0{}^D} \frac{t_{ox}^{'} \mathrm{e}^{(-Bq\sqrt{E_g}r_0\theta_0)}}{\sqrt{1-\left(\frac{t_{ox}^{'}}{r_0}\right)^2 r_0}} (\frac{r}{2} - r_0)r \Bigg|_{r_0}^{\infty}$$

$$I \approx \frac{WAE_G^{D-3/2}t_{ox}^{'}}{q^{D-1}B^2} \frac{1}{\theta_0{}^{D+2}r^{D+1}} \mathrm{e}^{(-Bq\sqrt{E_g}r_0\theta_0)} \tag{4.13}$$

We know for small value of θ, sinθ ≈θ. Hence it can be written that

$$\cos\theta_0 = \sin(\frac{\pi}{2} - \theta_0)$$

r_0 can be approximated as the function of gate voltage which can be expressed as

$$r_0 = t_{ox}^{'} / \sin\left(\frac{\pi(q\psi_g - E_G)}{2q\psi_g}\right) = \sin\left(\frac{\pi}{2} - \frac{\pi E_G}{2q\psi_g}\right) \tag{4.14}$$

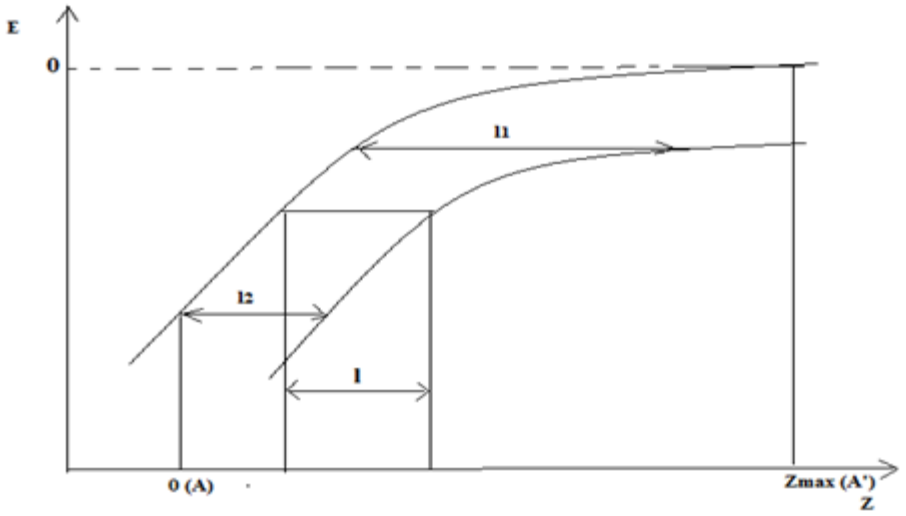
Hence $\theta_0 = \frac{\pi E_G}{2q\psi_g}$ and taking the value of D=2 as the default value the expression of the current due to point tunneling is found to be

$$I_p = W \frac{2A\sqrt{E_G}}{\pi q^3 B^2 t_{ox}^{'\,2}} \frac{q\psi_g}{E_G}\left(\frac{q\psi_g}{E_G} - 1\right)^2 e^{\frac{-Bq\sqrt{E_g}t_{ox}^{'}}{\left(\frac{q\psi_g}{E_G}-1\right)}} \tag{4.15}$$

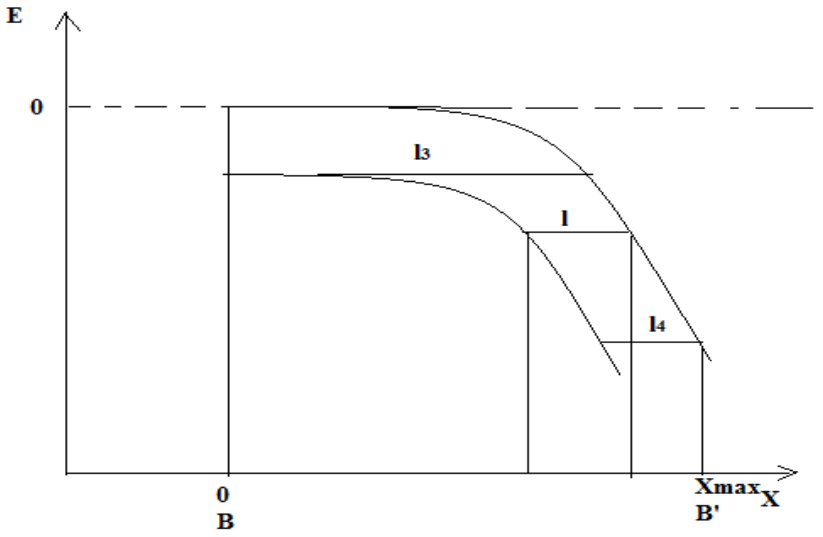
4.4.2 Line Tunneling

Line tunneling occurs at the area where gate and source overlap. As the gate is trench gate therefore line tunneling will occur in two directions along Lt1 and Lt2 shown in Fig 4.5.

Line tunneling along two cut lines AA' and BB' (Fig4.5) with the band diagrams are shown below:



(a)



(b)

Fig4.5: Line tunneling through the energy bands along cutline (a) AA' and (b) BB'.

From [20] the line tunneling current is calculated for the region L_{t1} and L_{t2} as the integration over total BTBT generation of charge which is given by

$$I_l = \frac{qWLA}{2}\left[\int_{l_1}^{l_2} P(l)dl + \int_{l_3}^{l_4} P(l)dl\right] \qquad (4.16)$$

where $P(l) = \frac{E_G^{D-1/2}}{q^D l^D} e^{(-Bq\sqrt{E_g}rl)}\left(1 - \frac{2E_G\varepsilon_s}{q^2 N_a}\frac{1}{l^2}\right)$ (4.17)

Here l is length of tunneling from l_1 to l_2 for L_{t2} and l_3 to l_4 for L_{t1}, L is the length of source covered by gate which is summation of L_{t1} and L_{t2} ($L=L_{t1}+L_{t1}$) as the trench gate covers source in two dimensions both vertically and horizontally. Doping concentration is defined by N_a.

Next it is assumed that variation of l have greater impact on the exponential terms over polynomial terns and value of D is taken to be 2 (default) along with V_{onset} as a function of gate voltage V_{gs} and $V_{onset} = V_{FB} + E_g$.

Current due to line tunneling is then approximated as

$$I_l \approx WLq^{1/2}\frac{A}{B}\frac{N_a}{2\varepsilon_s}\sqrt{\frac{1}{E_G\gamma}(V_{gs} - V_{onset})}\, e^{(-BqE_g\sqrt{2\varepsilon_s}/\sqrt{q^2N_a})+(Bq\sqrt{\frac{2E_G\varepsilon_s}{qN_a}\frac{1}{\gamma}})\sqrt{V_{gs}-V_{onset}}} \qquad (4.18)$$

where $V_{onset} = V_{FB} + \frac{E_G}{q}\left(1 + 2t_{ox}^{'}\sqrt{\frac{q^2N_a}{2E_g\varepsilon_s}}\right)$ and $\gamma = 1 + t_{ox}^{'}\sqrt{\frac{q^2N_a}{2E_g\varepsilon_s}}$

The total current can be calculated as the summation of point tunneling current (4.15) and line tunneling current (4.18) at the source side of the device that is given by

$$|I| = |I_p| + |I_l| \qquad (4.19)$$

4.5 Results and Discussions

In this section the outcome of the simulation considering classical behavior has been studied and the results in terms of transfer characteristics, band diagrams, electric field and potential along with contour diagrams are thoroughly investigated. Analytical current modelling which is performed in section 4.4 has also been validated based on the simulation result in this section. Quantum confinement has been taken into account and the outcomes of the same is compared with the classical behavior for different gate length variations. The results are examined and the

performance of the proposed structure has been examined based on the device parameters such as subthreshold slope, threshold voltage and ratio of ON and OFF current. The results are discussed in details below:

4.5.1 Optimum V_{DS}

The drain voltage of GCES SOI TFET has been varied for the gate length of 10nm. The subthreshold slopes are examined for three different V_{DS} values specifically 1V, 0.5V and 0.1V. The results found at different V_{DS} values are presented in the following Fig4.6. It is noticeable that 0.1V is optimum value for V_{DS} in this structure as it provides lowest SS.

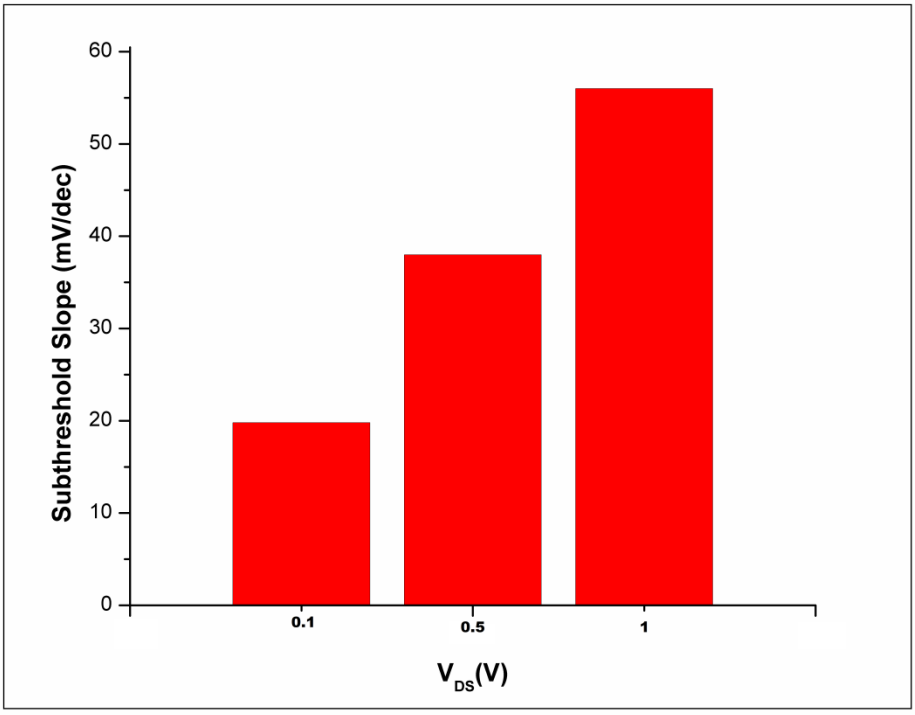


Fig 4.6: Variation of V_{DS} for 10nm gate length of GCES SOI TFET

4.5.2 Gate Centric Source Extension

The extension of source region is varied for 7nm gate length and compared for different device parameters such as threshold voltage and subthreshold slope. From the comparison explained in the Fig 4.7 it is evident that centre position (12-17nm) of gate length is optimum for source extension where both the threshold voltage and subthreshold slope are found to be suitable for

device operation unlike for the other two cases where either the SS is high or the threshold voltage requirement is high which is not desirable.

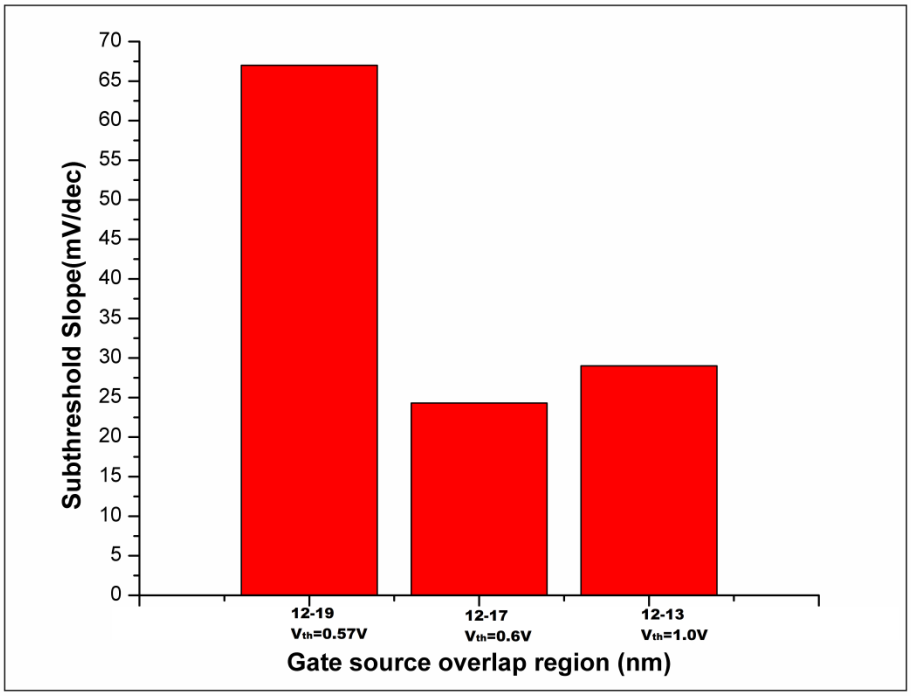


Fig 4.7: Variation of gate source overlap region for 7nm gate length of GCES SOI TFET

Thus we optimize the structure by taking V_{DS} as 0.1V and optimum source extension up to centre position of gate for all the gate lengths of 10nm, 7nm and 5nm respectively.

4.5.3 Position of Source and Drain Contact

Drain and source contact positions have been varied and it is observed that specifically for drain contact position variation there is a change in subthreshold slope but the overall ON and OFF current are found to be similar whereas variation of source contact position does not create much impact on the device parameters. The drain position is taken to be at the right side of vertical 5-10nm of height. The variations are shown in Fig 4.8 below.

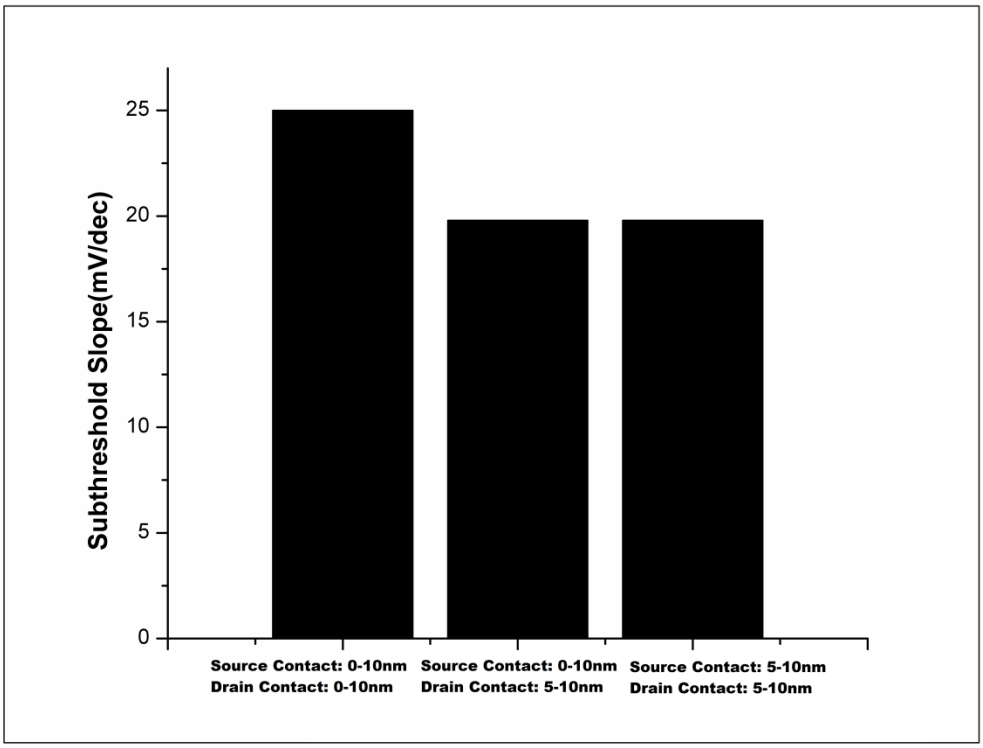


Table 4.8: Variation of drain and source contact position

4.5.4 Band Diagram

Band diagrams of GCES-SOI TFET for three different gate lengths such as 10nm, 7nm and 5nm has been illustrated in Fig4.9. The energy bands for each of the gate lengths are compared and it is evident from the graph that for 10nm gate length, tunneling is better at the source channel interface to some extent.

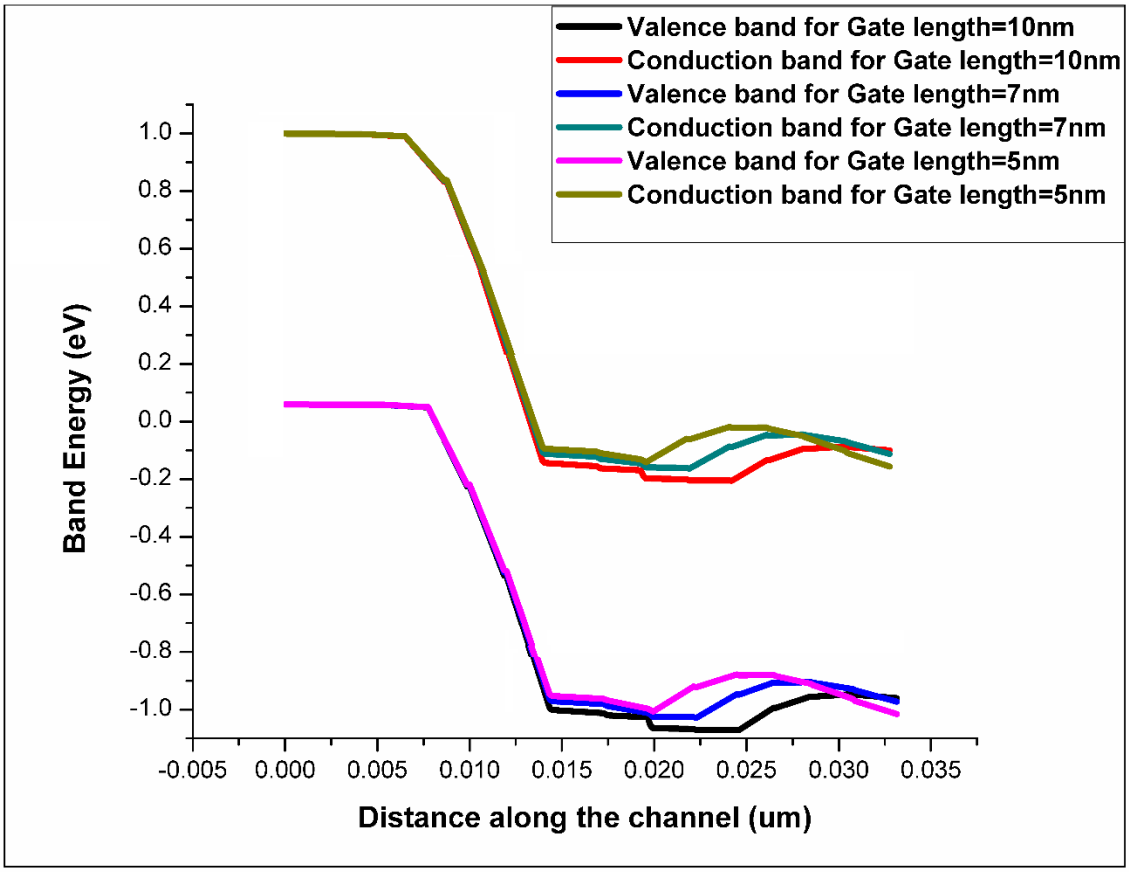


Fig4.9: Comparison of band diagrams of GCES SOI TFET for three different gate lengths of 10nm, 7nm and 5nm.

4.5.5 Electric Field

Electric field of GCES-SOI TFET has been illustrated in Fig4.10 for gate lengths 10nm, 7nm and 5nm. The cutline for electric field measurement has been taken at 5nm in vertical direction along the channel length of the device. It is evident from the graph that the electric field peak at the source channel interface for 10nm gate length is greater compared to 7nm and 5nm gate length. Also it is explicitly observable that the electric field peak regions in the curves are spread at the source channel interface due to extension of source region into channel that incorporates both line tunneling as well as point tunneling in the mentioned area.

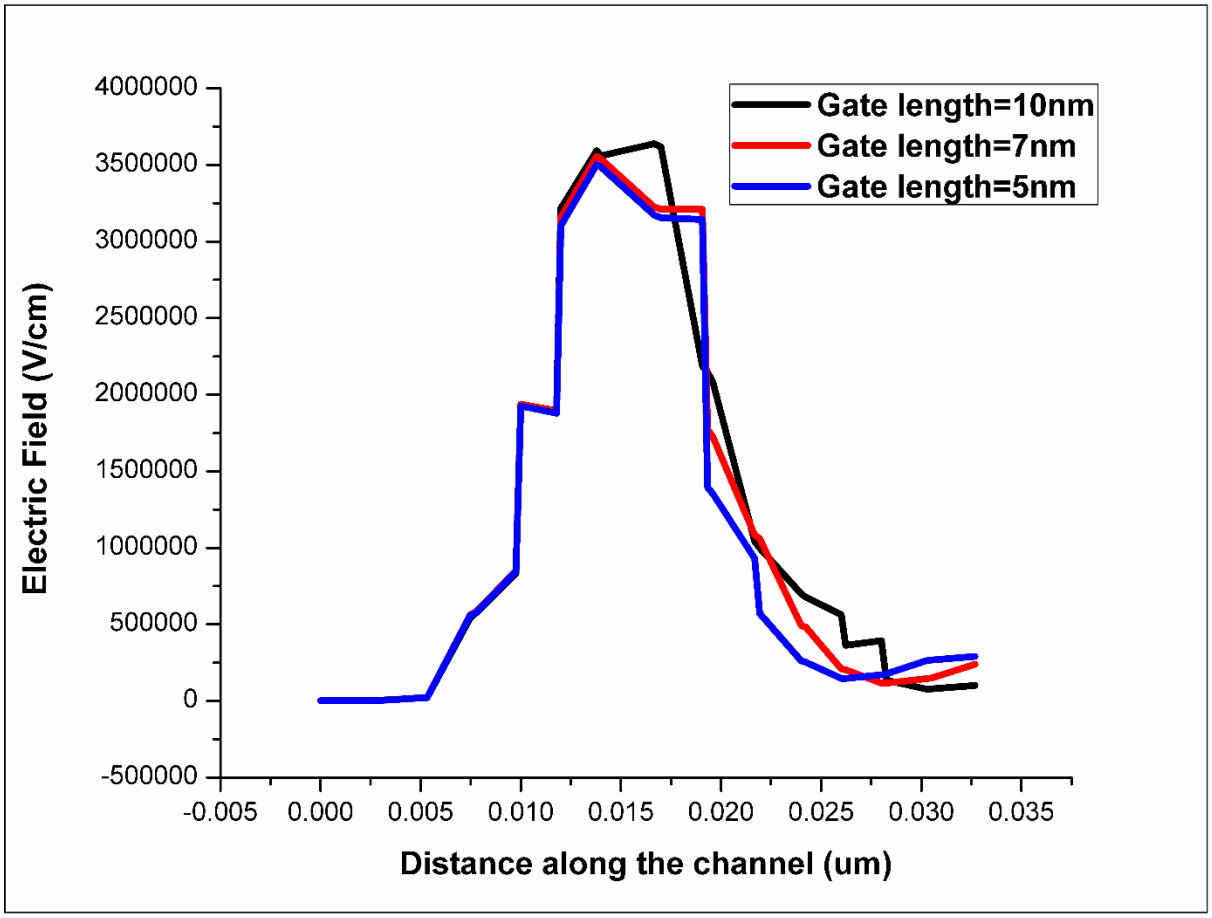


Fig4.10: Comparison of electric fields along the length of GCES-SOI TFET for three different gate lengths of 10nm, 7nm and 5nm.

4.5.6 Potential

Potential along the length of GCES-SOI TFET are compared for three different gate lengths of 10nm, 7nm and 5nm in Fig4.11. It is observable from the graph that potential for 10nm gate length structure is greater compared to 7nm and 5nm gate length structures. Potential has been measured along the cutline which has been taken at 5nm in vertical direction along the channel length of the device. The potential along the cutline shows that for 10nm gate length the peak value of the same along the channel is highest suggesting 10nm structure to be the best amongst the three compared here in terms of potential distribution. It indicates carriers have been effectively present along the channel after tunneling through the source channel interface.

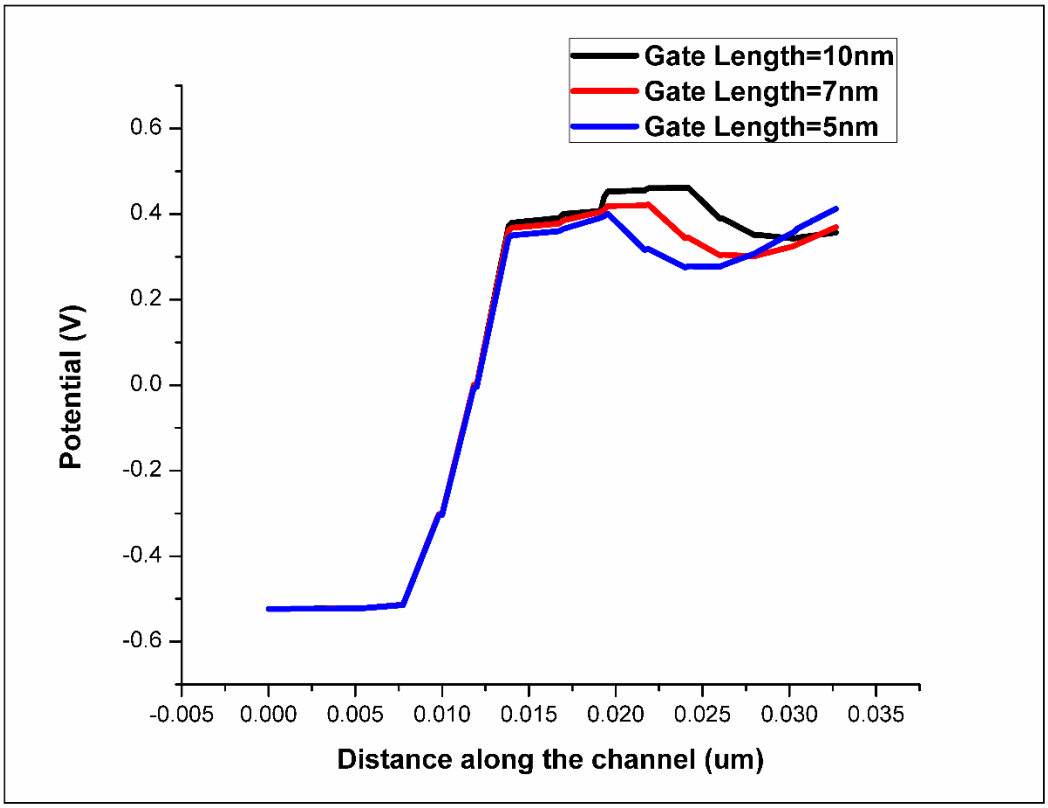


Fig4.11: Comparison of surface potential along the length of GCES-SOI TFET for three different gate lengths of 10nm, 7nm and 5nm.

4.5.7 Transfer Characteristics

The transfer characteristics of GCES SOI TFET has been studied for three different gate lengths of 10nm, 7nm and 5nm in Fig4.12. The figure illustrates that the current is measured for the variation of gate voltage from -1V to 2V whereas V_{DS} is kept constant at 0.1V. It is evident from the graph that the curves differ from each other due to variation of subthreshold slope while the ON and OFF currents remain the same. The structure has low dimensions together with extension of source region into the channel under gate. Lowering gate length makes the source and drain depletion region come even closer which may eventually affect the device performance. Subthreshold slope for 10nm gate length structure is found to be 19.8mV/dec which is minimum amongst the three and hence suggests that it is the most efficient one.

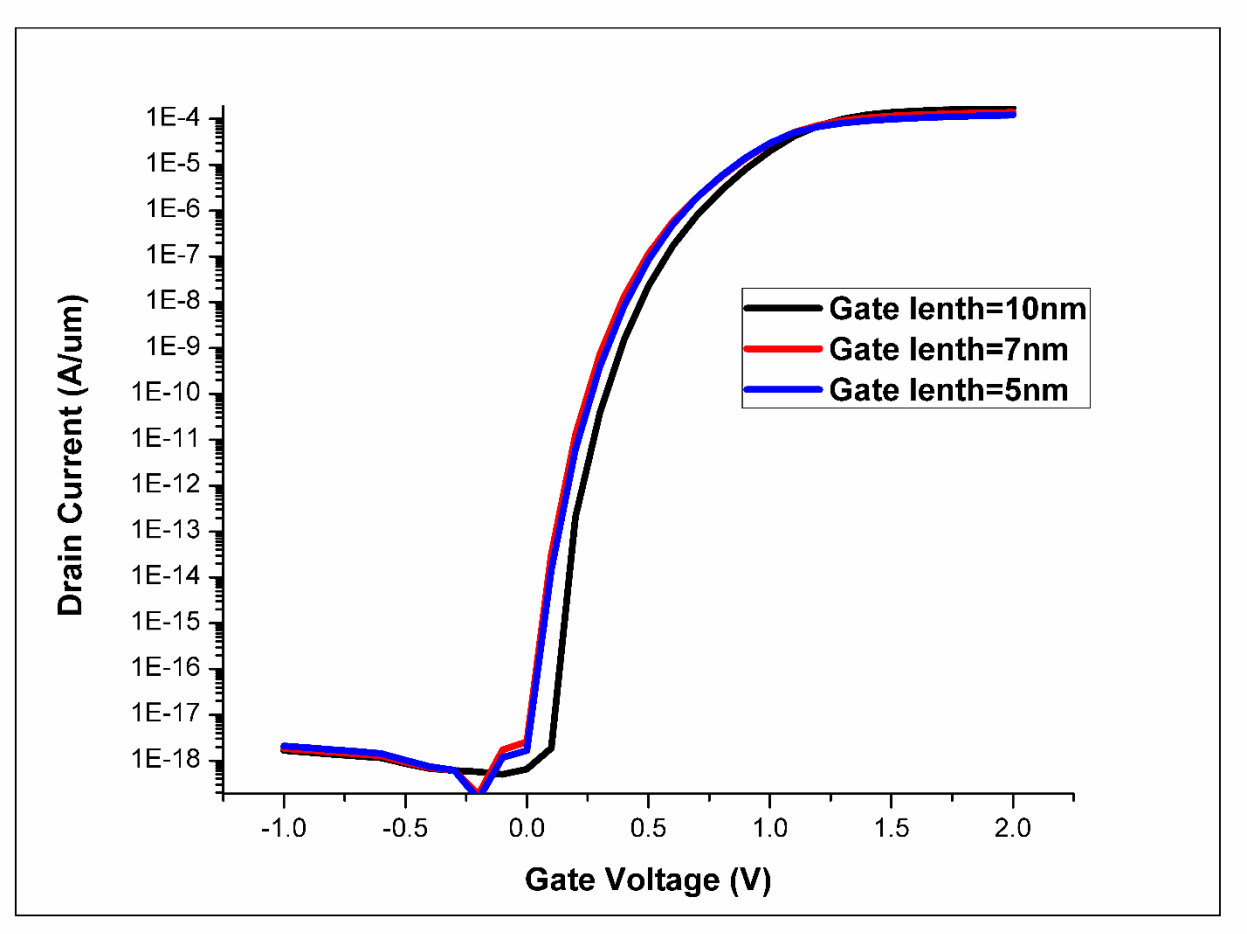


Fig.4.12: Transfer Characteristics for GCES SOI TFET for gate lengths of 10nm, 7nm and 5nm.

The comparison of current characteristics derived from analytical current modeling and simulation considering 10nm gate length dimension has been illustrated in Fig4.13. The calculation has been done at the source channel interface which contributes to the ON current that eventually reaches the drain end. Hence positive values of V_{GS} are considered. It is prominent from the figure that the current graphs of analytical model and simulation are analogous and hence the analytical current model has been validated.

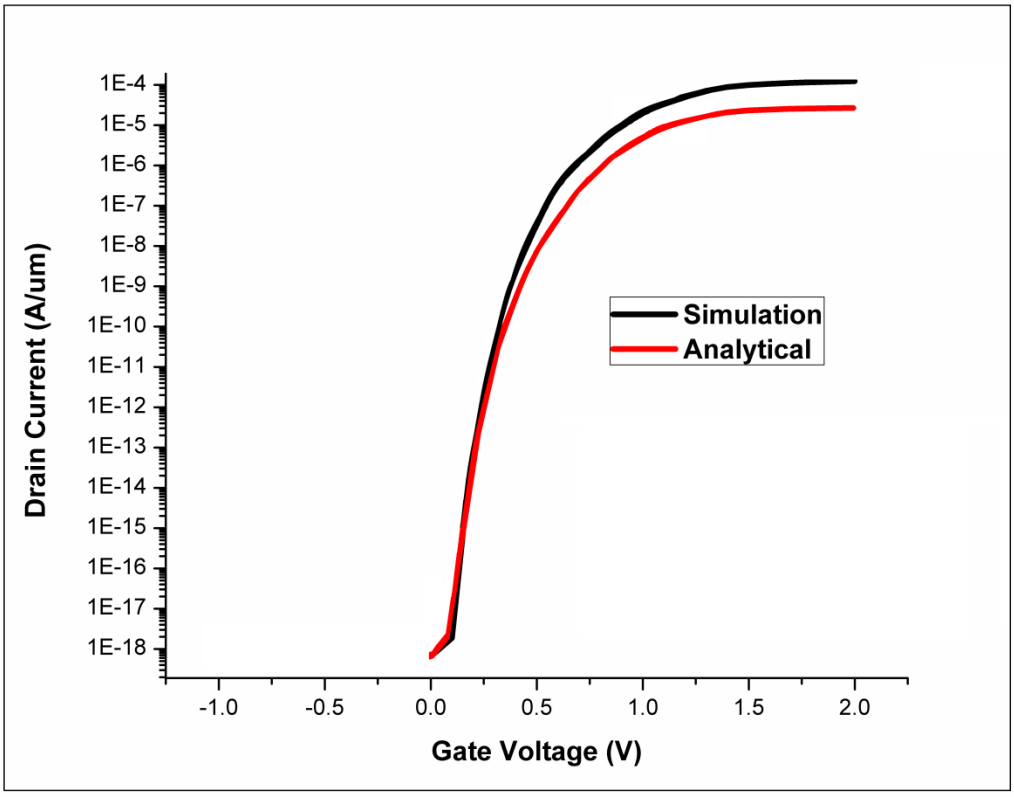


Fig 4.13: Comparison of analytical current modeling with simulation result of drain current for GCES SOI TFET.

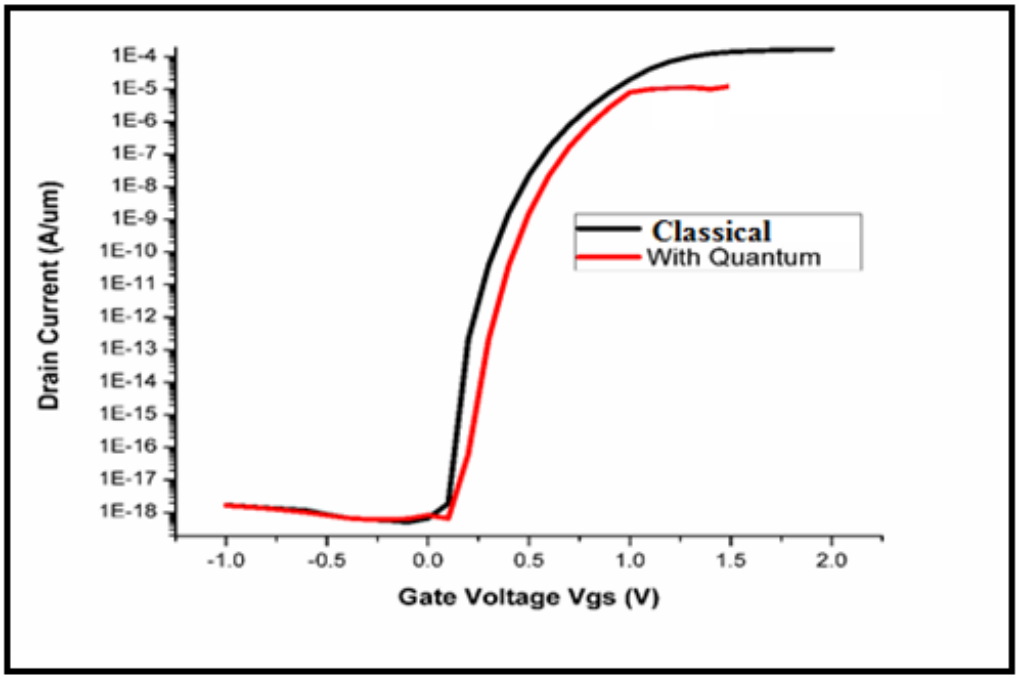
4.6 Quantum Confinement

In this section quantum confinement due to low dimensional device structure has been considered and outcomes of the same have been comparatively studied with results of classical behavior.

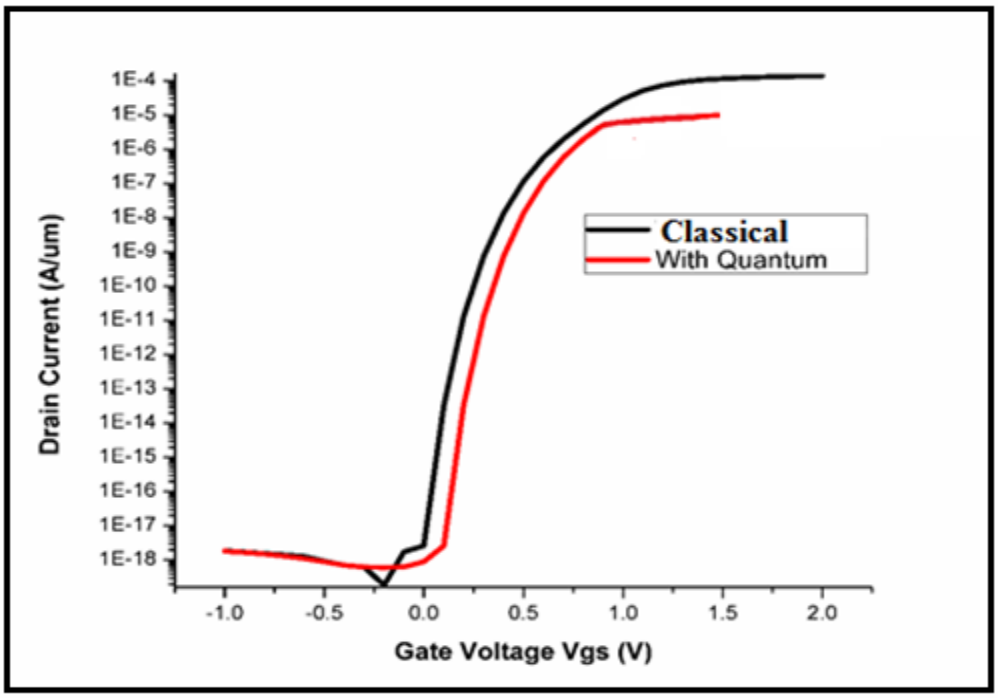
4.6.1 Transfer Characteristics

Transfer characteristics of GCES SOI TFET has been depicted in Fig4.14 for three different gate lengths such as 10nm, 7nm and 5nm and all are compared without and with considering quantum confinement. V_{DS} in all the cases are taken as 0.1V and VGS is varied from -1V to 2V. It is evident from the graphs that for three different gate lengths the ON current is higher (10^{-4} A/um)

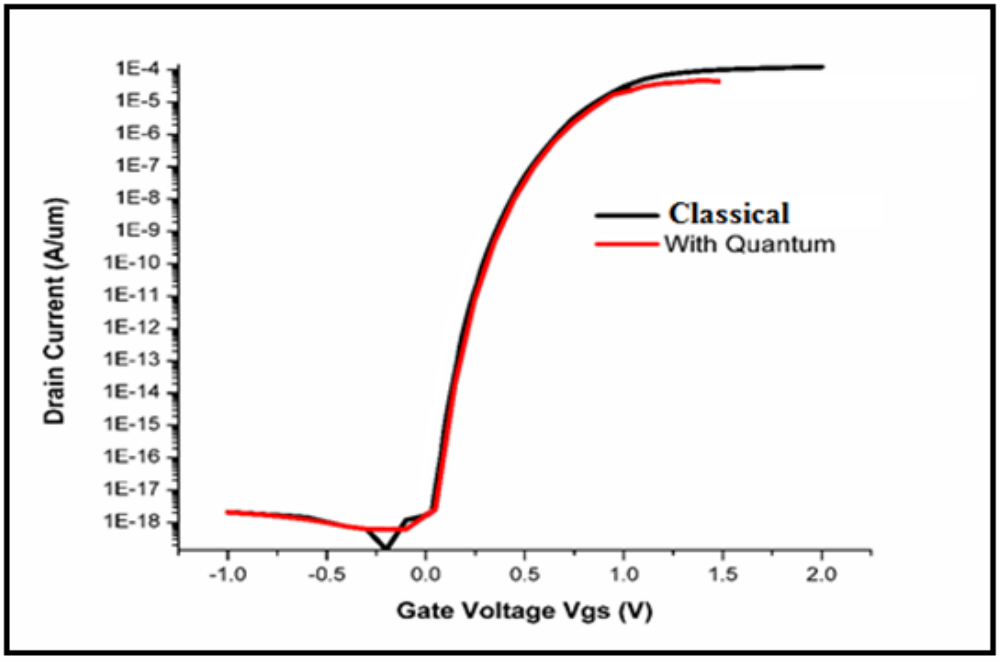
for classical approach than the ON current (10^{-5} A/um) achieved by considering quantum effects. The reason behind lower ON current for quantum confined results is the discretization of the energy bands at the source channel interface and thus the electrons can only tunnel through the first available empty energy state between the interfaces. There is no ambipolar conduction in all the cases taken into account and thus the device has the capability for low power applications. It is also evident from the graphs that subthreshold slope of the characteristics for classical is less than that of with quantum effects. I_{on}/I_{off} for all the drain currents for classical method has been found as 10^{15} whereas the same considering quantum confinement is 10^{14}. Thus it can be stated that due to quantum confinement the energy bands get discrete in nature and carriers such as electrons can only tunnel for the first available energy state between source and channel.



(a)



(b)

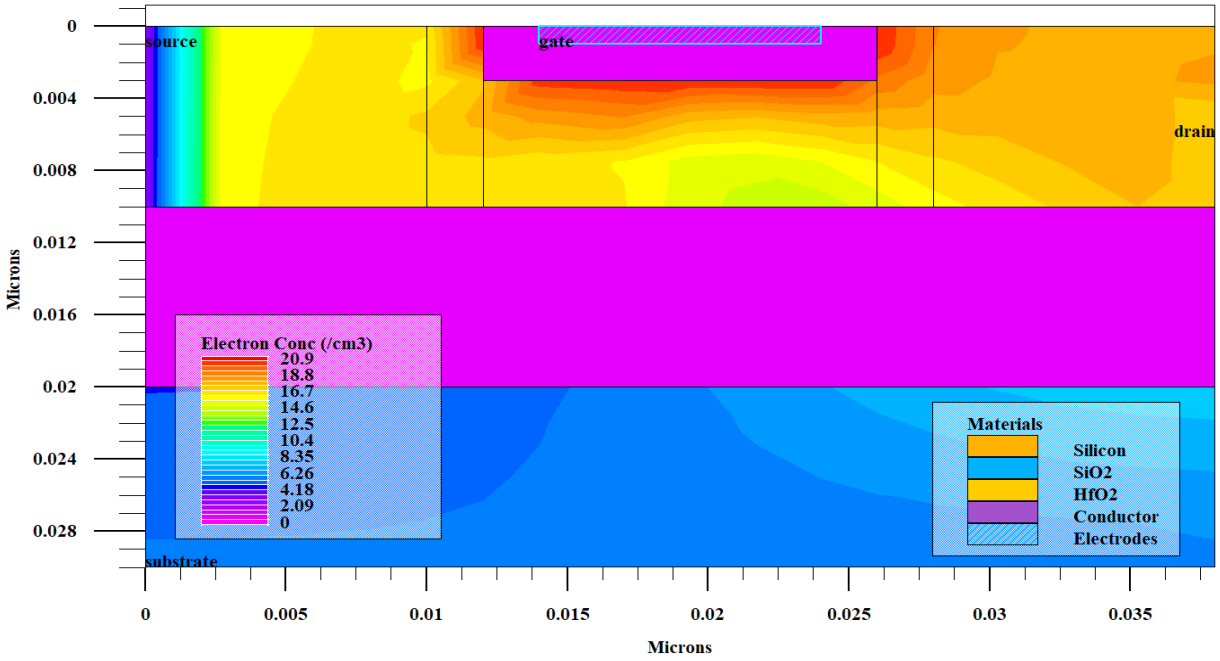


(c)

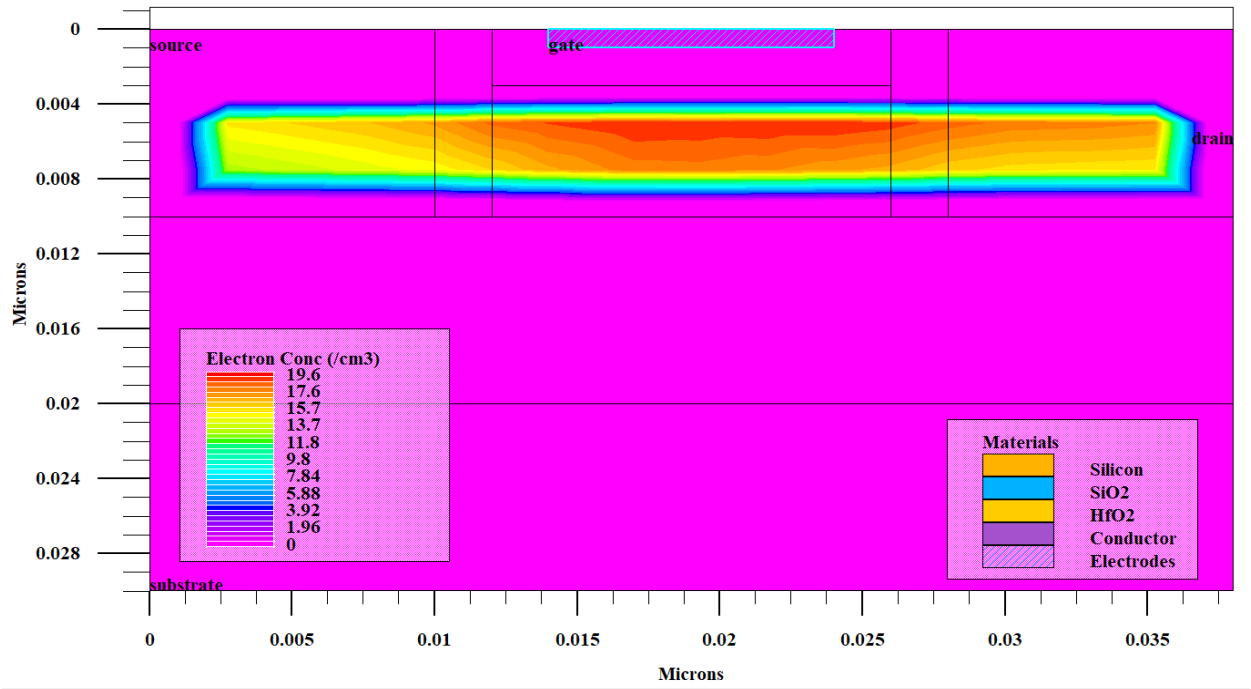
Fig 4.14: Comparison of Transfer characteristics of GCES SOI TFET with considering quantum effects and classical behavior for three gate lengths of (a)10nm, (b)7nm and (c)5nm.

4.6.2 Electron concentration

Electron concentration area within the device for quantum and classical method are different. It is illustrated and clearly visible from the contour diagrams that for all the three gate lengths of 10nm, 7nm and 5nm, electrons are confined within a particular area when quantum confinement has been considered whereas this confinement of electrons are absent in case of the same structures for classical behavior. The contour diagrams for the same are presented below in Fig4.15, 4.16 and 4.17.

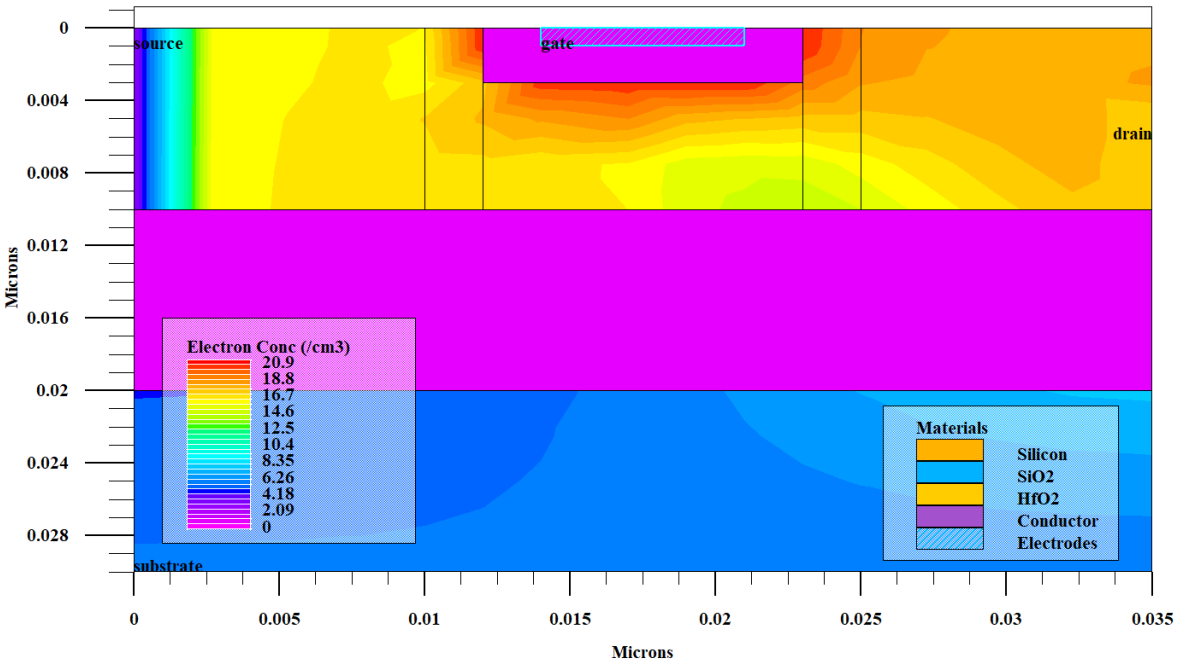


(a)

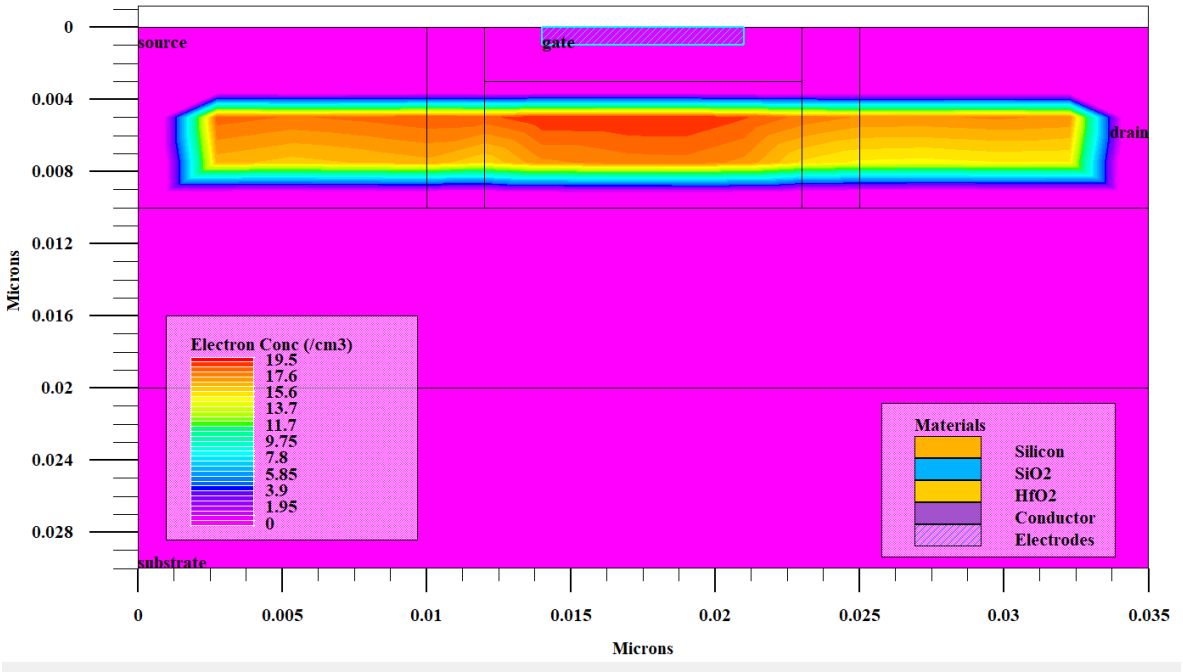


(b)

Fig4.15: Electron concentration for 10nm gate length of GCES SOI TFET for (a) classical behavior and considering (b) quantum confinement.

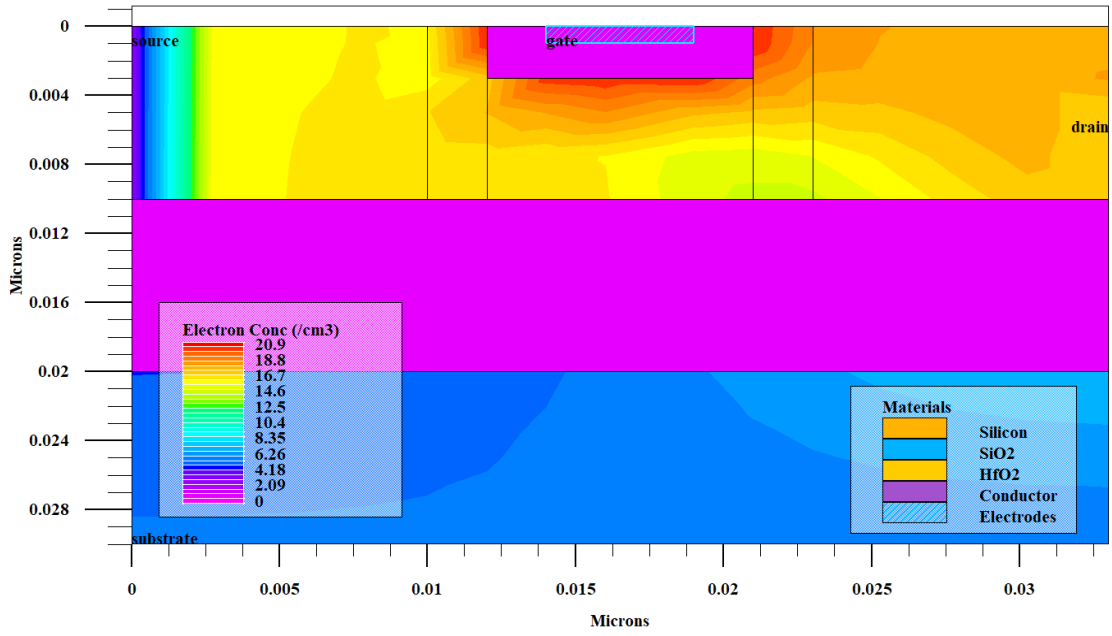


(a)

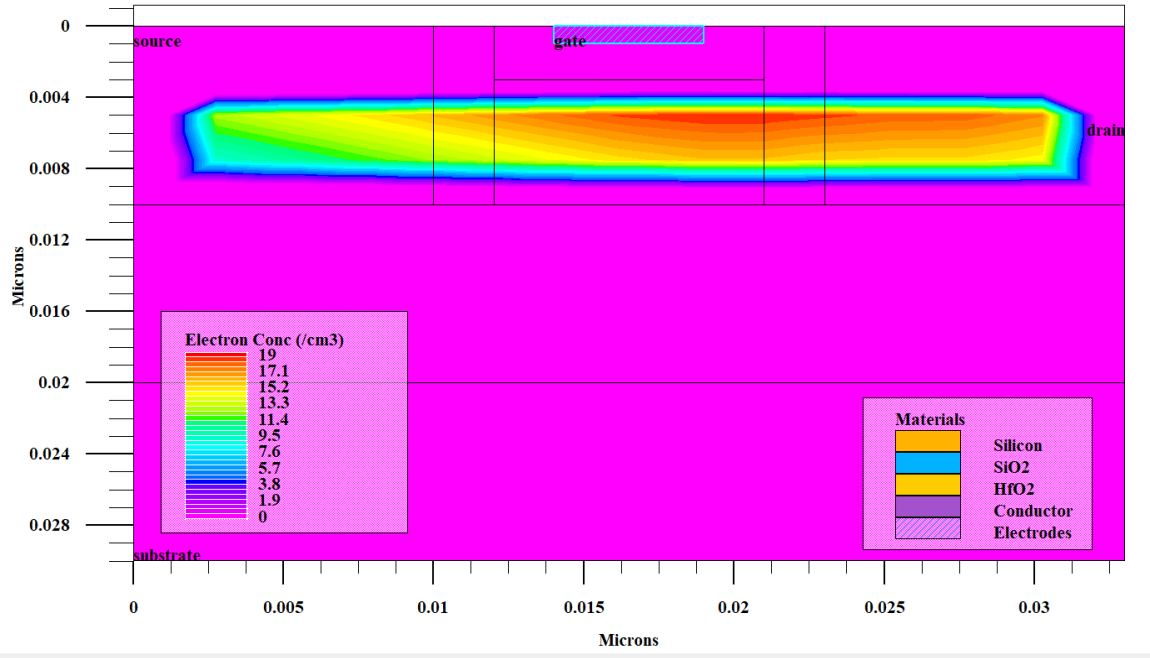


(b)

Fig 4.16: Electron concentration for 7nm gate length of GCES SOI TFET for (a) classical behavior and considering (b) quantum confinement.



(a)

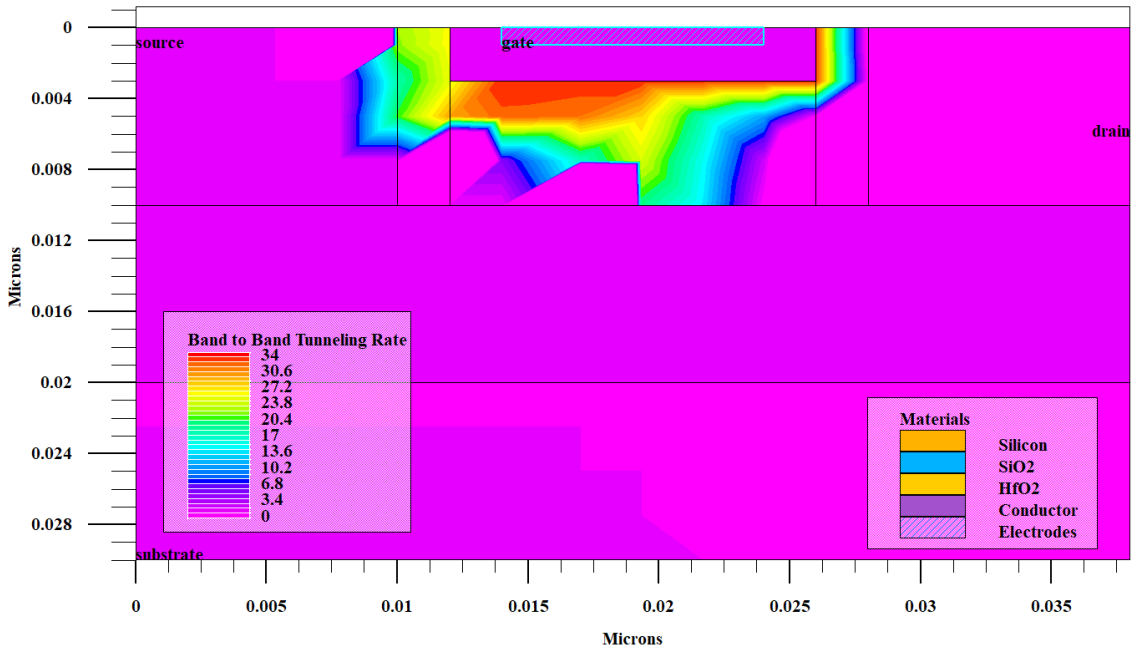


(b)

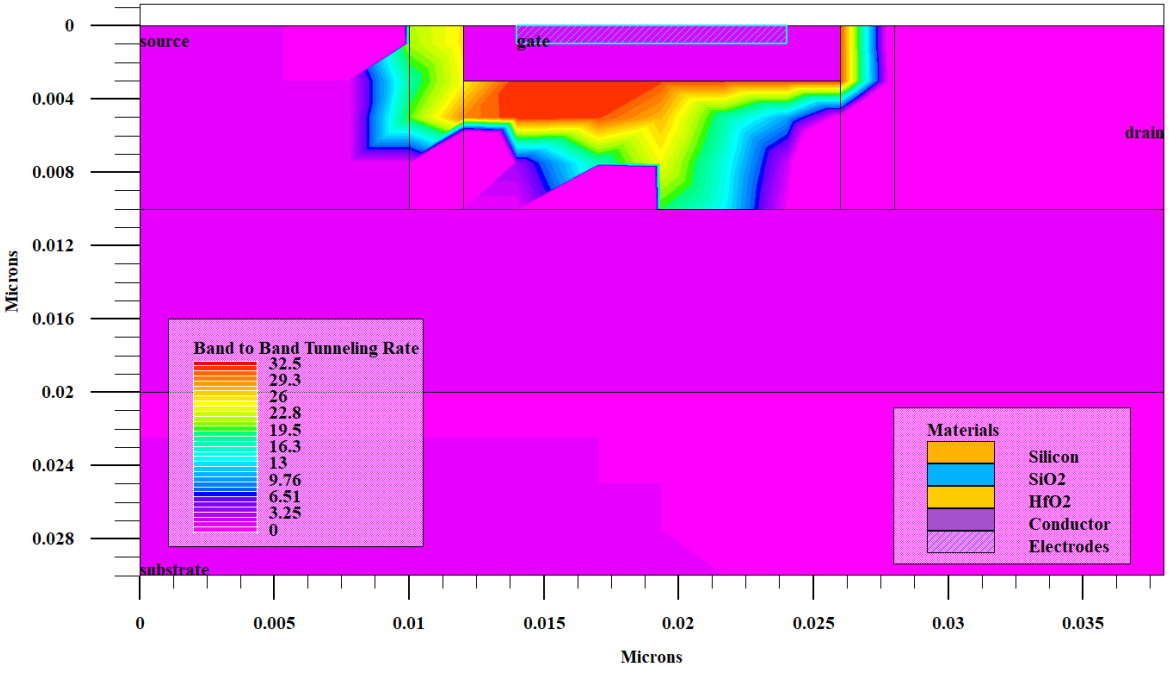
Fig 4.17: Electron concentration for 5nm gate length of GCES SOI TFET for (a) classical behavior and considering (b) quantum confinement.

4.6.3 Band to Band Tunneling Rate

Band to band tunneling rate for three different gate lengths of GCES SOI TFET has been illustrated in the Fig 4.18, 4.19 and 4.20. The BTBT rates are compared considering both quantum confinement and classical approach and it is noticeable from the contour diagrams that the rate is less when quantum confinement is considered than without considering the same. Also the maximum tunneling has been observed under the gate and above the extended source segment in all the three gate lengths which is due to line tunneling occurring at that section.

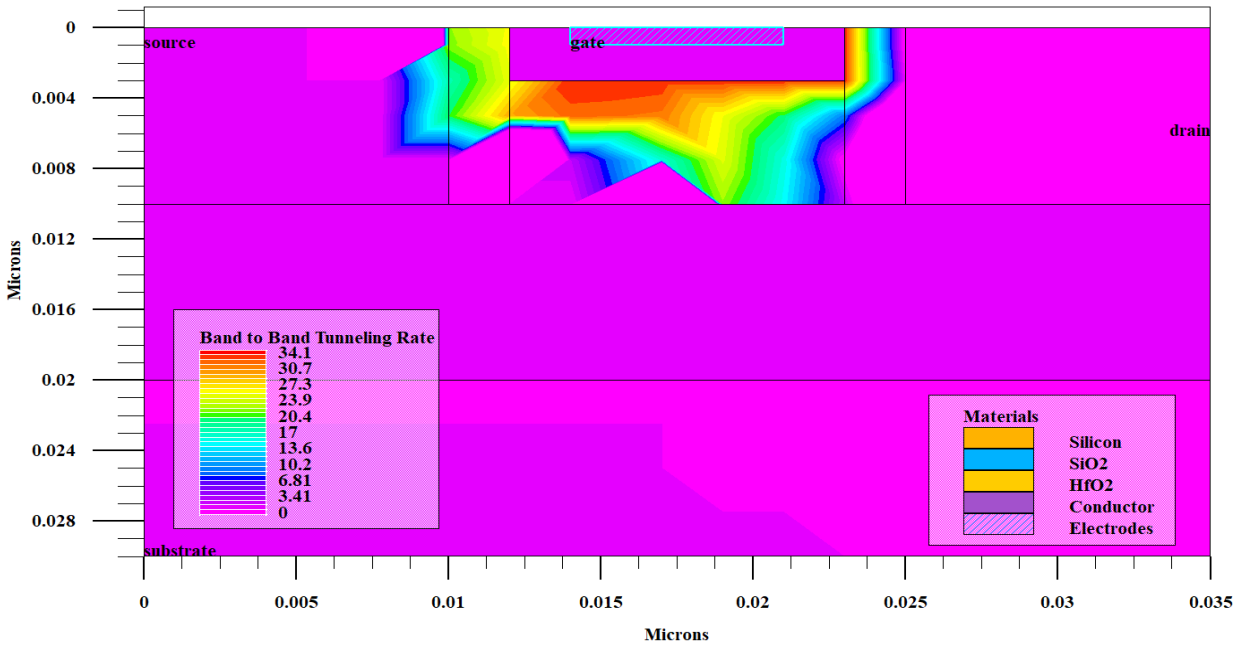


(a)

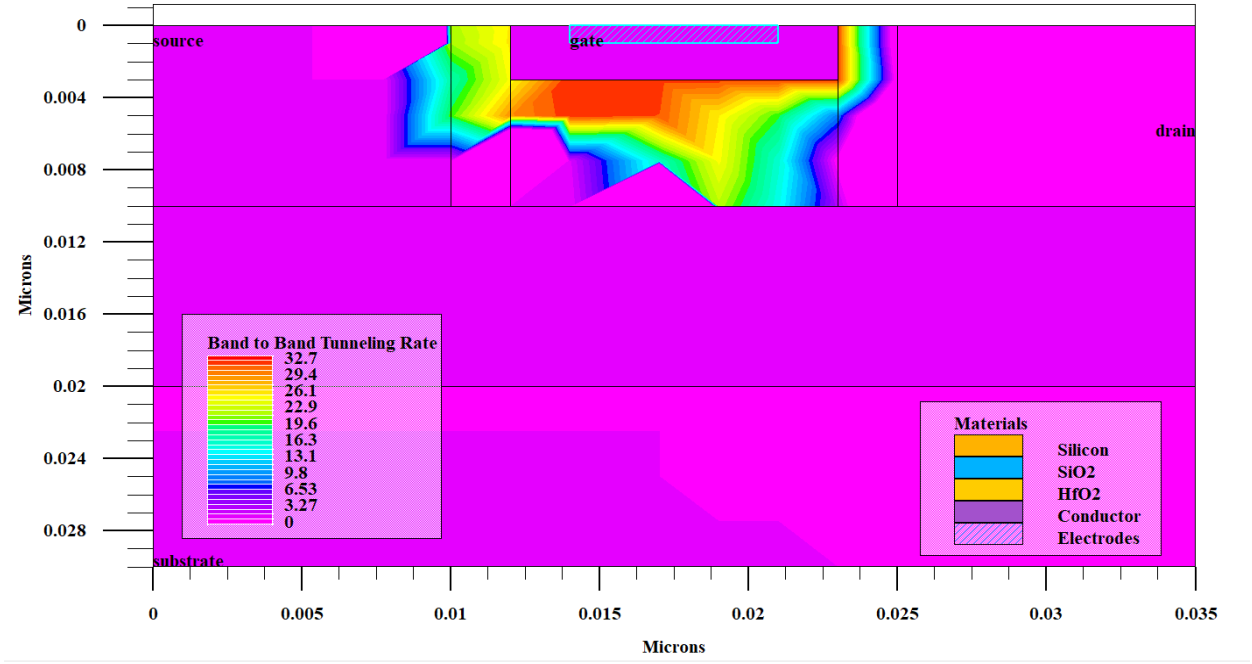


(b)

Fig 4.18: BTBT rate for 10nm gate length of GCES SOI TFET (a) with quantum and (b) classical behavior.

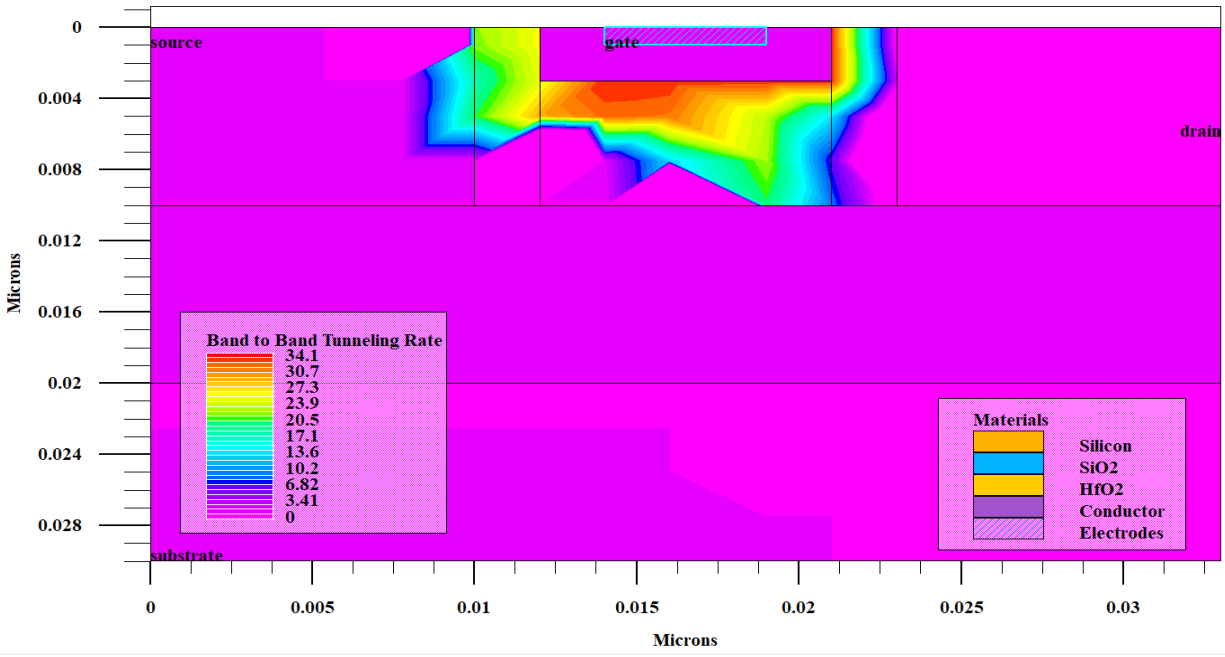


(a)

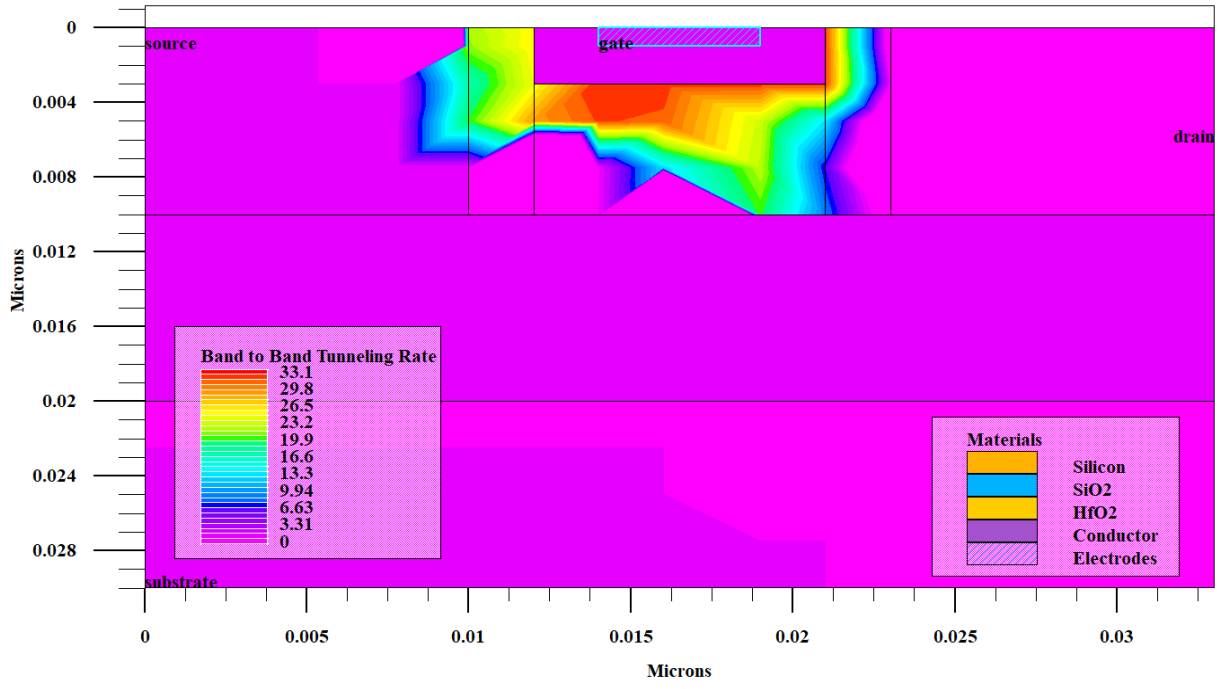


(b)

Fig4.19: BTBT rate for 7nm gate length of GCES SOI TFET (a) with quantum and (b) classical behavior.



(a)



(b)

Fig4.20: BTBT rate for 5nm gate length of GCES SOI TFET (a) with quantum and (b) classical behavior.

4.6.4 Comparison of Subthreshold Slope

The subthreshold slope from transfer characteristics has been derived for GCES SOI TFET. The SS for three different gate lengths such as 10nm, 7nm and 5nm have been compared and illustrated in the following Fig4.21 where it is prominent that SS with considering quantum confinement is less than that of classical behavior.

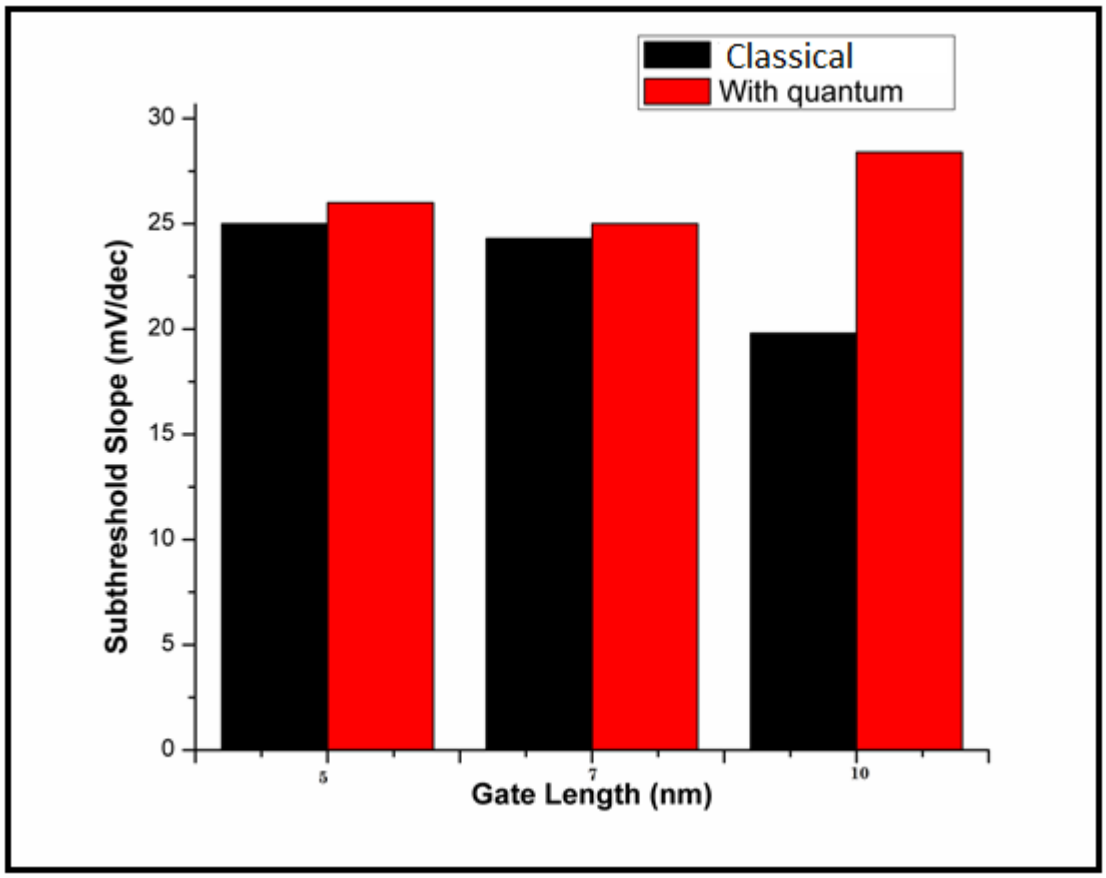


Fig4.21: Comparison of SS for gate length of 10nm, 7nm and 5nm of GCES SOI TFET.

In Table 4.3 the device performance parameters are compared for V_{DS}=0.1V and three different gate lengths of 10nm, 7nm and 5nm both considering quantum confinement and classical approach on the operation of the device. It is explicit from the table that 10nm gate length is optimum for the proposed structure as it is visible in the comparison that this particular gate length provides minimum SS along with suitable threshold voltage to turn the device ON. I_{on}/I_{off}

for all the cases with quantum confinement is found to be around 10^{14} whereas that of classical behavior is 10^{15}. ON current decreases when quantum effect is taken into account as it has an impact on the device performance.

Gate Length (nm)	Classical / Quantum	Subthreshold Slope (mV/dec)	V_{th} (V)	I_{on}/I_{off}
10	Classical	19.8	0.7	10^{15}
	Quantum	28.4	0.7	10^{14}
7	Classical	24.3	0.818	10^{15}
	Quantum	24.8	0.818	10^{14}
5	Classical	25	0.8	10^{15}
	Quantum	25.5	1.55	10^{14}

Table 4.3: Comparison of different performance parameters of GCES SOI TFET for three different gate lengths.

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Chapter 5
Conclusion and Future Scope

5.1 Conclusion

This work is focused on the potency of Nano devices in the field of electronics. The predominant device in this aspect that supersede the MOSFETs are TFET devices. Two different advanced TFET structures are investigated with extensive details on their behavior and characteristics. The proposed alternative TFET structures provide better performance than the conventional TFET structures. Also the suggested devices show remarkable outcomes at extremely low dimensions.

The Source Pocket Doping in PNPN-DG TFET structure is examined for different gate length variation. The device characteristics are intensively studied and it is found that the 7nm gate length is suitable for the particular structure as it displays no ambipolar conduction (Fig3.9). Hence it is suitable for low power applications. Analytical model has been derived for surface potential of the device and the same is verified with the simulated outcomes for three different gate lengths separately (Fig3.3).

An alternative SOI TFET structure precisely GCES SOI TFET has been proposed and studied by modifying its gate length for three different values. The device is optimized to suitable V_{DS} of 0.1V, extended source alignment with the center position of gate and optimum drain contact position. The band diagrams (Fig4.9), electric fields (Fig4.10), potential distributions (Fig4.11) and transfer characteristics (Fig4.12) are examined to analyze the device performance

parameters. The drain current of the structure has been analytically modeled taking into account of point tunneling as well as line tunneling (Fig4.5) due to trench gate structure of the device. The analytical current model has also been validated by simulation using Silvaco, Atlas (Fig4.13). It is evident from the results that the device performs best when gate length is 10nm having SS as low as 19.8mV/dec and ratio of ON current to OFF current as 10^{15} (Fig4.12). Transfer characteristics for three different gate lengths have been compared taking into account of quantum confinement with classical behavior (Fig4.14). SS increases and ON current decreases when quantum confinement has been taken into account due to discrete energy band at the source channel interface (Fig 4.21). Also all the variations show no ambipolar conduction suggesting the device to be beneficial for low power application.

5.2 Future Scope

The TFET devices explored as the alternative advanced device structures in Nano devices exhibit better performance than the conventional TFET devices and even more advantageous over the MOSFET devices. TFET can be integrated with CMOS process and hence it eases the process of fabrication and avoids difficulties in batch processing. Also the devices that are analyzed in this work are suitable for low power application due to negligible ambipolar conduction. Hence circuit analysis using these devices can be a prospect for future. In addition to this, analytical model of the device considering quantum confinement need to be calculated and analyzed further in future. The quantum analytical model also needs verification with simulated outcomes.

List of Publications Relevant to the Thesis

Accepted Papers in Conferences

1. Bijoy Goswami, Sutanni Bhowmick ,**Debadipta Basak**, Ayan Bhattacharya, Arindam Halder, Koelgeet Kaur, Subir Kumar Sarkar **"2-D Analysis of a Centrally Aligned PNPN-DG TFET to Preclude Ambipolar Conduction" ,** ECTI CON 2019,Thailand .(Acceptd)

2. Ayan Bhattacharya, **Debadipta Basak**,S Reddy,Subir Kumar Sarkar "**Impact of Source Engineering in Split Drain Tunnel Field Effect Transistor**" IEEE EDKCON 2018 , Pride Hotel, Kolkata. (Accepted)

3. Bijoy Goswami, **Debadipta Basak**, Ayan Bhattacharya, Koelgeet Kaur, Sutanni Bhowmick, Subir Kumar Sarkar "**Analytical Modeling and Simulation of Low Power Salient Source Double Gate TFET** " , Devices for Integarted Circuits (DevIC 2019),Kalyani University,23-24 March,2019. (Accepted)

4. Bijoy Goswami, Sutanni Bhowmick, Arindam Haldar, **Debadipta Basak**, Goutika Paul and Subir Kumar Sarkar, "**Implementation of L-shaped Double Metal Dual Gate TFET towards Improved Performance Characteristics and Reduced Ambipolarity**" in Information, Photonics and Communication 2019 (IPC'19) 1 st -3rd February, 2019, B. P. Poddar Institute of Management and Technology (BPPIMT), Kolkata.(Accepted)

Papers in Journal

1. Bijoy Goswami, **Debadipta Basak**, Koelgeet Kaur , Ayan Bhattacharya , Subir Kumar Sarkar,"**A Novel Source Pocket Doping in PNPN-DG TFET to Preclude Ambipolar Current –Two Dimensional Analytical Modelling of Surface Potential & Simulation**". (Communicating)

2. Bijoy Goswami, **Debadipta Basak**, Ayan Bhattacharya, Sutanni Bhowmick, Koelgeet Kaur, Subir Kumar Sarkar, "**Analytical Modeling and the Impact of Quantum Confinement on Subthreshold Swing of Salient Source DG-TFET**".(Communicated)

3. Debadipta Basak, Bijoy Goswami, Sutanni Bhowmick, Koelgeet Kaur, Ayan Bhattacharya, Subir Kumar Sarkar, " **Analytical Modeling and Simulation Based Validation for Gate Centric Extended Source SOI TFET** ".(Communicating)

4. Koelgeet Kaur**,** Bijoy Goswami, Sutanni Bhowmick, **Debadipta Basak**, Subir Kumar Sarkar, "**Analytical Modeling and Simulation Based Validation of Dual source TFET**".(Communicating)

5. Sutanni Bhowmick, Bijoy Goswami, **Debadipta Basak**, Koelgeet Kaur, Ayan Bhattacharya, Subir Kumar Sarkar "**Analytical Modeling and Simulation of Double Trench Gate Covered Source-Channel TFET towards Improved ON-Current**" (Communicating)