DELAY EFFICIENT ALL OPTICAL CARRY LOOKAHEAD ADDER

Thesis submitted in partial fulfilment of the requirement for the degree of

Computer Science and Engineering Department

by

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Examination Roll Number M6TCT19002

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2019

COMPUTER SCIENCE AND ENGINEERING DEPARTMENT

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ACKNOWLEDGEMENTS

I would first like to thank my supervisor Dr. Debesh Kumar Das, Professor, Department of Computer Science and Engineering,Jadavpur University. The door to my supervisor office were always open whenever I ran into a trouble spot or had a question about my research or writing. They steered me in the right direction whenever I needed it. The extreme energy and creativity of my supervisor have always been a constant source of motivation for me. The perfection that he brings to each and every piece of work that he does, always inspired me to do things right at first time. I will be always thankful to him.

Last but not the least,I would like to dedicate this thesis to my amazingly, loving and supportive parents and my family members who have always been with me, no matter where I am, and providing me with unfailing support and continuous encouragement throughout my years of study and through the process of researching and writing this thesis. This accomplishment would not have been possible without them.

(SAYANTANI ROY)

ABSTRACT

Adders are most commonly used in various electronic applications. Different types of adders are available such as ripple carry, carry look ahead, carry select, carry save and many more. Each one having their own benefits and limitations. But the main issue is to design an adder having less delay, low power consumption and reduced chip area. In past, the major challenge for VLSI designer was to reduce chip area by using efficient optimization techniques. Then the next phase is to increase the speed of operation to achieve fast calculations as, in today's microprocessors millions of instructions are executed per second. Now, as most of commercial electronic products are portable like mobile, laptops etc. These require more battery backup. So, lot of research is going on to reduce power consumption. Thus, there are three performance parameters on which a VLSI designer has to optimize their design i.e. area, speed and power. It is very difficult to achieve all constraints for particular design, therefore depending on demand or application some compromise between constraints has to be made.

Carry look ahead adders (CLA) are the fastest of all adders and achieve high speed through parallel carry computations. This method does not require the carry signal to propagate stage by stage.

In this thesis, an efficient all-optical realization of CLA is proposed using Mach–Zehnder interferometer (MZI) gates. Now-a days, Mach–Zehnder interferometer (MZI) plays a vital role in the field of ultra-fast all-optical signal processing. We have used all optical based Mach-Zehnder Interferometer (MZI) switches to implement the CLA circuit functionality. The design of the circuit with optical technology can be implemented using Mach-Zehnder Interferometer(MZI) switch, which has significant advantages of high speed, low power, fast switching time and ease of fabrication. Experimental results confirm the efficacy of the proposed design over similar existing designs.

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Chapter 1

Introduction

1.1. Introduction

The ultimate goal in present age of Information Technology is information generation and dissemination by anybody, anything and anywhere. Very Large Scale Integration (VLSI) technology has revolutionized the electronics industry and established the 20^{th} century as the computer age. If IC technology continues to follow the pattern predicted by the Moore's Law [1] , it is also estimated that the number of transistor switches that can be put onto a chip doubles every 18 months. But, it is approaching its fundamental limits in the sub-micron miniaturization process. Again energy loss is an important issue in digital logic design. Loss of energy is due to dissipation of heat from logic circuit.

As we are giving priority to high speed and low power designs, it alters the requirements and obligation of present-day circuits. As the aftermath, in the current arena, substitutions of the traditional computing systems are being explored. One of these technologies is Optical Circuit, due to advances in silicon photonics [4]. In electronic digital systems, optical technology is used as an ultra-fast interconnects [5]–[6]. Application of Optical technology can be seen in communication networks [2] and signal processing systems [3]. But due to the size constraint, these optical circuits and systems are not apt for chip based abbreviated computing devices.

Recently, the researchers are aiming at the development of the optical digital computer system for processing binary data using optical computation. Photons are the source of optical technology. This photonic particle provides unmatched speed with information as it has the speed of light. The installation of optical components in the electronic computer system produces optical-electronic hybrid network. The researchers are trying to combine the optical interconnects with the electronic computing devices.

The implementation of optical logic circuits can be performed using based Mach-Zehnder Interferometer (MZI) switches which has significant advantages of the high speed, low power, fast switching time and ease of fabrication [7]–[8]. Research into this field has also explored new concept and ideas. Various architectures, algorithms, logical and arithmetic operations have been proposed in the field of optical/ optoelectronic computing and parallel processing in last few decades. Most of the all-optical circuits largely depend on digital logic operations as well as switching operations. To increase the signal strength Semiconductor Optical Amplifier (SOA) are used along with MZI gates.

The application of such optical devices is not limited to the theoretical domain only. In fact, there are practical realizations as well. Designing important logic modules like multiplexers, adders, universal logic blocks with MZI [9]–[12] has received wide attention due such feasibility in practical realization. But a generalized way to design optical circuits for arbitrary logic functions remains essential as most of the logic modules those are previously made are basically on specific type of functional blocks and manually designed.

1.2. Scope and Organization of the Thesis

We address implementation and synthesis of Carry Look ahead Adder (CLA) using MZI switches. The contents of the remaining chapters are summarized below. In Chapter 2 we have given a brief introduction on carry look ahead adder (CLA) , semiconductor based amplifier (SOA), MZI architecture, beam splitter(BS) and beam combiner(BC), metrics to calculate optimization that is optical delay and optical cost and design of these gates using MZI switches. Chapter 3 deals with design and implementation of all optical 4 bit and 8 bit Carry Look ahead Adder (CLA) using MZI switches. A glimpse on future work and conclusion has been presented in Chapter 4.

Chapter 2

Background Review

2. 1 Introduction

In this chapter, we introduce some basic concepts those are used in the thesis. We first discuss the adder circuits. Then we discuss MZI gates and use of them in synthesis of Boolean functions.

2. 2 Adders

Adders are most commonly used in various electronic applications. Different types of adders are available such as ripple carry, carry look ahead, carry select, carry save and many more. Each one having their own benefits and limitations.

2. 2.1 Ripple Carry Adder

A ripple carry adder is a digital circuit that produces the arithmetic sum of two binary numbers. It can be constructed with full adders connected in cascaded with the carry output from each full adder connected to the carry input of the next full adder in the chain. Figure 2(a) shows the interconnection of four full adder (FA) circuits to provide a 4-bit ripple carry adder.

In the ripple carry adder, the output is known after the carry generated by the previous stage is produced. Thus, the sum of the most significant bit is only available after the carry signal has rippled through the adder from the least significant stage to the most significant stage. As a result, the final sum and carry bits will be valid after a considerable delay.

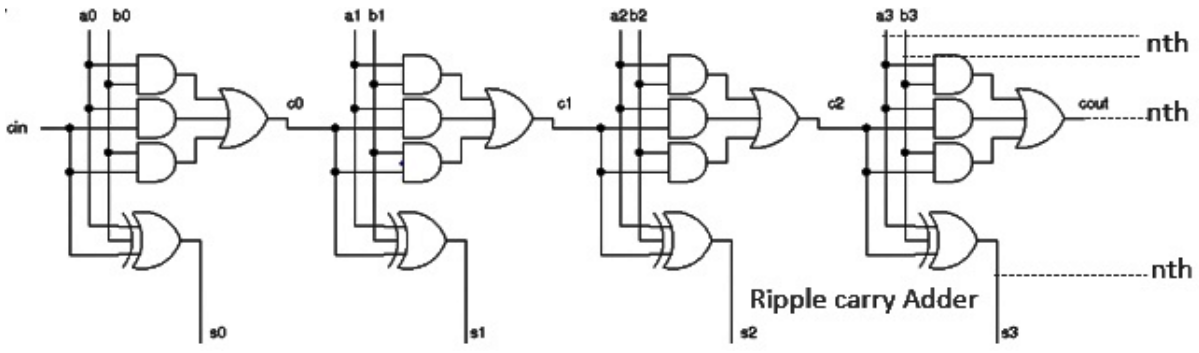

Figure 2(a): Diagram of Ripple carry Adder

2.2.2 Carry Look Ahead Adder

In this section, we first review and illustrate the basic concepts of CLA. Afterwards, we present the proposed all-optical realization of the CLA.

Carry Look ahead Adder is derived from ripple carry adder. In ripple carry adder data flow in a chain as the bit length go on increasing delay to overcome that problem carry look ahead adder was designed. Look ahead carry algorithm speed up the operation to perform addition, because in this algorithm carry for the next stages is calculated in advance based on input signals. Carry look ahead logic uses the concepts of generating and propagating carries. Although in the context of a carry look ahead adder, it is most natural to think of generating and propagating of binary addition, the concepts can be used more generally than this. There will be a carry propagation if OR operation is performed for that either one of the input is one or input carry also be 1. Generation and propagation can be represented by the Boolean expression in the following way:

$P_i = x_i$ or y_i --- Carry Propagation

$G_i = x_i$ and y_i --- Carry Generate

$C_{i+1} = G_i$ or (P_i and C_i) -- Next Carry

Figure 2(b) shows the diagram of CLA for 4 bits.

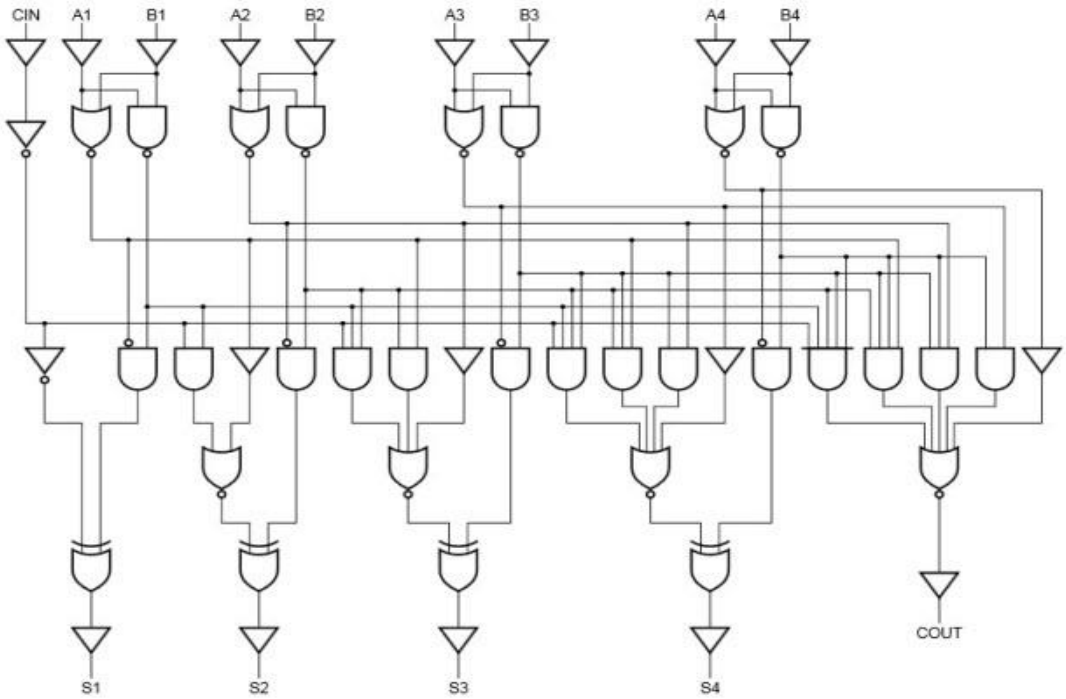

Figure 2(b) : Carry Look ahead Adder

Carry propagation time is an important attribute which limits the speed of operation of the adders. To reduce the carry propagation time, the concept of Carry Look-ahead logic is employed which computes all the carry outputs in parallel. The concept of look-ahead in order to generate carry bits completely removes the carry propagation delay and thereby enhances the operational speed of the adder. Adders relying on this concept of carry generation are known as Carry Look-ahead Adders (CLAs).

The general idea of CLA is as follows : For any input i, the outputs Sum and Carry can be defined as $S_i = P_i \oplus C_i$ and $C_{i+1} = G_i \mid (P_i \,\&\, C_i)$ respectively, where $P_i = A_i \oplus B_i$ denotes carry propagate and $G_i = A_i \,\&\, B_i$ denotes carry generate and symbols '$\oplus$, | , &' define XOR, OR and AND operations respectively. If we consider the addition of two n-bit numbers, say, A and B then, the final carry output C_{i+1} generated at the $i^{th}(0 \le i \le n-1)$ stage of addition can be expressed as $C_{i+1} = G_i + P_i G_{i-1} + ... + P_i P_{i-1} .. P_1 G_0$, considering no initial carry. This expression shows that any output carry C_{i+1} at any i^{th} stage does not depend on the output carry C_i of $(i-1)^{th}$ stage i.e. preceding stage. In fact, the output carry C_{i+1} of any i^{th} stage relies only on input carry G_0. For example, all the carry outputs $C_1, C_2, C_3, ..., C_{n-1}$ generated during the addition of two n-bit numbers, $A(a_{n-1}, a_{n-2}, ..., a_1, a_0)$ and $B(b_{n-1}, b_{n-2}, ..., b_1, b_0)$ can be expressed in terms of input carry as follows:

$C_1 = G_0$

$C_2 = G_1 + P_1 C_1 = G_1 + P_1 G_0$

$C_3 = G_2 + P_2 C_2 = G_2 + P_2 G_1 + P_2 P_1 G_0$

$C_4 = G_3 + P_3 C_3 = G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0$

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$C_n = G_{n-1} + P_{n-1} G_{n-2} + P_{n-1} P_{n-2} G_{n-3} + ... + P_{n-1} P_{n-2 .....} P_2 P_1 G_0$ where, $G_0 = A_0 B_0, G_1 = A_1 B_1,$

$G_2 = A_2 B_2, G_3 = A_3 B_3$

and $P_0 = A_0 \oplus B_0$, $P_1 = A_1 \oplus B_1, P_2 = A_2 \oplus B_2$, $P_{n-1} = A_{n-1} \oplus B_{n-1}$.

The result of the addition can be obtained now as $S_0 = A_0 \oplus B_0$, $S_1 = P_1 \oplus C_1$, $S_2 = P_2 \oplus C_2$, ... , $S_{n-2} = P_{n-2} \oplus C_{n-2}$, $S_{n-1} = P_{n-1} \oplus C_n$, $S_n = C_n$.

Now the total adder circuit can be designed as shown in Figure 2(b) that consist of three sub-circuits, the

first one (P & G generator) produces P_i's and G_i's the second one called as Carry Generator of CLA produces carries of different levels and third one sum generator generates the output sum result. Clearly first one or third one is providing single delay. The second one is basically a two level AND-OR circuit. Thus the total delay becomes 4. The problem in this CLA design is that to achieve the speed we need more hardware. Moreover in Carry Generator part are require AND and OR gates with higher inputs. The design of a Carry Lookahead Adder with n inputs is shown in Figure 2(c).

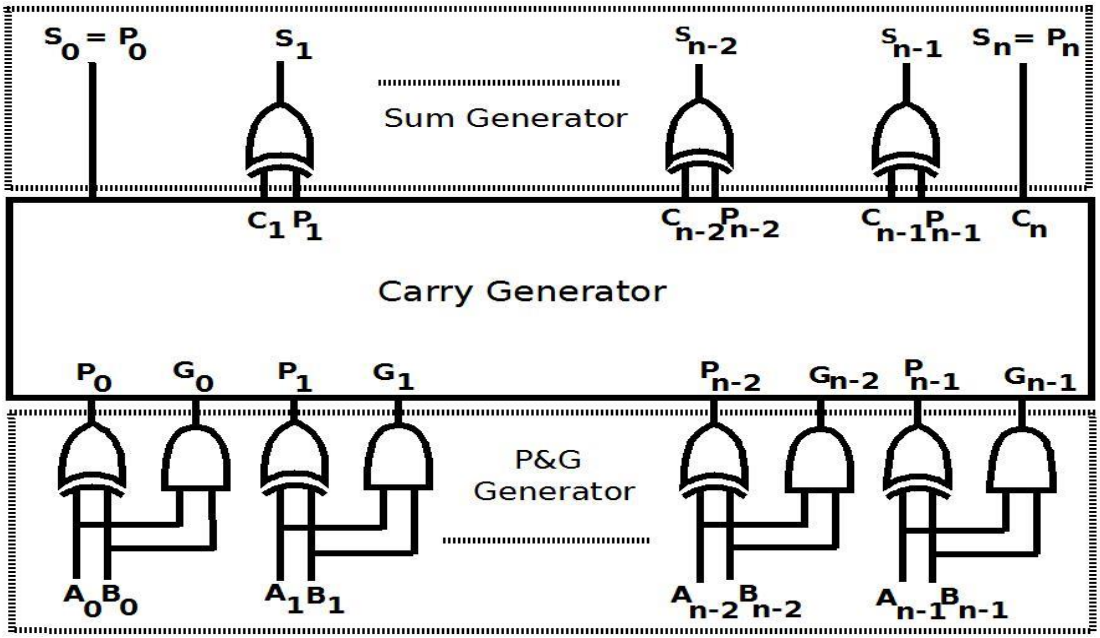


Figure 2(c): Structure of Carry Lookahead Adder

2.3. MZI Architecture

This section briefly reviews the common logic model and gate library used in the domain of optical logic synthesis. Mach-Zehnder Interferometer (MZI) can realize optical circuits. In the logic domain, this switch is abstracted to a so called MZI gate. Logically, an MZI gate is defined as follows [15]–[16]:

Definition 1: An MZI gate as shown in Figure 2(d) realizes a Boolean function composed of two optical inputs x and y as well as two optical outputs z and w. The absence of any input signal leads to the logic value 0 at the output z. The presence of input signal x and the absence of input signal y leads to the logic

value 1 at the output w. In the presence of both input signals, the outputs z and w produce 1 and 0, respectively. Therefore, the functions, $z = x \,\&\, y$ and $w = z \,\&\, \sim y$ are realized.

Definition 2: A splitter as shown in figure 2(e) divides an optical signal into two signals – each with only half of the incoming signal power. In contrast, a combiner merges two optical signals into a single one and, by this, inherently realizes the OR-function. A splitter (combiner) may have more than two outputs (inputs). Then, in case of a splitter, the strength of the signal is divided by the number as shown in Figure 2 of outputs.

An MZI gate, splitter and combiner together form an optical gate library which can realize any Boolean function.

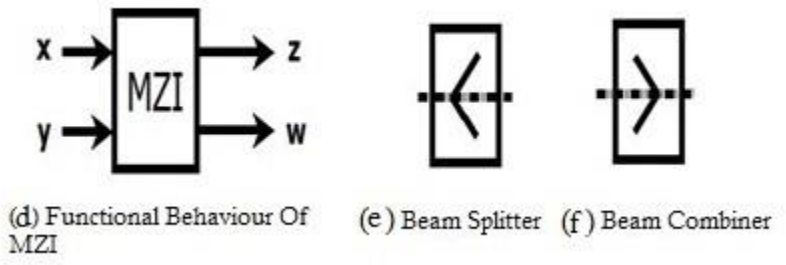


Figure 2 (d),(e),(f) : Optical Gate Library

The optical cost and the delay of beam combiner and beam splitter are negligible [4, 6] and while calculating optical cost of a circuit, it may be assumed as zero.
As the optical cost of BS and BC are relatively small, the optical cost of a given circuit is the number of MZI switches required to design the realization. The optical delay is estimated as the number of stages of MZI switches multiplied by a unit .

2.4. Semiconductor Optical Amplifier

Semiconductor optical amplifiers (SOA) are amplifiers which use a semiconductor to provide the gain medium. SOA is basically a laser diode (LD). The incident light is amplified through stimulated emission. Mirrors are absent so no feedback from its input and output. The schematic diagram of SOA is shown in figure 2(a) below.

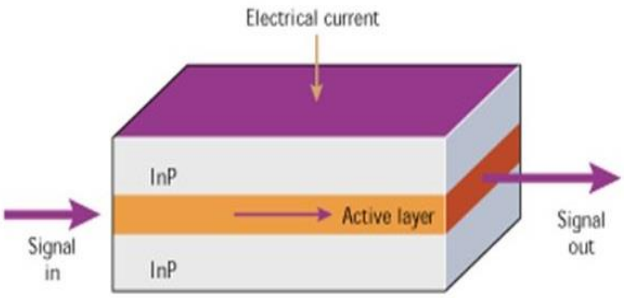


Figure 2(g) : Schematic Diagram of SOA

The input signal comes from fiber then passed through the active region which is pumped by external current injection and then transmits through the fiber. Only to get the amplification function the device must be protected from the self oscillations generating the laser effect. Semiconductor optical amplifiers have five basic parameters. These are i) Gain (Gs), ii) Gain Bandwidth, iii) High saturation output power (Psat), v) Noise figure (NF), v) Polarization dependent gain (PDG). It should have highest gain because it amplifies input light through stimulated emission. The optical gain depends on the frequency or wavelength of incident signal. Effective amplifier has an additional dependency on the intensity of local beam at any point inside the amplifier. High optical non-linearity makes semiconductor attractive for all optical signal processing (all optical switching, wave conversion) so, very high saturation output power is required to achieve linearity. This is an important criterion of an ideal SOA. Amplifier noise figure is a key consideration for amplification application. For optical communication system, an optical amplifier should have amplifier noise figure as low as possible. It depends on operating wavelength, operating current and input signal power range (6-10 dB). Gain of an SOA is dependent on the polarization of input light which is dependent on the local temperature and stress on the fiber. It should be very low polarization sensitivity to minimize the gain difference between the transverse electric mode (TE, i.e. light passing with polarization parallel to the junction plane) and Transverse magnetic mode (TM, i.e. light passing with polarization perpendicular to the junction plane). In optical networking system the SOA is recommended as an important technology for amplification, wavelength conversion, switching and all optical regeneration of signals. The wavelength conversion can be accomplished by either Cross Gain Modulation (XGM) or Cross Phase Modulation (XPM) or by Four Wave Mixing (FWM). All the process can be exploited with the application of SOA due to its high speed, high extinction ratio and also high integration potential. Optical switches can be constructed using SOA. The advantage of SOA gate is that they can be integrated monolithically on a substrate to form gate arrays. Injected current will control the SOA gate. When injected

current is high, SOA allows signal light with some amplification but when the injected current is near to zero the device blocks the signal. Therefore, SOA can be used as an optical switch.

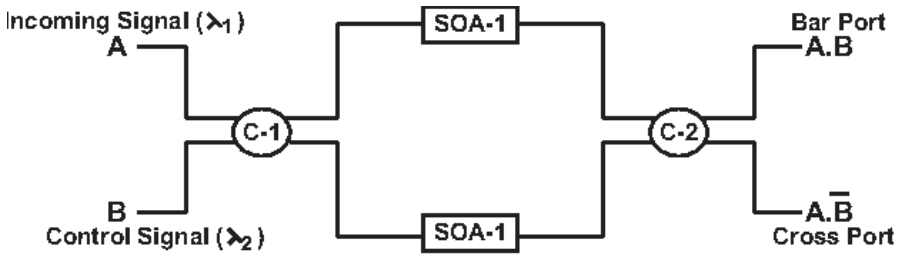
A semiconductor optical amplifier (SOA) is also an attractive switching device because of its compactness, high stability, and low switching power. One difficulty with SOA is the operating speed, which is limited by the slow gain recovery time of about 100 ps. It has been found that the SOA response can be improved by installing a detuned optical filter at the SOA output so that the slow gain recovery components can be removed. This scheme has been applied to 640 to 40 Gbit/s demultiplexing. However, the switching performance includes a large penalty because of the distortions in the switching gate induced by residual slow recovery components and the excessive loss caused by the optical filtering.

2.5 SOA based MZI Architecture

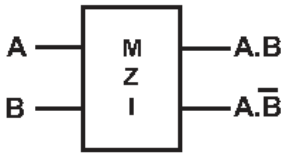
An optical MZI switch can be designed [17] using two Semiconductor Optical Amplifiers (SOA-1, SOA-2) and two couplers (C-1, C-2) as shown in Figure 2(b),(c). MZI switch has two inputs ports namely, A and B and two output ports called as bar port and cross port, respectively. The optical signals coming at port B and port A at the input side are control signal (λ2), and incoming signal (λ1),respectively. The working principle of a MZI is explained as follows:

When there is a presence of incoming signal at port A and control signal at port B, then a light would appear at the output bar port and no light would appear at the output cross port. Again on absence of control signal at input port B and presence of incoming signal at input port A, the light would appear at the output cross port and no light would appear at the output bar port.

The logic value of the absence of light and presence of light is denoted by 0 and 1, respectively. From the point of view of Boolean function, the above behaviour of MZI switch can be written as P (Bar Port) =A.B and Q (Cross Port) =A .



(h) Semiconductor Optical Amplifier based MZI



(i) Functional behaviour of MZI switch

Figure 2(h),(i) : SOA based MZI switch

2.6 Synthesis of Boolean Function using MZI gates:

As MZI gates can produce AND operation and NOT operations and Beam Combiner produce OR Operation, they are sufficient to synthesis any Boolean function. For example, An EX-OR realization of *x* & *y* using MZI gates, a combiner and two splitters is shown in Figure 2(j).

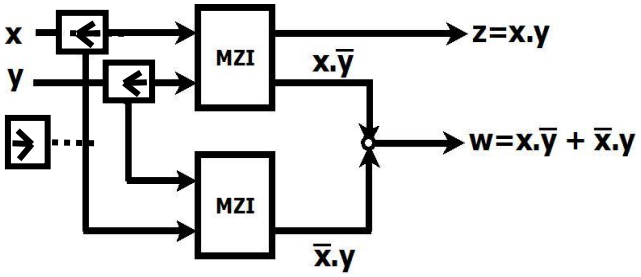


Figure 2(j): shows the EX-OR realization of *x & y*

Chapter 3

All Optical Implementation of Mach Zehnder Interferometer based Carry Look Ahead Adder circuit

3.1. Introduction

In this thesis, we propose all-optical implementations of Carry-Lookahead Adder (CLA), which is a fast carry propagation enhancement using Mach-Zehnder Interferometer (MZI). Analysis and discussion on the complexities of the designs and mathematical models are also presented. Finally, to check the efficacy of our proposed circuits, we have compared our design's cost parameters with related works data for fair evaluation.

We first discuss the implementation of ripple carry adder with MZI switches. Then we proposed our design of Carry Lookahead Adder using MZI switches.

3.2. Parallel Adder Circuit with MZI

In this section, we discuss about all-optical implementation of a binary adder using MZI switches. Figure 3(a), denotes a simplified diagram of the binary adder, in which A and B which are the two inputs are added, input carry is denoted by C_{in}, sum is denoted by S, and the output carry is denoted by C_{out}.

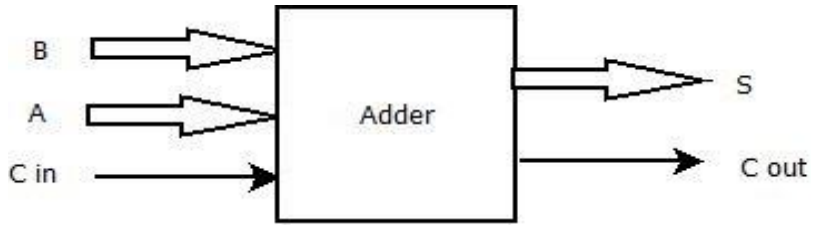


Figure 3(a): Simplified diagram of the binary adder

Full adders are needed as the basic building block to design a binary adder. Now we will draw the design of all-optical SOA based MZI based full adder (FA), parallel adder and carry look-ahead adder with an enhancement for faster carry propagation, along with their respective optical cost and delay analysis.

3.2.1 All-optical implementation of full adder

In this subsection we will discuss about implementations of binary adders using all-optical implementations of full adder (FA). Figure 3(b) denotes the simplified diagram of an all-optical full adder which consists of 4 MZI switches, 4 beam splitters or BS (denoted as solid dots), and 3 beam combiner or BC (denoted as hollow dots). Optical attenuator is used to maintain a constant power level of the incoming signal of MZI in each stage.

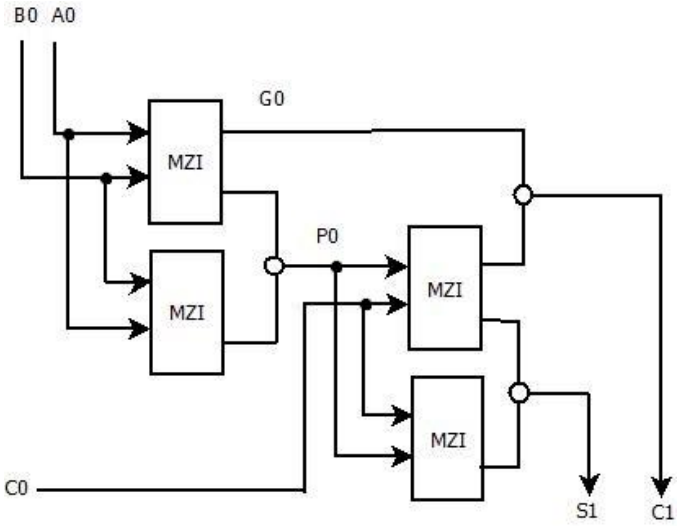


Figure 3(b): Full adder using MZI switch.

3.2.2 Implementation of Parallel adder

Figure 3(c) denotes the optimized design of 4-bit Parallel adder circuit using MZI switches. This circuit consists of four full adder circuits. The inputs to the 4 bit Parallel adder are A ($a_3a_2a_1a_0$), B ($b_3b_2b_1b_0$) and c_0. Here c_0 will acts as an input carry. This 4-bit Parallel adder performs addition of two 4 bit binary numbers. The outputs from the Parallel adder are sum (S) and carry(C). We will deduct the following relations from Figure 3(f).

$S_0 = P_0 \oplus C_0$, where $P_0 = a_0 \oplus b_0$ and $C_0 = c_0$

$S_1 = P_1 \oplus C_1$, where $P_1 = a_1 \oplus b_1$ and $C_1 = G_0 + P_0C_0$

$S_2 = P_2 \oplus C_2$, where $P_2 = a_2 \oplus b_2$ and $C_2 = G_1 + P_1C_1$

$S_3 = P_3 \oplus C_3$, where $P_3 = a_3 \oplus b_3$ and $C_3 = G_2 + P_2C_2$

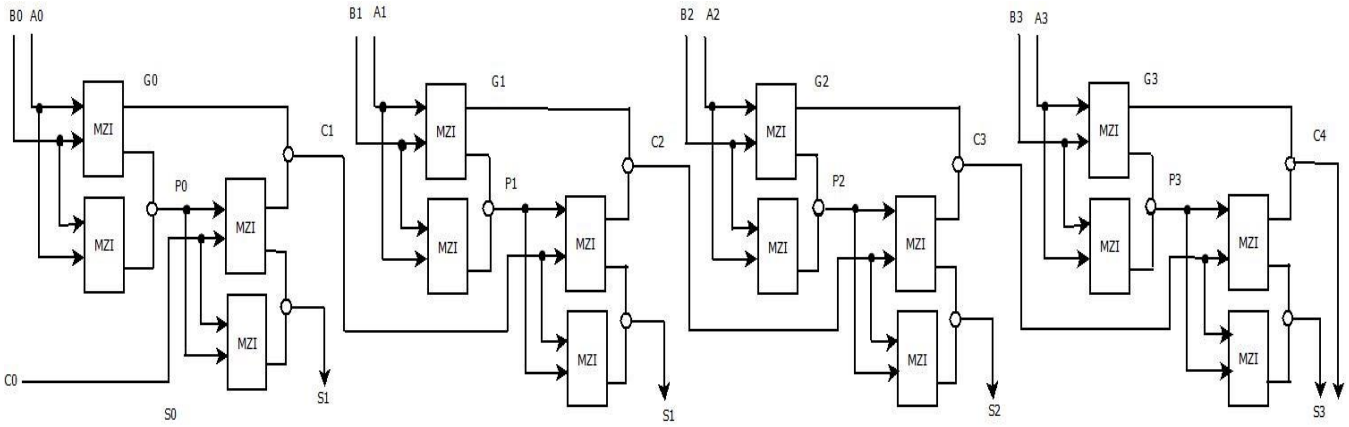


Figure 3(c): implementation of 4 bit Parallel Adder using Mach Zehnder Interferometer

3.3 *Proposed all-optical realization of CLA*

In this sub-section, we introduce the proposed design for all-optical CLA circuits. The expressions for CLA are mapped to the equivalent net lists of optical gates. The proposed all-optical designs for CLA utilize non-modular staircase like sub-circuits which finally leads to the improved all-optical realizations of CLAs.

The problem in the CLA design using MZI gates is that the MZI gates beam splitters and beam combiners have only two inputs. We cannot consider any AND gate or OR gate of more than two inputs. Thus as in the traditional logic gate, the carries are generated using multi-input AND gates in one level, it is not possible here.

To design AND gates with m inputs we require $\lceil \log n \rceil$ levels of MZI gates. For example if we like to design $P_3P_2P_1G_0$ for traditional design it becomes as shown in the Figure 3(f) but in case of MZI it is realized as in Figure 3(g).

The implementation of the expression of carries as given in Section 3.5 may be done in several ways. As the goal of CLA is achieving the speed, our first target is to minimize the delay. Obviously this delay is $\lceil \log n \rceil$ as expressions for C_n requires an AND gate realization of n inputs which needs to be implemented by a tree of MZI gates of $\lceil \log n \rceil$ levels. Keeping this value $\lceil \log n \rceil$ as maximum allowable delay, we now try to optimize the number of MZI gates. Thus this carry generator part requires at least $\lceil \log n \rceil$ levels for an n input adder. We now use the following algorithm to generate the carries of different levels as defined in the section using only MZI gates, beam splitter and beam combiner.

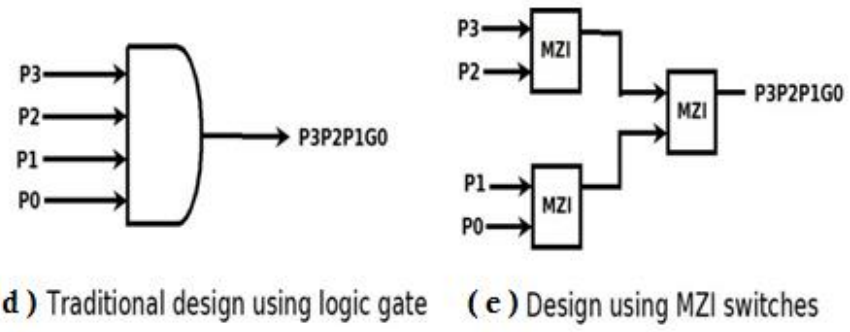


Figure 3 (d),(e) : Realization of $P_3P_2P_1G_0$ by traditional and MZI

3.3.1 Algorithm for Carry Generator:

Input : The set of P_i's and G_i's ($0 \le i \le n-1$),

where $P_i = a_i \oplus b_i$ and $G_i = a_i . b_i$

Output: Carries $C_1, C_2, \ldots\ldots, C_n$

1. Initialization:

for $j = 1$ to $n-2$ $\quad p^1_{0,j} = P_j$;

for $j = 0$ to $n-1$ $\quad g^1_{0,j} = G_j$;

2. for $i = 1\ to\ (\lceil \log n \rceil - 1)$

for $j = 2^i$ to $n-2$

$$p^2_{i,j} = p^{2^{i-1}}_{i-1,j} . p^{2^{i-1}}_{i-1,j-2^{i-1}} ;$$

3. for $i = 2\ to\ (n-1)$

for $j = i-1\ to\ (n-2)$

$$g^j_{\lceil \log i \rceil, j} = p^{2^{\lceil \log i \rceil - 1}}_{\lceil log\ i \rceil - 1, j} * g^{2^{\lceil \log i \rceil - 1}}_{\lceil \log i \rceil - 1, 2^{\lceil \log i \rceil - 1} + (j-i)} ;$$

4. $C_n = \sum g^i_{\lceil \log i \rceil, (n-1)}$

where $i = 1\ to\ n$ and $\sum$ represents the OR operation.

5. End of the algorithm.

Each $p_{i,l}^{2^i}$ $(1 \leq i \leq \lceil \log n \rceil - 1)$, $(2^i \leq l \leq n-2)$ obtained in step-2 of the algorithm is realized by an MZI gate to produce AND operation. Similarly, each $g^{i}_{\lceil \log i \rceil, j}$ obtained in step-3 of the above algorithm is realized by an MZI gate to produce AND operation. Each C_i obtained in step-4 of the algorithm is implemented by beam combiners. We are using some beam splitters as shown in Figure 2(b), when any signal line is used more than once. The sum-result is obtained by EX-OR gates as shown in Figure 3(c) and each EX-OR gate can be implemented as shown in previous chapter, Figure 2(g) .

A complete adder circuit for 4-inputs is shown in Figure 3(f) using MZI gates , combiners and splitters.

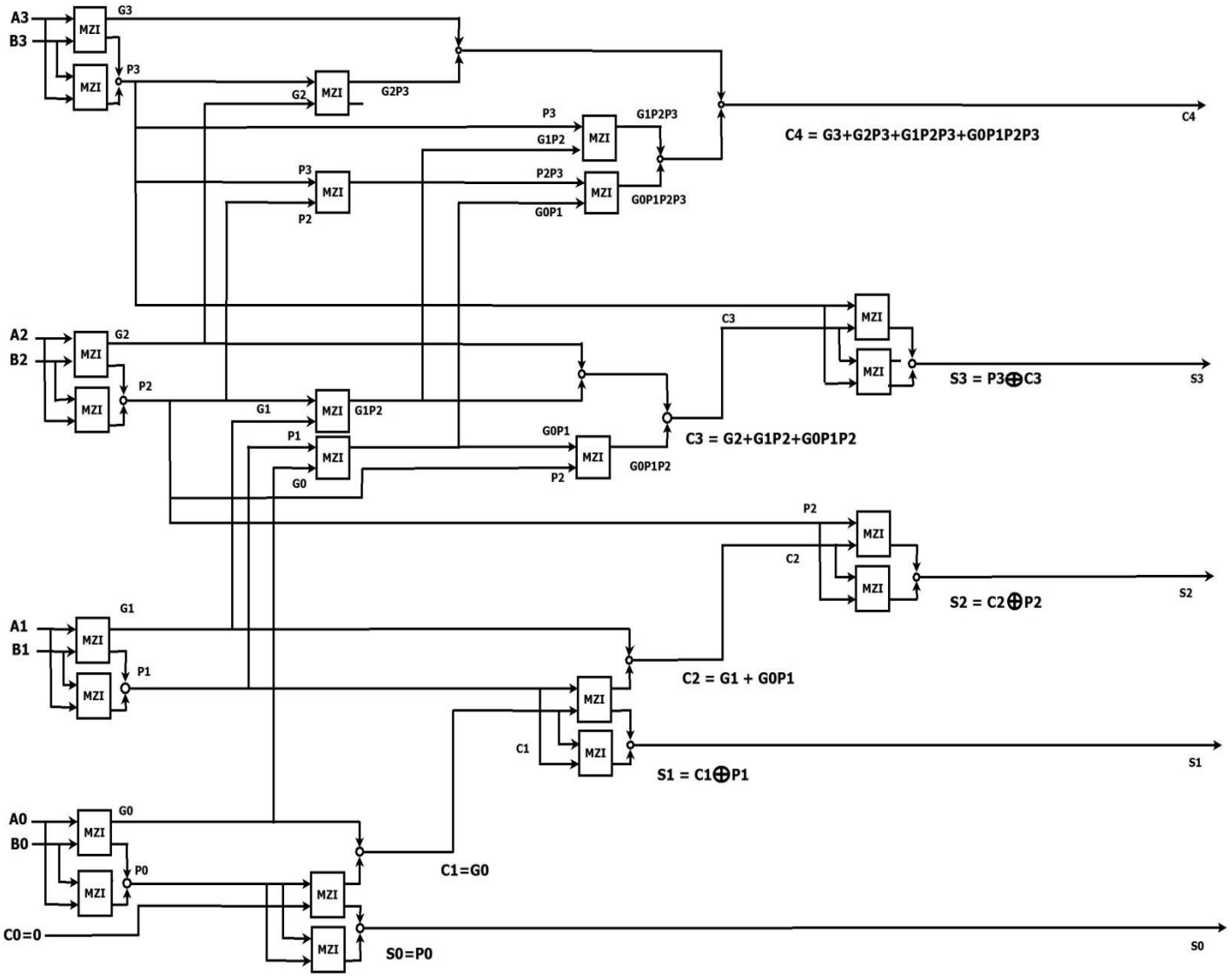


Figure 3(f) : Implantation of 4 bit Carry Look-ahead Adder using Mach Zehnder Interferometer

A complete adder circuit for 8-inputs is shown in Figure 3(g) using MZI gates , combiners and splitters.

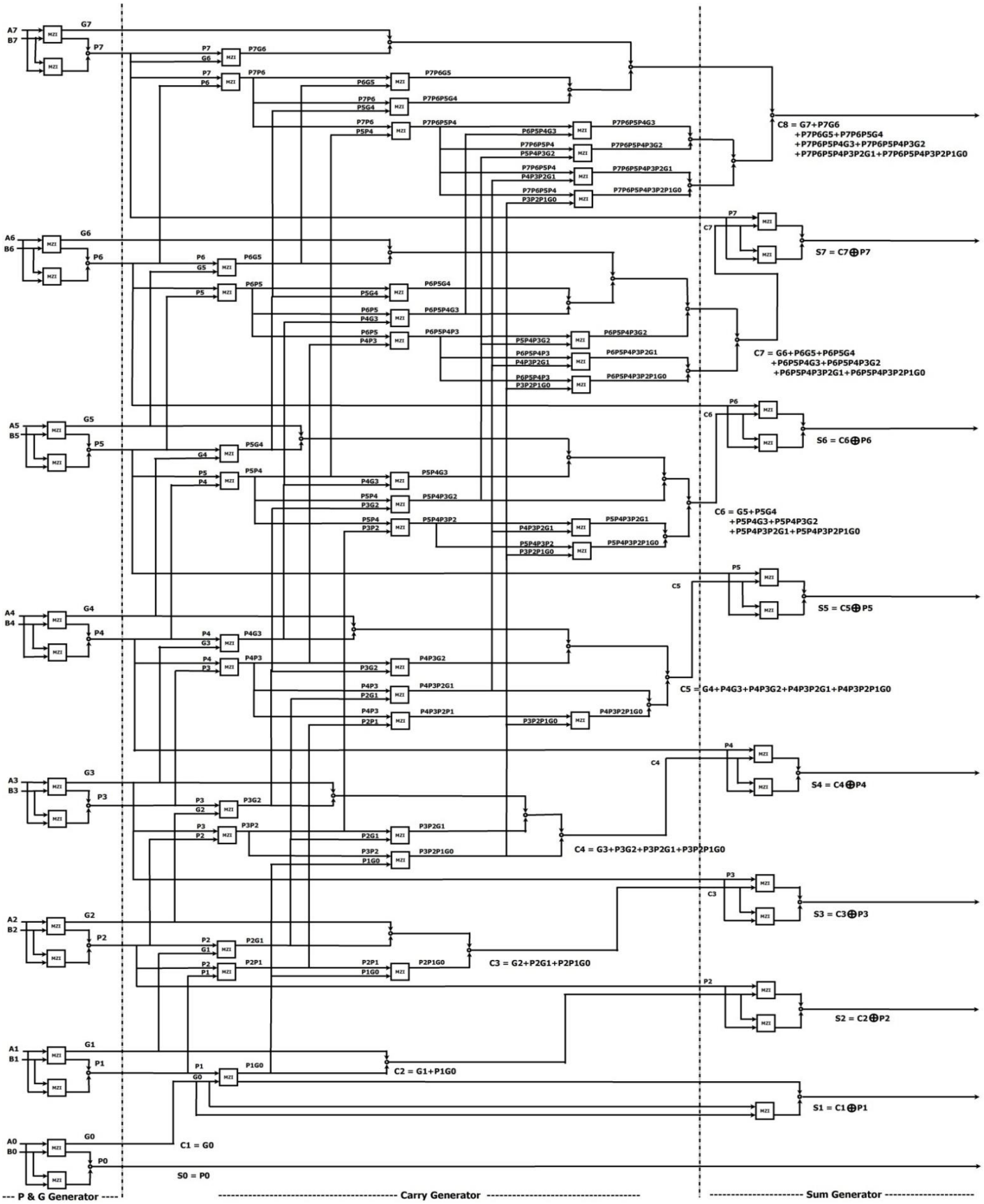


Figure 3(g): All-optical realization of 8-bit Carry-Lookahead Adder using Mach Zehnder interferometer

3.3.2. *Parameter Calculation for CLA*

Optical cost and delay:

As the optical cost of beam splitter and beam combiner are relatively small, the optical cost of a given circuit is the number of MZI switches required to design that circuit.

Figure 3(g) shows the complete realization of our proposed 8 bit Carry Look-ahead Adder.

Lemma 1: The number of MZI gates for the proposed design for an n-input adder is $\frac{n^2}{2} + n\lceil \log n \rceil + \frac{5n}{2} - 2^{\lceil \log n \rceil} - 1$.

Proof: The 1st stage (P & G generator) of Figure 3 requires *2n* MZI gates.

For the carry generator, the 2nd step of the **Algorithm Carry Generator** produces the number of gates

$(n-2) + (n-2^2) + (n-2^3) + \cdots + (n-2^{\lceil \log n \rceil - 1})$

$= n\lceil \log n \rceil - n - 2^{\lceil \log n \rceil} + 2$

For the 3rd step of algorithm the number of AND gates produced is $= (n-1) + (n-2) + \cdots + 1) = \frac{n(n-1)}{2}$

The 3rd step of Figure 3 requires $2(n-1) - 1$ AND gates. One AND gate P_1G_0 is actually produced in the first step of the algorithm.

Thus the total number of gates

$= 2n + n\lceil \log n \rceil - n - 2^{\lceil \log n \rceil} + 2 + \frac{n(n-1)}{2}$

$= \frac{n^2}{2} + n\lceil \log n \rceil + \frac{5n}{2} - 2^{\lceil \log n \rceil} - 1$ □

If $\lceil \log n \rceil =$ integer then,

$\frac{n^2}{2} + n\lceil \log n \rceil + \frac{5n}{2} - n - 1 = \frac{n^2}{2} + n\lceil \log n \rceil + \frac{3n}{2} - 1$

Lemma 2: The delay of MZI adder is $\lceil \log n \rceil + 2$.

The optical delay is estimated as the number of stages of MZI switches multiplied by a unit Δ. The P & G generator and sum generator requires one unit delay each. The carry generator requires ⌈log n⌉ units Δ. Hence the result. □

The Table 1 shows the comparison of different all-optical carry look-ahead adder with respect to delay and number of MZI gates. We have compared the result with an earlier work [18], [19] and [20]. The 2nd and 3rd columns in the Table 1 represent the result of [18], [19] and [20] and our work respectively.

The Table 2 shows the comparison of three adder designs with respect to different values of $n = 8, 16, 32, 64$. The first column in Table 1 represents the value n. The 2nd, 3rd, 4th and 5th columns in the table 2 represent the delay in [18], [19], [20] and proposed work respectively. The 6th, 7th, 8th and 9th columns represent the number of MZI gates required in [18], [19], [20] and proposed work respectively. As evident from the result our design is very efficient with respect to speed.

Table 1: Comparison of different All-Optical Carry Look-ahead Adder with respect to number of MZI gates and delay.

	[18]	[19]	[20]	Proposed Work
Delay	$n+3$	$3n+1$	n	$\lceil \log n \rceil + 2$
No of MZI	$6n$	$6n+1$	$2n$	$\frac{n^2}{2} + n\lceil \log n \rceil + \frac{5n}{2} - 2^{\lceil \log n \rceil} - 1$

Table 2: Shows the comparison of different All-Optical Carry Look-ahead Adder $n = 8, 16, 32, 64$

n	Delay				No of MZI			
	[18]	[19]	[20]	Proposed work	[18]	[19]	[20]	Proposed work
8	11	25	8	5	48	49	16	67
16	19	49	16	6	96	97	32	215
32	35	97	32	7	192	193	64	719
64	67	193	64	8	384	385	128	2527

Chapter 4

Conclusion and Future work

Conclusion and Future work

In this thesis, an efficient all-optical realization of Carry Look-ahead Adder(CLA) is proposed using Mach–Zehnder Interferometer (MZI) based switches along with analysis of the corresponding costs and delays. Design complexities presented ensure minimum delay in all optical carry look-ahead adder circuit realization. Our design technique has been compared with recently reported design techniques. The experimental results confirm the efficacy of the proposed design over similar existing designs with respect to speed. Though the number of MZI gates is more in our design, the low power properties of MZI gates do not demand much power. The work may be extended to find the techniques to reduce the number of MZI gates. The application of amplifiers may be done to improve the signal strength.

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