B.E. INSTRUMENTATION AND ELECTRONICS ENGINEERING
SECOND YEAR SECOND SEMESTER - 2019
ELECTRONIC CIRCUITS 1

Time : **Three hours** Full Marks : **100**

Answer any four questions

1. (i) Assuming the constant voltage model of a diode, plot the input output characteristics of the circuits shown in Fig. 1a, Fig 1b and Fig 1c respectively.

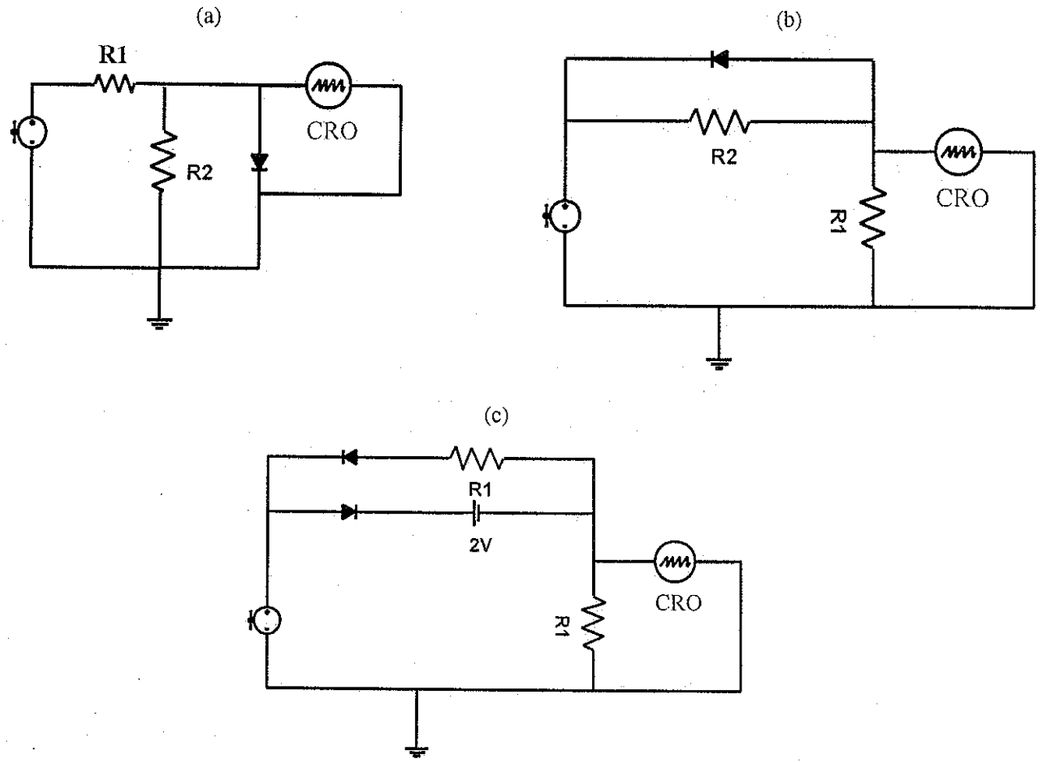

Figure 1

(ii) A sinusoidal signal $V(t) = V_0 + V_P \cos\omega t$ is applied across a diode. Considering $V_P << V_T$, determine the resulting diode current.

(iii) Design a full-wave rectifier to deliver an average power of 2 W to a tablet with a voltage of 3.6 V and a ripple of 0.2 V.

$(5 \times 3)+3+7=25$

2. (i) Find the transistor (β =100, I_{CB0} =20 nA and V_{BE}=0.7 V) currents (I_E, I_B and I_C) in the circuit shown in Fig. 2a. Also find the region of operation of the transistor as per its output characteristics.

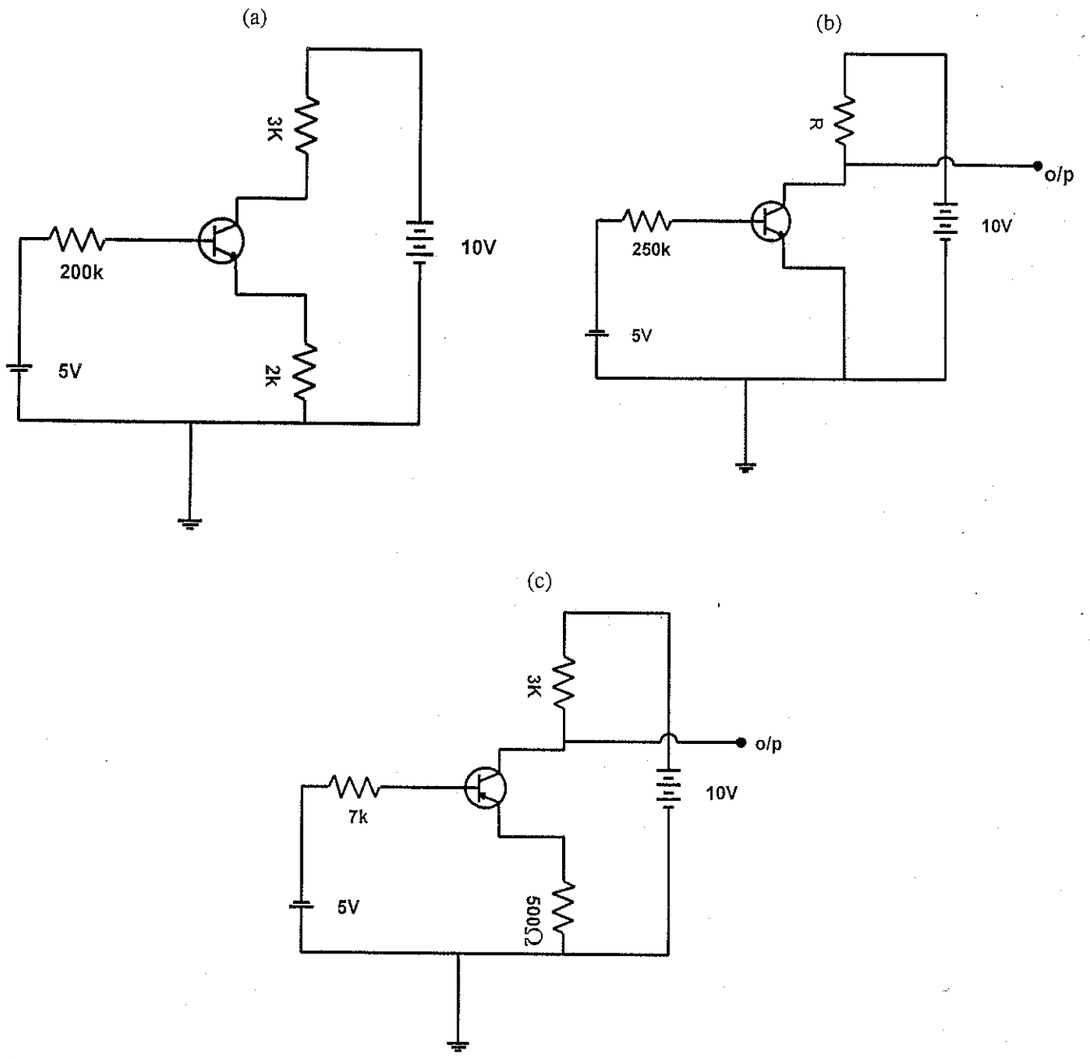

Figure 2

(ii) What is the maximum value of the collector resistance in the circuit shown in Fig. 2b such that the transistor will be saturated ? Consider β =100, V_{BE} =0.8 V and V_{CE} =0.2 V.

(iii) Find the output voltage of the circuit shown in Fig. 2c considering the same value of β, V_{BE} and V_{CE}.

(iv) Design a circuit using only diodes (constant voltage) and 10 kΩ resistors to provide an output signal limited to -2.17 V and above.

(v) Assuming the constant voltage model of a diode, design a two sided limiting circuit which can drive a 1 kΩ load with nominal limiting levels of ±3 V and having a voltage gain of 0.95 V in the nonlimiting region.

(3+2)+5+5+4+6=25

3. (i) What is the value of the emitter current in the circuit shown in Fig. 3a ?

(ii) Find the output voltage and the emitter current of the circuit shown in Fig. 3b.

(iii) If the collector voltage is -4V, find the emitter voltage in the circuit shown in Fig. 3c.

(iv) Find the emitter current and V_1 in the circuit shown in Fig. 3c.

(v) A pnp transistor has v_{EB} =0.8 V at a collector current of 1A. When i_C =10 mA, what should v_{EB} be ?

5 × 5=25

4. (i) A pnp transistor is biased to operate at I_C=2 mA.

(a) What is the associated value of g_m ?

(b) If β=50, what is the value of r_e seen looking into the emitter ?

(c) How does this resistance change when looked into the base ?

(d) If the collector is connected to a 5 kΩ load, with a signal of 5 mV(p-p) applied between the base and emitter, what is the resultant output ?

(ii) A transistor ($50 \geq \beta \leq 200$) operating with nominal g_m of 60 mAV has a ±20 % variation in I_C. Find the extreme values of the resistance while looking into the base.

(iii) The transistor in the circuit shown in Fig. 4a, has β=100.

(a) What is the dc collector current and the dc voltage at the collector ?

(b) Draw the small signal equivalent circuit of this amplifier.

(c) What is the voltage gain ?

(iv) For the amplifier shown in Fig. 4b,

(a) what should should be the value of I so that the input resistance at E is equal to that of the source ?

(b) What is the resulting voltage gain from the source to the load ?

(v) A particular BJT operating at I_C=2 mA has C_μ=1pF, C_π=10pF and β=150. Find the value of f_T and f_B for this situation.

(2 × 4) + 3 + (2+4+2) + (2+2) + 2 = 25

5. (i) An n-channel JFET operating in the active region carries a drain current of 4 mA when V_{GS}=-2V, and a drain current of 6 mA, when V_{GS}=-1V.

(a) Calculate the pinch-off voltage.

(b) Calculate the saturated drain current for V_{GS}=0V.

(c) If V_{DS}=10V, find the channel resistance for V_{GS}=-2V, -1V and 0V.

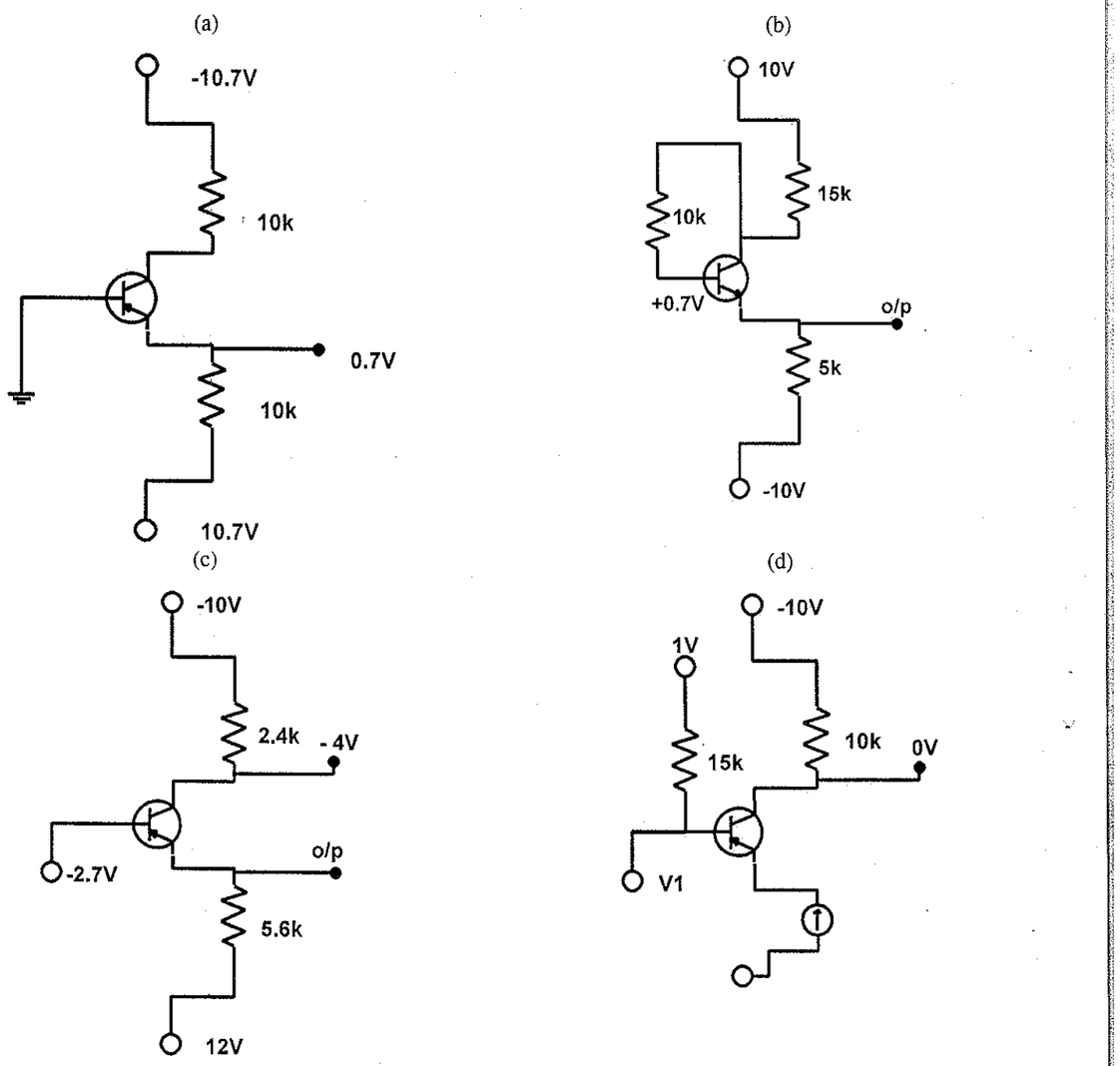

Figure 3

(ii) The transconductance and the ac drain resistance of a FET are 0.2 mA/V and 150 kΩ respectively. What is the small-signal voltage gain when this device is used in the CS configuration with a load resistance of 150 kΩ ?

(iii) A small-signal common-source FET amplifier has a variable load resistance R_L. For what value of R_L will the ac power dissipated in the load be maximum ?

(iv) For a constant V_{GS}, the drain current of an FET changes by 20 μA when V_{DS} is changed by 2V. What is the ac drain resistance of the FET ?

(v) Draw the equivalent circuit of the one shown in Fig. 5a and find the small signal voltage gain with $g_m = 4 \times 10^{-3}$ mS and r_d =70 kΩ. Consider the capacitive reactances to be negligible at the operating frequency.

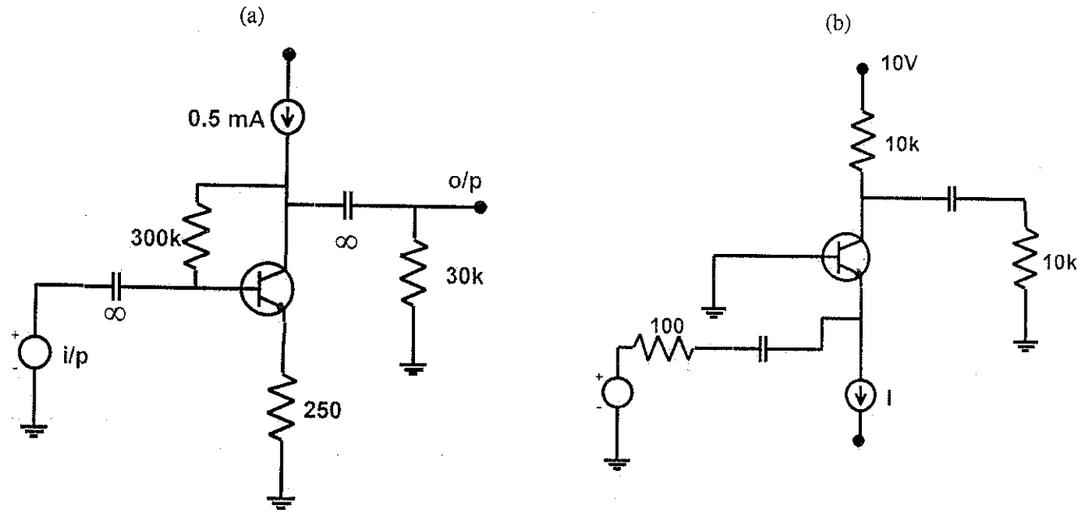

Figure 4

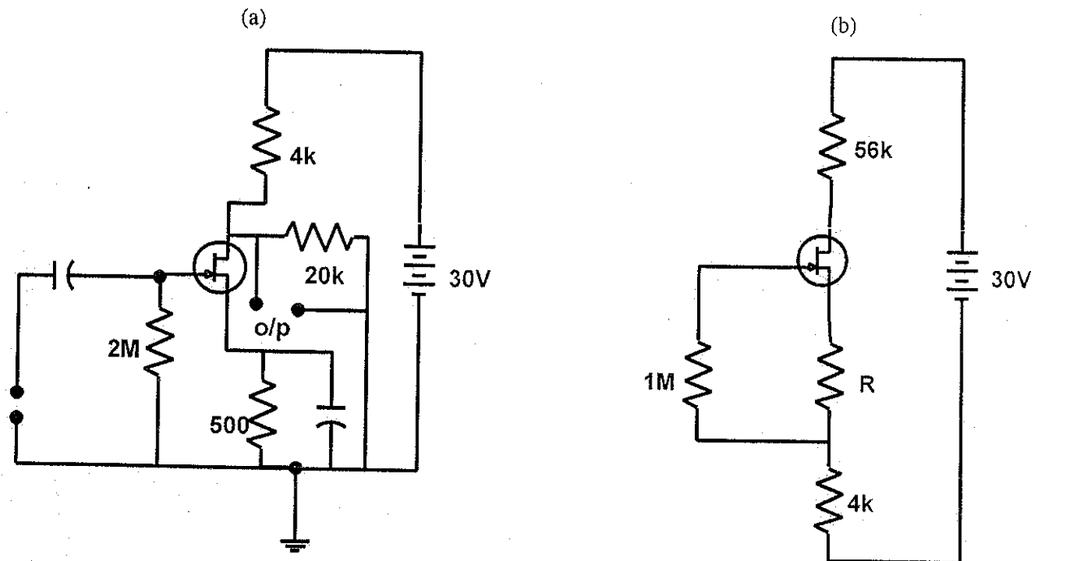

Figure 5

(vi) For the circuit shown in Fig. 5b, calculate the resistance R such that the quiescent value of V_{DG} =16 V. Find the transconductance at this point. Given I_{DSS} =1 mA and V_p =-1 V.

(2+2+3) + 3 + 3 + 2 + 5 + 5= 25