Bachelor of Instrumentation and Electronics Engineering, 2019
2nd year, 2nd semester
DIGITAL ELECTRONICS

Time : Three hours **Full Marks : 100**

ALL MODULES ARE COMPULSORY.

Module – I (4 Marks)

Q1. (a) Convert $(408C1.D6)_{16}$ to **base-4** system.

(b) What are Self-Complementing BCD codes ? Give an example. (2+2)

Module – II (6 Marks)

Q2. Perform the following arithmetic operations :

(a) **(-39) + (-28)** using **7-bit 2's** complement number system.

(b) **(9659) + (6738)** using **Normal BCD** system. (3+3)

Module – III (40 Marks)

(Answer **Any TWO** from Q3, Q4 and Q5)

Q3. (a) Draw the **p-MOS** circuit which realizes the following function :

F(A, B, C) = A'C' + ABC

(b) What logic function is realized by the circuit shown in **Figure P3(b)** ?

(c) In **Figure P3(c)**, a circuit is implemented using one **4:1 MUX**. What is the function, **F**, available at its output in minimal form ?

(d) Realize a **two input XNOR** function using **only two 2:1 Multiplexers**.

(5 + 5 + 5 + 5)

Q4. (a) Can we use the hypothetical logic Gate shown in **Figure P4(a)** as one **Universal Logic Gate** ? Explain.

(b) In the circuit shown in **Figure P4(b)**, if the output required is **F = A'B'C + A'B'D**, what type of gates are **G1** and **G2** ?

(c) Using **a** suitable **decoder** and necessary **OR-gates** realize a **full-subtractor**. Use **proper** input and output **signal names**.

(5 + 5 + 10)

Q5. Using **Quine-McCluskey's tabular method**, obtain the **minimized SOP** realization for the function :

$$F(A, B, C, D) = \sum m(0, 1, 2, 7, 9, 13, 15) + d(8, 10, 14)$$

(a) **ignoring** combinational hazard, and

(b) **removing** combinational hazard.

(15 + 5)

Module – IV (50 Marks)

(Answer **Q6 and Any TWO** from Q7, Q8 and Q9)

Q6. (a) In the circuit shown in **Figure P6(a)**, the flip-flops have **set-up time of 5 nSec** and a worst case **clock-to-output delay of 10 nSec**. The **AND gate** has a delay of **5 nSec**. What is the **maximum possible clock rate** for the circuit to operate faithfully ?

(b) Find out the count sequence ($Q_2Q_1Q_0$) for the circuit shown in **Figure P6(b)**. Assume initially all the three memory elements were in reset state.

(c) The circuit shown in **Figure P6(c)**, performs a certain function. Derive an expression for the next state Q_{n+1} **in terms of X and** previous state Q_n.

(5 + 10 + 5)

Q7. (a) What is the "**decoding spike problem**" ? How can it be **avoided** ?

(b) Using **SR-flip flop** as the memory element realize a sequential **binary to gray code converter**. The input binary bits are coming serially starting from the MSB.

(5 + 10)

Q8. Realize a sequence detector circuit which produces a logic 1 output whenever it detects a sequence "**110**". The output is zero otherwise. Use **T-Flip flops** as the memory elements. Is there any **lock-out possibility** in your design ?

(14 + 1)

Q9. Design a **sequence generator** which generates the sequence **... 100110...** repeatedly. Use **minimum number of D-Flip flops**.

(15)

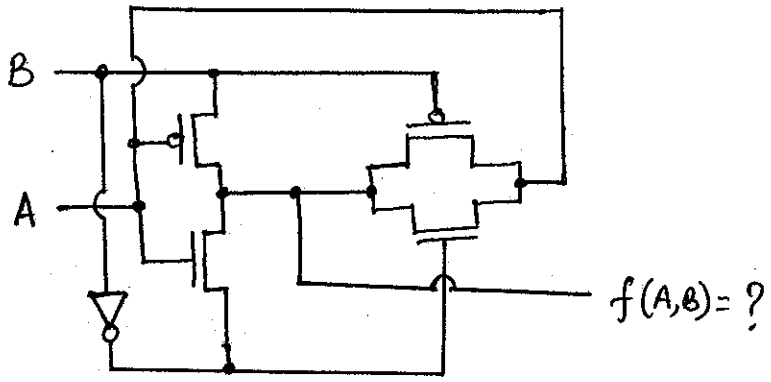

FIGURE P3(b)

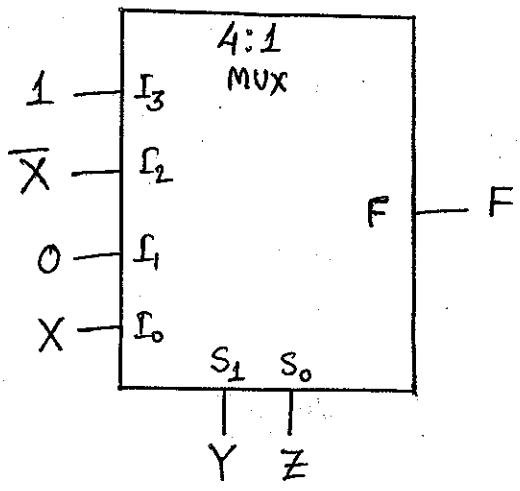

FIGURE P3(c)

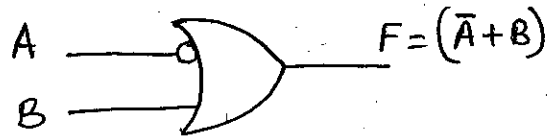

FIGURE P4(a)

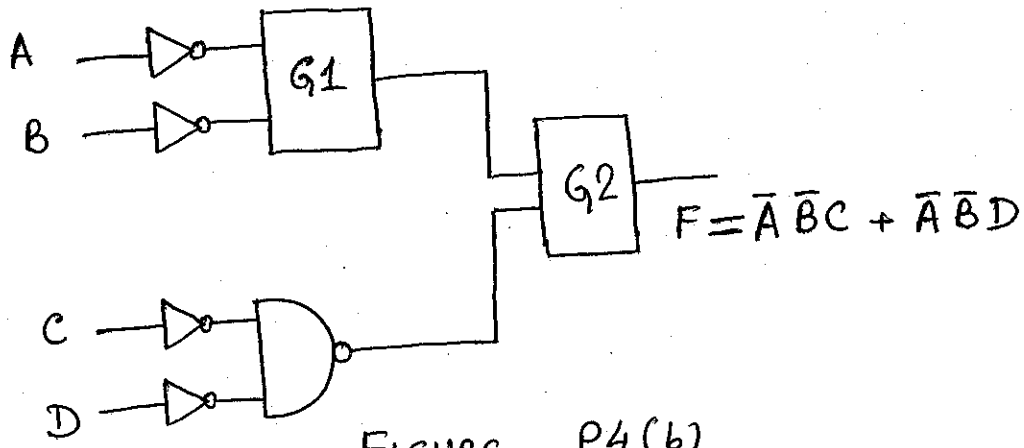

FIGURE P4(b)

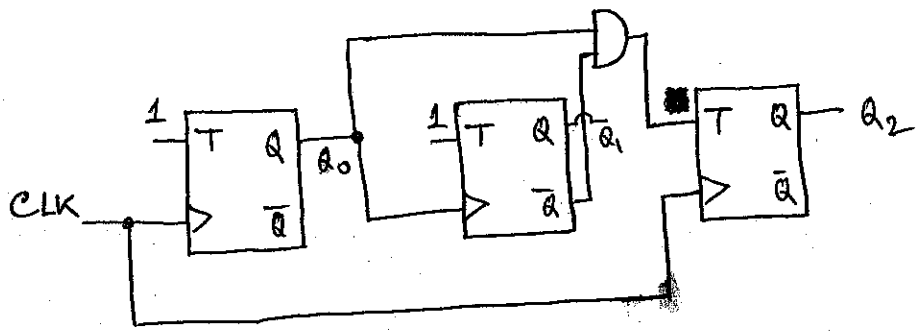

FIGURE P6(a)

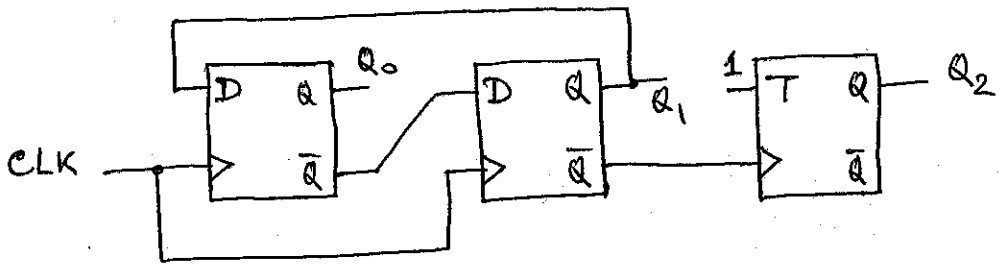

FIGURE P6(b)

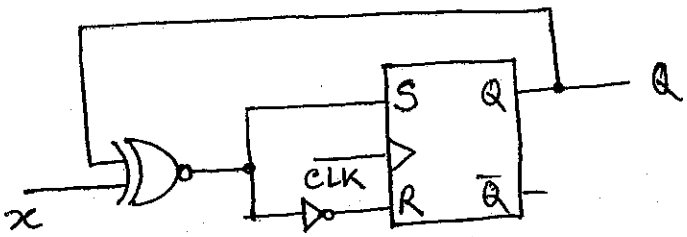

FIGURE P6(c)