BE INFO TECH 2nd YEAR 1st SEMESTER EXAMINATION, 2019

Computer Architecture

Time: 3 Hours

Full Marks: 100

Answer Any Five

1.a) Write (-153) in binary using 3 major representations viz., Sign-Magnitude, One's Complement and Two's Complement number systems both in 8 bit format and 16 bit format.

b) Convert the Decimal number (20.8125×10^{-2}) to Binary (not more than 8 bits after the binary point). Also convert the Binary fraction (1010.0101×2^{-3}) to Decimal.

c) Represent 0.075 as per IEEE 754 Half Precision Formats, Single Precision Formats and Double Precision Formats.

d) Write your understanding about UNUM (Universal Number) briefly.

(6+4+6+4)

2. a) Using proper diagram, illustrate the concept of Memory Interleaving.

b) Using proper diagram, illustrate the concept of 'Set-associative Mapping' in a cache.

c) Using proper diagram, illustrate how 64Kbyte of memory can be achieved using (16K x 1) memory chips.

(6+8+6)

3.a) Draw the internal diagram of a CPU (having Single Bus Organization) clearly showing all the different components.

b) With respect to the above diagram, show the sequence of micro-operations performed by CPU to do the following operation.
"To load the contents of R1 into the memory location specified by R2".

c) Draw the detail block diagram of the control unit of a CPU and explain it.

d) Briefly explain the following terminologies:
Control Word, Control Store, Microroutine, Microinstruction.

(6+4+5+5)

4.a) For a CPU which supports 'Zero-Address' instruction format, write down a set of assembly language instruction which will evaluate the expression X = (A+(B*W)) * (C+(D/Y)). All values are available in the memory; also the result has to be stored back in the memory.

b) The current values of different registers are R1=2, R2=4, R3=0, R4=5 and R5=2. What will be the values of the different registers after executing the set of instructions shown below and why? Please note that the first instruction of the set is a "register immediate" instruction.

MOV 9, R3; ADD R1, R4; MOV R4, [R5];

c) With proper instruction example, illustrate your understanding about "Base with Index and Offset Addressing".

d) Typical example of an "Index Addressing" instruction is LD ADR(X). For a "32bit data and address" CPU, what will be the minimum byte length of this instruction and why? Also, explain this instruction with suitable example.

(6+4+4+(3+3))

5.a) With proper examples and diagram, illustrate your understanding about "Interrupt Driven I/O".

b) There are three types of I/O transfer; Programmed Controlled I/O, Interrupt Driven I/O and DMA based on I/O. But DMA includes all three types of I/O. Explain this.

c) Using proper diagram, illustrate how bits are stored in the CD-ROM so that reading and writing on the CD-ROM can be done.

d) Using proper diagram, illustrate how data are stored in the Magnetic Tape.

(5+5+4+6)

6.a) With proper diagram, illustrate how disks are organized in RAID0 and RAID5.

b) Draw a 3-D Mesh Network of dimension 3. Also, compute their basic characteristic parameters.

c) Explain how Cache Coherency problem gets solved in a Centralized Multiprocessor type of machine.

d) With proper diagram, illustrate how Directory Based Protocol works for NUMA type of Multiprocessor machine.

((2+3)+(3+2)+5+5)

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