Ex/IT/IEE/T/123/2019 (Old)

JADAVPUR UNIVERSITY

B.E. INFORMATION TECHNOLOGY

1st Year, 2nd Semester Examination 2019 (Old)

DIGITAL LOGIC & DIGITAL CIRCUIT **Time : 3 hours** **Full Marks : 100**

General instructions (read carefully)

1. *Special credit will be given to answers which are brief and to the point.*
2. *Answer to every question should start on a new page.*
3. *Do not write answers to various parts of a question at different locations of your answer-script.*
4. *Do not write on the front back cover of your answer booklet.*

Question No. 1 is compulsory. Answer any 4 (four) from the rest.

Each question carries 20 marks. Question for each sub-part is mentioned at the right margin of a part question or set of part questions.

1. Answer ***any 10 (ten)*** of the following questions. Be specific and very brief in answering each question. (10 X 2)

i) Find the binary equivalent of the decimal number 19.875 ?
ii) Add two binary numbers A and B, where A = 1 0 0 1 1 0 and B = 0 1 1 1 0 1
iii) The solution to the quadratic equation $x^2 - 11x + 13 = 0$ (in number system with radix r) are x = 2 and x = 4. Then the base (r) of the number system is ?
iv) Simplify the Boolean expression Y = A B' C + (B' + C') (B' + D') = (A + C + D)'
v) The circuit that will work as OR gate in positive logic will work as _____ gate in negative logic.
vi) Which code is used in K-map for representing the minterm ?
vii) What will be the number of select lines in a 32 X 1 multiplexer ?
viii) In a D type latch ENABLE input is HIGH and D = 1. The output will then be ?
ix) How can we construct a D flip flop using an SR flip flop ?
x) The initial state of a MOD 16 down counter is 0 1 1 0. The state after 37 clock pulses will be ?
xi) A 5 (five) bit ripple counter uses flip-flops with propagation delay of 40 ns each. What is the maximum clock frequency that can be used ?
xii) There are how many address and data lines in a 2048 X 8 PROM ?
xiii) Distinguish between volatile and non-volatile memory with examples.
xiv) Which digital logic family has the highest speed ? At the expense of what other parameter (any one) ?

2. i) Convert the following decimal numbers to binary numbers and add them using 2's complement method (– 6 4 and + 4 6). (2 + 2)

ii) State and prove DeMorgan's Theorem. (2 + 2)

iii) Simplify the following function using Karnaugh map (5)

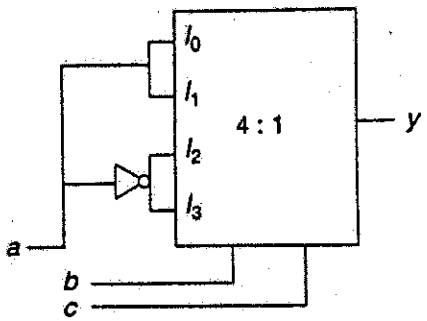
$$Y = \sum m\,(0, 2, 3, 6, 7, 8, 10, 11, 12, 15)$$

iv) Prove NOR gate as a universal gate. (3)

v) Implement XOR gate using a) basic gates, and b) minimum number of NAND gates. (4)

3. i) Design an 8:1 MUX using 4:1 and 2:1 MUXes. (4)

ii) Find the output of the circuit shown. (4)



iii) Implement the digital circuit of a Full Subtractor using (9)

a) only logic gates
b) 4 X 1 multiplexer
c) 3 to 8 decoder.

iv) Tabulate the differences between combinational and sequential digital circuits. (3)

4. i) Explain the operation of an SR latch using NAND gate. (4)

ii) Explain the operation of an JK flip-flop using NAND gates, with the help of neatly labelled diagram and truth table. (6)

iii) Mention any two applications of flip-flops. (2)

iv) Design an asynchronous modulo 10 (decade) counter using JK flip-flops. (8)

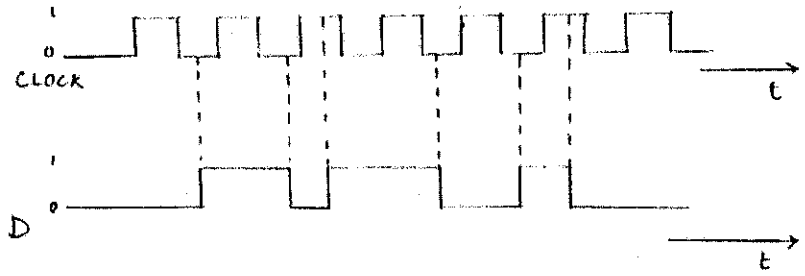
5. (i) For a master-slave D flip-flop, with a uniform CLOCK signal and with input waveform D, as shown below, draw the output waveforms at the (4 X 2½)

a) master Q output, Q_M

b) slave Q output, Q_S

c) output Q_P, when the flip-flop is positive edge triggered,

d) output Q_N, when the flip-flop is negative edge triggered.



(ii) Design an asynchronous (ripple) counter using JK flip-flops to count from **6** to **14**. (10)

6. (i) Design a 3 (three) bit synchronous counter using JK flip-flops and explain its operation. What are the advantages of such a counter over a ripple counter ? (6 + 2)

(ii) Explain the operation of a 4 (four) bit shift right register using D flip-flops. (6)

(iii) Explain the function of the LOAD and CLEAR inputs of a shift register. (4)

(iv) What are the different modes of operation of a shift register ? (2)

7. Write short notes on ***(any five)*** (5 X 4)

i) 3 (three) bit binary to gray code converter.
ii) Full subtractor.
iii) Even parity generator and checker.
iv) 3 (three) bit binary up counter.
v) Excitation table and state diagram of a JK flip-flop.
vi) PAL (Programmable Array Logic).
vii) Noise margin.
viii) CMOS digital logic family.

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