Bachelor of Information Technology
3rd year, 1st Semester Supplementary Examination, 2018
Subject: Operating Systems

Time - Three Hours | Full Marks – 100

Answer question number 1 and any 5 (five) from the rest.

1. 10x2=20

a) Distinguish between *multiprogramming* and *multi-tasking* environment.

b) Write the contents of Process Control Block (PCB)?

c) Consider a logical address space of eight pages of 1024 words each, mapped onto a physical memory of 32 frames. How many bits are there in the logical and physical address?

d) Consider a system having m resources of same type. These resources are shared by 3 processes A, B and C which have peak demands of 3, 4 and 6 respectively. For what value of m deadlock will not occur?

e) Suppose jobs p, q, r, s and t have arrived at time 0 in this order with CPU burst time 4, 1, 8, 1, 2 respectively. Calculate the departure time of p if scheduling is round-robin with time slice 1.

f) Which page replacement algorithm removes a page containing a heavily used variable that was initialized very early and is in constant use?

g) What is the reason that a segment table must have a page table in a paged segmented scheme?

h) Which is the most suitable CPU scheduling policy for a time shared OS?

i) Describe the difference between *short-term* and *long-term* scheduler.

j) What is the meaning of the term *busy waiting*?

2. [4+6+6]

a) Describe the notion of *atomic instruction.*

b) Write a solution to the Dinning-Philosopher problem which avoids deadlock.

c) Two concurrent processes P1 and P2 use four shared resource R1, R2, R3 and R4 as shown below

P1	P2
Use R1	Use R1
Use R2	Use R2
Use R3	Use R3
Use R4	Use R4

Both processes are started at same time, and each resource can be accesses only one process at a time. The following scheduling constraints exist.

i) P2 must complete use of R1 before P1 gets access to R1
ii) P1 must complete use of R2 before P2 gets access to R2
iii) P2 must complete use of R3 before P1 gets access to R3
iv) P1 must complete use of R4 before P2 gets access to R4

What is the minimum number of binary semaphores requires enforcing the above scheduling constraints? Provide a solution.

3. [(2+2)+6+6]

a) In a Round Robin CPU scheduling algorithm, s represents the time of context switching, q represents the round-robin time quantum and r represents the average time a process runs before blocking on I/O. Calculate the CPU efficiency for each of the following cases:

i) $s<q<r$

ii) $s=q<r$

b) A certain processor provides a 'test and set' instruction that is used as follows
TSET register flag
This instruction atomically copies flag to register and sets flag to 1. Give pseudo code for implementing the entry and exit code to a critical section using this instruction.

c) Two shared resources R_1 and R_2 are used by processes P_1 and P_2. Each process has a certain priority for accessing each resource. Let T_{ij} denotes the priority of P_i for accessing R_j. A process P_i can snatch a resource R_k from process P_j if $T_{ik} > T_{jk}$. Find condition(s) that ensure(s) that P_1 and P_2 can never deadlock.

4. [4+6+6]

a) What are the necessary and sufficient conditions must hold for a deadlock to occur?

b) Consider three processes all arriving at time zero with total execution time of 10, 20 and 30 time units respectively. Each process spends the first 20% of execution time doing I/O, the next 70% of time doing computation and the last 10% of time doing I/O again. The OS uses a SRTF scheduling algorithm and schedules a new process either when the running process gets blocked on I/O or when the running process finishes its compute burst. Assume that all I/O operations can be overlapped as much as possible. For what percentage of time does the CPU remain idle?

c) In a system, n threads T_1, T_2, T_3...T_n want to execute within a critical section in the order T_1, T_2, T_3...T_n. How many semaphores will be required to achieve this ordering, and what should be their initial values? Sketch the code for the n threads.

5. [4+(3+3)+6]

a) A process has been allocated 3 page frames. Assume that none of the pages of the process are available in the memory initially. The process makes the following sequence of page references: 1, 2, 1, 3, 7, 4, 5, 6, 3, 1. How many page faults occur for the above reference string if optimal replacement policy is used?

b) A uni-processor computer system has only two processes, both of which alternate 10 ms CPU burst with 90 ms I/O burst. Both the processes were created at nearly the same time. The I/O of both processes can proceed in parallel. Calculate the CPU utilization (over a long period of time) for SJF and RR scheduling.

c) In a computer system where the 'best-fit' algorithm is used for allocating 'jobs' to 'memory partitions', the following situation was encountered:

Partition sizes in KB	4K 8K 20K 2K
Jobs sizes in KB	2K 14K 3K 6K 6K 10K 20K 2K
Time for execution	4 10 2 1 4 1 8 6

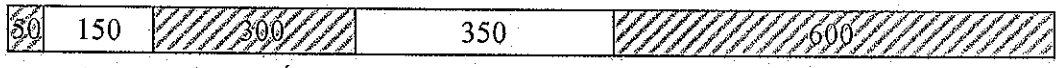
When will the 20K job complete?

6. [4+6+6]

a) Suppose the time of servicing a page fault is on the average 10 ms, while a memory access takes 1 μs. What is the average memory access time if the hit ratio is 99.99?

b) The address sequence generated by tracing a particular program executing in a pure demand paging system with 100 records per page with 1 free main memory frame is recorded as follows. What is the number of page faults?
100, 200, 430, 499, 510, 530, 560,120,220,240, 260, 320

c) Consider the following memory heap in which blank regions are not in use and hatched regions are in use. Which of the policies first-fit, best-fit, and worst-fit satisfies the sequence of requests for blocks of size 300, 25, 125 and 50?



7. [4+6+6]

a) Explain the term *locality of reference.*

b) A demand paged virtual memory system uses 16-bit virtual address, page size of 256 bytes, and has 1 KB of main memory. LRU page replacement is implemented using list, whose current status (page number in decimal) is

17	1	63

For each of the hexadecimal address in the address sequence 00FF, 010D, 10FF, 11B0 indicate

i) new status in the list
ii) page faults, if any
iii) page replacement, if any

c) Consider a small two-way set-associative cache memory consisting of four blocks. For a block to be replaced, LRU scheme is used. Calculate the number of cache misses for the following sequence of block addresses: 8, 12, 0, 12, 8