Ref. No: EX/IT/T/224/2018

BACHELOR OF INFORMATION TECHNOLOGY EXAMINATION, 2018

(2nd year, 2nd semester)

Microprocessors

Time: 3 Hours

Full Marks: 100

CO1 [20]	**[1] Answer any one from (A) and (B) in this block** A. (i) Explain the operations of BIU in 8086. (ii) Explain the concept of pipeline architecture in 8086? What is its advantage? (iii) What is the size of data bus, address bus and addressable memory in 8086? (iv) How can a microprocessor distinguish between data and instruction? [5+5+4+6] B.(i) Describe the flag register in 8086. (ii) What are the different types of segment registers used in 8086. (iii) Describe with example the physical address formation in 8086. (iv) What are the advantages of indirect addressing over direct addressing? [6+4+5+5]
CO2 [20]	[2] **Answer any two from (A), (B) and (C) in this block** A. Write a recursive subroutine in 8086 assembly language programming to generate sum of first N natural numbers. N is passed as a parameter through register BL and store the sum in a 16 bit variable SUM stored in memory. [10] B. (i) What is the function of XCHG instruction? Explain its restrictions. (ii) Explain with example PUSH and POP instruction. (iii) What is the function of the operation: LES AX, 2000H . [3+4+3] C. Write a program to add consecutive 2 data bytes stored at offset 200H in segment 1000H with other 2 data bytes available at offset 500H in the same segment and stored the result in an appropriate variable in the same segment. [10]

CO3 [20]	[3] **Answer all the questions** (i) Draw and discuss the timing diagram of I/O read cycle of 8086 in minimum mode. (ii) What is Interrupt Vector Address of INT 21H? How the interrupts are handled in 8086 microprocessor? (iii) How are address and data buses (AD15 - AD0) de-multiplexed in 8086? (iv) What is the purpose of $\overline{\text{LOCK}}$ signals in 8086? [6+3+6+3+2]
CO4 [20]	[4] **Answer any two from (A), (B) and (C) in this block** A. Design an interface between 8086 CPU and two chips of 8Kx8 EPROM and two chips of 8 Kx8 RAM. Select the starting address of EPROM and RAM suitably. [10] B. Interface an input port 74LS245 to read the status of switches SW1 to SW8. The switches, when on, input a '1' else input a '0' to the microprocessor system. Store the status in register CL. The address of the port is 0A21H. [10] C. Interface an 8255 with 8086 to work as an I/O port. Initialize port A as Input port, port B as an output port. Port A address should be 0820 H. write a program to sense switch positions SW0 – SW7 connected at port A. the sensed pattern is to be displayed on port B, to which 8 LEDS are connected. [10]
CO5 [20]	[5] **Answer all the questions** (i) How do you generate delays in software? What are the limitations of this method? Design a programmable timer using 8253 and 8086. Interface 8253 at an address 0740H for counter 0 and write an ALP to generate an interrupt after 10ms. The 8086 and 8253 run at 5MHz and 1.5 MHz respectively. (ii) Explain the 'mode instruction control word' format of 8251 in Asynchronous mode. What will be the value in "Mode Instruction control word" to initialize 8251 in asynchronous mode with odd parity enable, 8-bits character length, and one stop bit, frequency 160 kHz? [(2+1+7)+(4+6)]