

BE INFO TECH 2nd YEAR 1st SEMESTER EXAMINATION, 2018

Computer Architecture

Time: 3 Hours

Full Marks: 100

Answer Any Five

- 1.a) Write (-113) in binary using 3 major representations viz., Sign-Magnitude, One's Complement and Two's Complement number systems both in 8 bit format and 16 bit format.
- b) Convert the Decimal fraction (0.8125×10^{-2}) to Binary. Also convert the Binary fraction (10.01×2^{-3}) to Decimal.
- c) Represent 0.075 as per IEEE 754 Single Precision Formats.
- d) Represent 0.0098 as per IEEE 754 Double Precision Formats.

(6+4+5+5)

2. a) List down the names of various types of Memory. Explain 'Temporal Locality of Reference' and 'Spatial Locality of Reference'.
- b) With respect to Cache, explain the concept of 'Set-associative Mapping'. Use relevant diagram.
- c) List down the various Cache Replacement Algorithms. With proper diagram, explain one of them.
- d) With proper diagram, explain the concept of 'Memory Interleaving'.

((3+2)+5+(1+4)+5)

- 3.a) List down and explain the three components of the Central Processing Unit(CPU).
- b) List down the names of the various Registers inside the CPU.
- c) Draw the internal diagram of a CPU (having Single Bus Organization) showing all the different components.
- d) With respect to the above diagram, show the sequence of micro-operations performed by CPU to do the following operation.

"To store the contents of R1 into the memory location specified by R3"

(5+3+7+5)

4.a) For a CPU which supports 'Three-Address' instruction format, write down a set of assembly language instruction which will evaluate the expression $X = (A+(B*W)) * (C+(D/Y))$. All values are available in the memory; also the result has to be stored back in the memory.

b) With proper instruction example, illustrate your understanding about "Relative Addressing".

c) With proper instruction example, illustrate your understanding about "Base with Index and Offset Addressing".

d) List down the categories of various types of Instructions. Give at least three examples of each of the categories.

(4+5+5+(2+4))

5.a) With proper examples and diagram, illustrate your understanding about "Program-controlled I/O".

b) List down the Mechanism for Determining the Source of Interrupts. Illustrate one of them in full details.

c) List down at least 4 different devices in a computer which may get performance benefit because of DMA mode of I/O transfer. With respect to DMA operation, using Timing Diagram, show how BR, BG and BGACK signals work together.

d) There are three types of I/O transfer; Programmed Controlled I/O, Interrupt Driven I/O and DMA based on I/O. But DMA includes all three types of I/O. Explain this.

(5+(1+4)+(2+4)+4)

6.a) Explain your understanding about 'Fragmentation' with respect to a Disk.

b) Consider a block-addressable disk with the following characteristics.

- Size of the Track: 20,000 bytes
- Non-data overhead per block = 300 bytes
- Record Size = 100 byte

How many records can be stored per track if blocking factor is 10 and 60?

c) Given the following Disk Characteristics:

- 20 Surfaces
- 800 tracks/surface
- 25 sectors/track
- 512 bytes/sector
- 3600 RPM
- 7 ms track-to-track seek time
- 28 ms avg. seek time
- 50 ms max seek time.

Find:

- i) Average Latency Time
- ii) Disk Capacity in Bytes

iii) Time to read the entire disk, one cylinder at a time.

d) Given the following Disk Characteristics:

- Average seek time = 8 ms
- Average rotational delay = 3 ms
- Maximum rotational delay = 6 ms
- Spindle speed = 10,000 RPM
- Sectors per Track = 170
- Sector Size = 512 bytes

What is the average time to read one sector?

$$(3+(2+2)+(3+3+3)+4)$$

7.a) With proper example, explain the four different criteria to evaluate Processor Interconnection Matrix.

b) Draw three Hyper Cubes of depth 2, 3 and 4 respectively. Also, compute their basic characteristic parameters.

c) Explain how Cache Coherency problem gets solved in a Centralized Multiprocessor type of machine.

d) With a proper diagram, explain your understanding about NUMA type of Multiprocessor machine.

$$(4+(1+2+3)+5+5)$$

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