JADAVPUR UNIVERSITY

B.E. INFORMATION TECHNOLOGY

1st Year, 2nd Semester Examination - 2018

DIGITAL LOGIC & DIGITAL CIRCUIT **Time : 3 hours** **Full Marks : 100**

General instructions (read carefully)

1. Special credit will be given to answers which are brief and to the point.
2. Answer to every question should start on a new page.
3. Do not write answers to various parts of a question at different locations of your answer-script.
4. Do not write on the front back cover of your answer booklet.

Question No. 1 is compulsory. Answer any 4 (four) from the rest.

Each question carries 20 marks. Question for each sub-part is mentioned at the right margin of a part question or set of part questions.

1. Answer ***any 10 (ten)*** of the following questions. Be specific and very brief in answering each question. (10 X 2)

i) What is $(0.25)_{10}$ in binary number system?

ii) What is the signed 2's complement representation of $(-17)_{10}$?

iii) The value of r, for which $\sqrt{(224)_r} = (13)_r$ is a valid expression, in number system with radix r ?

iv) Simplify the Boolean function Y = A (A + B) + B (A' +B).

v) The circuit that will work as OR gate in positive logic will work as _____ gate in negative logic.

vi) What is the minimum number of NAND gates required to implement $A \oplus B \oplus C$?

vii) An AND gate has 6 inputs. How many input words are there in its Truth Table ?

viii) Using N flip flops, we can divide the input clock frequency by ?

ix) By using a Modulo 1024 ripple counter, we need to count a pulse train having a frequency of 1 MHz. What is the maximum permissible propagation delay of each flip flop ?

x) Data from a satellite is received in serial form. If the data is coming at the rate of 8 MHz, how long will it take to serially load a word in a 40 bit shift register ?

xi) What is the circuit requirement for a master-slave JK flip flop to work as a positive edge triggered flip flop ?

xii) Size of a PROM increases _____ with increase in the number of inputs, and _____ with increase in the number of outputs.

xiii) Name any two digital logic families or sub-families (series), where the speed of the signals is increased by preventing the transistor from going into saturation.

xiv) A PAL (Programmable Array Logic) has a _____ AND array and a _____ OR array.

xv) Which digital logic family offers the highest noise margin ?

xvi) Except for very short wires of a few centimeters, why must ECL (Emitter Coupled Logic) outputs use coaxial cable with a resistor termination ?

2. i) Simplify the following functions using Karnaugh map, and design the circuit using basic fundamental gates. List the inventory required in the implementation. (2 X 8)

a) $F(A, B, C, D) = \sum m(0, 2, 6, 10, 11, 12, 13) + d(3, 5, 14)$

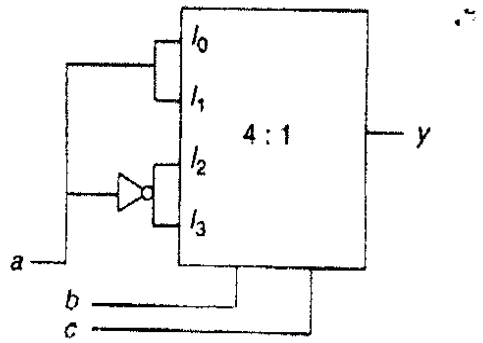
b) $F(A, B, C, D) = \prod M(3, 6, 8, 11, 13, 14) \cdot d(1, 5, 7, 10)$

ii) Explain why we use Gray code instead of natural binary code while minimizing logic circuits using Karnaugh map. (2)

iii) Distinguish between combinational and sequential circuits (any two points) (2)

3. i) Construct an 8-line to 256-line decoder using 4-line to 16-line decoder. (5)

ii) Find the output of the circuit shown. (3)



iii) Implement the digital circuit of a Full Subtractor using (12)

a) only logic gates

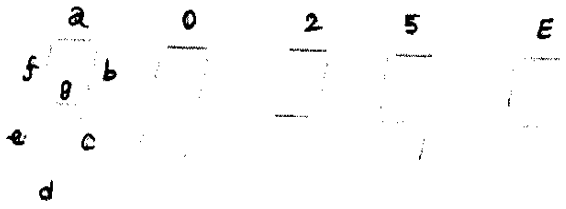
b) 4 X 1 multiplexer

c) 3 to 8 decoder.

4. i) Two products are sold from a vending machine, which has two push buttons P_1 and P_2. When a button is pressed, the price of the corresponding product is displayed in a 7-segment display.

- If no buttons are pressed, '0' is displayed, signifying "Rs 0'.
- If only P_1 is pressed, '2' is displayed, signifying 'Rs 2'.
- If only P_2 is pressed, '5' is displayed, signifying 'Rs 5'.
- If both P_1 and P_2 are pressed, 'E' is displayed, signifying "Error'.

The names of the segments in the 7-segment display and the glow of the display for '0', '2', '5', 'E', are shown in the following figure.



Consider

- Push button pressed / not pressed is equivalent to logic 1 / 0, respectively
- A segment glowing / not glowing in the display is equivalent to logic 1 / 0, respectively.

1. If segments a to g are considered as functions of P_1 and P_2, then find g in terms of P_1 and P_2. *(Hint – make a Truth Table of different combinations of P_2 and P_1 and their corresponding values for each of the segments).*
2. What are the minimum numbers of NOT gates and 2-input OR gates required to design the logic of the driver for this 7-segment display ? Explain. (5 + 5)

ii) Draw the circuit diagram of a JK master-slave flip-flop and explain its operation. How is racing avoided in such a flip-flop ? (8)

iii) Mention any two applications of flip-flops. (2)

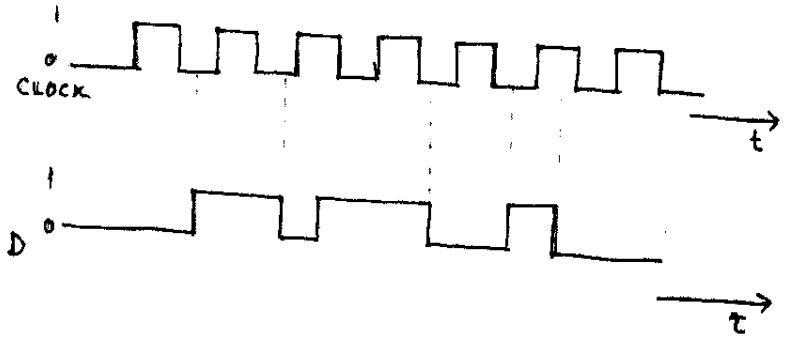
5. (i) For a master-slave D flip-flop, with a uniform CLOCK signal and with input waveform D, as shown below, draw the output waveforms at the (4 X 2.5)

a) master Q output, Q_M

b) slave Q output, Q_S

c) output Q_P, when the flip-flop is positive edge triggered,

d) output Q_N, when the flip-flop is negative edge triggered.



(ii) Design an asynchronous (ripple) counter using JK flip-flops to count from **3** to **12**. (10)

6. i)Design a 4(four) bit synchronous counter using JK flip-flops and explain its operation.(6)

ii) What are the advantages of a synchronous counter over a ripple counter ? What are the disadvantages, if any ? (2 + 1)

iii) Explain the function of the LOAD and CLEAR inputs of a shift register. (4)

iv) What are the different modes of operation of a shift register ? Write about one application of each. (2 + 4)

v) What is a Universal Shift Register ? (1)

7. i) Implement an arbitrary sequence counter to count 1, 4, 3, 5, 2, 6 using the generalized model of a state machine using JK flip-flops. Draw the state graph / diagram, write the state table and transition table. Design the combinational / steering circuit. (14)

ii) Write and explain the specifications of PAL (Programmable Array Logic) with a concrete example. (3)

iii) Which of the three PLDs (Programmable Logic Devices), PROM, PLA and PAL, is the most efficient and why ? What is reason of its commercial failure ? (3)

8. Write short notes on ***(any five)*** (5 X 4)

i) 4 (four) bit adder-subtractor using Full Adders.

ii) 3 (three) bit binary down counter.

iii) Excitation table and state diagram of an SR flip-flop.

iv) PROM (Programmable Read Only Memory).

v) Power dissipation, with concrete values of any one digital logic family.

vi) Propagation delay, with concrete values of any one digital logic family.

vii) CMOS digital logic family.

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