Ex/IT/IEE/T/113/2018

JADAVPUR UNIVERSITY

B. E. INFORMATION TECHNOLOGY

1st Year, 1st Semester Examinations - 2018

BASIC ELECTRONICS **Time : 3 hours** **Full Marks : 100**

General instructions (read carefully)

1. Special credit will be given to answers which are brief and to the point.
2. For any value related to any device parameter, which is not given in a question, assume suitable standard value for such parameter.
3. **Answer to every question should start on a new page.**
4. **Do not write answers to various parts of a question at different locations of your answer-script.**
5. The final answer (numerical values with unit) should be underlined or enclosed within a box.
6. Do not write on the front back cover of your answer booklet.

Question No. 1 is compulsory. Answer any 4 (four) from the rest.

Each question carries 20 marks. Question for each sub-part is mentioned at the right margin of a part question or set of part questions.

1. *Answer any 10 (ten) of the following questions. Be specific and very brief in answering each question.*

(10 X 2)

i) What is the value of the energy gap between the valence and the conduction band in a semiconductor in terms of eV and J ?

ii) What are the two most important specifications of a Zener diode ?

iii) What is *diffusion capacitance* ? In which bias is it dominant ?

iv) Assuming ideal diode, derive the dc voltage in *a full wave bridge rectifier* in terms of the peak voltage.

v) Comment on the relative width and doping levels of the base of a BJT w.r.t. that of the collector and emitter. Why is it so ?

vi) In a BJT in CE configuration, will there be any collector current, I_C if the base current, I_B is reduced to zero ? Justify your answer.

vii) Contrast the values of the output current, when output voltage is zero for a BJT in common base (CB) and common emitter (CE) configurations respectively.

viii) In what mode of operation (active or saturation) will a Si npn transistor in common emitter (CE) configuration be if V_{CE} = 0.2V ? Justify your answer.

ix) Can we use a BJT in common base (CB) configuration for current amplification purposes ? Justify your answer.

x) In a BJT *in common emitter (CE) configuration* does the input current increase or decrease for a particular value of input voltage, with increase in output voltage ?

xi) If the Q point is shifted from the centre of the Load Line to too close to the *cut-off* region, which swing (positive or negative) of the output signal will be clipped ? Why is it so ?

xii) In what application is an OP-AMP without any feedback (i.e. open loop) used ? Give an example where you have practically used.

xiii) If the supply voltage of a practical OP-AMP (say IC 741C) is +/- 15V, what will be the maximum output voltage in a closed loop application ? What property (name only) restricts, if any, the output voltage to such values ?

xiv) At what frequencies is an *RC oscillator* used ? What type of waveform(s) is generated at such frequencies ?

2.i) Consider a gallium arsenide (GaAs) sample at T = 300K with doping concentration of $N_A = 0$ and $N_D = 10^{16}$ / cm^3. Assume complete ionization and assume μ_n = 8500 cm^2 / V-s and μ_p = 400 cm^2 / V-s. Calculate the minority carrier hole concentration and the drift current density, if the applied electric field is E = 10 V / cm. Given $n_i = 1.8 \times 10^6$ / cm^3. (2 + 2)

ii) For a heavily doped n-type semiconductor, parameters are as follows

a. Hole - electron mobility ratio is 0.4
b. Doping concentration is 4.3×10^8 atoms / m^3
c. Intrinsic concentration is 1.6×10^5 atoms / m^3

The ratio of the conductivity of n-type semiconductor to that of intrinsic semiconductor of same material and at same temperature is (3)

iii) Derive the formula for finding the electron concentration in an p-type semiconductor material. (4)

iv) How is the width of the space charge (depletion) region related to the doping concentration ? Will the space charge region extend further into or less in a lower doped region ? (2 + 1)

v) The reverse saturation current for a p-n junction is measured as 30 nA at 30^0 C. Calculate the current at 25^0 C. (2)

vi) Draw the circuit schematic of a *full wave rectifier using centre tapped transformer*. Draw the input (sinusoidal) and output waveforms. (4)

3. i) Draw and explain the input characteristic of a BJT in *common base configuration* for different values of collector base voltage, V_{CB}. (5)

ii) Draw and explain the output characteristic of a BJT in *common base configuration* for different values of input current. Mention realistic values of input current and output current and voltage values along the axis. Show the different regions of operation and input current - output current relation in each region. (5+5)

iii) What are the functions of the coupling capacitors and the emitter bypass capacitor in a BJT used for amplification ? Are these capacitor values chosen to be high or low ? Why ? (3+2)

4. i) Analyse the reasons for the decrease of voltage gain of a BJT amplifier in the lower and upper frequency ranges, compared to the mid-frequency range, using representative values of the different capacitors contributing to the decrease in gain. Draw the small signal equivalent circuit using capacitors. (8)

ii) What is the significance of the cut-off frequency of an audio amplifier to be at 0.707 times (or -3 dB below) the mid-frequency gain ? (2)

ii) For a pnp BJT in common emitter configuration and with voltage divider bias, draw the circuit (showing v_s, v_i, and v_o among other parameters) and the ac equivalent circuit using **either** the r_e model **or** the h-parameter transistor model. Calculate the *input impedance, Z_i and overall voltage gain, A_{vs}* of such a circuit. How is A_{vs} related to the voltage gain A_v of the circuit ? (5 + 4 + 1)

5. i) What are the different feedback amplifier topologies ? (Mention as "_ amplifier with _ feedback").

Describe in detail any one of the above using block diagram. (4 + 4)

ii) Draw the drain and transfer characteristics of an n-channel *depletion type* MOSFET identifying clearly the ohmic (triode) region, saturation region and cut-off region. Give representative values of the parameters used to draw the characteristic. (8)

iii) Define "threshold voltage" and I_{DSS} of an n-channel depletion mode MOSFET. (4)

6. i) List the characteristics of a practical OP-AMP (any six). Give representative values of these characteristics for an OP-AMP that is extensively used in the Laboratory and also commercially. (3)

ii) Draw the *Summer circuit* using OP-AMP. Derive the closed loop voltage gain of such a circuit. (5)

iii) Enumerate any three advantages and any one disadvantage of using negative feedback amplifiers. (2)

iv) Draw the circuit of a Hartley oscillator using OP-AMP and explain its operation. Explain how Barkhausen criteria is complied with ?

What is the frequency, f_o at which such an oscillator will oscillate ? What will be the gain of the OP-AMP at this frequency ?

What is the advantage of using an OP-AMP instead of a BJT in building a Hartley oscillator ? (6 + 2 + 2)

7. i) Name any four devices belonging to the family of p-n-p-n devices. For what application are these devices extensively used ? (2 + 1)

ii) By using two-transistor equivalent circuit, briefly describe the basic operation of an SCR. Draw typical forward and reverse characteristics of an SCR, marking all relevant device parameters and "regions" of operation. (5 + 5)

iii) What are the advantages of using SCR over power transistors in circuits that need to handle high power ? (2)

iv) How can we control the conduction angle of an SCR by applying a Gate voltage ? Explain using a circuit with resistive load with a sinusoidal AC input. Draw appropriate voltage and current waveforms. (5)

8. Write short notes on (**any five**) (5 X 4)

i) Intrinsic and extrinsic semiconductors.
ii) Different current flow mechanisms in a semiconductor.
iii) Built-in or barrier potential of a pn junction and the effect of bias on it.
iv) Different models of a semiconductor diode.
v) Space charge or transition or junction capacitance of a pn junction diode.
vi) Block diagram of a power supply to convert an ac (230V, 50Hz) to dc, with a sketch of the waveform at each stage. Brief description (maximum one sentence) of each stage.
vii) Positive feedback amplifiers and its application.
viii) Pinch-off in an n-channel enhancement mode MOSFET.

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