Ref. No.: Ex/FTB/ET/T/225/2018

B.E. FOOD TECHNOLOGY AND BIO-CHEMICAL ENGINEERING
SECOND YEAR, SECOND SEMESTER - 2018

Subject: ELEMENTARY ELECTRONICS **Time: Three Hours** **Full Marks: 100**

Answer any **FIVE** questions. 5x20

(Questions must be answered serially and
All parts of the same question must be answered at one place only)

1. (a) Draw and discuss the potential and field distribution curves across the depletion region of a p-n junction diode.
   (b) Compare between avalanche and zener breakdown mechanisms.
   (c) Define a.c. and d.c. resistances of a p-n junction diode.
   (d) Explain the working principle of a Light Emitting Diode.
   (e) Calculate the ratio of the current for a forward bias of 0.06 V to the current for the same value of reverse bias applied to a Ge p-n diode at 27^0C. (3+3)+(2+2)+(1+1)+3+5=20

2. (a) Draw the potential and space charge distribution in a uniformly doped p-n junction assuming the junction to be abrupt. Explain.
   (b) A silicon p-n junction at $T = 300K$ with zero applied bias has doping concentrations of $N_d = 5\times10^{16} cm^{-3}$ and $N_a = 5\times10^{15} cm^{-3}$. Determine i) x_n, ii) x_p, iii) W and iv) $|E_{max}|$. Derive the necessary equations.
   (c) Discuss the formation of junction capacitance in an abrupt p-n junction diode. 4+8+8=20

3. (a) Why the base width of a BJT is kept narrow? Why the device is named BJT?
   (b) Define α and β of a transistor. Derive the relation between them.
   (c) Show with the help of a diagram, the different current components with proper directions for an n-p-n transistor.
   (d) An n-p-n transistor with $\alpha = 0.98$ is operated in the CB configuration. If the emitter current is 3 mA and the reverse saturation current is $I_{CO} = 10\mu A$, what are the base current and the collector current? (2+2)+(4+3)+4+5=20

4. (a) Draw a self-biased transistor circuit in CE mode. Explain its working principle.
   (b) A CE transistor amplifier is characterized by $h_{ie} = 2k\Omega$, $h_{re} = 2\times10^{-4}$, $h_{fe} = 50$ and $h_{oe} = 20\times10^{-6} A/V$. If the load resistance is $4k\Omega$ and the source resistance is 200Ω, determine the input resistance, the output resistance and the voltage, current and power gains. Derive the formula you use. 5+5x3=20

5. (a) Define pinch-off voltage of a JFET.
   (b) An n-channel silicon JFET has a donor concentration of $2x10^{21}/m^3$ and a channel width of 4 μm. If the dielectric constant (ε_r) of silicon is 12, find the pinch-off voltage. Derive the formula you use. (Given $\varepsilon_0 = 8.854x10^{-12}$ F/m)

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(c) Define FET parameters μ, r_d and g_m. Derive and draw the small signal a.c. equivalent circuit of a FET.

(d) Mention three advantages of FET over BJT. 2+(2+4)+(6+3)+3=20

6. (a) Explain the operation of a depletion mode MOSFET. Also explain its drain and transfer characteristic curves. Clearly mention whether you are considering p-substrate or n-substrate device.

(b) Give proper justification for the non-uniform shape of the depletion region of a JFET.

(c) Derive the expression for trans-conductance of a FET starting from Shockley's equation. 10+6+4=20

7. (a) Derive the logic expressions of a full-adder circuit from its truth table.

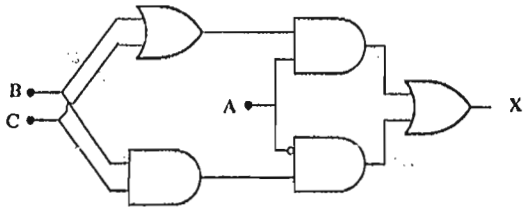
(b) Perform the addition of 11011 and 10011 using block level diagrams of full-adder.

(c) What is the fundamental difference between combinational and sequential digital circuits?

(d) Explain the operation of a clocked (i) S-R and (ii) D flip-flop. 6+4+2+8=20

8. (a) In the following circuit, which of the following expressions give the output X?

(i) $A\overline{B}+B\overline{C}+C\overline{A}$, (ii) $AB+BC+CA$, (iii) $\overline{A}.\overline{B}+\overline{B}.\overline{C}+\overline{C}.\overline{A}$



(b) Show that, $A \oplus B = \overline{\overline{A+B}+\overline{\overline{A}+\overline{B}}}$

(c) Draw a logic circuit using NOR gates to implement the Boolean expression $AB+\overline{B}.\overline{C}$.

(d) Implement the Boolean expression $Y=(A+B)(\overline{A}+\overline{B})$ in a logic diagram. Construct the truth table and hence show that the logic diagram is equivalent to an XOR gate. 4x5=20