Ex/ET/T/413/2018

Department of Electronics and Telecommunication Engineering, Jadavpur University

B. E. Electronics and Telecommunication Engineering Fourth year 1st semester Examination 2018.

Attempt any five questions and all question carry equal marks.. Missing data may be assumed.

Subject : VLSI Design

Time : Three Hours Full marks : 100

Q1. How one nMOS and one pMOS transistor are combined to behave like an ideal switch? Why leakage power is an important in the deep sub micron technology? List various sources of leakage currents , Briefly discuss various mechanisms responsible for this leakage current? 4+4 +4 + 8 = 20

Q1. a). Why low power has become an important issue in the present day VLSI circuit realization?
b). Draw the ideal characteristics of a CMOS inverter and compare it with the actual characteristics. What is noise margin? Find out the noise margin from the actual characteristics of the inverter.8+12 =20

Q3. a). What are different power dissipations in a CMOS circuits? Write the names of different parameters that control those power components. Explain how those parameters can be adjusted to reduce various power dissipation
b).Describe with necessary diagram, how will you reduce the propagation delay of an inverter? 16 + 4 = 20

Q4. Give the justification with proper explanation and diagram if any (related to Low power VLSI) for the following comments:
i). "Minimize activity on long bus"
ii). "Dynamic Power Consumption is Data Dependent"
iii). "Use reduced supply voltage in sleep mode."
IV). "Low Vth for speed critical circuits"
V). "Lost performance can be compensated by parallelism" 4+4+4+4+4 = 20

Q5. a). Define the symmetric and asymmetric logic gates with an example for each. Explain why the input ordering of a logic gate may affect propagation delays.
b). Using equivalent NOT gate , drive the threshold voltage of a two-input NAND gate.
c). Describe single-rail and dual –rail logic circuits 8+8+4 = 20

Q6 a). For inverter design, why depletion load n-MOS inverter is preferred ? Explain the operation of TG – based NAND gate.
b). Design a two input XOR gate using CMOS logic. Explain fan-in and fan-out of logic gates.
c).How is a CMOS inverter different from a resistive load inverter? Which is preferred and why?
6+10+4=20

Q7. a). What are high and low –skewed logic gates? Explain GDI logic with an example.
b). Implement two-input (i) XOR and (ii) NOR gates with GDI logic. Explain their operations.
c). Explain pseudo and Ganged CMOS logic. 6+ 8 + 6 =20

Q8. Write notes on any four of the following:

a) Body effect b) Parasitic Bipolar Effect. c). Mobility reduction by gate-induced surface fields d) Fringing field e) Constant Field Scaling versus Constant voltage Scaling f) Hot Carrier Effect

4x5= 20