Ref. No.: Ex//ET/T/311/2018

BACHELOR OF ENGG. (ELECTRONICS & TELE-COMM. ENGG.) EXAM., 2018
(3rd Year, 1st Semester Examinations, 2018)

MICRPROCESSORS & MICROCONTROLLERS

Time: Three Hours Full Marks: 100

Answer **Q. No.1** and any **Four** from the rest.
(All Parts of a question must be answered at one place only)

1. Fill-in the Blanks / State True or False (T/F) **[2 Marks X 10]**

(a) _____ is a Program written either in mnemonics of an assembly language or in English-like statements of a high-level language (before it is assembled or compiled).

(b) Addressing mode is the method of specifying the _____

(c) The last memory address of a 2K memory chip is FFFFH. Identify the memory address of the starting location of the memory chip and the number of address lines required for the memory chip would be _____

(d) If the 8085 Microprocessor has fetched the machine code located at the memory location 205FH, specify the contents of the Program Counter.

(e) The number of Input / Output Ports in a Peripheral-mapped I/O scheme is restricted to _____.

(f) Specify the 8085 Microprocessor signals that are used to enable an Input Port.

(g) During the execution of Jump Instructions, the Program Counter is loaded by updating the contents of the _____

(h) The single byte instruction _____ can be used to clear the accumulator, and _____ flags are altered to reflect the results of the operation.

(i) Buffer is a commonly used device to interface an output port. (T / F)

(j) JMP instructions can be used to access the Subroutine. (T / F)

2. (a) List the limitations of 8085 Microprocessor as a Microprocessing Unit (MPU).
(b) (i) Explain the operation of Transparent Latch (ii)Explain the schematic of Latching Low-order Address Bus and Demultiplexing the Bus AD_7-AD_0.
(c) List the 8085 Interrupts and Externally initiated signals and give a brief description of each signals. [2+12+6]

3. (a) List the 8085 MPU Peripheral I/O Instructions and their operation.
(b) List the different Machine cycles involved in the I/O execution and the corresponding control signals in each machine cycle.
(c) Based on the information from the (a) and (b), list the design steps involved in Device Selection and Data Transfer
(d) Based on the information from (c), show the decode logic for DIP Switch Port with address FFH and explain the same [2+4+6+8]

4. (a) Explain the function of the following program:

```
        MVI A, Byte
        ORA A
        JM  OUTPRT
        OUT 01H
        HLT
OUTPRT: CMA
        ADI 01H
        OUT 01H
        HLT
```

(b) Write an 8085 Assembly Language Program (ALP) to implement the equation $(a+b)^2$

(c) Load the BC & DE pair registers with the data (2233H) and (4455H) respectively. Write an 8085 ALP to exchange the contents of BC & DE Pair using Stack related instructions. [3+12+5]

5. (a) Explain the instructions EI, DI & RST and their functions in the 8085 interrupt process.

(b) List the steps to initiate and implement the 8085 interrupts

(c) Show the schematic to implement a suitable RST instruction and explain. [6+10+4]

6. (a) The 8255 Programmable Peripheral Interface (PPI) Chip Select - $\overline{CS}$ logic is connected to the 6-input NAND gate The msb among the 6-input is directly connected to the NAND gate while other inputs are connected via inverter gate. Show (i) the complete Chip Select - $\overline{CS}$ logic and (ii) I/O Port & Control Register addresses of 8255 PPI.

(b) The 8255 PPI has to read an input port and to display the same at one of the output port. Write the 8255 PPI control word and the 8085 ALP to perform the same.

(c) (i) Explain the mode 3 operation of 8254 Timer. (ii) The CLK input of the Counter of 8254 Timer is connected to the 2 MHz source. Calculate the COUNT in Hex number to be loaded in the counter to generate 2 KHz signal at the OUT pin of the Counter. [5+8+7]

7. (i) Demonstrate 8085 MPU can be used as a Process Controller.

(ii) Draw the Block Diagram of the system and explain the concept with an appropriate Algorithm / Flow chart, and ALP. [4+16]

8. Write short notes:

(a) Programmable Interrupt Controller - The 8259A

(b) Intel 8051 Microcontroller : Block Diagram and Features

[2 X 10]