B. ETCE 3RD YEAR 2ND SEMESTER EXAMINATION-2018

Subject: IC DESIGN Time: 3 Hours Full Marks: 100

All parts of the same question must be answered at one place only

Model parameters for NMOS and PMOS device

Parameters	NMOS	PMOS
L_{min}	180nm	180nm
W_{min}	240nm	240nm
V_{th}	0.7V	-0.8V
λ (V^{-1})	0.1	0.2
μ (cm^2/Vs)	350	100
C_{ox} ($fF/\mu m^2$)	6	6

PART-I

1. **Answer any Five** Questions: [Marks: 5×8=40]

A) What is sub threshold conduction? Why MOS in sub threshold produces higher gain than MOS in saturation *(Explain with $log(I_D)$-V_{GS} plot)?*

B) What is channel length modulation effect? How the voltage current characteristics are affected because of this effect?

C) What is trans-conductance (g_m) of a MOS transistor? Plot g_m-V_{GS} with V_{DS} as a parameter and g_m-V_{DS} with V_{GS} as a parameter.

D) Draw the ideal characteristics of a CMOS inverter and explain the different parts of the characteristic based on the operation point of those MOSFETs.

E) How body bias changes the threshold voltage of a MOSFET? Explain with diagram.

F) Explain why the structures shown below cannot operate as a current source even though the transistors are in saturation.

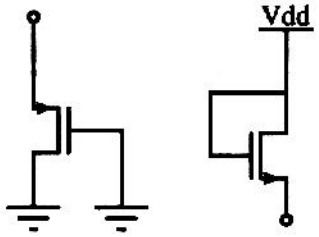

Figure 1

G) What is delta delay in VHDL? How Transport and inertial delays are described?

PART-II
(Compulsory)

2. **Design** one cascode current mirror with output resistance not less than 1 MΩ. Find the **maximum voltage variation** at the output node of the current mirror.

OR

Design one cascode amplifier with resistive load for a voltage gain more than 100. Find the **maximum voltage variation** at the output node of the amplifier. [Marks =20]

PART-III
(Answer any Two)

3. Find the gain expressions of the amplifier circuits shown below. [Marks: 2×10 =20]

A) Consider $\lambda \neq 0$ and $\gamma \neq 0$.

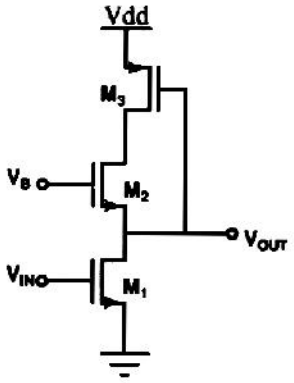

Figure 2

B) Consider $\lambda \neq 0$ and $\gamma = 0$.

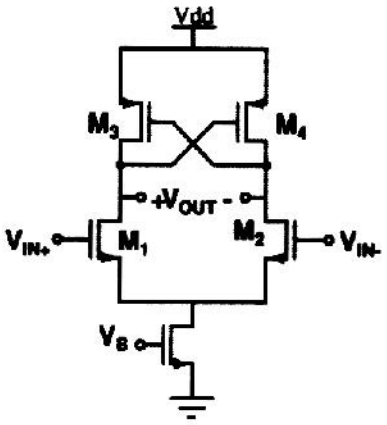

Figure 3

4. Find I_x vs V_x plot of the circuit shown below when V_x is varied from 0V to V_{DD}. Specify the voltage ranges corresponding to different transistor operating region. [Marks: 14+6 =20]
(Consider supply voltage V_{dd}= 3V, I_1=1μA(ideal), V_{THN}=0.7V and K = $\mu C_{ox}W/L$= 200 μA/V² and R_1 = 20KΩ)

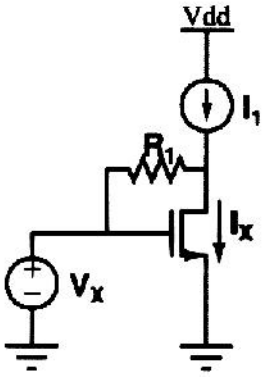

Figure 4

5. **A)** The circuit shown in Figure 2 has following characteristics: V_B=2V, I_1=1μA(ideal), V_{THN}=0.7V and K = $\mu C_{ox}W/L$= 200 μA/V² with V_{BODY} =0V. If the initial voltage on the capacitor is 3V, **plot** V_x with respect to time. *(keep in mind that body to source conduction starts if $V_{SB} \leq$ -0.7V because of forward bias between body to source junction)* [Marks: 12]

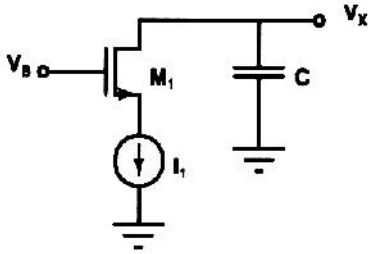

Figure 5

B) Find the Voltage V_x plot of the circuit with respect to time. *(Consider zero charge on the capacitor at time t=0).* [Marks: 8]

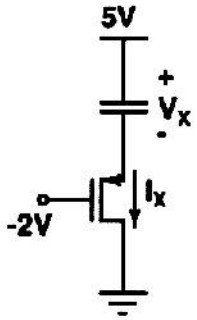

Figure 6