BACHELOR OF ETCE EXAMINATION, 2018
(2^{nd} yr, 1^{st} Semester)

DIGITAL LOGIC CIRCUITS

Time : Three Hours | Full Marks : 100

Answer any ***five*** questions.

1. a) Let, f (A, B, C, D) = Σ (5, 6, 13) and
f_1 (A, B, C, D) = Σ (0, 1, 2, 3, 5, 6, 8, 9, 10, 11, 13)

i) Find f_2 such that $f = f_1 . \bar{f_2}$ (Show in K-map).
ii) Is f_2 unique? If not, indicate the total number of possibilities.
iii) Give the minimal value of f_2. 4+2+2

b) Realize the following function using a number of 2-line to 1-line multiplexers.
Z = x3 (x1 + x2 . x0) 6

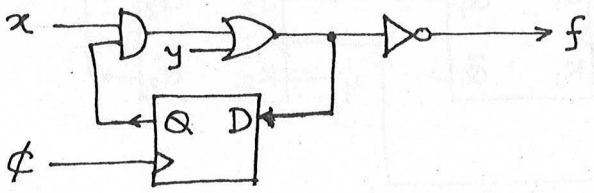
c) Design a circuit using appropriate combinational blocks to compute the maximum of two 4-bit numbers A and B. 6

2. a) Design a priority encoder with four active high inputs p_0, p_1, p_2 and p_3 and three active outputs, A and B indicating the number of the highest priority device requesting service, and N, indicating no active requests. Input p_0 is the highest priority line and p_3 the lowest. 8

b) We have two 4-bit comparators (without cascading facilities) that produce greater than (>), equal (=) and less than (<) outputs. Show the external logic that can be used to cascade them, and obtain the overall result of comparison. 6

c) Design a 5 x 32 decoder using one 2 x 4 decoder and four 3 x 8 decoders (available with suitable enable inputs). 6

3. a) Analyze the following circuit and hence obtain the state diagram. 10



b) Design a sequence detector to detect a sequence 111. Assume overlapping sequence and use D flip-flops to implement the sequence detector. 10

4. a) We have a new trailing-edge triggered flip-flop with three inputs, S, R and T. No more than one of these inputs may be 1 at any time. The S and R inputs behave exactly as they do in SR flip-flop. The T input behaves as it does in a T flip-flop. Obtain the
i) function table,
ii) characteristic equation and
iii) state diagram.
4+3+3

b) Design a 3-bit controlled register with LOAD, SHR and SHL control lines. Assume that LOAD line has the lowest priority and SHL line has the highest priority. 10

5. a) Draw the circuit diagram and hence the timing diagram of a 3-stage ring counter and comment on its decoding logic. Introduce appropriate START, STOP and RESET lines in your design. By what number N does the system divide? 5+5

b) Design a circuit using 74164 ICs and SSI gates to produce a series of four pulses repetitively every 70 μs. The pulses are to be HIGH during the following times:

A: 0 - 20 μs, B: 15 - 45 μs, C: 35 - 60 μs, D: 55-70 μs 10

6. a) Draw the circuit diagram of a 4-bit weighted resistor DAC and explain its operation. Can you modify the circuit to have an eight bit DAC without consequent spread in resistor values? 10

b) Draw the circuit diagram of a successive approximation type of ADC and explain its operation. 10

7. a) Design an up/down synchronous saturation counter with one input x, using JK flip-flops. If x=0 it counts 0, 1, 2, 3, 3, ...; if x=1, it counts 3, 2, 1, 0, 0, ... 10

b) Draw the timing diagram and hence determine the modulus of the following circuit. 10