B.ETCE 2nd yr. Examination 2018
First Semester (**Supplementary**)

DIGITAL LOGIC CIRCUITS

Time: 3 hours | Full Marks : 100

Answer any ***five*** questions
All questions carry equal marks

1. (a) Obtain the maxterm and minterm representations of the following Boolean function.

$f(A, B, C) = A + B + A' C$

(b) Obtain the simplified expression for the following Boolean function using K-map.

$f(A, B, C, D) = \Sigma (0, 2, 5, 7, 8, 10, 13, 15)$

2. (a) Design a 8:1 Multiplexer using 2:1 MUX units and explain its working principle.

(b) Realize the following Boolean function using a 4:1 multiplexer .and other SSI gates if necessary.

$f(A, B, C) = AB + BC + AC$

3. (a) Design a 3-bit binary adder and explain its working principle.

(b) Realize the following functions using a decoder and minimum number of SSI gates.

$F_1 (A, B, C) = A' B + A C$

$F_2 (A, B, C) = A B + A' C$

4. (a) Design a 6-bit magnitude comparator circuit using one 7485 IC and other SSI gates if required and explain the design steps.

   (b) Design a 11-bit parity checker circuit using one 74180 IC and other SSI gates if required and explain the design steps.

5. (a) Draw the circuit diagram of a JK flip-flop using NAND gates only, explain its operation and hence obtain the truth table.

   (b) Convert a D flip-flop into a JK flip-flop. Obtain an expression for f_{max} of the resulting circuit.

6. (a) Design a 4-bit buffer register with appropriate control line and explain its operation.

   (b) Design a 4-bit ring counter and explain its operation with the help of a timing diagram. Mention the advantages and disadvantages of a ring counter.

7. (a) Design a mod-5 ripple counter using JK flip-flops. Consider low active CLR lines for your design. How will you modify the design if low active PRESET lines are available?

   (b) Design a mod-5 synchronous up / down counter using JK flip-flops.