Ref. No.: Ex/ET/T/222 /2018

Department of Electronics and Telecommunication Engineering, Jadavpur University

B. E. Electronics and Telecommunication Engineering 2nd year 2nd semester Examination 2018.

Attempt any five questions and all question carry equal mark. The figures in the right hand margin indicate marks. *Symbols carry usual meaning.*

Time : Three hours **Subject :Digital circuits and systems** **Full Marks: 100**

Q1 (a) Explain , using example , a fault table. Discuss the advantage and disadvantages of fault table method. What is fault dictionary ? Explain with one example

(b) Develop the fault table for the circuit of Fig1:

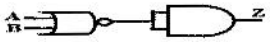

Fig1

(c) Discuss the condition under which faults cannot be located and establish it with one example. (11+ 5+ 4 =20)

Q2 (a) what are asynchronous sequential logic circuit (ASLC) and fundamental-mode circuits. Explain pulse-mode operation of ASLCs.

(b) Define the following terms:

i. Input states ii. Secondary (internal) states iii. Excitation variables iv. Total state v. Stable state

(c) What are races? Explain critical and non-critical races with suitable examples .

(d) What are cycles? Explain these terms by quoting appropriate examples. (4 + 5 + 6+ 5 = 20)

Q.3 (a) Discuss the Boolean difference method with suitable examples. What are the properties of Boolean differences? Verify all of them (at least 5 features)

(b) Obtain the test faults in the following circuit using Boolean difference method. (Fig 2)

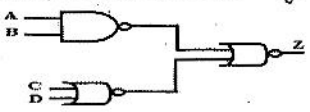

Fig2

(c) Analyze the logic circuit shown in the Fig2 A

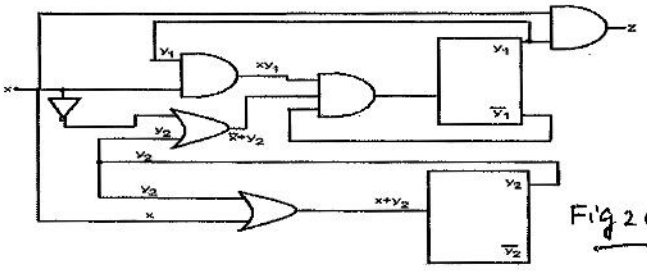

Fig 2 A.

(11 + 4 + 5 =20)

Q4 (a) Discuss the steps involved in the design of an SSLC. Illustrate your explanation by using a suitable example.

(b) Design a parity generator to detect the odd and even sequences.

a) Discuss the SPOOF method of fault detection. Use the SPOOF method in finding the tests required for the circuit shown Fig3

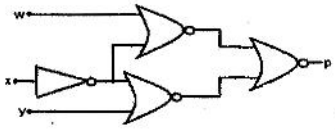

Fig3 (8+6+6 = 20)

[Turn over

5 a). Explain the advantages of Booth's algorithm. How can you justify its fastness compared to other multiplication scheme?

b) Multiply the two numbers a_2a_1(A) x b_2b_1(B) and realize it by hardware.

c). Multiply using Booth's algorithm : **-16 x -12**

d) Show the steps for Restoring and Non-restoring method of division when 9 is divided by 2 using 4-bit representation. Draw the block diagram and explain. [(2+ 3) +3+4 +8 = 20]

Q6. a) What do you mean by timing signal generation? Explain the statement: "Intel i5, 3 GHz, 1 TB SDRAM."

b) Why do we need clock pulse and what are the ways we can get it?

C) Describe the structures of 74121 IC and 74123 iC. Use 74121 as a monoshot to get a pulse of 1 ms width. Explain the difference between non-retriggerable and re-triggerable monoshot

d) Design an astablemultivibrator using 74132 for a frequency of 10 kHz. Extend the design with 7400 NAND gates.

e) How is a sine wave converted to a square wave? (2+ 3 + 7+ 6+2 = 20)

Q7. (a) Explain the following: (i) Micro- operations , (ii) RTL (iii) Virtual Memory , (iv) cache memory , (v) Compact Disk , (vi) **IEEE 754 standard representation**

(b) what is memory and why do we require it? Give the detailed classification of memory along with some explanation of each. (12 + 8=20)

Q8 Write notes on four of the following: (4x5= 20)

(a) Serial multiplier (b) Function hazards (c) Multiple – level fault detection (d) Moore and Mealy machines

(e) Equivalence and minimization