B.E. ELECTRONICS AND TELE-COMMUNICATION ENGINEERING

2ND YEAR 1ST SEMESTER EXAM, 2018

ANALOG CIRCUITS- I **Time: Three hours** **Full Marks: 100**

Use a separate Answer-Script for each Part

PART-I (50 MARKS)

Answer ***Q.1***, any ***two*** from ***the rest*** [10+2×20=50]

1. Answer any ***five*** from the following : [5×2=10]
   a) Define threshold voltage of MOSFET.
   b) Compare Z_{in}, Z_{out}, A_v and A_i for common source and common drain amplifier.
   c) What is a cascode amplifier?
   d) Define Input Offset Voltage for OP AMP
   e) A differential amplifier has difference gain 20000, CMRR 20 dB. Calculate the common mode gain.
   f) Why does the gain of transistor amplifier falls at high frequency?
   g) Write the properties of buffer amplifier.

2. a) Draw a common source MOSFET amplifier. With the help of it small signal equivalent circuit calculate voltage gain, input resistance and output resistance. [12]
   b) Draw an astable multivibrator circuit and explain how does it generate square wave at its output. [8]

3. a) Draw a Dual Input, Balanced Output Difference Amplifier. With the help of ac analysis calculate its difference voltage gain, input resistance and output resistance. [10]

   b) The following specifications are given for the dual input, balanced-output differential amplifier: R_C = 2.2 kΩ, R_E = 4.7 kΩ, R_{B1} = R_{B2} = 50Ω, $+V_{CC}$ = 10V, $-V_{EE}$ = -10 V, β_{dc} = 100 and V_{BE} = 0.7V. Determine the voltage gain, input resistance and output resistance. [10]

4. a) Why Integrators are preferred over differentiators in analog computation. [3]
   b) Design an analog computer to solve $12\frac{d^2y}{dt^2} - 0.5\frac{dy}{dt} = 2$ with $y(t=0) = 2$. [5]
   c) Write the advantages of Schmitt trigger over normal comparator. [4]
   d) What is the Butterworth response of 2nd order low pass filter? [2]
   e) Design a 2nd order Butterworth low pass filter with cut of frequency of 1 KHz. Given that $R_1=R_2=R_3$= 33 KΩ. Draw the frequency response. Qualitative hand drawing. [6]

5. Short note [4×5=20]
   a) E-MOSFET biasing
   b) Source follower MOSFET amplifier
   c) Non inverting Schmitt Trigger
   d) Current source and current sink.

PART- II

(Answer any Five)

1. A periodic waveform is applied to a voltage multiplier circuit as shown in Figure 1. Plot the voltage V_1, V_2 and V_3 with respect to time for the first 3 input cycles. [*Consider $C_1 >> C_2 >> C_3$ and all those diodes are ideal*] [Marks: 10]

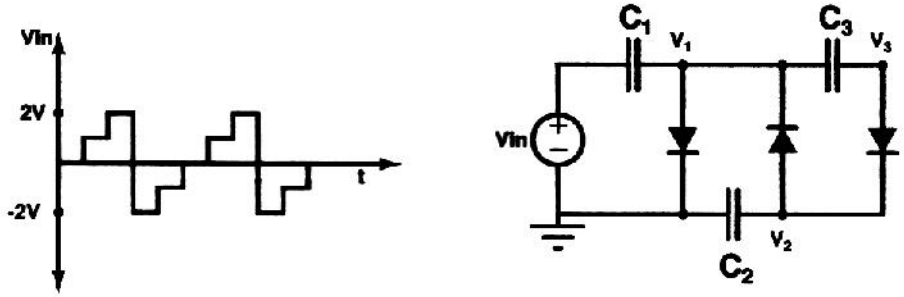

Figure 1

2. A) Draw the output waveform of the circuit shown below. *(V_{B1}= 2V, V_{B2}= 3V and diodes are real with 0.7 volt cut in voltage)*
   B) Determine the minimum or maximum value of V_{B1} and V_{B2} to avoid the clipping of output waveform for the same input condition. [Marks: 6+4=10]

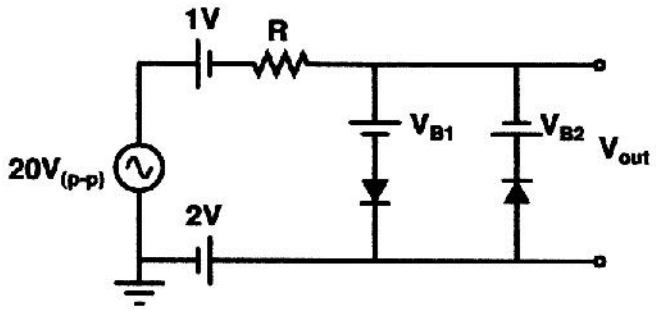

Figure 2

3. A) The half wave rectifier shown in Figure 3 is implemented using one ideal diode. Find the value of V_{dc}, V_{rms} and V_{rrms} (ripple rms).
   B) Design one capacitive filter (*find the value of the capacitor*) to reduce the peak to peak ripple voltage across load less then 100mV . (*Assume R_L is 20kΩ*) [Marks: 6+4=10]

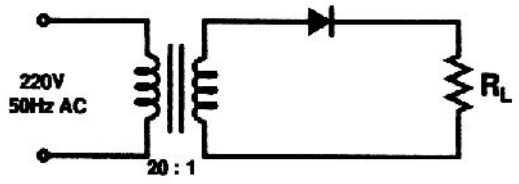

Figure 3

4. Find the output voltage $\mathbf{V_O}$ (at room temperature) of the circuit shown in Figure 4 and **plot** the same for a temperature range of 0 to 100°C. [*All diodes are real and identical*] [Marks: 5+5=10]

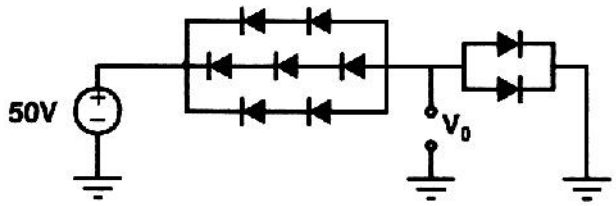

Figure 4

5. Determine the expression of stability factor **S(Ico) and S(V_{BE})**for a voltage divider network. [Marks: 5+5=10]

6. One CE amplifier with proper biasing arrangement is shown in Figure 5. Find the following parameters: [β= *100*, $C_E = C_C = C_B = 1\ \mu F$ *and neglect* r_o]
   A) **Midband gain(V_{out}/V_{in}) of the arrangement.**
   B) All low frequency poles and zeros due to coupling capacitor and lower cut-off frequency.
   C) Gain versus frequency plot (for very low to mid frequency range) [Marks: 4+4+2=10]

7. The BJT used in the CE amplifier shown in Figure 5 is now operated in high frequency range with β=100, C_π= 20pF and C_μ=10pF. Find the following parameters:
   A) High frequency poles due to parasitic capacitors and higher cutoff frequency.
   B) The value of unity gain bandwidth f_T. [Marks: (6+2)+2=10]

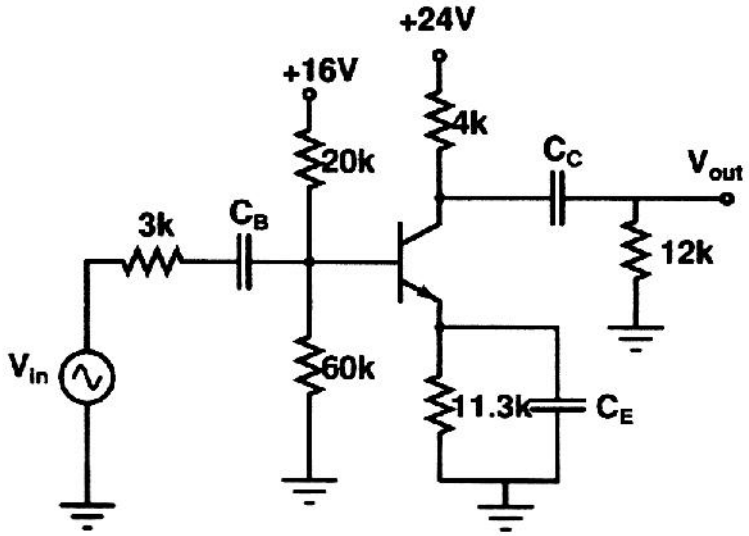

Figure 5