## B.E. ELECTRONICS AND TELE-COMMUNICATION ENGINEERING 2<sup>ND</sup> YEAR 1<sup>ST</sup> SEMESTER SUPPLEMENTARY EXAM, 2018

ANALOG CIRCUITS- I

Time: Three hours

Full Marks: 100

Use a separate Answer-Script for each Part

## PART-I (50 MARKS)

Answer Q.1, any two from the rest

 $[10+2\times20=50]$ 

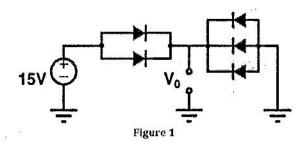
[5+5]1. a) Explain the detrimental consequence of Miller effect associated with common source MOS amplifier. Explain the operation of a cascode amplifier. 2. a) With the help of small signal equivalent circuit calculate and compare voltage gain, input impedance and [20] output impedance of Common Source and Common Gate amplifier. 3. a) List and explain basic building blocks of and OPAMP. Explain why open loop OPAMP is not suitable as [5+2+3] linear applications. Why negative feedback is required for amplifier operation. b) Write the important features of Instrumentation amplifier (IA). Draw and explain the circuit of IA whose [5+5] gain is controlled by an adjustable resistor. 4. a) Why do we use higher order filters? Define 2nd order low and high pass filters. [2+3] b) Explain why a narrow band pass filter can't be designed by cascading one LPF and one HPF. [4] c) Define Bessel, Butterworth and Chebyshev filters and compare their frequency response. [6] d) Design a 2nd order Butterworth high pass filter with cut of frequency of 1 KHz. Given that C= 0.1 uF. Draw the frequency response. (Qualitative hand drawing). [5] 5. Short note b) Voltage divider bias of BJT a) Differential Amplifier Circuit using BJT  $[4 \times 5 = 20]$ 

[Turn over

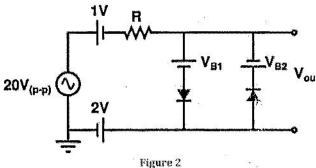
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## PART- II (Answer any Five Questions)

- 1. Explain the working principle of a voltage multiplier with proper circuit diagram. [Marks: 10]
- 2. Explain the working principle of a half wave rectifier. Find  $V_{dc}$ ,  $V_{rms}$  and efficiency( $\eta$ ) of a half wave rectifier. [Marks: 10]
- 3. Find the output voltage **V**<sub>0</sub> of the diode circuit shown below and **plot** the output voltage for a temperature range 0 to 100°C. [All diodes are real and identical] [Marks: 6+4=10]



- 4. A) Draw the output waveform of the circuit shown below.  $(V_{B1}=2V, V_{B2}=3V \text{ and diodes are real})$ 
  - B) Determine the minimum or maximum value of  $V_{B1}$  and  $V_{B2}$  to avoid the clipping of output waveform. [Marks: 6+4=10]



- 5. Determine the expression of stability factor S(Ico) for a voltage divider network. [Marks: 10]
- 6. Explain the function of a current mirror circuit. Design one current mirror with  $1\mu A$  current in primary branch and 0.75  $\mu A$  in secondary branch. (Available transistors are identical with  $\beta$ =1000 and  $V_{BE}$  =0.7V. Supply voltage 3V)

- 7. One CE amplifier with proper biasing arrangement is shown below. Find the following parameters:  $[\beta = 100, C_E = C_C = C_B = 1 \, \mu F$  and neglect  $r_o$ ]
  - A) All low frequency poles and zeros due to coupling capacitor and lower cut-off frequency.
  - B) Gain versus frequency plot (for very low to mid frequency range)

[Marks: 7+3=10]

