B.E. ELECTRONICS AND TELE-COMMUNICATION ENGINEERING

SECOND YEAR SECOND SEMESTER EXAM, 2018

ANALOG CIRCUITS- II **Time: Three hours** **Full Marks: 100**

Use a separate Answer-Script for each Part

PART-I (70)

1. Answer any ***one*** from the following : [1×05=05]

   a) In the circuit shown in figure below that its transistor operates in saturation region with I_D = 0.5 mA and V_D = 3.0V. The enhancement-type PMOS transistor have V_{TH}= -1.0V and K = 0.5 mA/V^2. What is the largest value of R_D can have while maintaining saturation-region operation? RG_1 and RG_2 are in MΩ (1to 10 MΩ) range. [5]

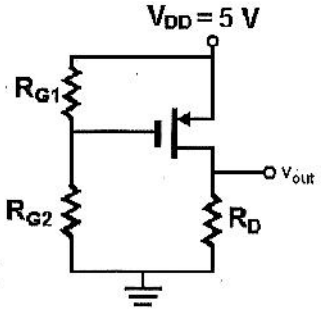

Figure 1

   b) Which type of coupling can be used to amplify extremely low frequency signal? How will you achieve impedance matching in multistage transistor amplifier? [2+3]

2. Answer any ***two*** from the following : [2×10=20]

   a) How power amplifiers are different from voltage amplifiers? Define Class A, B and C power amplifiers. Draw and explain the frequency response of double tuned amplifier for different coupling coefficients. [2+3+5]

   b) What are tuned amplifiers and where are they used? Write a short note on staggered tuned amplifier. [4+6]

   c) With proper schematic describe the working of series-fed class A power amplifier. Why practical efficiency of such amplifiers is always less than 25 %? [8+2]

   d) Illustrate how can a linear series voltage regulator maintain a constant output voltage irrespective of any fluctuation in input voltage or load. Explain the modifications done in the circuit to avoid the eventuality if the load is accidentally shorted. [6+4]

3. Answer any ***one*** from the following : [1×15=15]

   a) What are three terminals and the range of regulated voltages of fixed voltage regulator? What are the outputs of 7810 and 7912. With the help of proper circuit diagram explain how the regulated output voltage can be changed in an adjustable positive IC voltage regulator. State purpose of the capacitances connected in the circuit. [3+2+8+2]

   b) Define Lock range and capture range of PLL. With the help of pin and block diagram explain how LM565 works at different input frequency? Draw the basic amplifier circuit using IC audio power amplifier. [4+7+4]

4. Answer any ***two*** from the following : [2×10=20]

   a) Determine the maximum efficiency of class B push pull power amplifier. [10]

   b) If a 5 V power supply has an output resistance of 1 Ω and a specified maximum current of 10 mA. What is the % and %/mA load regulation? Line regulation is given as 0.3 %/V. Determine the line regulation in % and the change in output voltage if input voltage is decreased by 2 V. [6+4]

   c) Draw the circuit and analyze the step down switching voltage regulator to determine the power efficiency. [10]

5. Answer any ***one*** from the following : [1×10=10]

   a) Design a Step-Down Switching Voltage Regulator with following specifications

   V_{IN} = 25V, $I_{OUT(max)}$ = 500 mA, V_{OUT} = 10V and V_{RIPPLE} < 1% [10]

   b) Design a cascaded two stage single tuned amplifier with 9 kHz bandwidth and effective quality factor is 40. Given that output resistance and capacitance are 20 kΩ and 50 pF, respectively. [10]

PART –II (30 Marks)

Answer **Question 1 and** any **two** Questions from rest

1. Using 555 **Implement** an Astable multivibrator and plot the following waveforms with explanations: $V_{Trigger}$, V_{Cap}, $V_{ff\text{-}Set}$, $V_{ff\text{-}Reset}$ and V_{Out}. Find the value of external components so that T_H= 1msec and T_L= 0.5msec. *(Assume the SR flip-flop used in the IC is a positive edge trigger FF and the IC is using a 5V supply voltage)* [Marks: 3+5+2=10]

OR

Describe the working principle of an attenuator circuit. Draw magnitude (in dB) versus frequency(in rad/s) **plot**. Draw the **waveform** of the output voltage if a gate pulse of 10V is applied to the attenuator shown in Figure 1. **Compensate** the network shown in Figure 2 so that the attenuated output voltage becomes independent of the frequency of input signal.

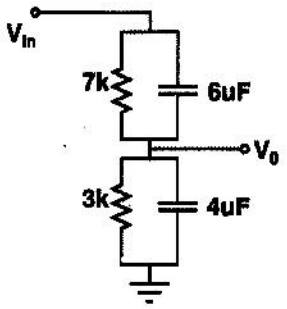

Figure 1

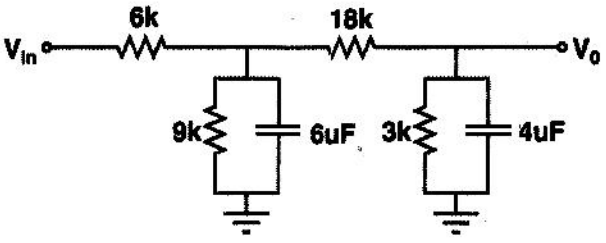

Figure 2

[Marks: (3+2+2)+3=10]

2. For the voltage controlled oscillator shown in Figure 3 derive the expression of T_L and T_H. If the input voltage to the circuit is 5V and the supply voltage of each Op-amp is ±15V plot V_{Cap} *(voltage across capacitor),* V_{Out1} and V_{Out2} with respect to time. [Marks: (2+2)+(2+2+2)=10]

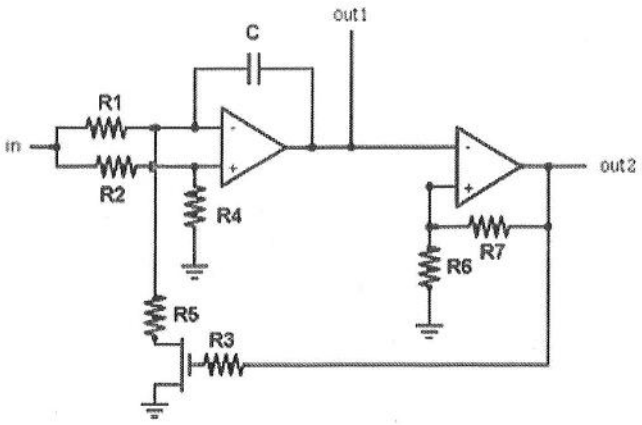

Figure 3

3. An astable multivibrator circuit is modified as shown in the figure 4. Assume the diode shown in the figure is ideal. Plot waveforms V_{01}, V_{02}, V_{x1} and V_{x2} with respect to time (*use proper labels, shapes and maintain approximate visualization of duty cycle and voltage values in your plot*). Calculate the **time period** and **duty cycle** of the output waveform V_{o2}.

[Marks: (2+2+2+2)+(1+1)=10]

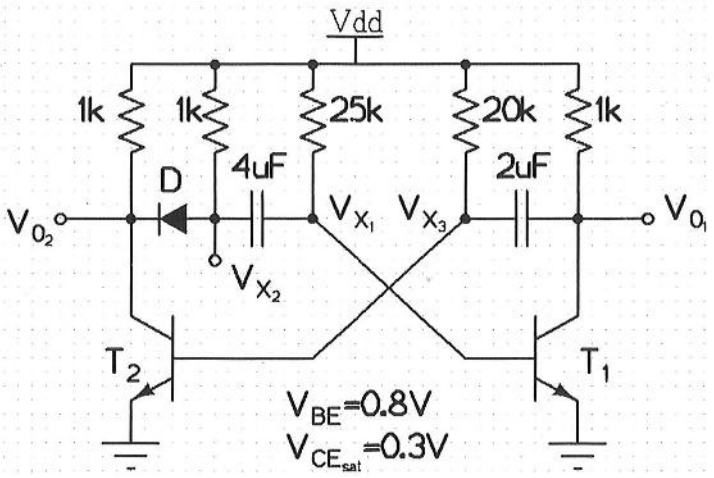

Figure 4

4. The circuit shown in Figure 5 is implemented using all ideal components with sufficient supply voltage to the Op-amps. If R = 10KΩ and C = 1μF find the **Condition** for sustained oscillation and **Frequency** of oscillation (in Hz). [Marks: 5+5=10]

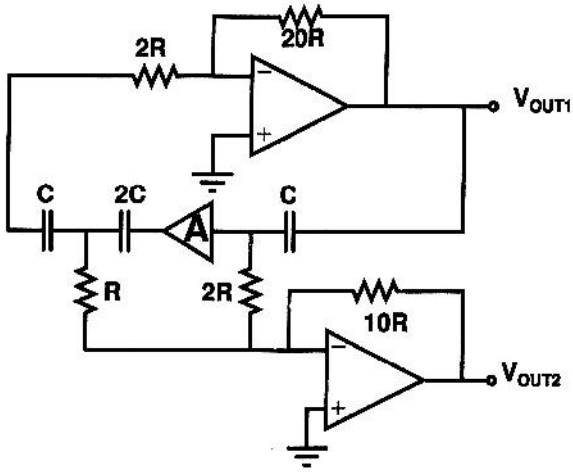

Figure 5