B. ELECTRICAL ENGINEERING 2ND YEAR 2ND SEMESTER EXAMINATION, 2018

Subject: SEQUENTIAL SYSTEMS & MICROPROCESSORS   Time: Three Hours   Full Marks: 100

<u>Use a separate Answer-script for each Part</u>
**Part I** (50 marks)
<u>Question 1 is compulsory</u>
Answer *Any Two* questions from the rest (2×20)

| Question No.			Marks
Q1		Answer *any Two* of the following:	
	(a)	A JK master-slave flip-flop has its J and K inputs tied to $+V_{CC}$ and a series of pulses are applied to its clock input. Describe the waveform at its output Q.	5
	(b)	Describe the operation of a T flip-flop. Derive T flip-flop from D flip-flop.	5
	(c)	Draw the logic circuit diagram of a 3-bit asynchronous up-counter employing T flip-flops. Show how it can be converted to a 3-bit down counter.	5
	(d)	With the help of block diagrams discuss the differences in the basic operations of PROM, PAL and PLA.	5

Q2 (a) Analyze the circuit shown in Figure Q2 and find the output *Y*. Consider that the flip-flops are initially reset.

Figure Q2

8
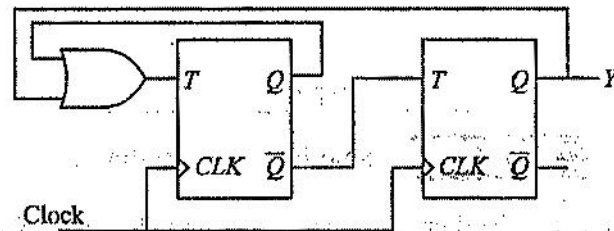
(b) What is Excitation Table for a Flip-flop? How is it different from the Truth Table? With the help of Excitation Table show how SR-flip-flop can be converted to JK-flip-flop.   2+2+8

Q3 (a) Design a modulo-4 irregular counter with the following counting sequence using D flip-flop.

$$00 \longrightarrow 10 \longrightarrow 11 \longrightarrow 01$$

8
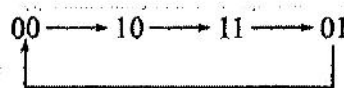
(b) Draw the block diagram of a 4-bit Shift-Right Register realized using JK flip-flops. Show, with the help of timing diagram, how "0100" can be entered serially into the register.   4+8

[Turn over

Q4 (a) What is a Finite State Machine? Explain the function of the circuit shown in Figure Q4 with the help of state transition diagram.
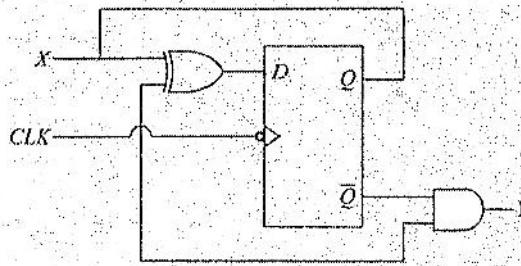
2+6

Figure Q4

(b) A sequential circuit has one input X and one output Z. The circuit is to recognize the occurrence of the sequence of bits "1101" on X by making Z equal to 1 when the previous three inputs to the circuit were "110" and current input is a 1. Otherwise, Z equals 0. Assume that Reset is applied to the direct reset inputs on its flip-flops to initialize the state of the circuit to all zeros. Describe, with the help of state transition table and state diagram, the synthesis process of the circuit using D flip-flop.

12

Q5 (a) Show how a PLA can be used to recognize each of the 10 decimal digits represented in binary form and to correctly drive a 7-segment display.

10

(b) Draw the block diagrams for an SRAM cell and a DRAM cell and discuss the operational difference between them.

4

(c) Show, using block diagram, how 64K × 16 RAM can be constructed with two 64K × 8 RAM chips.

6

B.E. ELECTRICAL ENGINEERING SECOND YEAR SECOND SEMESTER - 2018

SEQUENTIAL SYSTEM AND MICROPROCESSORS

Time: Three hours   (50 marks for each Part)   Full Marks: 100

Use a separate Answer-Script for each Part

PART- II

Group-A

Answer any four questions: 4X5=20

1) Explain with suitable diagram why de-multiplexing of address and data bus is required?

2) What is the function of accumulator and GP registers?

3) Why are program counter and stack pointer 16-bit registers?

4) What are the different addressing modes in 8085? Give examples in each case.

5) What do you mean by wait state? Why is it needed?

6) Distinguish between Partial and Full memory address decoding methods with necessary example.

7) Distinguish between memory mapped and I/O mapped I/O address decoding method with necessary example.

8) What are the advantages of subroutine programming? Give example.

Group-B

Answer any three questions: 3X5=15

1) Show the timing diagram for LXI H <16-bit operand> which consumes 3 machine cycles and 10 T states. The hex code for LXI H is 21H.

2) What are the vector interrupts of 8085. Explain with the help of suitable functional diagram, how branching address are generated?

3) Debug the following 8085 programmes and correct these.

     a) RPT: MVI C ,06H
                      DCR C
                      JNZ RPT
                      HLT

b) LDA 2000H
   MOV B, A
   LDA 3000H
   ADD B
   STA 4000H
   LDA 2001H
   MOV B, A
   LDA 3001H
   ADD B
   STA 4001H
   HLT

4) An 8085 microprocessor is run by external clock signal with frequency 6.144 MHz. Write a programme to generate time delay of 1Sec by using Nested branching method.

5) Specify the addressing mode of following 8085 instructions:
   a) LDA 8000H , b) DAA c) MOV A,M d) STAX D e) SHLD 2000H

6) Discuss the control word format of 8255 PPI interfaced with 8085 in BSR mode with suitable example.

7) Draw interfacing diagram for interfacing a memory IC (2K size) and I/O with 8085 CPU at address 2000H for memory and 07H address for I/O.

Group-C
Answer any three questions: 3X5=15

1) Calculate the sum of series of odd numbers from the list of numbers. The length of the list is in memory location 2200H and the series itself begins from memory location 2201H. Assume the sum to be 16-bit. Store the sum at memory locations 2300H and 2301H.

2) Write 8085 assembly language program to SORT an array of 10 bytes in descending order.

3) Search the given byte in the list of 50 numbers stored in the consecutive memory locations and store the address of memory location in the memory locations 2200H and 2201H. Assume byte is in the C register and starting address of the list is 2000H. If byte is not found store 00 at 2200H and 2201H.

4) Add 2 arrays having ten 8-bit numbers each and generate a third array of result. It is necessary to add the first element of array 1 with the first element of array-2 and so on. The starting addresses of array 1, array2 and array3 are 2200H, 2300H and 2400H, respectively.

5) Write assembly language program in 8085 to convert any 8 bit Hexadecimal number to Binary digits.