Ref No: Ex/EE/T/226/2018 (Old)

B.E. ELECTRICAL ENGINEERING - SECOND YEAR - SECOND SEMESTER 2018(OLD)

(~~1st~~/ 2nd Semester/~~Repeat/Supplementary/Annual/Bi-Annual~~)

SUBJECT: - PROGRAMMABLE LOGIC AND SEQUENTIAL SYSTEMS

Full Marks 100

Time: Three hours (50 marks for each part)

Use a separate Answer-Script for each part

No. of Questions	PART I	Marks
	Answer any three Questions Two marks are for neat and systematic answers	
Q1.	a) A system is described by, Y=A+B.((A+B)+AB) i) Implement the expression through digital circuit. ii) Implement the above expression through ladder diagram. iii) Implement the simplified expression through ladder diagram.	4+6+6
	b) Name four field switches that are used as digital input in PLC based system.	4
Q2.	a) Draw the basic block diagram of a Moore machine and describe the functions of each block.	8
	b) Draw the block diagram and explain the operation of a 4-bit controlled shift left register using D-FF.	8
Q3.	a) Show with suitable sketch how a common bus can be shared for data transfer between four different 4-bit registers. Show the instructions to transfer a data of 1101 between any two registers sharing a common bus.	4+4
	b) Draw and explain the functions of different symbols used to draw state diagram of a sequential system.	8
Q4.	a) Define Read Cycle time, Write Cycle time and Access time with respect to the specification of a memory chip.	6
	b) Design a 1024X4 bit Read and Write Memory (RWM) chip using 512X4 bit memory chips. Sketch the final memory system taking any starting address.	8
	c) Explain the function of Chip Select signal with respect to a memory chip.	2

[Turn over

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Use a separate Answer-Script for each part

No. of Questions	PART I	Marks
Q5.	a) Draw the Ladder diagram to implement a DOL starter of a three phase induction motor having following functions: The motor will run when START button is pressed and will stop when STOP button is pressed while running. Also the motor is provided with overload and over temperature protection for safety purpose. Indicate the inputs and outputs to PLC for the above system.	16

Ex/EE/T/226/2018 (Old)

B. E. ELETRICAL ENGG SECOND YEAR SECOND SEMESTER EXAMINATION 2018 (OLD)

PROGRAMMABLE LOGIC AND SEQUENTIAL SYSTEM

Time: Three hours | Full Marks: 50

(50 marks for each part)
Use separate answer script for each part.
PART II
Answer **any five** questions.
Figures in the margin indicate full marks

1. Discuss about different switching techniques employed in configurable hardware. (10)

2.(a) Illustrate with relevant circuits the principle of operation of an AND matrix within a PLA device. (6)

(b) Write a program in VHDL to implement an OR gate. (4)

3. Draw simple macrocell architecture and explain how it adds versatility to a configurable hardware. (10)

4. What do you understand by Application Specifics ICs and Fixed Function ICs? Write their relative merits and demerits. (10)

5. Discuss about transistor pair architecture used in FPGA. (10)

6. With the help of a block diagram discuss the functions of different components of a PLA device. (10)

7. What is a CAD system? Write the advantages of a CAD system. Discuss about the different stages of a CAD system. (10)